SN65LBC172、SN75LBC172 四通道低功耗差分线路驱动器

1 特性

- 超出或符合 EIA 标准 RS-485
- 适用于嘈杂环境中长总线上的高速多点传输
- 支持高达并超过每秒 1000 万次传输的数据速率
- 提供 −7V 至 12V 的共模输出电压范围
- 提供正负电流限制
- 功耗低，最大 1.5mA（输出禁用）
- 与 SN75172 在功能上可以互换

2 应用

- 电机驱动
- 工厂自动化和控制

3 说明

SN65LBC172 和 SN75LBC172 是具有三态输出的单片四通道差分线路接驱动器。这两种器件都符合 RS 标准 EIA-485 的要求。这些器件经优化，能够以高达和超过 10Mbit/s 的数据速率实现平衡多点总线传输。每个驱动器都具有较宽的正负共模输出电压范围、电流限制和热关断电路，适用于嘈杂环境中的合用线应用。这两种器件采用 LinBiCMOS™ 进行设计，有助于实现超低功耗和固有的稳健性。

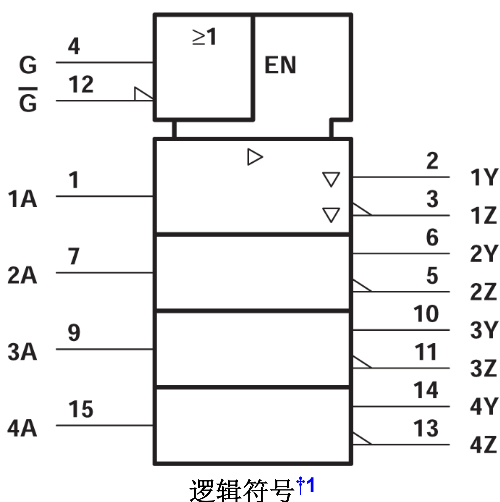
SN65LBC172 和 SN75LBC172 均可提供正负电流限制和热关断功能，避免传输总线出现线路故障状况。这些器件在与 SN75LBC173 或 SN75LBC175 四通道线路接收器配合使用时，可提供卓越性能。SNSN65LBC172 和 SN75LBC172 采用 16 引脚 DIP 封装 (N) 和 20 引脚宽体 Small-outline Integrated Circuit (SOIC) 封装 (DW)。

SN75LBC172 可在 0°C 至 70°C 的商业温度范围内运行。SN65LBC172 可在 –40°C 至 85°C 的工业温度范围内运行。

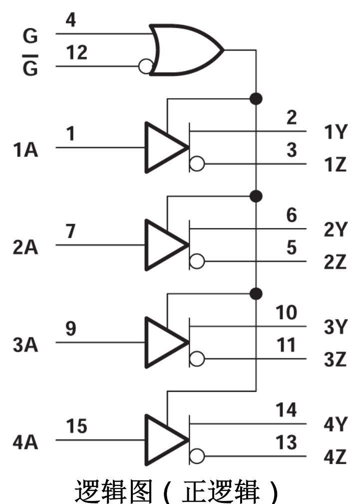
封装信息

器件型号	封装[1]	封装尺寸[2]
SN65LBC172 SN75LBC172	DW（SOIC，20）	10.3mm x 10.3mm
	N（PDIP，16）	19.3mm x 9.4mm

(1) 有关更多信息，请参阅节 10。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。



逻辑符号†1



逻辑图（正逻辑）

† 此符号符合 ANSI/IEEE 标准 91-1984 和 IEC 出版物 617-12。
1 所示引脚编号适用于 N 封装。

本资源的原文使用英文撰写。为方便起见，TI 提供了译文；由于翻译过程中可能使用了自动化工具，TI 不保证译文的准确性。为确认准确性，请务必访问 ti.com 参考最新的英文版本（控制文档）。

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4 Pin Configuration and Functions

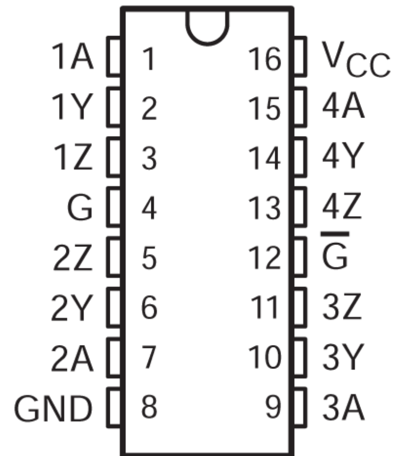

图 4-1. N Package (Top View)

表 4-1. Pin Functions

PIN		TYPE[(1)]	DESCRIPTION
NAME	NO.		
1A	1	I	Driver 1 input
1Y	2	O	Driver 1 output
1Z	3	O	Driver 1 inverted output
G	4	I	Active high enable all drivers
2Z	5	O	Driver 2 inverted output
2Y	6	O	Driver 2 output
2A	7	I	Driver 2 input
GND	8	G	Ground pin
3A	9	I	Driver 3 input
3Y	10	O	Driver 3 output
3Z	11	O	Driver 3 inverted output
$\overline{G}$	12	I	Active low enable all drivers
4Z	13	O	Driver 4 inverted output
4Y	14	O	Driver 4 output
4A	15	O	Driver 4 input
V_{CC}	16	P	Power pin

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

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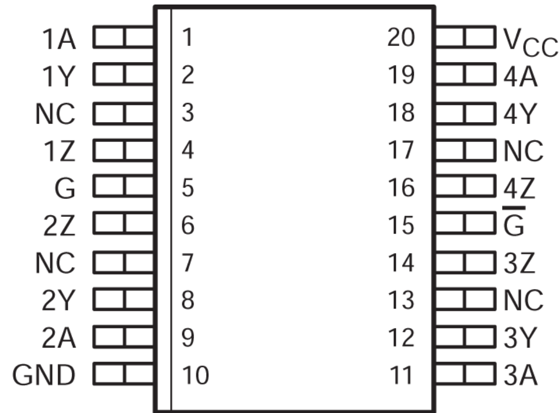

NC – No internal connection

图 4-2. DW Package (Top View)

表 4-2. Pin Functions

PIN		TYPE[(1)]	DESCRIPTION
NAME	NO.		
1A	1	I	Driver 1 input
1Y	2	O	Driver 1 output
NC	3	-	No Internal Connection
1Z	4	O	Driver 1 inverted output
G	5	I	Active high enable all drivers
2Z	6	O	Driver 2 inverted output
NC	7	-	No Internal Connection
2Y	8	O	Driver 2 output
2A	9	I	Driver 2 input
GND	10	G	Ground pin
3A	11	I	Driver 3 input
3Y	12	O	Driver 3 output
NC	13	-	No Internal Connection
3Z	14	O	Driver 3 inverted output
$\overline{G}$	15	I	Active low enable all drivers
4Z	16	O	Driver 4 inverted output
NC	17	–	No Internal Connection
4Y	18	O	Driver 4 output
4A	19	I	Driver 4 input
V_{CC}	20	P	Power pin

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

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5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
V_{CC}	Supply voltage range, (see [3])	−0.3	7	V
V_O	Output voltage range	−10	15	V
V_I	Voltage range at A, $\overline{G}$, G	−0.3	V_{CC} + 0.5	V
P_D	Continuous power dissipation	Internally limited[2]		
T_{stg}	Storage temperature range	−65	150	°C
T_{LEAD}	Lead temperature 1,6mm (1/16 inch) from case for 10 seconds		260	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The maximum operating junction temperature is internally limited. Use the dissipation rating table to operate below this temperature.
(3) All voltage values are with respect to GND.

5.2 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
High-level input voltage, V_{IH}		2			V
Low-level input voltage, V_{IL}				0.8	V
Voltage at any bus terminal (separately or common mode), V_O	Y or Z	-7		12	V
High-level output current, I_{OH}	Y or Z			−60	mA
Low-level output current, I_{OL}	Y or Z			60	mA
Continuous total power dissipation		See Dissipation Rating Table			
Junction temperature, T_J				140	°C
Operating free-air temperature, T_A	SN65LBC172	−40		85	°C
	SN75LBC172	0		70	

5.3 Dissipation Rating Table

PACKAGE	THERMAL MODEL	T_A < 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
DW	Low K[1]	1094mW	10.4mW/°C	625mW	469mW
	High K[2]	1669mW	15.9mW/°C	954mW	715mW
N		1150mW	9.2mW/°C	736mW	598mW

(1) In accordance with the low effective thermal conductivity metric definitions of EIA/JESD 51−3.
(2) In accordance with the high effective thermal conductivity metric definitions of EIA/JESD 51−7.

5.4 Thermal Information

THERMAL METRIC[(1)]		N (PDIP)	DW (SOIC)	UNIT
		16 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	60.6	66.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	48.1	34.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	40.6	39.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	27.5	8.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	40.3	39	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP [(1)]	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = -18mA				-1.5	V
$\|V_{OD}\|$	Differential output voltage[(2)]	R_L = 54Ω See 图 6-1	SN65LBC172	1.1	1.8	5	V
			SN75LBC172	1.5	1.8	5	
		R_L = 60Ω, See 图 6-2	SN65LBC172	1.1	1.7	5	
			SN75LBC172	1.5	1.7	5	
$\Delta\|V_{OD}\|$	Change in magnitude of common-mode output voltage[(3)]	R_L = 54Ω,	See 图 6-1			±0.2	V
V_{OC}	Common-mode output voltage			-1		3	V
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage[(3)]					±0.2	V
I_O	Output current with power off	V_{CC} = 0,	V_O = - 7V to 12V			± 100	μA
I_{OZ}	High-impedance-state output current	V_O = - 7V to 12V				± 100	μA
I_{IH}	High-level input current	V_I = 2.4V				-100	μA
I_{IL}	Low-level input current	V_I = 0.4V				-100	μA
I_{OS}	Short-circuit output current	V_O = -7V to 12V				±250	mA
I_{CC}	Supply current (all drivers)	No load	Outputs enabled			7	mA
			Outputs disabled			1.5	

(1) All typical values are at V_{CC} = 5V and T_A = 25°C.
(2) The minimum V_{OD} specification does not fully comply with EIA-485 at operating temperatures below 0°C. The lower output signal should be used to determine the maximum signal-transmission distance.
(3) $\Delta_{|VOD|}$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input changes from a high level to a low level.

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5.6 Switching Characteristics

V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$t_{d(OD)}$	Differential output delay time	R_L = 54Ω,	See 图 6-3	2	11	20	ns
$t_{t(OD)}$	Differential output transition time			9	15	25	
t_{PZH}	Output enable time to high level	R_L = 110Ω,	See 图 6-4		20	30	ns
t_{PZL}	Output enable time to low level	R_L = 110Ω,	See 图 6-5		21	30	ns
t_{PHZ}	Output disable time from high level	R_L = 110Ω,	See 图 6-4		48	70	ns
t_{PLZ}	Output disable time from low level	R_L = 110Ω,	See 图 6-5		21	30	ns

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5.7 Typical Characteristics

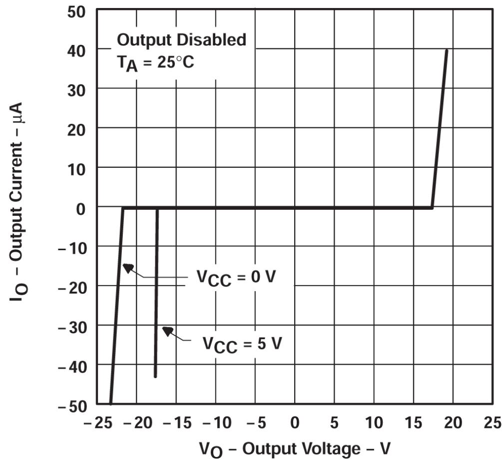

图 5-1. Output Current vs Output Voltage

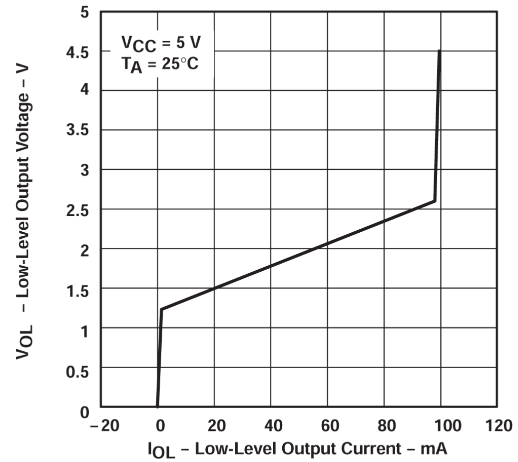

图 5-2. Low-level Output Voltage vs Low-level Output Current

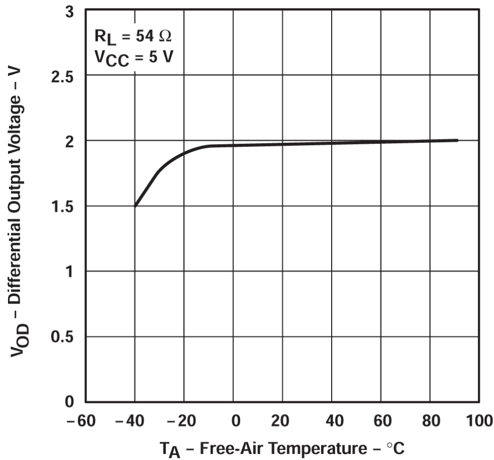

图 5-3. Differential Output Voltage vs Free-air Temperature

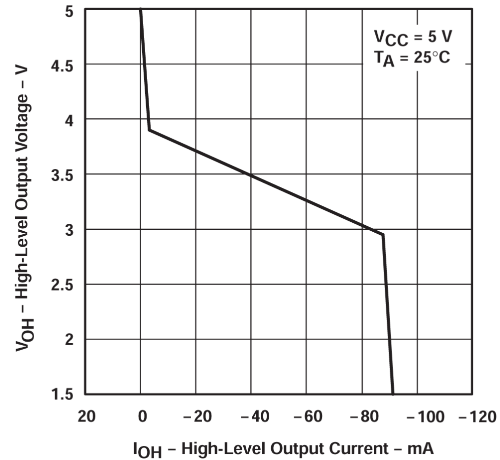

图 5-4. High-level Output Voltage vs High-level Output Current

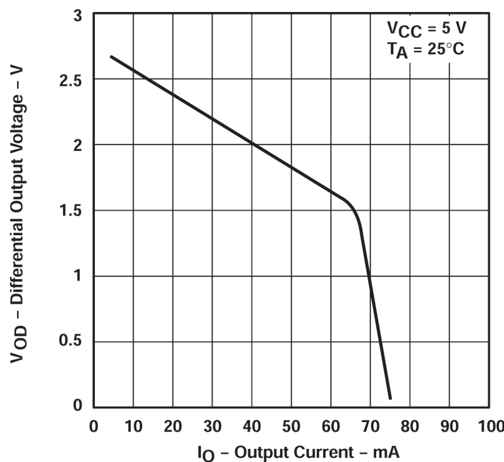

图 5-5. Differential Output Voltage vs Output Current

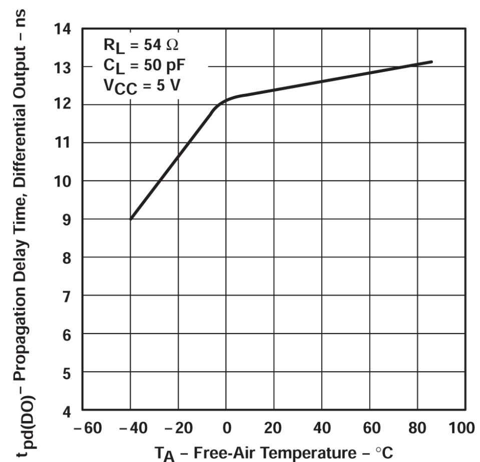

图 5-6. Propagation Delay Time, Differential Output vs Free-air Temperature

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6 Parameter Measurement Information

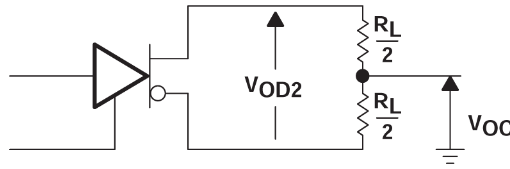
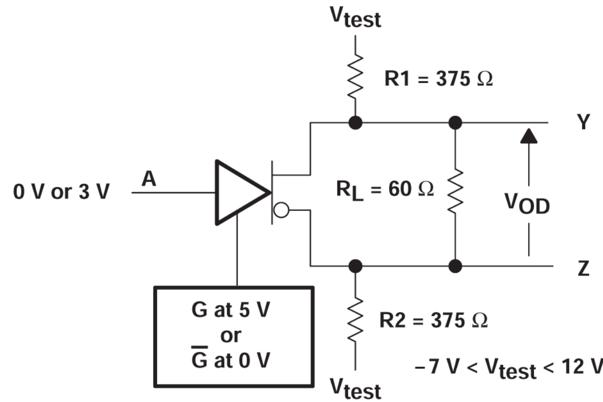


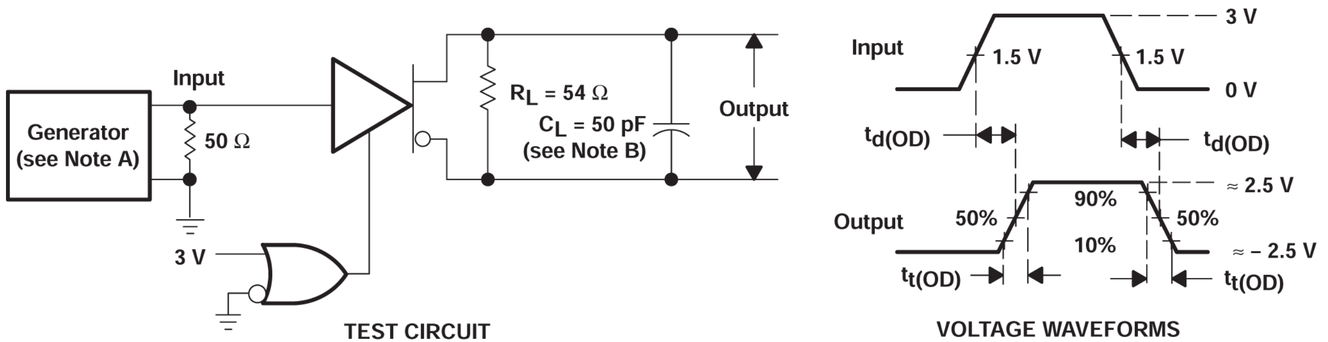
图 6-1. Differential and Common-Mode Output Voltages



A. The input pulse is supplied by a generator having the following characteristics: PRR ⩽ 1 MHz, duty cycle = 50%, t_r ⩽ 5 ns, t_f ⩽ 5 ns, Z_O = 50 Ω.

B. C_L includes probe and stray capacitance.

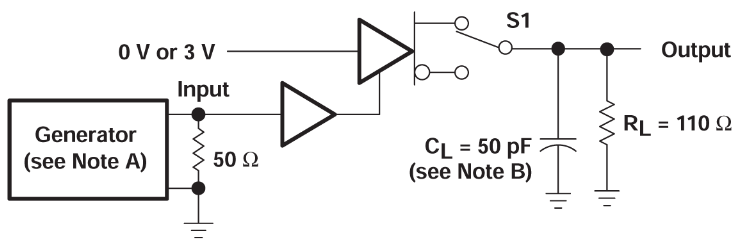
图 6-2. Driver V_{OD} Test Circuit

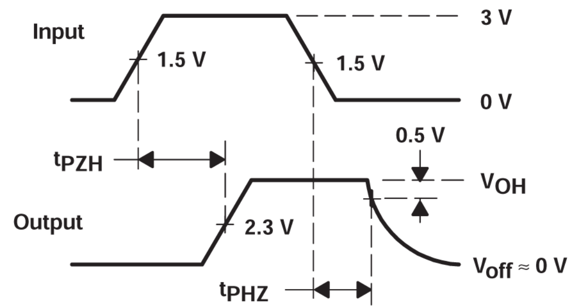


A. The input pulse is supplied by a generator having the following characteristics: PRR ⩽ 1 MHz, duty cycle = 50%, t_r ⩽ 5 ns, t_f ⩽ 5 ns, Z_O = 50 Ω.

B. C_L includes probe and stray capacitance.

图 6-3. Driver Differential-Output Test Circuit and Delay and Transition-Time Waveforms



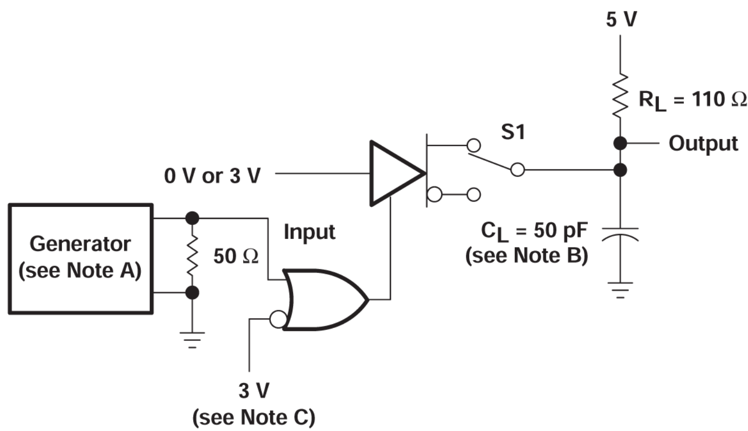


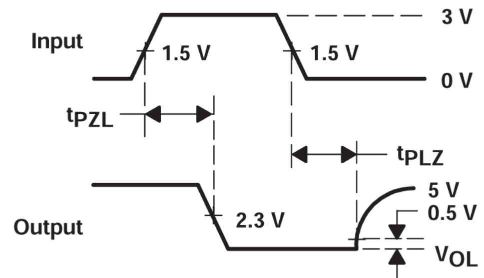
TEST CIRCUIT

VOLTAGE WAVEFORMS

A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle = 50%, t_r ≤ 5 ns, t_f ≤ 5 ns, Z_O = 50 Ω.
B. C_L includes probe and stray capacitance.

图 6-4. t_{PZH} and t_{PHZ} Test Circuit and Voltage Waveforms





TEST CIRCUIT

VOLTAGE WAVEFORMS

A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, duty cycle = 50%, t_r ≤ 5 ns, t_f ≤ 5 ns, Z_O = 50 Ω.
B. C_L includes probe and stray capacitance
C. To test the active-low enable $\overline{G}$, ground G and apply an inverted waveform to $\overline{G}$.

图 6-5. t_{PZL} and t_{PLZ} Test Circuit and Waveforms

7 Detailed Description

7.1 Thermal Characteristics of Ic Packages

Θ_{JA} (Junction-to-Ambient Thermal Resistance) is defined as the difference in junction temperature to ambient temperature divided by the operating power

Θ_{JA} is NOT a constant and is a strong function of

- the PCB design (50% variation)
- altitude (20% variation)
- device power (5% variation)

Θ_{JA} can be used to compare the thermal performance of packages if the specific test conditions are defined and used. Standardized testing includes specification of PCB construction, test chamber volume, sensor locations, and the thermal characteristics of holding fixtures. Θ_{JA} is often misused when it is used to calculate junction temperatures for other installations.

TI uses two test PCBs as defined by JEDEC specifications. The low-k board gives *average* in-use condition thermal performance and consists of a single trace layer 25mm long and 2 oz thick copper. The high-k board gives *best case* in−use condition and consists of two 1-oz buried power planes with a single trace layer 25mm long with 2-oz thick copper. A 4% to 50% difference in Θ_{JA} can be measured between these two test cards

Θ_{JC} (Junction-to-Case Thermal Resistance) is defined as difference in junction temperature to case divided by the operating power. It is measured by putting the mounted package up against a copper block cold plate to force heat to flow from die, through the mold compound into the copper block.

Θ_{JC} is a useful thermal characteristic when a heatsink is applied to package. It is NOT a useful characteristic to predict junction temperature as it provides pessimistic numbers if the case temperature is measured in a non-standard system and junction temperatures are backed out. It can be used with Θ_{JB} in 1-dimensional thermal simulation of a package system.

Θ_{JB} (Junction-to-Board Thermal Resistance) is defined to be the difference in the junction temperature and the PCB temperature at the center of the package (closest to the die) when the PCB is clamped in a cold−plate structure. Θ_{JB} is only defined for the high-k test card.

Θ_{JB} provides an overall thermal resistance between the die and the PCB. Including a bit for the PCB thermal resistance (especially for BGAs with thermal balls), and can be used for simple 1-dimensional network analysis of package system (see 图 7-1).

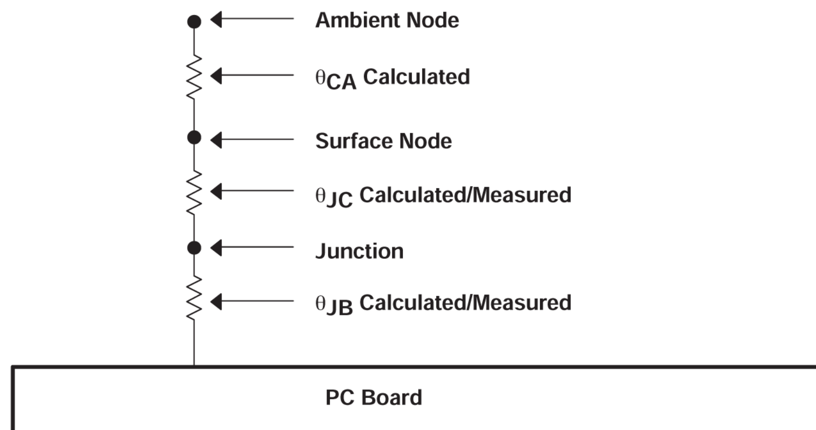


图 7-1. Thermal Resistance

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7.2 Device Functional Modes

表 7-1. Function Table (Each Driver)

INPUT A	ENABLES[1]		OUTPUTS	
	G	$\overline{G}$	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off)

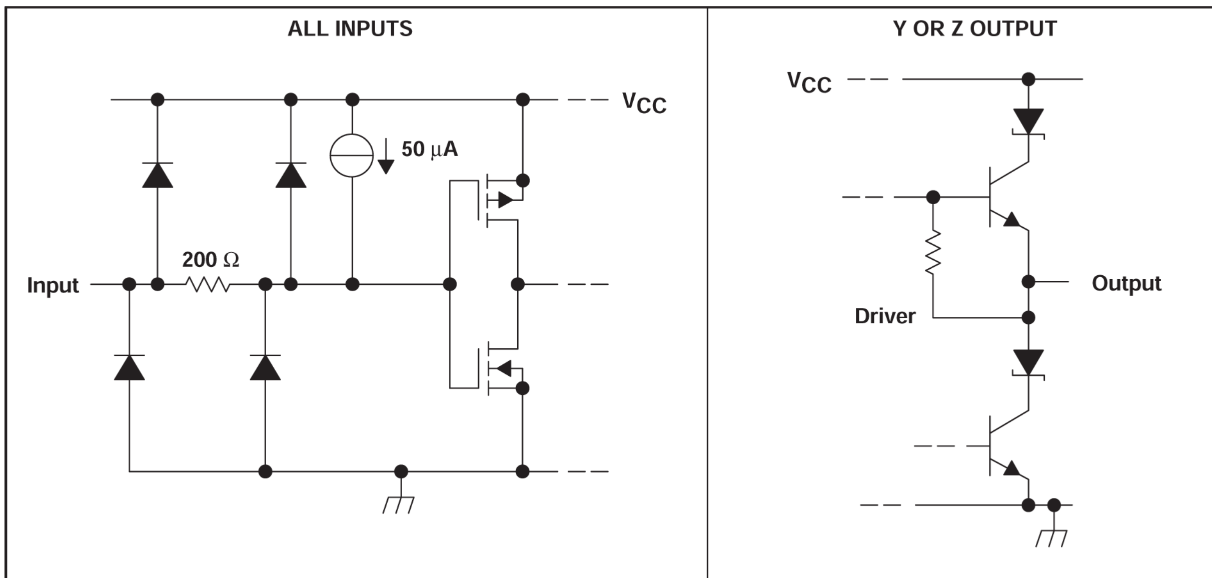

图 7-2. Schematic Diagrams of Inputs and Outputs

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8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.2 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

8.3 Trademarks

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所有商标均为其各自所有者的财产。

8.4 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.5 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

9 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision E (April 2006) to Revision F (April 2024) **Page**

- 更改了整个文档中的表格、图和交叉参考的编号格式....................1
- Added the *Thermal Information* table....................6

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65LBC172DW	ACTIVE	SOIC	DW	20	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	SN65LBC172	Samples
SN65LBC172N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN65LBC172N	Samples
SN75LBC172DW	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	0 to 70	SN75LBC172	
SN75LBC172DWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	SN75LBC172	Samples
SN75LBC172N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN75LBC172N	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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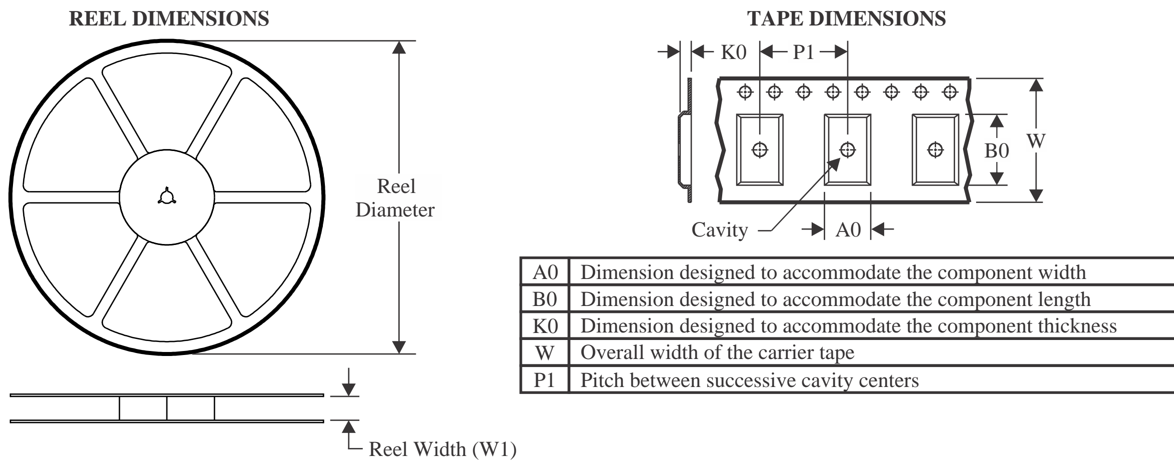
OTHER QUALIFIED VERSIONS OF SN75LBC172 :

- Military : SN55LBC172

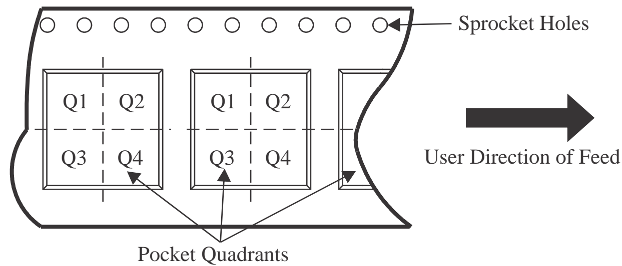
NOTE: Qualified Version Definitions:

- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

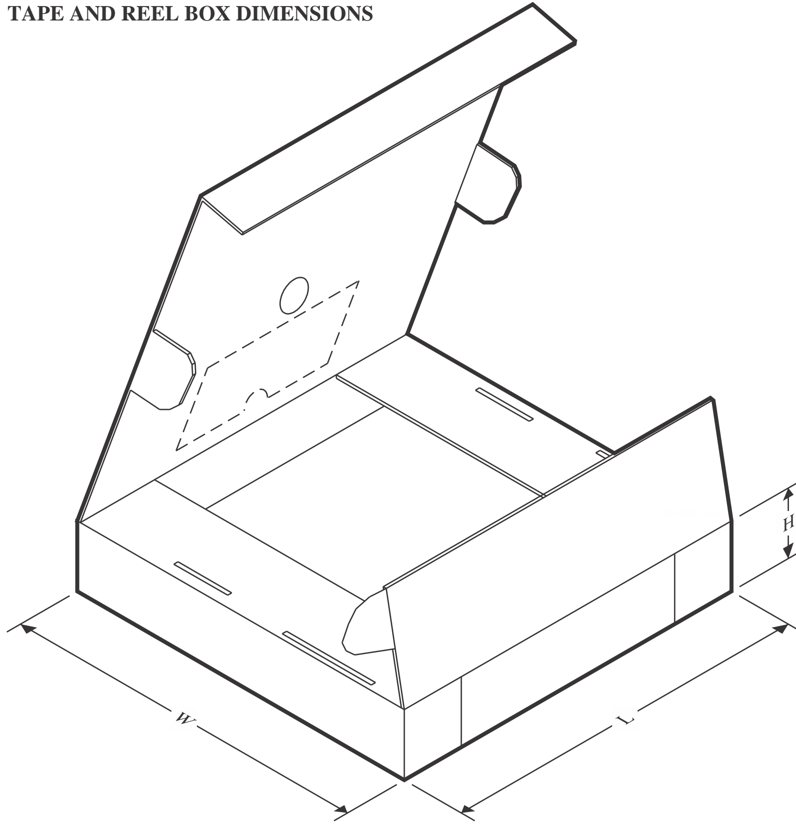


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

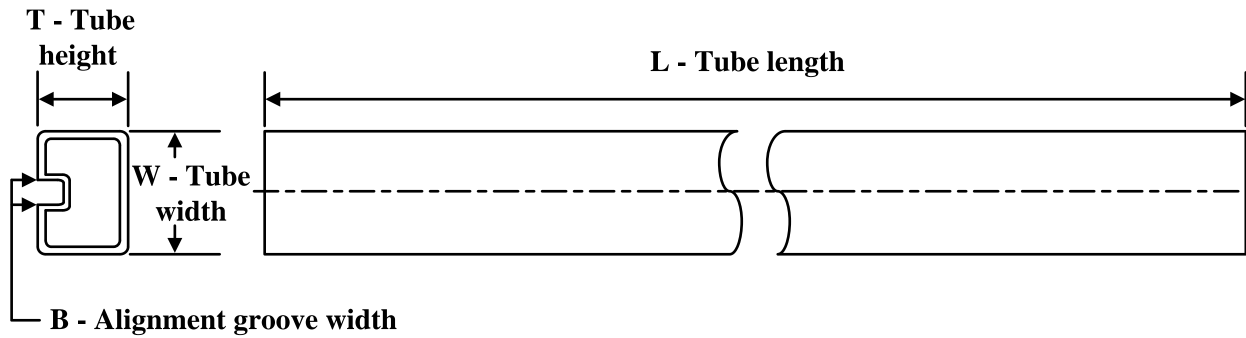
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75LBC172DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN75LBC172DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75LBC172DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN75LBC172DWR	SOIC	DW	20	2000	356.0	356.0	45.0

TUBE

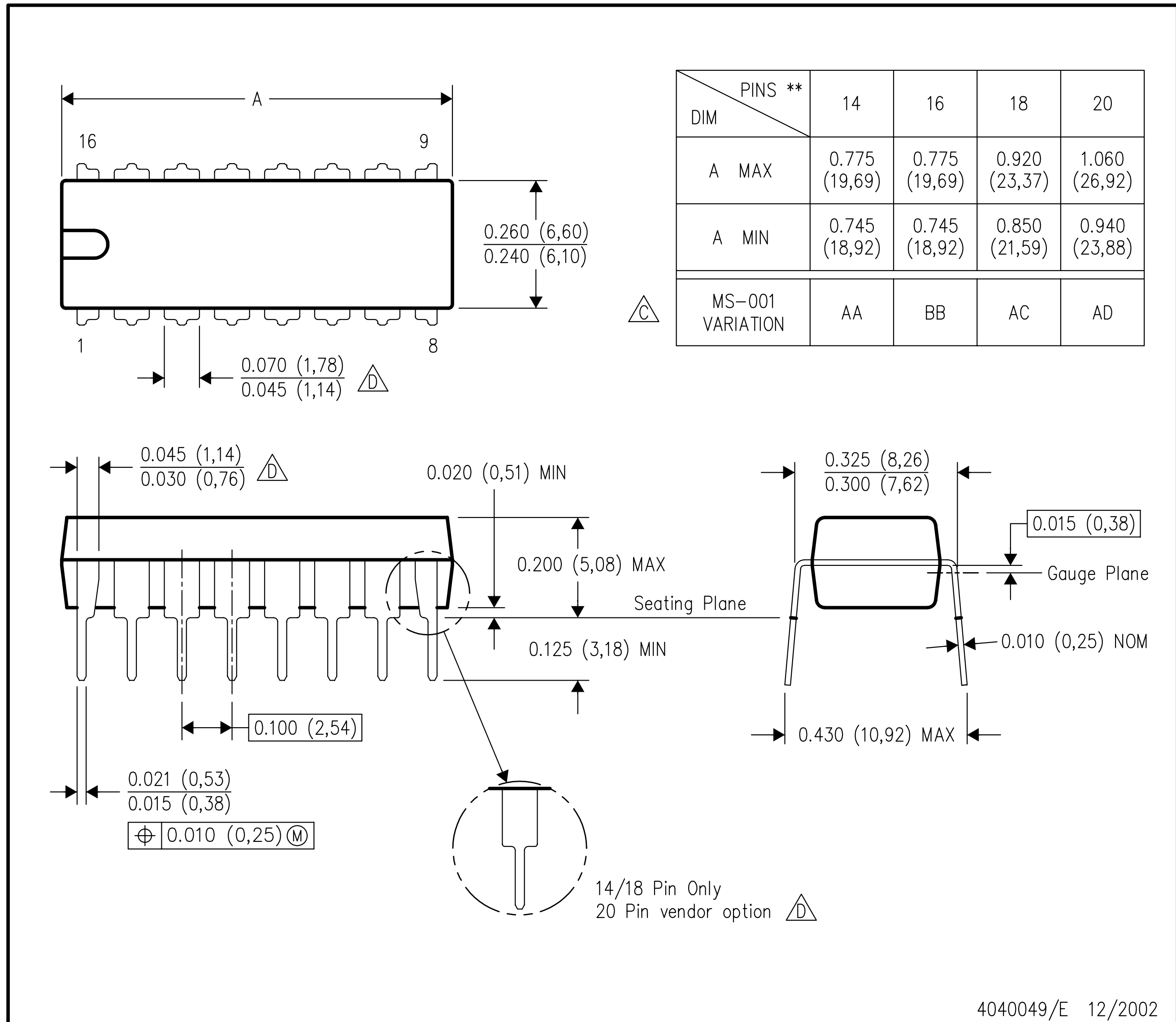


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN65LBC172DW	DW	SOIC	20	25	506.98	12.7	4826	6.6
SN65LBC172DW	DW	SOIC	20	25	507	12.83	5080	6.6
SN65LBC172N	N	PDIP	16	25	506	13.97	11230	4.32
SN75LBC172N	N	PDIP	16	25	506	13.97	11230	4.32

N (R–PDIP–T**) PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION	AA	BB	AC	AD

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

10.63
9.97 TYP

PIN 1 ID
AREA

A

18X 1.27

1

20

2X
11.43

13.0
12.6
NOTE 3

10

11

20X 0.51
0.31

0.25Ⓜ C A B

B

7.6
7.4
NOTE 4

C

SEATING PLANE

0.1 C

2.65 MAX

0.33
0.10 TYP

SEE DETAIL A

0.25

GAGE PLANE

0° - 8°

1.27
0.40

0.3
0.1

DETAIL A
TYPICAL

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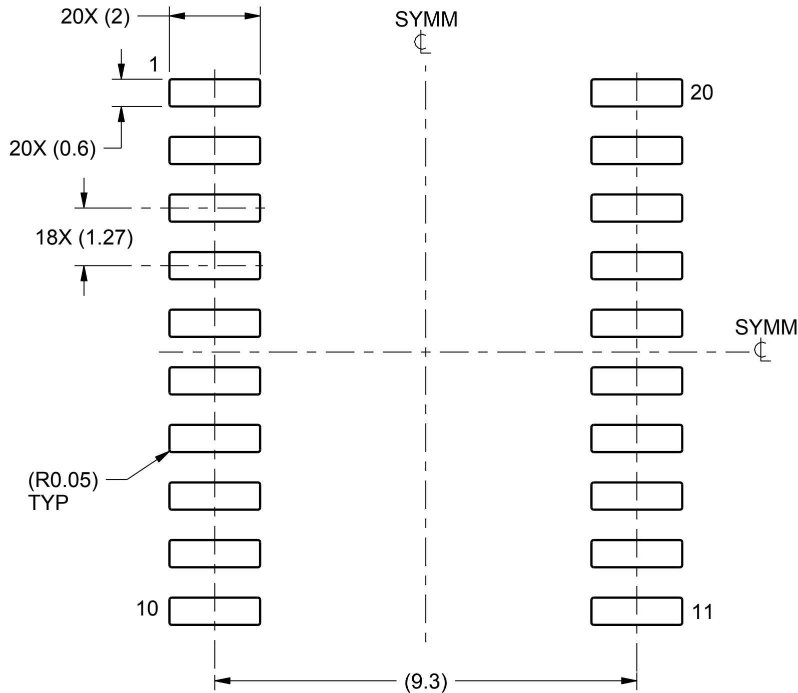
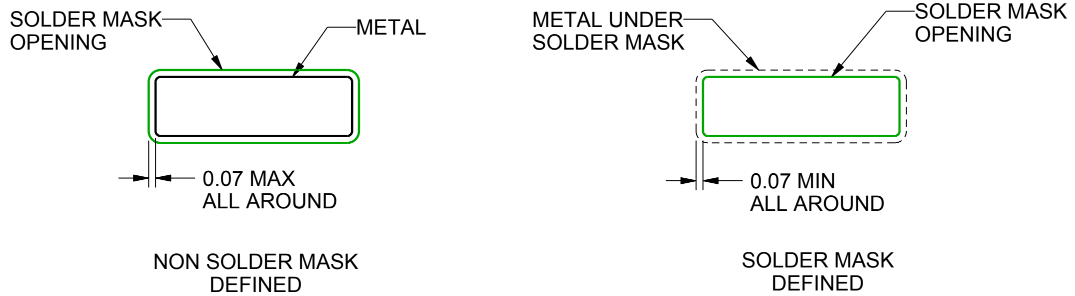
NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:6X



NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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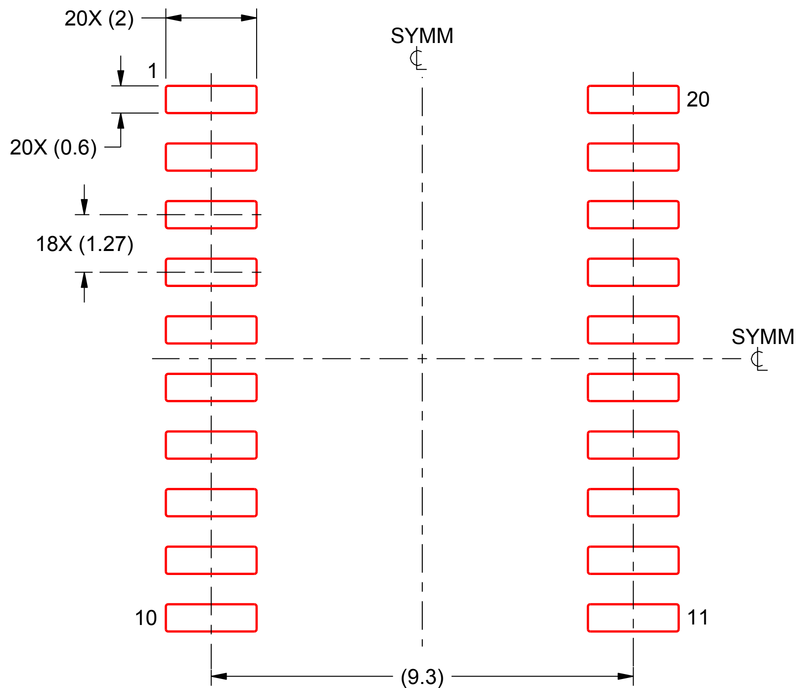
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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