Dual Channel x1 PCIe Redriver/Equalizer

Check for Samples: SN65LVPE501

FEATURES

- **Single Lane PCIe Equalizer/Redriver**
- **Support for Both PCIe Gen I (2.5Gbps) and Gen II (5.0 Gbps) Speed**
- **Selectable Equalization, De-emphasis and Output Swing Control**
- **Integrated Termination**
- **Hot-Plug Capable**
- **Receiver Detect**
- **Low Power:**
  - **330mW(TYP), V_{CC} = 3.3V**
- **Auto Low Power Modes:**
  - **5mW (TYP) When no Connection Detected**
  - **70mW (TYP) When in Auto-Low Power Mode**
- **Excellent Jitter and Loss Compensation Capability:**
  - **30" of 6 mil Stripline on FR4**
- **Small Foot Print – 24 Pin 4 × 4 QFN Package**
- **High Protection Against ESD Transient**
  - **HBM: 3,000 V**
  - **CDM: 1,500 V**
  - **MM: 200 V**

APPLICATIONS

- **PC MB, Docking Stations, Backplane and Cabled Application**

DESCRIPTION

The SN65LVPE501 is a dual channel, single lane PCIe redriver and signal conditioner supporting data rates of up to 5.0Gbps. The device complies with PCIe spec revision 2.1.

Programmable EQ, De-Emphasis and Amplitude Swing

The SN65LVPE501 is designed to minimize the signal degradation effects such as crosstalk and inter-symbol interference (ISI) that limits the interconnect distance between two devices. The input stage of each channel offers selectable equalization settings that can be programmed to match loss in the channel. The differential outputs provide selectable de-emphasis to compensate for the anticipated distortion PCIe signal will experience. Level of de-emphasis will depend on the length of interconnect and its characteristics. Both equalization and de-emphasis levels are controlled by the setting of signal control pins EQ1, EQ2 and DE1, DE2.

To provide additional control of signal integrity in extended backplane applications LVPE501 provides independent output amplitude control for each channel. See Table 2 for setting details.

Device PowerOn

Device initiates internal power-on reset after V_{CC} has stabilized. External reset can also be applied at anytime by toggling $\overline{RST}$ pin. External reset is recommended after every device power-up. When $\overline{RST}$ is driven high, the device samples the state of EN_RXD, if it is set H device enters Rx.Detect state where each channel will perform Rx.Detect function (as described in PCIe spec). If EN_RXD is set L, automatic RX detect function is disabled and both channels are enabled with their termination set to Z_{DC_RX}.

Receiver Detection

While EN_RXD pin is H and device is not in sleep mode ($\overline{RST}$ is H), SN65LVPE501 performs RX.Detect on both channels indefinitely until remote termination is detected on both channels. Automatic Rx detection feature can be forced off by driving EN_RXD low. In this state both channels input termination are set to Z_{DC_RX}.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION CONTINUED

Sleep (Shut_Down) Mode

This is low power state triggered by $\overline{RST}$ = L. In sleep mode receiver termination resistor for each of the two channels is switched to $Z_{RX\text{-}HIGH\_IMP}$ of >50 KΩ and transmitters are pulled to Hi-Z state. Device power is reduced to <1mW (TYP). To get device out of sleep mode $\overline{RST}$ is toggled L-H.

Electrical Idle Support

A link is in an electrical idle state when the TX± voltage is held at a steady constant value like the common mode voltage. SN65LVPE501 detects an electrical idle state when RX± input voltage of the associated channel falls below V_{EID_TH} min. After detection of an electrical idle state in a given channel the device asserts electrical idle state in its corresponding TX. When RX± voltage exceeds V_{EID_TH} max, normal device operation is restored and output starts passing input signal. Electrical idle exit and entry time is specified at ≤6ns.

Electrical idle support is independent for each channel.

Power Save Features

The device supports three power save modes as described below.

1. Sleep (Shut_Down) Mode

   This mode can be enabled from any state (Rx detect or active) by driving $\overline{RST}$ L. In this state both channels have their termination set to $Z_{RX\text{-}HIGH\_IMP+}$ and outputs are at Hi-Z. Device power is 1mW (MAX)

2. Auto Low Power Mode

   This mode is enabled when PS pin is tied H and device is in active mode. In this mode anytime Vin_{diff_pp} falls below selected V_{EID_TH} for a *given channel* and stays below V_{EID_TH} for >1µs (TYP), the associated CH will enter auto low power (ALP) mode where power/CH will be reduced to <1/3rd of normal operating power/CH or about 70mW under typical voltage of 3.3V when ALP conditions are met for both channels. A CH will exit ALP mode whenever Vin_{diff_pp} exceeds max V_{EID_TH} for that channel. Exit latency is 30ns max. To use this mode link latency will need to account for the ALP exit time for N_FTS. ALP mode is handled by each channel independently based on its input differential signal level. This mode can be disabled by leaving PS as NC or tying PS to GND via 4.7kΩ.

3. Cable Disconnect Mode

   This mode is activated when $\overline{RST}$ is H, EN_RXD = H, and no termination is detected by either channel. Device is in the Rx.Detect state whereby it is continuously performing Rx.Detect on both channels. In this state total power consumed by device is typically <3% of normal active power. Or <10mW (MAX).

Beacon Support

With its broadband design, the SN65LVPE501 supports low frequency Beacon signal (as defined by PCIe 2.1 spec) used to indicate wake-up event to the system by a downstream device when in L2 power state. All requirements for a beacon signal as specified in PCI Express specification 2.1 must be met for device to pass beacon signals.

Devic Power

The SN65LVPE501 is designed to operate from a single 3.3V supply. Always practice proper supply sequencing procedure. Apply V_{CC} first before any input control pin signals are applied to the device. Power-down sequence is in reverse order.

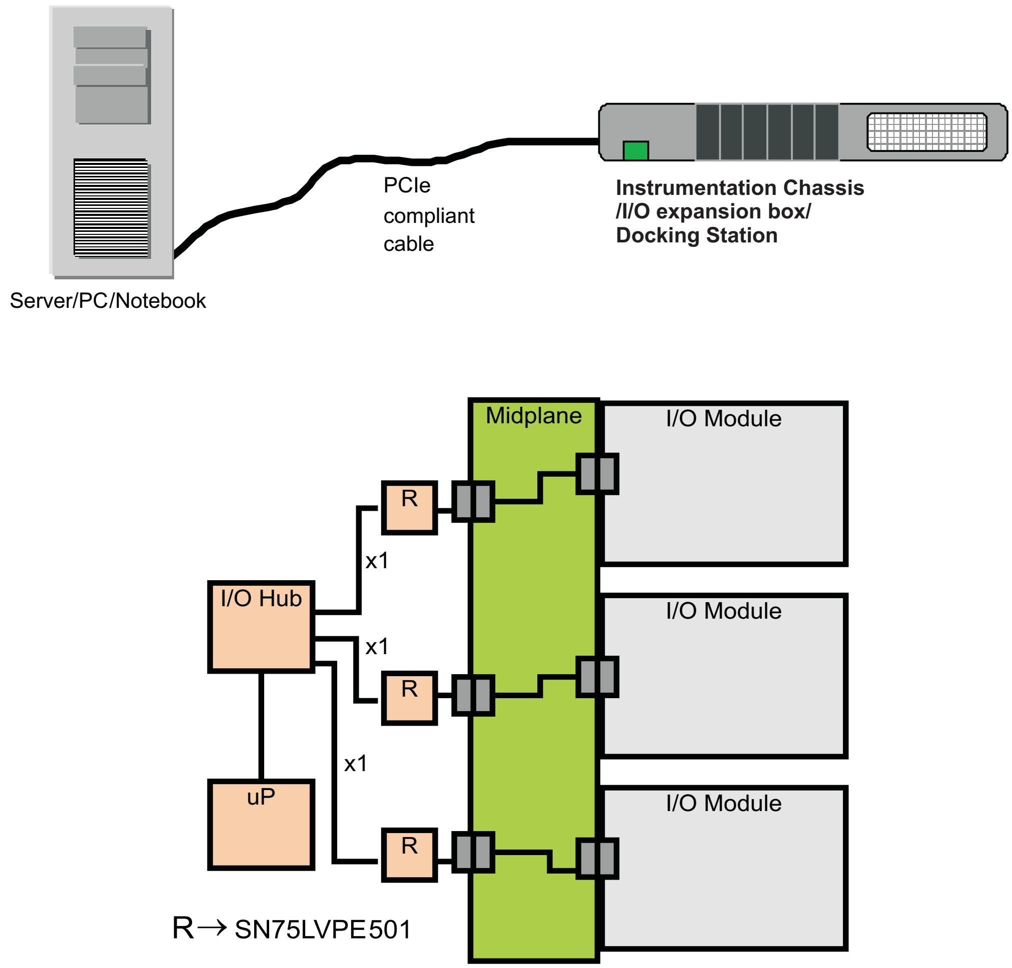


Figure 1. SN65LVPE501 Typical Applications

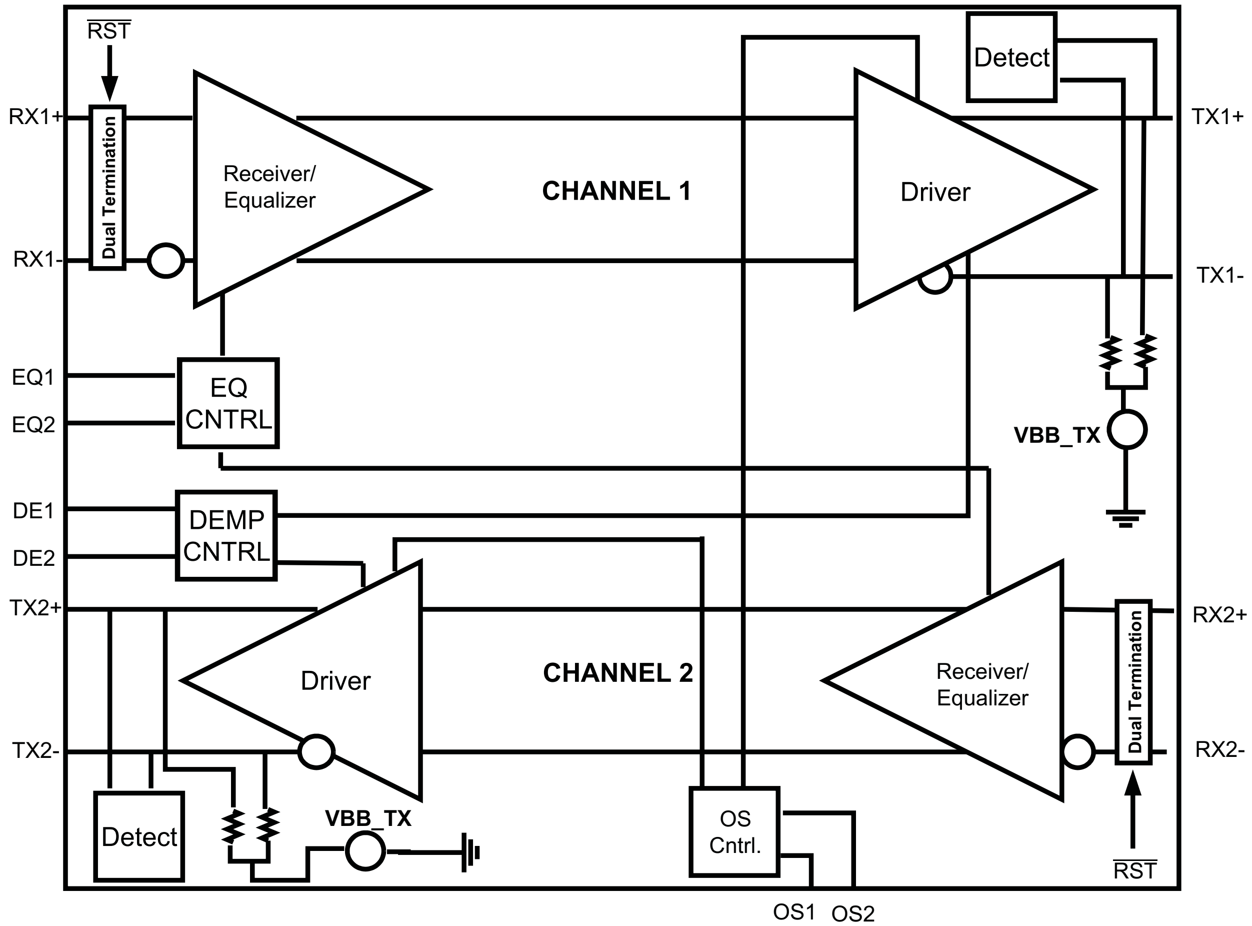


Figure 2. Data Flow Block Diagram

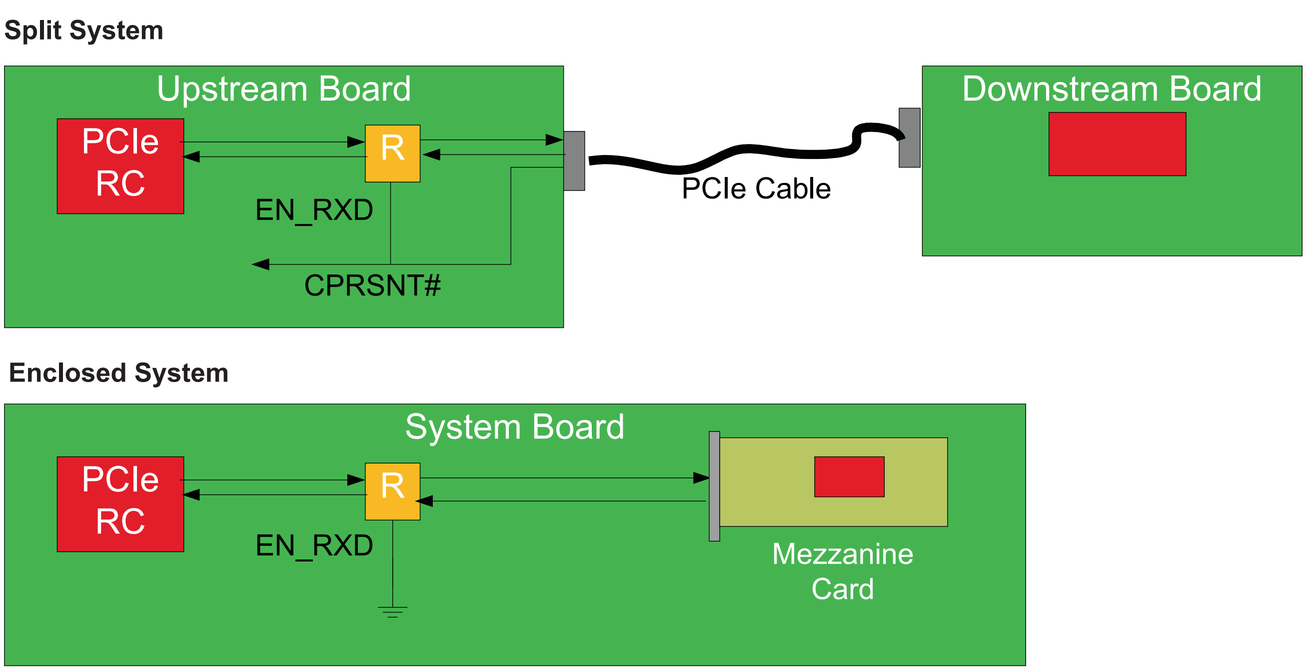


Figure 3. Typical Implementation

Table 1. Pin Description

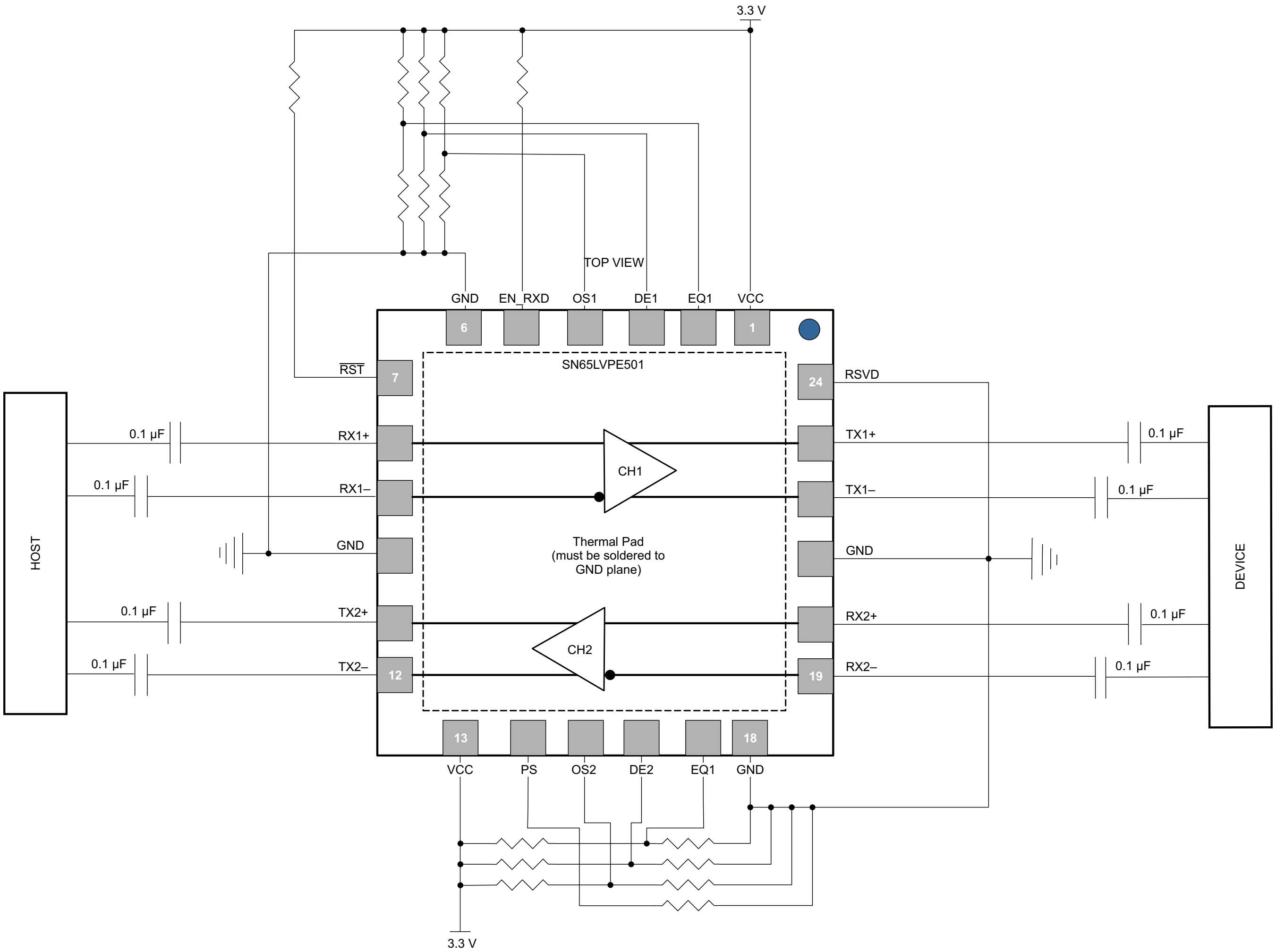
PIN			
NUMBER	NAME	I/O TYPE	DESCRIPTION
HIGH SPEED DIFFERENTIAL I/O PINS			
8	RX1+	I, CML	Non-inverting and inverting CML differential input for CH 1 and CH 2. These pins are tied to an internal voltage bias by dual termination resistor circuit.
9	RX1–	I, CML	
20	RX2+	I, CML	
19	RX2–	I, CML	
23	TX1+	O, CML	Non-inverting and inverting CML differential output for CH 1 and CH 2. These pins are internally tied to voltage bias by termination resistors.
22	TX1–	O, CML	
11	TX2+	O, CML	
12	TX2–	O, CML	
DEVICE CONTROL PIN(1)			
5	EN_RXD	I, LVCMOS	Sets device operation modes per Table 2. Internally pulled to VCC
14	PS	I, LVCMOS	Select auto-low power save mode per Table 2. Internally pulled to GND
7	$\overline{RST}$	I, LVCMOS	Reset device, input active Low. Internally pulled to VCC
24	RSVD	I, LVCMOS	Reserved for factory test. Must be connected to GND
SIGNAL CONTROL PINS(2)			
3,16	DE1, DE2	I, LVCMOS	Selects de-emphasis settings for CH 1 and CH 2 per Table 2. Internally tied to V_{CC}/2
2,17	EQ1, EQ2	I, LVCMOS	Selects equalization settings for CH 1 and CH 2 per Table 2. Internally tied to V_{CC}/2
4, 15	OS1, OS2	I, LVCMOS	Selects output amplitude for CH 1 and CH 2 per Table 2. Internally tied to V_{CC}/2
POWER PINS			
1,13	VCC	Power	Positive supply should be 3.3V ± 10%
6,10,18,21	GND	Power	Supply ground

(1) When not used can be left as NC or connected to V_{CC}/GND via 4.7kΩ resistor.
(2) Internally biased to V_{CC}/2 with >200kΩ pullup/pulldown. When 3-state pins are left as NC board leakage at the pin pad must be <1 µA otherwise drive to V_{CC}/2 to assert mid-level state.

Table 2. Signal Control Pin Setting

OSx		*TRANSITION* BIT AMPLITUDE (TYP mVpp)	
NC		1000	
0		875	
1		1100	
DEx(1)	**OSx(1) = NC**	**OSx(1) = 0**	**OSx(1) = 1**
NC	–3.7 dB	–2.5 dB	–4.6 dB
0	–6.4 dB	–5.5 dB	–6.6 dB
1	–9.4 dB	–9.5 dB	–8.7 dB
EQx(1)		**EQUALIZATION dB (At GenII Speed)**	
NC		0	
0		7	
1		15	
EN_RXD		**DEVICE FUNCTION**	
0		Set input termination to Z_{DC_RX} and disable Rx. Detect	
1		Perform Rx.Detect (**default**, internally pulled to Vcc)	
$\overline{RST}$		**DEVICE FUNCTION**	
0		Device in quiescent state and inputs set to Hi-Z	
1		Device not in shut_down mode (**default**, internally pulled to Vcc)	
PS		**DEVICE FUNCTION**	
0		Auto-low power mode disabled (**default**, internally pulled to GND)	
1		Auto-low power mode enabled	

(1) Applies to Channel 1 and Channel 2 at 2.5 GHz.



(1) This is a reference example and it is not intended to represent the best configuration; every designer should select the EQ and DE settings that better fits the system needs. All DEx, EQx and OSx pins default to NC.

(2) The recommended value for all the resistors shown in the Figure is 4.9K Ω.

(3) For terminals OSx, DEx, and EQx, populate only pull-up or only pull-down according to the desired setting.

Figure 4. Reference Device Implementation

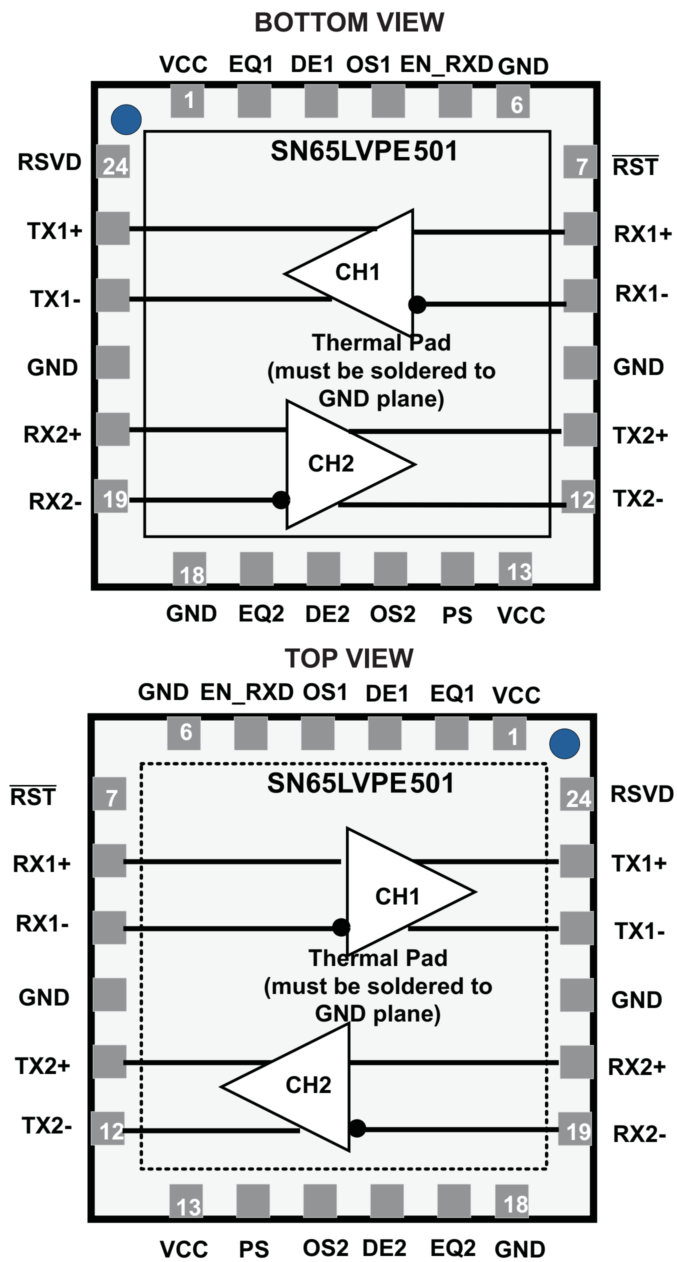


Figure 5. Flow-Through Pin-Out

ORDERING INFORMATION(1)

PART NUMBER	PART MARKING	PCAKAGE
SN65LVPE501RGER	LVPE501	24-pin RGE Reel (large)
SN65LVPE501RGET	LVPE501	24-pin RGE Reel (small)

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)[1]

		UNIT / VALUES
Supply Voltage Range[2]	V_{CC}	–0.5 V to 4 V
Voltage Range	Differential I/O	–0.5V to 4 V
	Control I/O	–0.5 V to V_{CC} + 0.5
Electrostatic Discharge	(Human Body Model) QSS 009-105 (JESD22-A114B)	±3000 V
	(Charged Device Model) QSS 009-147 (JESD22-C101-A)	±1500 V
	(Machine Model) JESD22-A115-A	±200 V
Continuous power dissipation		See Thermal Information Table

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to network ground terminal.

THERMAL INFORMATION

THERMAL METRIC[1]		SN65LVPE501 RGE 24 PINS	UNITS
θ_{JA}	Junction-to-ambient thermal resistance[2]	46	°C/W
$\theta_{JC(TOP)}$	Junction-to-case(top) thermal resistance [3]	42	
θ_{JB}	Junction-to-board thermal resistance [4]	13	
ψ_{JT}	Junction-to-top characterization parameter [5]	0.5	
ψ_{JB}	Junction-to-board characterization parameter [6]	9	
$\theta_{JC(BOTTOM)}$	Junction-to-case(bottom) thermal resistance [7]	4	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
(3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
(4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
(5) The junction-to-top characterization parameter, ψ_{JT}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA}, using a procedure described in JESD51-2a (sections 6 and 7).
(6) The junction-to-board characterization parameter, ψ_{JB}, estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
(7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	3	3.3	3.6	V
$C_{COUPLING}$	AC Coupling Capacitor	75		200	nF
	Operating free-air temperature	–40		85	°C

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DEVICE PARAMETERS (under recommended operating conditions, unless otherwise noted)						
I_{CC}	Supply Current	$\overline{\text{RST}}$, DEx, EQx, OSx = NC, EN_RXD = NC, K28.5 pattern at 5 Gbps, V_{ID} = 1000m$V_{p\text{-}p}$		101	120	mA
ICC_{idle}	Supply Current	PS=1; When auto-low power conditions are met		21	26	mA
$ICC_{shut\text{-}down}$	Supply Current	$\overline{\text{RST}}$ = GND		0.2	1	mA
$ICC_{RX.Detect}$	Supply Current	$\overline{\text{RST}}$, EN_RXD = NC		2		mA
	Maximum Data Rate				5	Gbps
$AutoLP_{ENTRY}$	Auto Low Power Entry Time	Electrical Idle at Input, Refer to Figure 9	1.0	1.3		µs
$AutoLP_{EXIT}$	Auto Low Power Exit Time	After first signal activity, Refer to Figure 9		15	30	ns
t_{PU}	Power Up Time	Rx Detect Start Event, Vcc = Stable $\overline{\text{RST}}$, EN_RXD = H		15	30	µs
t_{DIS}	Sleep (shut-down) Mode Entry Time	$\overline{\text{RST}}$ H→L; EN_RXD=X			1	µs
T_{ENB}	Sleep (shut-down) Mode Exit Time	$\overline{\text{RST}}$ L→H; EN_RXD=H, Start of Ex detect event			10	µs
CONTROL LOGIC (under recommended operating conditions, unless otherwise noted)						
V_{IH}	High level Input Voltage		1.4		V_{CC}	V
V_{IL}	Low Level Input Voltage		–0.3		0.5	V
V_{HYS}	Input Hysteresis			150		mV
I_{IH}	High Level Input Current	OSx, EQx, DEx = V_{CC}			30	µA
		EN_RXD, $\overline{\text{RST}}$ = V_{CC}			1	µA
I_{IL}	Low Level Input Current	OSx, EQx, DEx = GND	–30			µA
		PS = GND	–1			µA
		EN_RXD, $\overline{\text{RST}}$ = GND	–20			µA
RECEIVER AC/DC (under recommended operating conditions, unless otherwise noted)						
Vin_{diff_pp}	RX1, RX2 Input Voltage Swing	AC coupled differential signal	100		1200	mVp-p
V_{CM_RX}	RX1, RX2 Common Mode Voltage		0		3.6	V
Vin_{COM_P}	RX1, RX2 AC Peak common mode voltage				150	mVP
Z_{DC_RX}	DC single ended impedance		40	50	60	Ω
Z_{diff_RX}	DC Differential Input impedance		80	100	120	Ω
$Z_{RX\_High\_IMP+}$	DC Input High Impedance	Device in sleep mode Rx termination not powered; Measured with respect to GND over 200mV max	50	74		kΩ
V_{EID_TH}	Electrical Idle Detect Threshold	Measured at receiver pin (see Figure 7)	65	84	175	mVpp
$RL_{RX\text{-}DIFF}$	Differential Return Loss	50 MHz – 1.25 GHz	10			dB
		1.25 GHz – 2.5 GHz; Operating temperature 0°C to 85°C	8			dB
		1.25 GHz – 2.5 GHz; Operating temperature –40°C to 85°C	7			dB
$RL_{RX\text{-}CM}$	Common Mode Return Loss	50 MHz – 2.5 GHz	10			dB

ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
TRANSMITTER AC/DC (under recommended operating conditions, unless otherwise noted)						
V_{TXDIFF_PP}	Differential peak-to-peak Output Voltage	R_L =100Ω ±1%, DEx, OS = NC, Transition Bit	800	1000	1200	mV
		R_L =100Ω ±1%, DEx = NC, OSx = GND Transition Bit		875		
		R_L =100Ω ±1%, DEx = NC, OSx = VCC Transition Bit		1100		
$V_{TXDIFF\_NTB\_PP}$		R_L =100Ω ±1%, DEx=NC, OSx = 0,1,NC Non-Transition Bit		655		mV
		R_L =100Ω ±1%, DEx=0,OSx = 0,1,NC Non-Transition Bit		495		
		R_L =100Ω ±1%, DEx=1, OSx = 0,1, NC Non-Transition Bit		350		
	De-Emphasis Level	DEx, OSx = NC, See Figure 11 ; (for OS1,2 = 1 and 0 see Table 2); Operating temperature 0°C to 85°C	–3.0	–3.7	–4.0	dB
		DEx, OSx = NC, See Figure 11 ; (for OS1,2 = 1 and 0 see Table 2); Operating temperature –40°C to 85°C	–3.0	–3.7	–4.2	
		DEx = 0, OSx = NC		–6.4		dB
		DEx = 1, OSx = NC		–9.4		
T_{DE}	De-Emphasis Width	At 5Gbps		0.8		UI
Z_{diff_TX}	DC Differential Impedance	Defined during signaling	80	100	120	Ω
RL_{diff_TX}	Differential Return Loss	f = 50 MHz – 1.25 GHz. Operating temperature 0°C to 85°C	10			dB
		f = 50 MHz – 1.25 GHz. Operating temperature –40°C to 85°C	9.5			
		f = 1.25 GHz – 2.5 GHz, Operating temperature 0°C to 85°C	6			
		f = 1.25 GHz – 2.5 GHz, Operating temperature –40°C to 85°C	5.5			
RL_{CM_TX}	Common Mode Return Loss	f = 50 MHz – 2.5 GHz	10			dB
I_{TX_SC}	TX short circuit current	TX± shorted to GND		60	90	mA
$V_{TX\_CM\_DC}$	Transmitter DC common-mode voltage	Allowed DC CM voltage at TX pins	2.1	2.65	3.1	V
$V_{TX\_CM\_AC2}$	TX AC common mode voltage at GEN II speed	$Max(V_{d+} + V_{d-})/2 – Min(V_{d+} + V_{d-})/2$		26	100	mVpp
$V_{TX\_CM\_AC1}$	TX AC common mode voltage at GEN I speed			2	20	mV
$V_{TX\_CM\_DeltaL0-L0s}$	Absolute Delta DC CM voltage during active and idle states	$\lvert V_{TX\_CM\_DC\ [L0]} – V_{TX\_CM\_DC\ [L0s]} \rvert$, PS=L	0		100	mV
$V_{TX\_CM-DC-Line-Delta}$	Absolute Delta of DC CM voltage between D+ and D–	$\lvert V_{TX\_CM\_DC-D+\ [L0]} – V_{TX\_CM\_DC-D-\ [L0]} \rvert$	0		25	mV
$V_{TX\_idle\_diff-AC-p}$	Electrical idle differential peak output voltage	$\lvert V_{TX-Idle-D+} – V_{TX-Idle-D–} \rvert$ HP filtered to remove any DC component	0	1	10	mVpp
$V_{TX\_idle\_diff-DC}$	DC Electrical idle differential output voltage	$\lvert V_{TX\_idle-D+} – V_{TX\_idle-D–} \rvert$ LP filtered to remove any AC component		3.5		mV
V_{detect}	Voltage change to allow receiver detect	Positive voltage to sense receiver			600	mV
t_R,t_F	Output Rise/Fall time	DEx = NC, OS = NC (CH 0 and CH 1) 20%-80% of differential voltage at the output; VID > 1000mVpp	30	53		ps
t_{RF_MM}	Output Rise/Fall time mismatch	DEx = NC, OS = NC (CH 0 and CH 1) 20%-80% of differential voltage at the output		1	20	ps
T_{diff_LH}, T_{diff_HL}	Differential Propagation Delay	DEx = NC (CH 0 and CH 1). Propagation delay between 50% level at input and output. See Figure 6		280	330	ps
$t_{idleEntry}$ $t_{idleExit}$	Idle entry and exit times	See Figure 7		4	6	ns
Tx EQUALIZATION at GEN II Speed (under recommenced operating conditions)						
T_{TX-TJ} (1)	Total Jitter	At point A in Figure 10 (2)		30	50	ps pp
		At point B in Figure 10 (2)		25	80	
T_{TX-DJ}	Deterministic Jitter	At point A in Figure 10 (2)		16	30	ps pp
		At point B in Figure 10 (2)		11	60	

(1) Includes RJ at 10^{-12}
(2) Refer to Figure 10 with ± K28.5 pattern at 5Gbps, –3.5dB DE from source AWG .

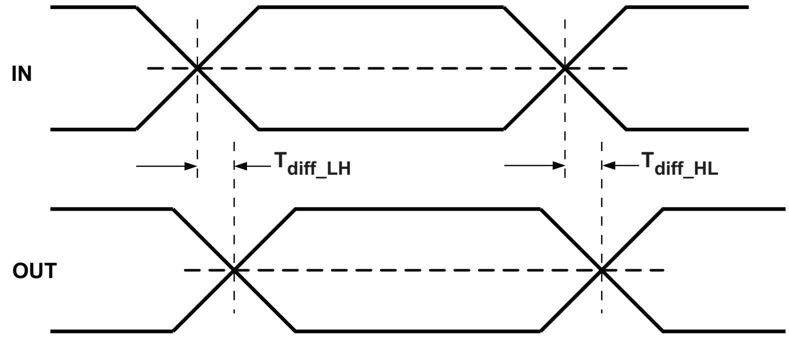


Figure 6. Propagation Delay

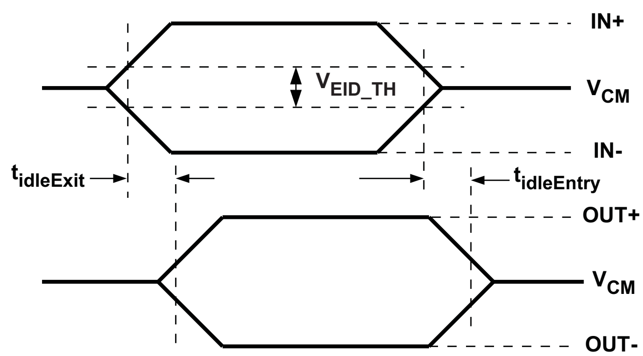


Figure 7. Idle Mode Exit and Entry Delay

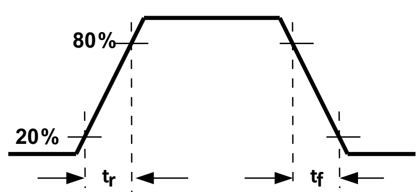


Figure 8. Output Rise and Fall Times

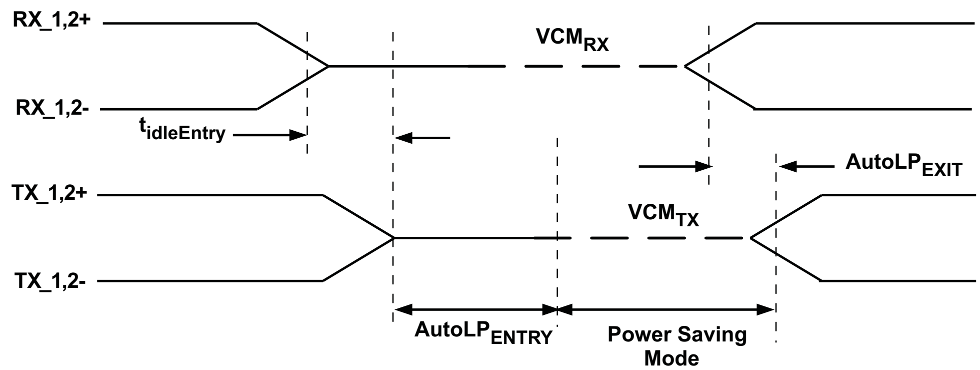


Figure 9. Auto Low Power Mode Timing (when enabled)

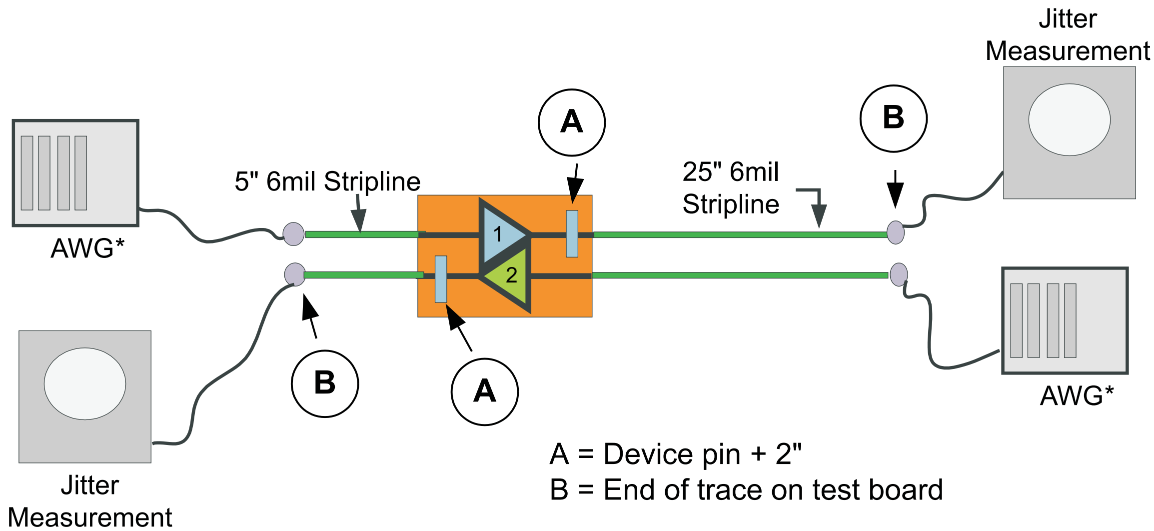


Figure 10. Jitter Measurement Setup

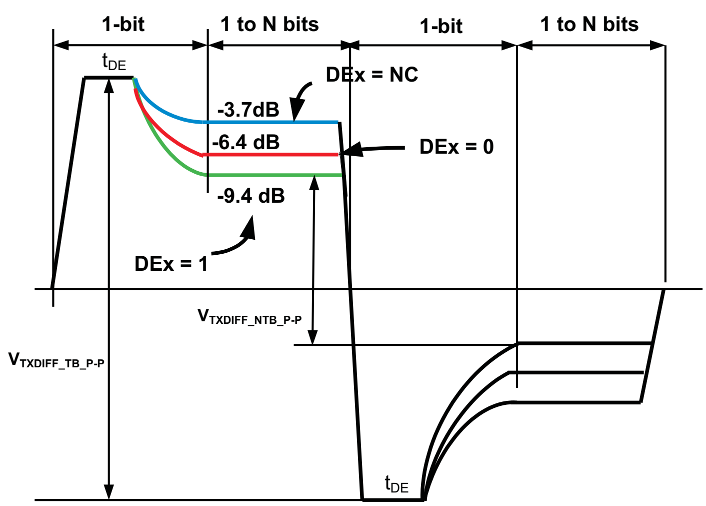


Figure 11. Output De-Emphasis Levels OSx = NC

Typical Eye Diagram and Performance Curves at Output

Input Signal Characteristics: Data Rate = 5 Gbps, V_{ID} = 1000 mVpp, DE = -3.5 dB, Pattern = K28.5
Device Operating Conditions: VCC = 3.3 V, Temp = 25°C
Device EQ settings (EQ/DE/OS) adjusted for best eye performance

Output Trace Length Held Constant and Input Trace Length Varied

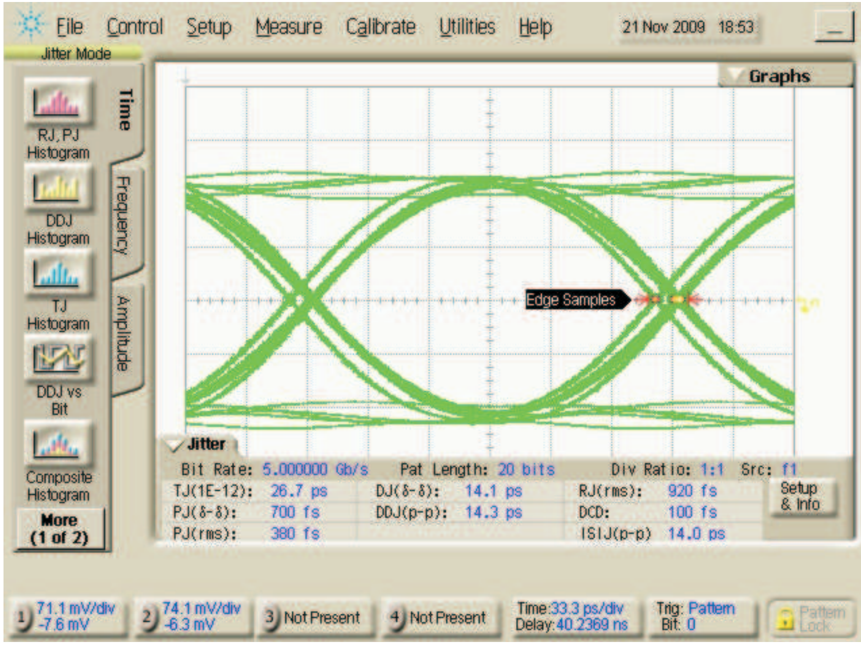


Figure 12. Input Trace = 4 Inches, 6 mil, and Measured at Output Trace = 4 Inches

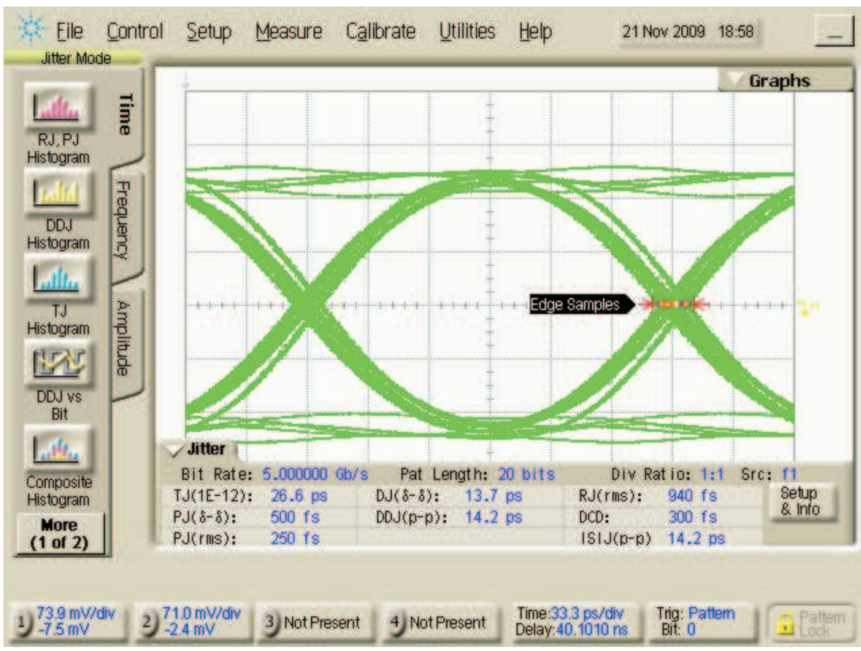


Figure 13. Input Trace = 20 Inches, 6 mil, and Measured at Output Trace = 4 Inches

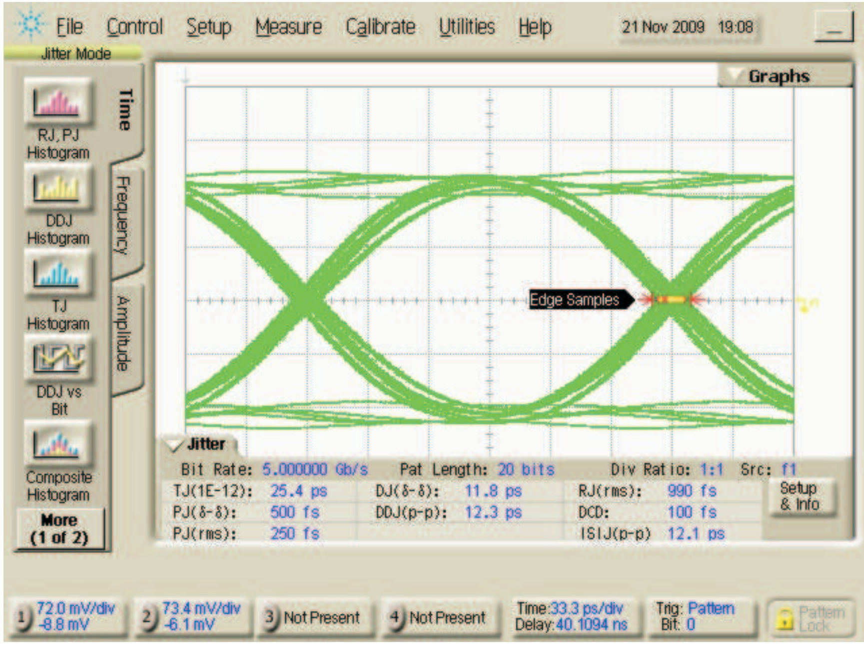


Figure 14. Input Trace = 32 Inches, 6 mil, and Measured at Output Trace = 4 Inches

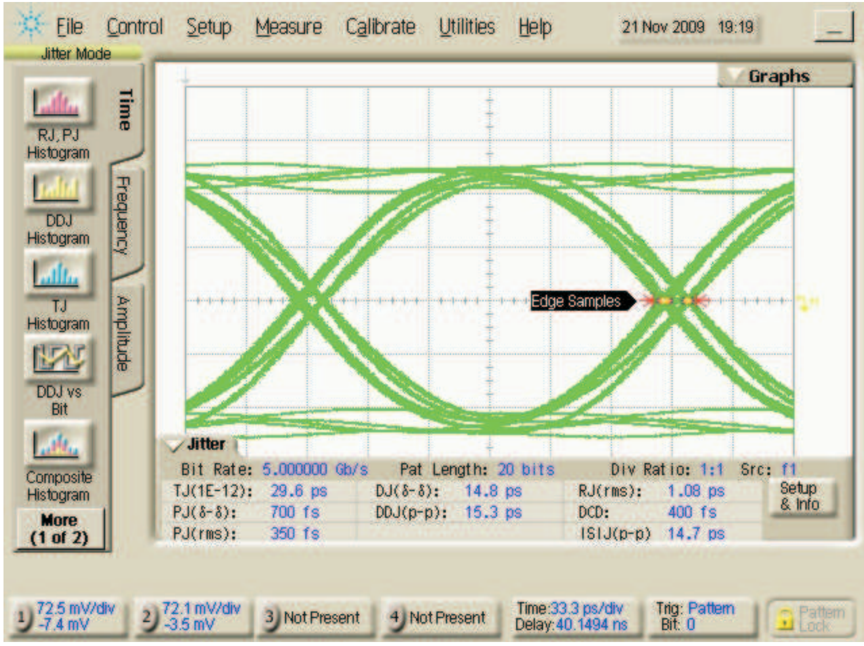


Figure 15. Input Trace = 44 Inches, 6 mil, and Measured at Output Trace = 4 Inches

Variable Trace Lengths at Input and Output

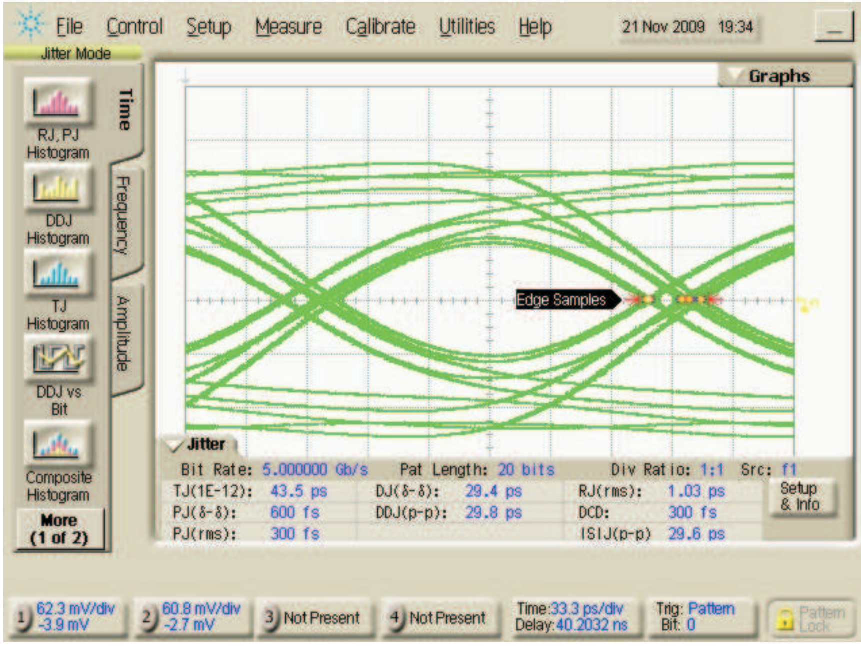


Figure 16. Input Trace = 28 Inches, 6 mil, and Measured at Output Trace = 24 Inches

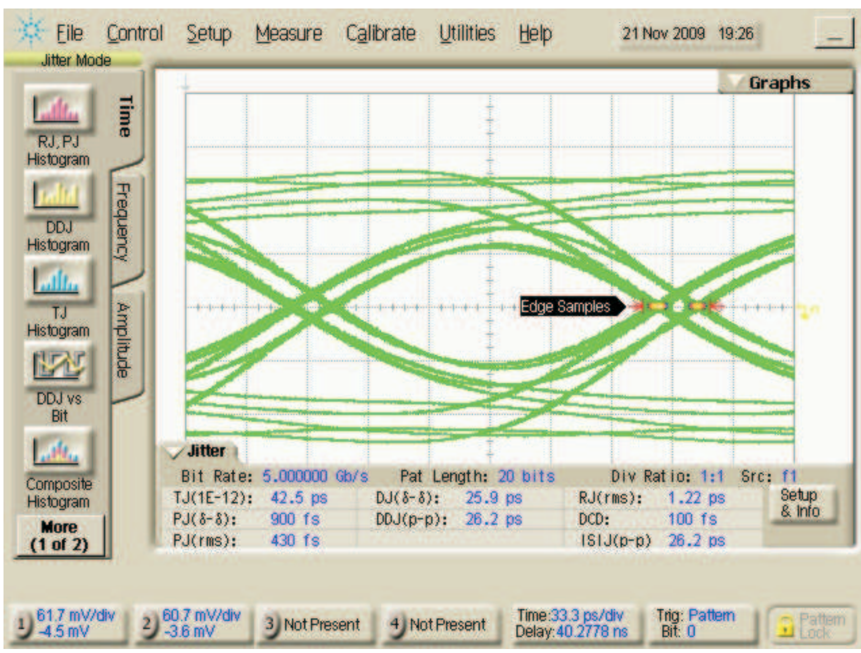


Figure 17. Input Trace = 44 Inches, 6 mil, and Measured at Output Trace = 24 Inches

REVISION HISTORY

Changes from Original (May 2010) to Revision A	Page
• Added Figure 4	7

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65LVPE501RGER	ACTIVE	VQFN	RGE	24	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVPE501	Samples
SN65LVPE501RGET	ACTIVE	VQFN	RGE	24	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LVPE501	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

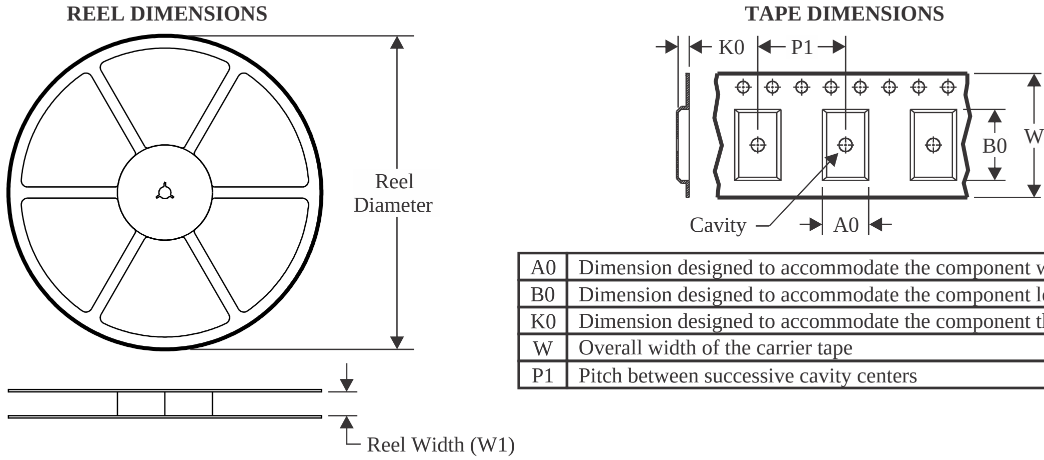
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

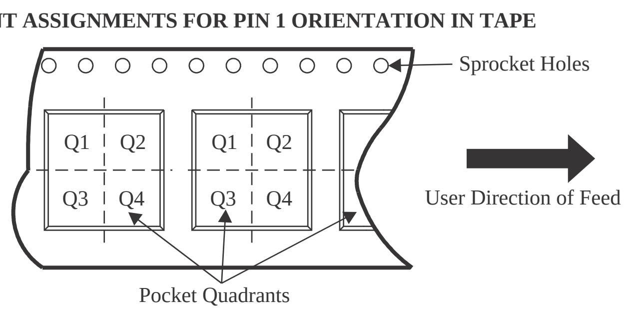
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION



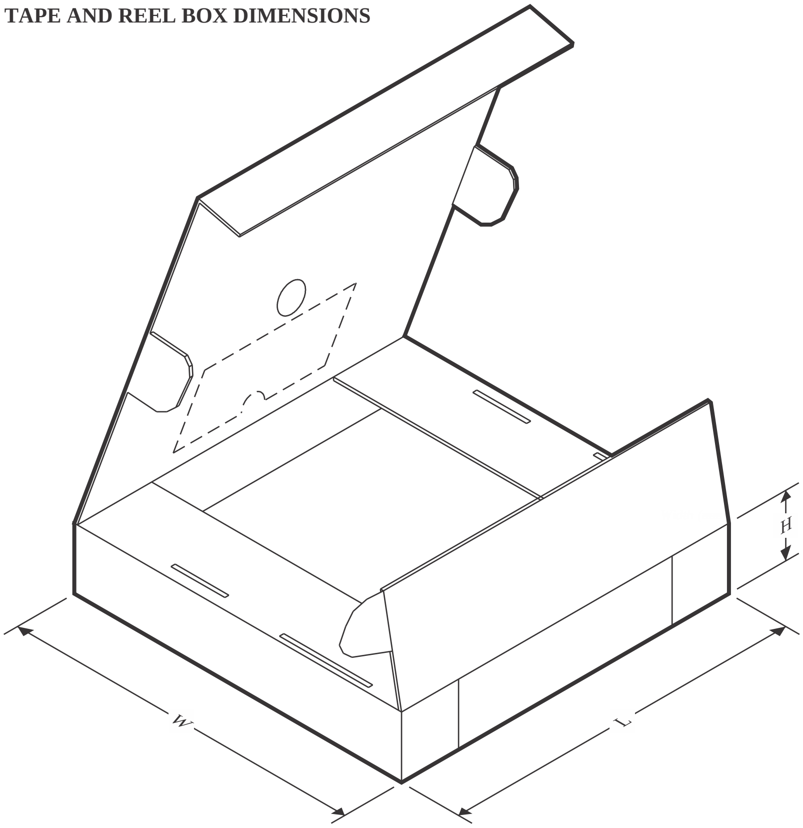
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LVPE501RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
SN65LVPE501RGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



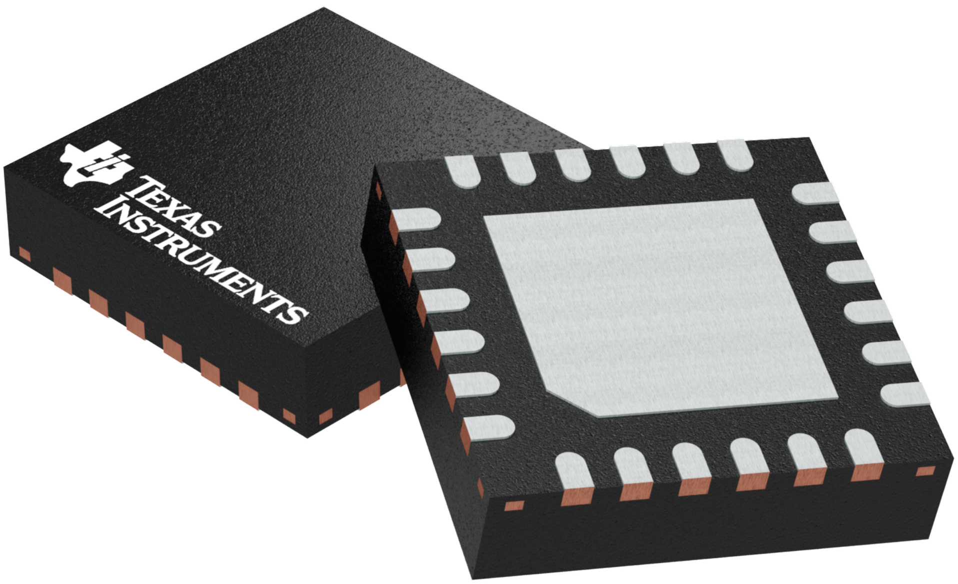
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LVPE501RGER	VQFN	RGE	24	3000	356.0	356.0	35.0
SN65LVPE501RGET	VQFN	RGE	24	250	210.0	185.0	35.0

RGE 24

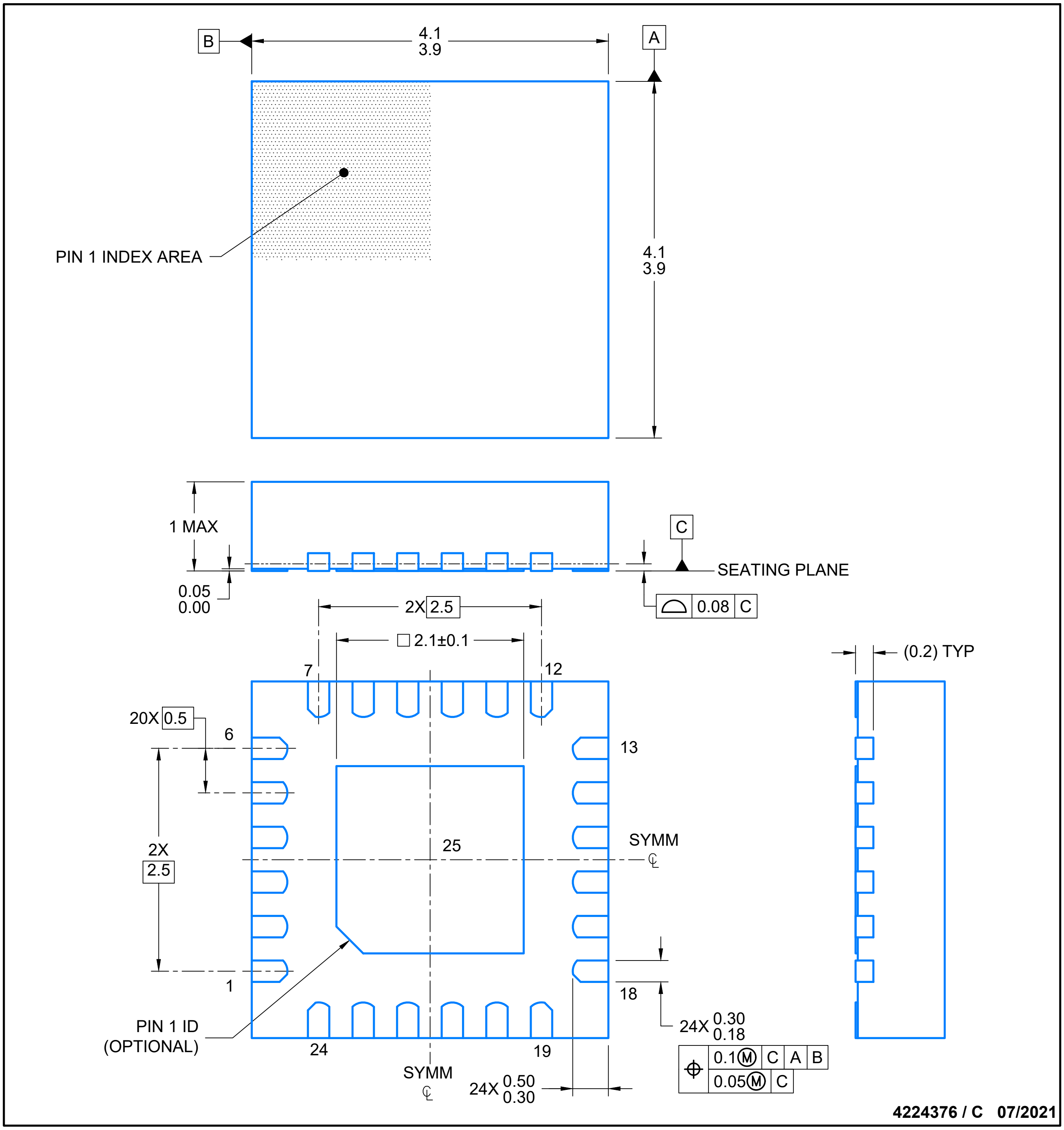
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



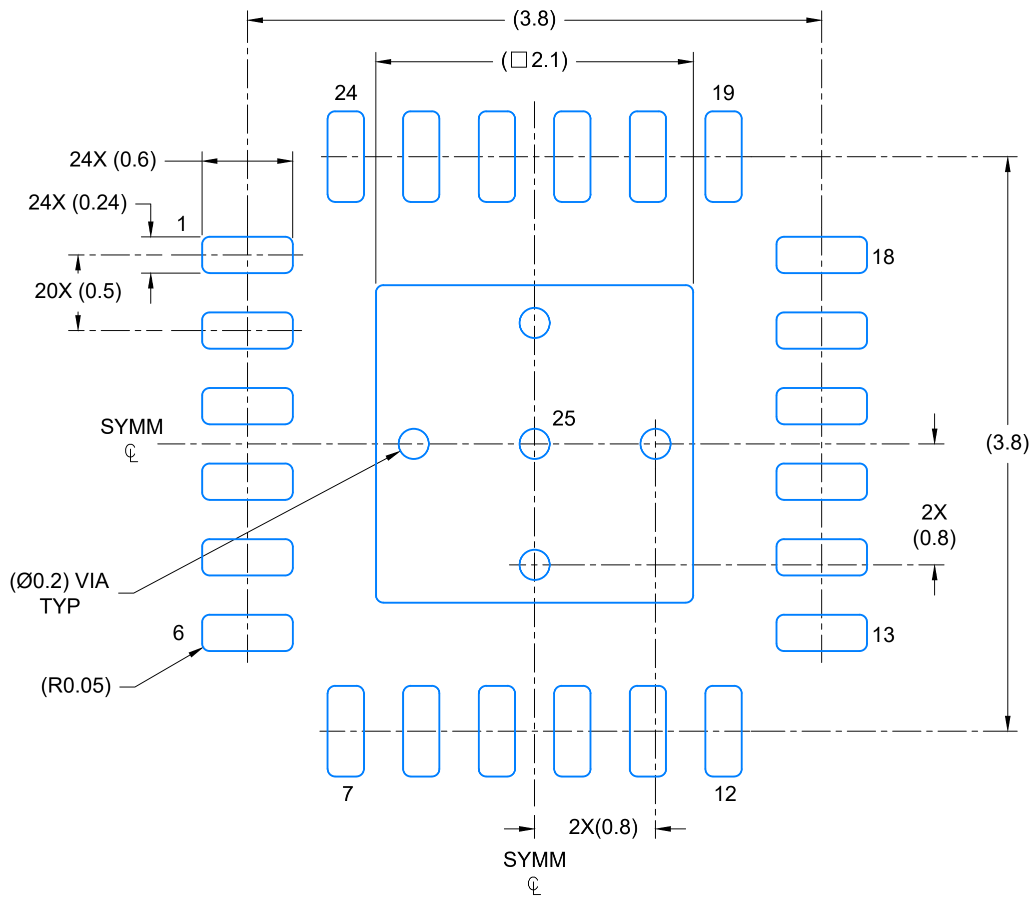
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4204104/H

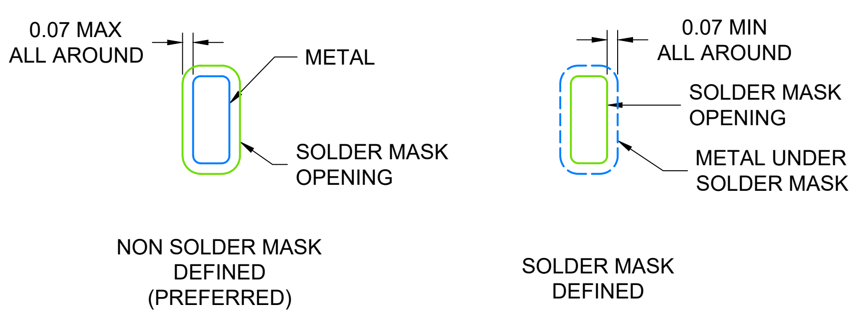


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE: 20X

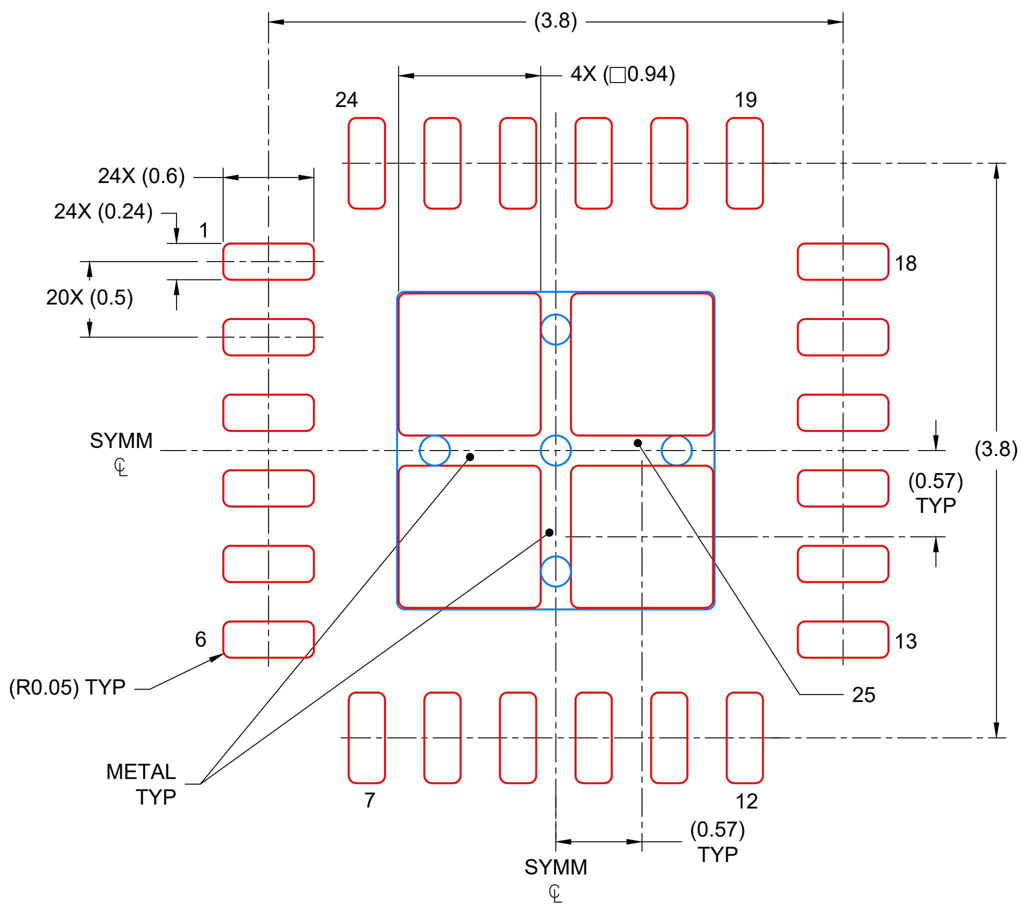


SOLDER MASK DETAILS

4224376 / C 06/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
80% PRINTED COVERAGE BY AREA
SCALE: 20X

4224376 / C 06/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..