SN65MLVD203B 具有 IEC ESD 保护功能的全双工 1 类多点 LVDS 收发器

1 特性

- 与 M-LVDS 标准 TIA/EIA-899 兼容，可进行多点数据交换
- 低电压差分 30Ω 至 55Ω 线路驱动器和接收器，信号传输速率(1) 高达 200Mbps，时钟频率高达 100MHz
  - 1 类接收器具有 25mV 迟滞
- 总线 I/O 保护
  - ±8kV HBM
  - ±8kV IEC 61000-4-2 接触放电
- 驱动器输出电压转换时间可控，可改善信号质量
- –1V 至 3.4V 共模电压范围，可实现在 2V 接地噪声下进行数据传输
- 总线引脚在禁用或 V_{CC} ≤ 1.5V 时具有高阻抗
- 提供 100Mbps 器件 (SN65MLVD202B)
- SN65MLVD203 的改进备选器件 [1]

2 应用

- TIA/EIA-485 的低功耗、高速和短距备选器件
- 背板或电缆式多点数据和时钟传输
- 蜂窝基站
- 局端交换机
- 网络交换机和路由器

3 说明

SN65MLVD203B 器件是一款多点低电压差分信号 (M-LVDS) 线路驱动器和接收器，经优化，能够以最高 200Mbps 的信号传输速率运行。该器件具有稳健耐用的 3.3V 驱动器和接收器，并且采用标准 QFN 封装，适用于严苛的工业应用。总线引脚可耐受 ESD 事件，具有针对人体模型和 IEC 接触放电规范的高级保护。

该器件包含一个差分驱动器和一个差分接收器（收发器），由 3.3V 电源供电。该收发器经过优化，能够以最高 200Mbps 的信号传输速率运行。

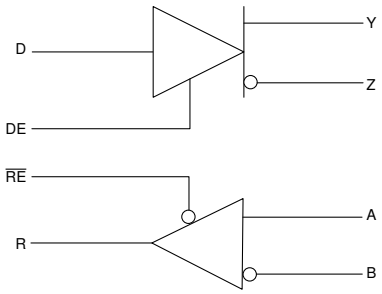
SN65MLVD203B 较同类器件具有增强特性。改进的特性包括驱动器输出端可控的压摆率，有助于尽量减少无端桩线的反射，从而提高信号完整性。这些器件的额定工作温度范围为 -40°C 至 125°C。

SN65MLVD203B M-LVDS 接收器是 TI 广泛的 M-LVDS 产品系列的其中一款器件。

封装信息(1)

器件型号	封装	封装尺寸（标称值）
SN65MLVD203B	RUM（WQFN，16）	4.00mm × 4.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



简化版原理图，SN65MLVD203B

[1] 线路的信号传输速率是指每秒钟的电压转换次数，单位为 bps（每秒比特数）。

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision A (November 2020) to Revision B (November 2022) **Page**

- 将*器件信息*表更改为*封装信息* 1
- 更新了*绝对最大额定值*一节中的表注 4
- 更新了“ESD 等级”一节中的 CDM 测试 4
- Added *RX Maximum Jitter While DE Toggling* section 16
- Moved the *Power Supply Recommendations* and *Layout* sections to the *Application and Implementation* section 23

Changes from Revision * (September 2020) to Revision A (November 2020) **Page**

- 将器件状态更新为*量产数据* 1
- 在“电气特性 - 驱动器”中，将 I_{IL}（最小值）从 0μA 更改为 -1μA 5
- 在“电气特性 - 接收器”中，将 I_{IH}（最大值）从 0μA 更改为 1μA 7
- 在“开关特性 - 驱动器”中，删除了 $t_{sk(p)}$ 脉冲偏斜规格 7
- 将禁用时间高电平至高阻抗输出从典型值 4ns 更改为典型值 5ns 7
- 将禁用时间低电平至高阻抗输出从典型值 4ns 更改为典型值 5ns 7
- 在“开关特性 - 接收器”中，将 $t_{sk(p)}$ 脉冲偏斜最大值从 300ps 更改为 600ps，并将典型值从 100ps 更改为 80ps 8

5 Pin Configuration and Functions

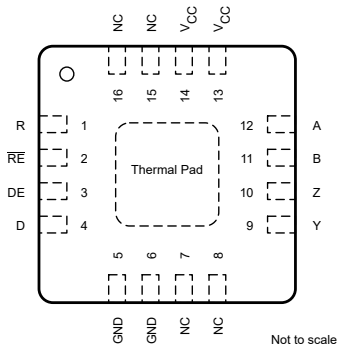


图 5-1. RUM Package, 16-Pin WQFN (Top View)

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
R	1	Output	Receiver output
$\overline{RE}$	2	Input	Receiver enable pin; High = Disable, Low = Enable
DE	3	Input	Driver enable pin; High = Enable, Low = Disable
D	4	Input	Driver input
GND	5	Power	Supply ground
GND	6	Power	Supply ground
NC	7	NC	No internal connection
NC	8	NC	No internal connection
Y	9	Output	Differential output
Z	10	Output	Differential output
B	11	Input	Differential input
A	12	Input	Differential input
V_{CC}	13	Power	Power supply, 3.3 V
V_{CC}	14	Power	Power supply, 3.3 V
NC	15	NC	No internal connection
NC	16	NC	No internal connection
Thermal Pad		Power	Thermal pad. Connect to a solid ground plane.

6 Specifications

6.1 绝对最大额定值

在自然通风条件下的工作温度范围内测得 (除非另有说明) (1)

		最小值	最大值	单位
电源电压范围 V_{CC} (2)		-0.5	4	V
输入电压范围	D、DE、$\overline{RE}$	-0.5	4	V
	A、B	-4	6	V
输出电压范围	R	-0.3	4	V
	Y、Z	-1.8	4	V
连续功耗		请参阅*热性能信息*表		
贮存温度，T_{stg}		-65	150	°C

(1) 超出*绝对最大额定值*的运行可能会对器件造成永久损坏。*绝对最大额定值*并不表示器件在这些条件下或在*建议运行条件*以外的任何其他条件下能够正常运行。如果超出*建议运行条件*、但在*绝对最大额定值*范围内使用，器件可能不会完全正常运行，这可能影响器件的可靠性、功能和性能并缩短器件寿命。
(2) 除差分 I/O 总线电压外的所有电压值都是相对于网络接地引脚的值。

6.2 ESD 等级

				值	单位
$V_{(ESD)}$	静电放电	接触放电，符合 IEC 61000-4-2 标准	A、B、Y 和 Z	±8000	V
		人体放电模型 (HBM)，符合 ANSI/ESDA/JEDEC JS-001，所有引脚(1)	A、B、Y 和 Z	±8000	
			除 A、B、Y 和 Z 外的所有引脚	±4000	
		充电器件模型 (CDM)，符合 JEDEC JS-002，所有引脚(2)	所有引脚	±1500	

(1) JEDEC 文档 JEP155 指出：500V HBM 可实现在标准 ESD 控制流程下安全生产。
(2) JEDEC 文档 JEP157 指出：250V HBM 可实现在标准 ESD 控制流程下安全生产。

6.3 建议运行条件

在自然通风条件下的工作温度范围内测得 (除非另有说明)

		最小值	标称值	最大值	单位
V_{CC}	电源电压	3	3.3	3.6	V
V_{IH}	高电平输入电压	2		V_{CC}	V
V_{IL}	低电平输入电压	0		0.8	V
	任何总线端子 V_A、V_B、V_Y 或 V_Z 上的电压	-1.4		3.8	V
$\|V_{ID}\|$	差分输入电压幅度			V_{CC}	V
R_L	差分负载电阻	30	50		Ω
$1/t_{UI}$	信令速率			200	Mbps
T_A	自然通风工作温度，采用 RUM 封装	-40		125	°C

6.4 热性能信息

热指标(1)		SN65MLVD203B RUM (WQFN) 16 引脚	单位
$R_{\theta JA}$	结至环境热阻	39.0	°C/W
$R_{\theta JC(top)}$	结至外壳（顶部）热阻	34.7	
$R_{\theta JB}$	结至电路板热阻	17.7	
ψ_{JT}	结至顶部特征参数	0.6	
ψ_{JB}	结至电路板特征参数	17.7	
$R_{\theta JC(bot)}$	结至外壳（底部）热阻	7.5	

(1) 有关传统和新热指标的更多信息，请参阅半导体和 IC 封装热指标应用报告。

6.5 电气特性

在建议运行条件下测得（除非另有说明）(1)

参数			测试条件	最小值	典型值	最大值	单位
I_{CC}	电源电流	仅驱动器	$\overline{RE}$ 和 DE（V_{CC} 时），R_L = 50Ω，所有其他均为开路		13	22	mA
		两者都禁用	$\overline{RE}$（V_{CC} 时），DE（0V 时），R_L = 空载，所有其他均为开路		1	4	
		两者都启用	$\overline{RE}$（0V 时），DE（V_{CC} 时），R_L = 50Ω，所有其他均为开路		16	24	
		仅接收器	$\overline{RE}$（0V 时），DE（0V 时），所有其他均为开路		4	13	
P_D	器件功率耗散		R_L = 50Ω，D 的输入为 50MHz 50% 占空比方波，DE = 高电平，$\overline{RE}$ = 低电平，T_A = 85°C			100	mW

(1) 所有典型值均在 25°C 和 3.3V 电源电压条件下测得。

6.6 电气特性 - 驱动器

在建议运行条件下测得（除非另有说明）

参数		测试条件	最小值(1)	典型值(2)	最大值	单位
$\lvert V_{YZ}\rvert$	差分输出电压幅度(4)	请参阅图 7-2	480		650	mV
$\Delta\lvert V_{YZ}\rvert$	逻辑状态之间的差分输出电压幅度变化		-50		50	mV
$V_{OS(SS)}$	稳定状态共模输出电压	请参阅图 7-3	0.8		1.2	V
$\Delta V_{OS(SS)}$	逻辑状态之间的稳态共模输出电压变化		-50		50	mV
$V_{OS(PP)}$	峰峰值共模输出电压				150	mV
$V_{Y(OC)}$	最大稳态开路输出电压	请参阅图 7-7	0		2.4	V
$V_{Z(OC)}$	最大稳态开路输出电压		0		2.4	V
$V_{P(H)}$	电压过冲，低电平至高电平输出	请参阅图 7-5			$1.2V_{SS}$	V
$V_{P(L)}$	电压过冲，高电平至低电平输出		$-0.2V_{SS}$			V
I_{IH}	高电平输入电流（D、DE）	V_{IH} = 2V 至 V_{CC}	0		10	μA
I_{IL}	低电平输入电流（D、DE）	V_{IL} = GND 至 0.8V	-1		10	μA
$\lvert I_{OS}\rvert$	差分短路输出电流幅度	请参阅图 7-4			24	mA
I_{OZ}	高阻抗状态输出电流（仅驱动器）	–1.4V ≤（V_Y 或 V_Z）≤ 3.8V，其他输出 = 1.2V	-15		10	μA
$I_{O(OFF)}$	断电输出电流	–1.4V ≤（V_Y 或 V_Z）≤ 3.8V，其他输出 = 1.2V，0V ≤ V_{CC} ≤ 1.5V	-10		10	μA

在建议运行条件下测得（除非另有说明）

参数		测试条件	最小值(1)	典型值(2)	最大值	单位
C_Y 或 C_Z	输出电容	V_I = 0.4 sin(30E6 π t) + 0.5V(3)，其他输入为 1.2V，禁用驱动器		6		pF
C_{YZ}	差分输出电容	V_{AB} = 0.4 sin(30E6 π t)V(3)，禁用驱动器		4.5		pF
$C_{Y/Z}$	输出电容平衡，(C_Y/C_Z)		0.98		1.02	

(1) 本数据表采用将最小正值（最大负值）指定为最小值的代数约定。
(2) 所有典型值均在 25°C 和 3.3V 电源电压条件下测得。
(3) HP4194A 阻抗分析仪（或等效产品）
(4) –40°C 时的测量设备精度为 10mV

6.7 电气特性 - 接收器

在建议运行条件下测得（除非另有说明）

参数			测试条件	最小值	典型值 (1)	最大值	单位
V_{IT+}	正向差分输入电压阈值(2)	1 型	请参阅图 7-9 和表 7-1			50	mV
V_{IT-}	负向差分输入电压阈值(2)	1 型		-50			mV
V_{HYS}	差分输入电压迟滞，(V_{IT+} – V_{IT-})	1 型			25		mV
V_{OH}	高电平输出电压 (R)		I_{OH} = –8 mA	2.4			V
V_{OL}	低电平输出电压 (R)		I_{OL}=8mA			0.4	V
I_{IH}	高电平输入电流 ($\overline{RE}$)		V_{IH} = 2V 至 V_{CC}	-10		1	μA
I_{IL}	低电平输入电流 ($\overline{RE}$)		V_{IL} = GND 至 0.8V	-10		0	μA
I_{OZ}	高阻抗输出电流 (R)		V_O = 0 V 或 3.6 V	-10		15	μA
C_A 或 C_B	输入电容		V_I = 0.4 sin(30E6 π t) + 0.5V(3)，其他输入为 1.2V		6		pF
C_{AB}	差分输入电容		V_{AB} = 0.4 sin(30E6 π t)V(3)		4.5		pF
$C_{A/B}$	输入电容平衡，(C_A/C_B)			0.94		1.06	

(1) 所有典型值均在 25°C 和 3.3V 电源电压条件下测得。
(2) -40℃ 时的测量设备精度为 10mV
(3) HP4194A 阻抗分析仪（或等效产品）

6.8 开关特性 - 驱动器

在建议运行条件下测得（除非另有说明）

参数		测试条件	最小值	典型值 (1)	最大值	单位
t_{pLH}	传播延时，低至高电平输出	请参阅 图 7-5	2	2.5	3.5	ns
t_{pHL}	传播延时，高至低电平输出		2	2.5	3.5	ns
t_r	差分输出信号上升时间			2.0		ns
t_f	差分输出信号下降时间			2.0		ns
$t_{sk(pp)}$	器件间偏斜(2)				0.9	ns
$t_{jit(per)}$	周期抖动，rms（1 个标准差）(3)	62.5MHz 时钟输入(4)			5	ps
$t_{jit(per)}$	周期抖动，rms（1 个标准差）(3)	100MHz 时钟输入(4)			2	ps
$t_{jit(pp)}$	峰峰值抖动(3) (6)	125Mbps 8b10b 输入(5)			250	ps
$t_{jit(pp)}$	峰峰值抖动(3) (6)	200Mbps 8b10b 输入(5)			325	ps
$t_{jit(pp)}$	峰峰值抖动(3) (6)	200Mbps 2^{15} – 1 PRBS 输入(5)			325	ps
t_{PHZ}	禁用时间，高电平至高阻抗输出	请参阅图 7-6		5	7	ns
t_{PLZ}	禁用时间，低电平至高阻抗输出			5	7	ns
t_{PZH}	启用时间，高阻抗至高电平输出			4	7	ns
t_{PZL}	启用时间，高阻抗至低电平输出			4	7	ns

(1) 所有典型值均在 25°C 和 3.3V 电源电压条件下测得。
(2) 器件间偏斜定义为在相同 V/T 条件下运行的两个器件之间的传播延迟差异。
(3) 抖动由设计和特性来确保。已从数字中减去激励抖动。
(4) t_r = t_f = 0.5ns（10% 至 90%），对 30K 个样本测得。
(5) t_r = t_f = 0.5ns（10% 至 90%），对 100K 个样本测得。
(6) 峰峰值抖动包括脉冲偏斜 ($t_{sk(p)}$) 引起的抖动。

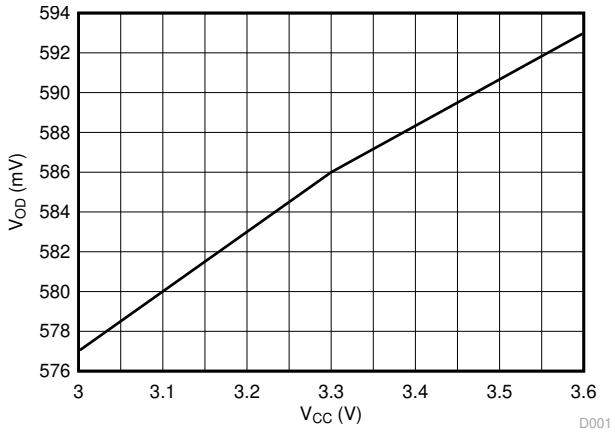
6.9 开关特性 - 接收器

在建议运行条件下测得（除非另有说明）

参数			测试条件	最小值	典型值 (1)	最大值	单位
t_{PLH}	传播延时，低至高电平输出		C_L = 15pF，请参阅图 7-10	2	6	10	ns
t_{PHL}	传播延时，高至低电平输出			2	6	10	ns
t_r	输出信号上升时间					2.3	ns
t_f	输出信号下降时间					2.3	ns
$t_{sk(p)}$	脉冲偏斜 ($\lvert t_{pHL} - t_{pLH} \rvert$)	1 型	C_L = 15pF，请参阅图 7-10		80	600	ps
$t_{sk(pp)}$	器件间偏斜(2)		C_L = 15pF，请参阅图 7-10			1	ns
$t_{jit(per)}$	周期抖动，rms（1 个标准差）(3)		62.5MHz 时钟输入(4)			5	ps
$t_{jit(per)}$	周期抖动，rms（1 个标准差）(3)		100MHz 时钟输入(4)			3	ps
$t_{jit(pp)}$	峰峰值抖动(3) (6)	1 型	125Mbps 8b10b 输入(5)			130	ps
$t_{jit(pp)}$	峰峰值抖动(3) (6)	1 型	200Mbps 8b10b 输入(5)			250	ps
$t_{jit(pp)}$	峰峰值抖动(3) (6)	1 型	200Mbps 2^{15} – 1 PRBS 输入(5)			300	ps
t_{PHZ}	禁用时间，高电平至高阻抗输出		请参阅图 7-11		6	10	ns
t_{PLZ}	禁用时间，低电平至高阻抗输出				6	10	ns
t_{PZH}	启用时间，高阻抗至高电平输出				10	15	ns
t_{PZL}	启用时间，高阻抗至低电平输出				10	15	ns

(1) 所有典型值均在 25°C 和 3.3V 电源电压条件下测得。
(2) 器件间偏斜定义为在相同 V/T 条件下运行的两个器件之间的传播延迟差异。
(3) 抖动由设计和特性来确保。已从数字中减去激励抖动。
(4) V_{ID} = 200mV$_{pp}$，V_{cm} = 1V，t_r = t_f = 0.5ns（10% 至 90%），对 30K 个样本测得。
(5) V_{ID} = 200mV$_{pp}$，V_{cm} = 1V，t_r = t_f = 0.5ns（10% 至 90%），对 100K 个样本测得。
(6) 峰峰值抖动包括脉冲偏斜 ($t_{sk(p)}$) 引起的抖动

6.10 Typical Characteristics



T_A = 25°C

图 6-1. Differential Output Voltage vs Supply Voltage

7 Parameter Measurement Information

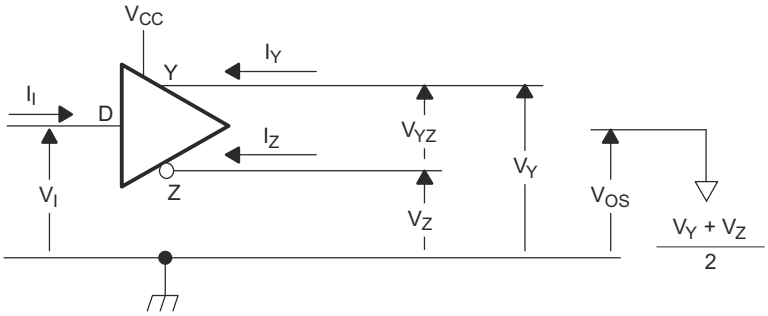
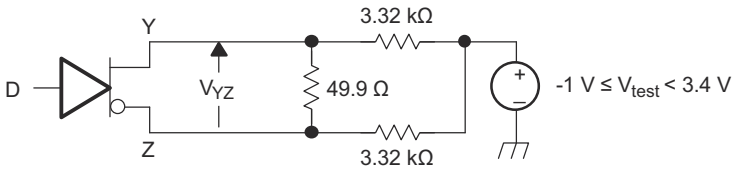
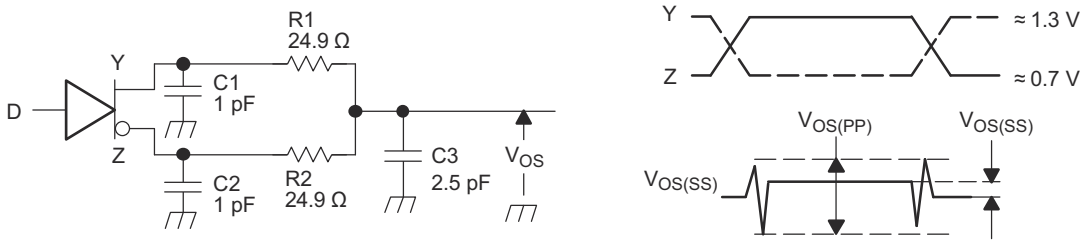


图 7-1. Driver Voltage and Current Definitions



A. All resistors are 1% tolerance.

图 7-2. Differential Output Voltage Test Circuit



A. All input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 1 ns, pulse frequency = 1 MHz, duty cycle = 50 ± 5%.
B. C1, C2 and C3 include instrumentation and fixture capacitance within 2 cm of the D.U.T. and are ±20%.
C. R1 and R2 are metal film, surface mount, ±1%, and located within 2 cm of the D.U.T.
D. The measurement of $V_{OS(PP)}$ is made on test equipment with a -3 dB bandwidth of at least 1 GHz.

图 7-3. Test Circuit and Definitions for the Driver Common-Mode Output Voltage

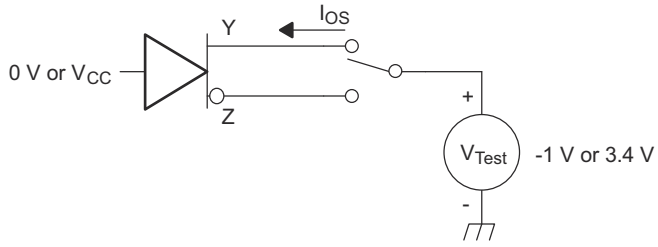
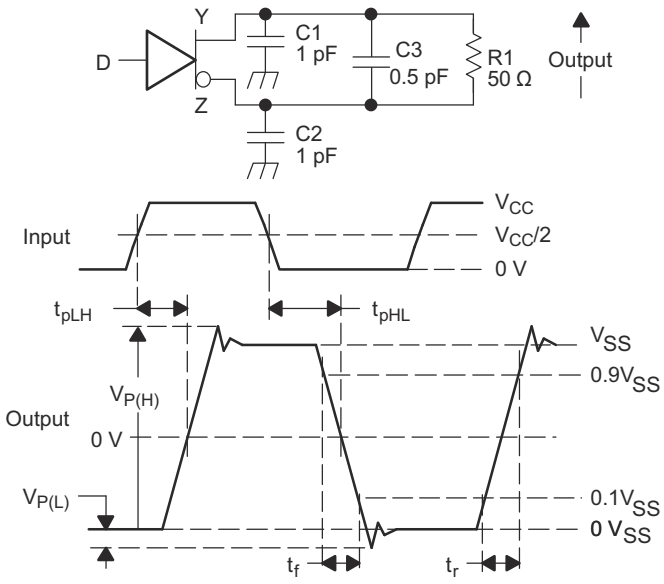
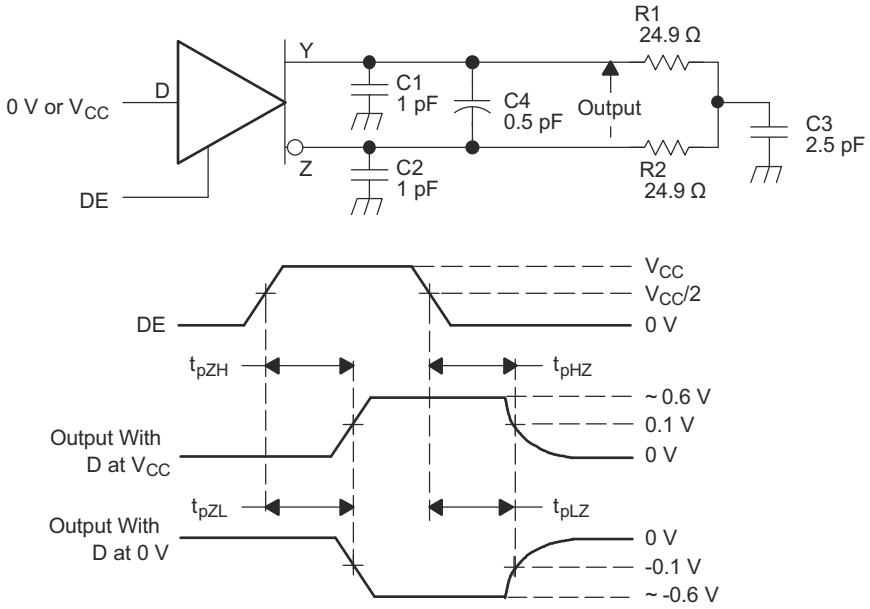


图 7-4. Driver Short-Circuit Test Circuit



A. All input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 1 ns, frequency = 1 MHz, duty cycle = 50 ± 5%.
B. C1, C2, and C3 include instrumentation and fixture capacitance within 2 cm of the D.U.T. and are ±20%.
C. R1 is a metal film, surface mount, and 1% tolerance and located within 2 cm of the D.U.T.
D. The measurement is made on test equipment with a -3 dB bandwidth of at least 1 GHz.

图 7-5. Driver Test Circuit, Timing, and Voltage Definitions for the Differential Output Signal



A. All input pulses are supplied by a generator having the following characteristics: t_r or t_f ≤ 1 ns, frequency = 1 MHz, duty cycle = 50 ± 5%.
B. C1, C2, C3, and C4 includes instrumentation and fixture capacitance within 2 cm of the D.U.T. and are ±20%.
C. R1 and R2 are metal film, surface mount, and 1% tolerance and located within 2 cm of the D.U.T.
D. The measurement is made on test equipment with a -3 dB bandwidth of at least 1 GHz.

图 7-6. Driver Enable and Disable Time Circuit and Definitions

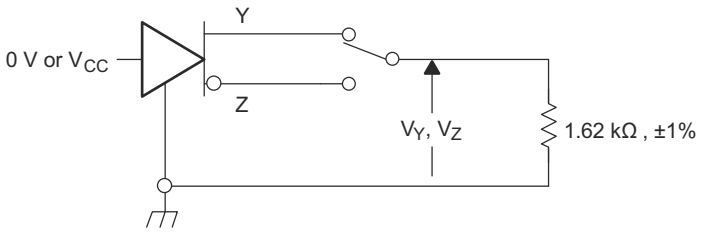
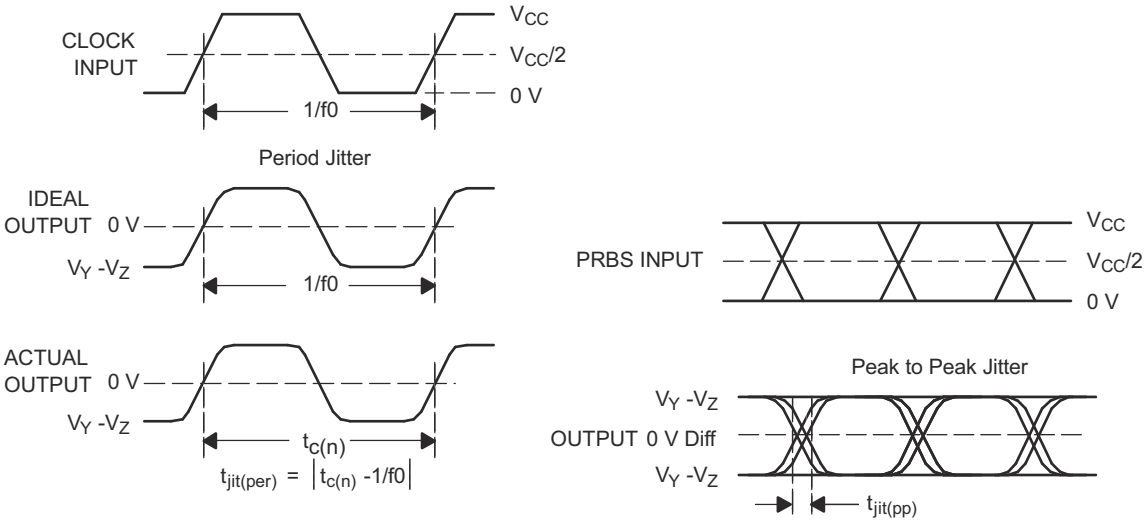


图 7-7. Maximum Steady State Output Voltage



A. All input pulses are supplied by an Agilent 81250 Stimulus System.
B. The measurement is made on a TEK TDS6604 running TDSJIT3 application software
C. Period jitter is measured using a 100 MHz 50 ±1% duty cycle clock input.
D. Peak-to-peak jitter is measured using a 200 Mbps 2^{15} – 1 PRBS input.

图 7-8. Driver Jitter Measurement Waveforms

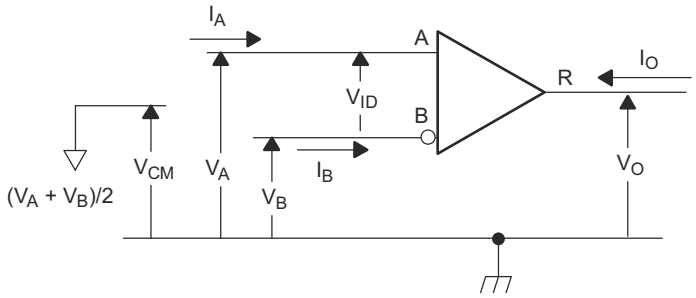
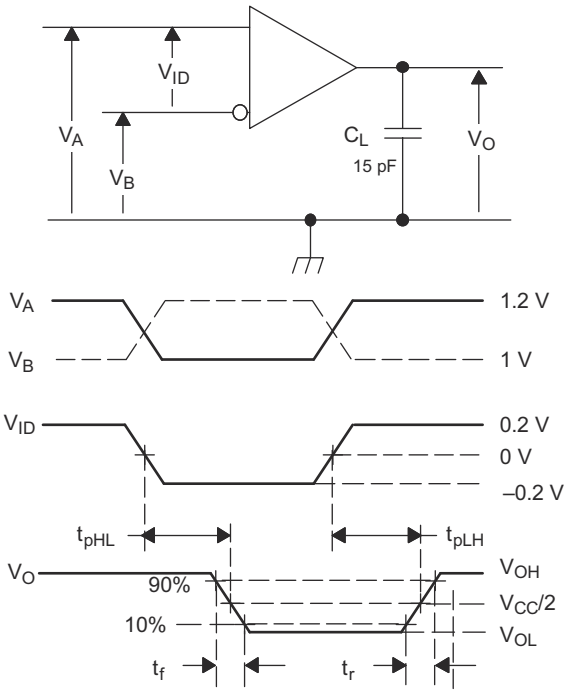


图 7-9. Receiver Voltage and Current Definitions

表 7-1. Type-1 Receiver Input Threshold Test Voltages

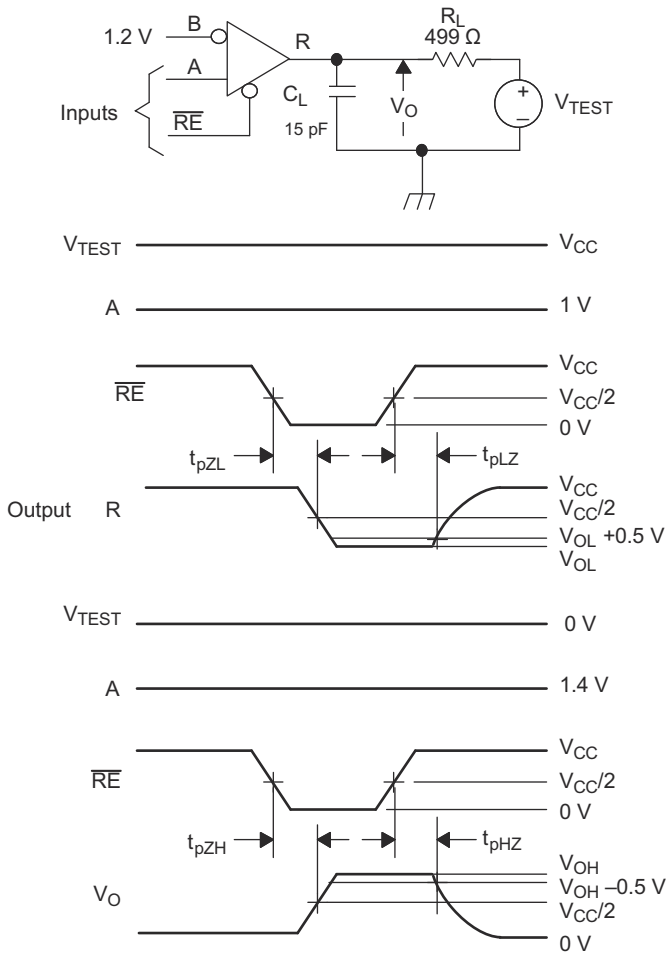
APPLIED VOLTAGES		RESULTING DIFFERENTIAL INPUT VOLTAGE	RESULTING COMMON-MODE INPUT VOLTAGE	RECEIVER OUTPUT
V_{IA}	V_{IB}	V_{ID}	V_{IC}	
2.400	0.000	2.400	1.200	H
0.000	2.400	– 2.400	1.200	L
3.425	3.375	0.050	3.4	H
3.375	3.425	– 0.050	3.4	L
– 0.975	– 1.025	0.050	– 1	H
– 1.025	– 0.975	– 0.050	– 1	L



A. All input pulses are supplied by a generator having the following characteristics: t_r or t_f ⩽ 1 ns, frequency = 1 MHz, duty cycle = 50 ± 5%. C_L is a combination of a 20%-tolerance, low-loss ceramic, surface-mount capacitor and fixture capacitance within 2 cm of the D.U.T.

B. The measurement is made on test equipment with a – 3 dB bandwidth of at least 1 GHz.

图 7-10. Receiver Timing Test Circuit and Waveforms

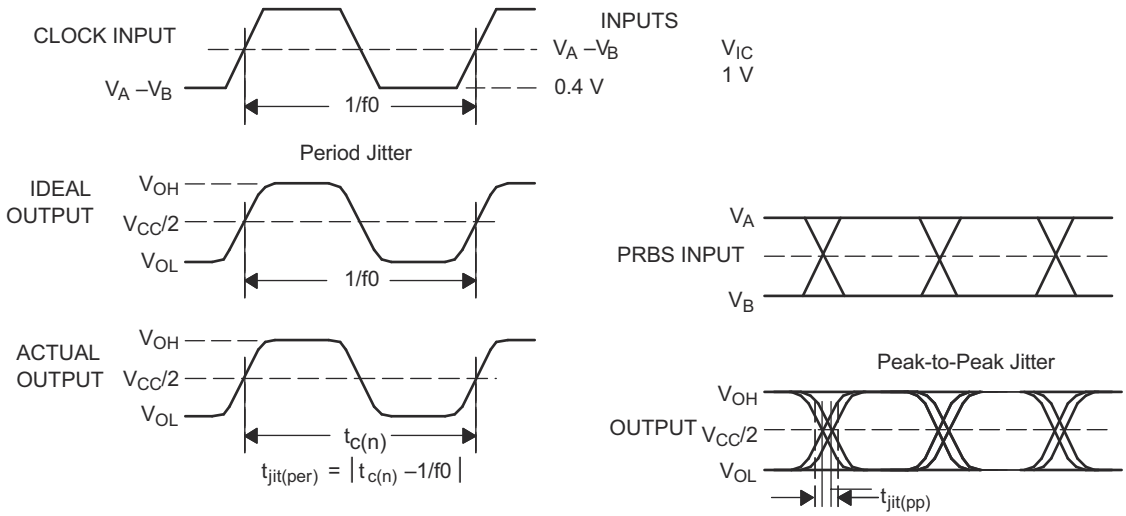


A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leqslant 1$ ns, frequency = 1 MHz, duty cycle = 50 ± 5%.

B. R_L is 1% tolerance, metal film, surface mount, and located within 2 cm of the D.U.T.

C. C_L is the instrumentation and fixture capacitance within 2 cm of the DUT and ±20%.

图 7-11. Receiver Enable and Disable Time Test Circuit and Waveforms



A. All input pulses are supplied by an Agilent 8304A Stimulus System.
B. The measurement is made on a TEK TDS6604 running TDSJIT3 application software
C. Period jitter is measured using a 10 MHz 50 ±1% duty cycle clock input.
D. Peak-to-peak jitter is measured using a 200 Mbps 2^{15}-1 PRBS input.

图 7-12. Receiver Jitter Measurement Waveforms

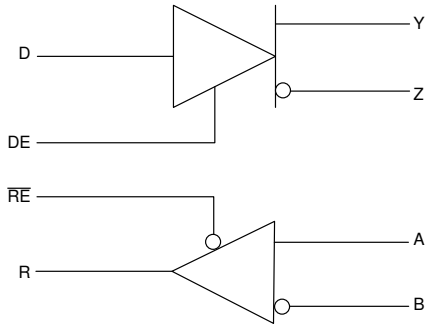
8 Detailed Description

8.1 Overview

The SN65MLVD203B is a multipoint-low-voltage differential (M-LVDS) line driver and receiver, which is optimized to operate at signaling rates up to 200 Mbps. the device complies with the multipoint low-voltage differential signaling (M-LVDS) standard TIA/EIA-899. These circuit is similar to the TIA/EIA-644 standard compliant LVDS counterpart, with added features to address multipoint applications. The driver output has been designed to support multipoint buses presenting loads as low as 30 Ω, and incorporates controlled transition times to allow for stubs off of the backbone transmission line.

The SN65MLVD203B has a Type-1 receivers exhibit 25 mV of differential input voltage hysteresis to prevent output oscillations with slowly changing signals or loss of input.

8.2 Functional Block Diagrams



8.3 Feature Description

8.3.1 Power-On-Reset

The SN65MLVD203B operates and meets all the specified performance requirements for supply voltages in the range of 3 V to 3.6 V. When the supply voltage drops below 1.5 V (or is turning on and has not yet reached 1.5 V), power-on reset circuitry set the driver output to a high-impedance state.

8.3.2 ESD Protection

The bus terminals of the SN65MLVD203B possess on-chip ESD protection against ±8-kV human body model (HBM) and ±8-kV IEC61000-4-2 contact discharge. The IEC-ESD test is far more severe than the HBM-ESD test. The 50% higher charge capacitance, CS, and 78% lower discharge resistance, R_D of the IEC model produce significantly higher discharge currents than the HBM-model.

As stated in the IEC 61000-4-2 standard, contact discharge is the preferred test method; although IEC air-gap testing is less repeatable than contact testing, air discharge protection levels are inferred from the contact discharge test results.

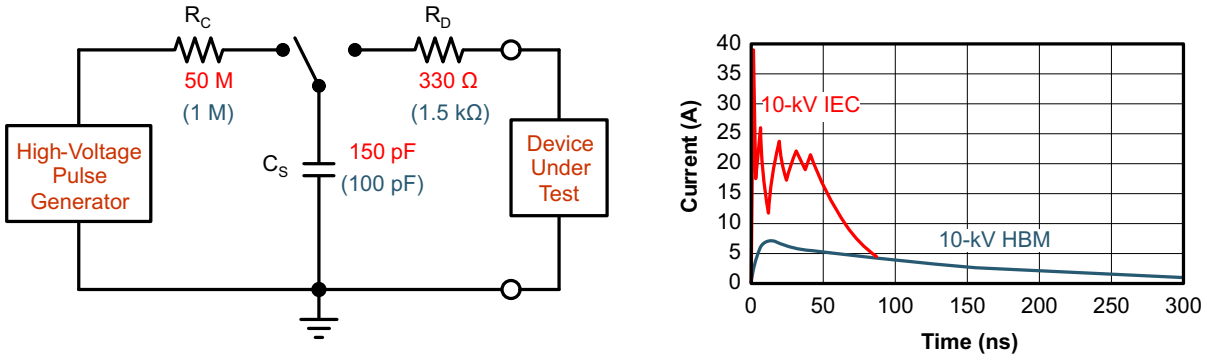


图 8-1. HBM and IEC-ESD Models and Currents in Comparison (HBM Values in Parenthesis)

8.3.3 RX Maximum Jitter While DE Toggling

Due to the internal circuitry of the Receiver and Driver Enable/Disable (DE), toggling the DE pin disrupts the biasing of the receiver and results in a current change. This current change adds jitter to the receiver. If the DE pin is toggled, the maximum peak-to-peak jitter of the receiver is estimated to be 2.1 ns.

8.4 Device Functional Modes

8.4.1 Operation with V_{CC} < 1.5 V

Bus pins are high impedance under this condition.

8.4.2 Operations with 1.5 V ⩽ V_{CC} < 3 V

Operation with supply voltages in the range of 1.5 V ⩽ V_{CC} < 3 V is undefined and no specific device performance is guaranteed in this range.

8.4.3 Operation with 3 V ⩽ V_{CC} < 3.6 V

Operation with the supply voltages greater than or equal to 3 V and less than or equal to 3.6 V is normal operation.

8.4.4 Device Function Tables

表 8-1. Type-1 Receiver

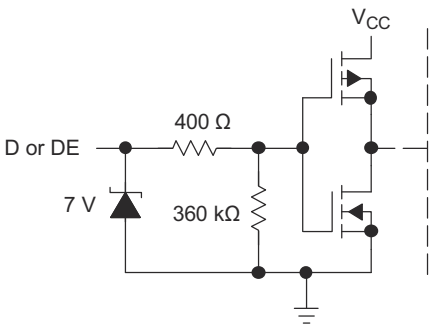
INPUTS		OUTPUT
$V_{ID} = V_A - V_B$	$\overline{RE}$	R
V_{ID} ⩾ 50 mV	L	H
-50 mV < V_{ID} < 50 mV	L	?
V_{ID} ⩽ -50 mV	L	L
X	H	Z
X	Open	Z

表 8-2. Driver

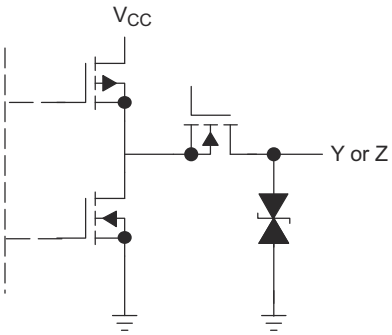
INPUTS	ENABLE	OUTPUTS	
D	DE	X	Y
L	H	L	H
H	H	H	L
Open	H	L	H
X	Open	Z	Z
X	L	Z	Z

8.4.5 Equivalent Input and Output Schematic Diagrams

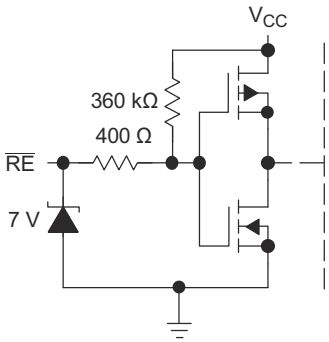
DRIVER INPUT AND DRIVER ENABLE



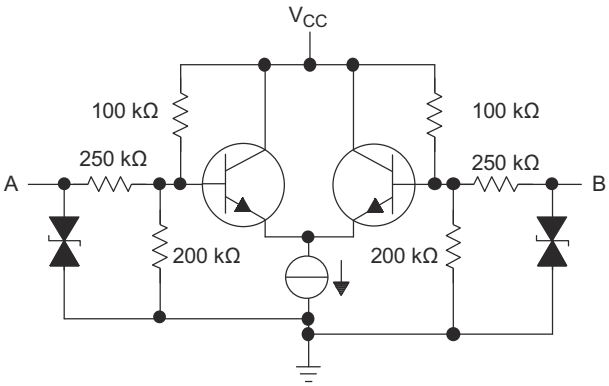
DRIVER OUTPUT



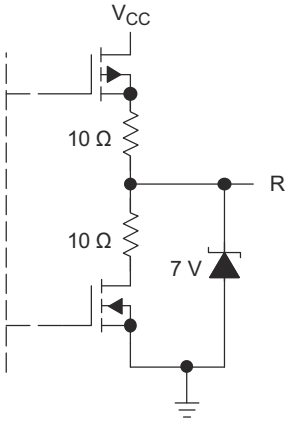
RECEIVER ENABLE



RECEIVER INPUT



RECEIVER OUTPUT



9 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

The SN65MLVD203B is a multipoint line driver and receiver. The functionality of the device is simple, yet extremely flexible, leading to their use in designs ranging from wireless base stations to desktop computers.

9.2 Typical Application

9.2.1 Multipoint Communications

In a multipoint configuration many transmitters and many receivers can be interconnected on a single transmission line. The key difference compared to multi-drop is the presence of two or more drivers. Such a situation creates contention issues that need not be addressed with point-to-point or multidrop systems. Multipoint operation allows for bidirectional, half-duplex communication over a single balanced media pair. To support the location of the various drivers throughout the transmission line, double termination of the transmission line is now necessary.

The major challenge that system designers encounter are the impedance discontinuities that device loading and device connections (stubs) introduce on the common bus. Matching the impedance of the loaded bus and using signal drivers with controlled signal edges are the keys to error-free signal transmissions in multipoint topologies.

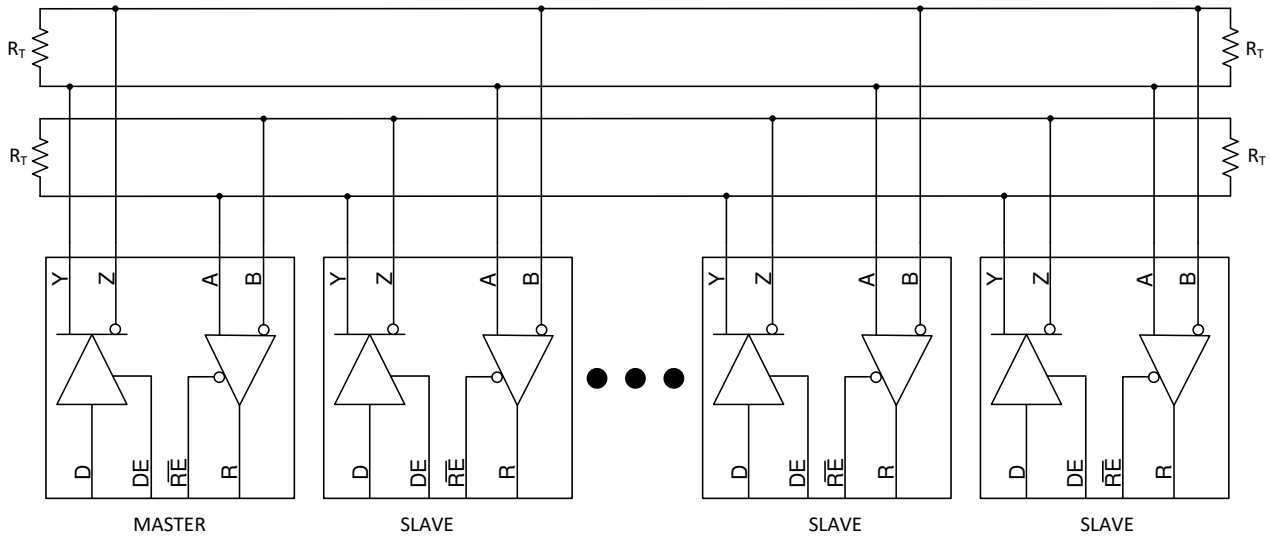


图 9-1. Multipoint Configuration

9.2.2 Design Requirements

For this design example, use the parameters listed in 表 9-1.

表 9-1. Design Parameters

PARAMETERS	VALUES
Driver supply voltage	3 to 3.6 V
Driver input voltage	0.8 to 3.3 V
Driver signaling rate	DC to 200 Mbps
Interconnect characteristic impedance	100 Ω
Termination resistance (differential)	100 Ω
Number of receiver nodes	2 to 32
Receiver supply voltage	3 to 3.6 V
Receiver input voltage	0 to (V_{CC} – 0.8) V
Receiver signaling rate	DC to 200 Mbps
Ground shift between driver and receiver	±1 V

9.2.3 Detailed Design Procedure

9.2.3.1 Supply Voltage

The SN65MLVD203B is operated from a single supply. The device can support operations with a supply as low as 3 V and as high as 3.6 V.

9.2.3.2 Supply Bypass Capacitance

Bypass capacitors play a key role in power distribution circuitry. At low frequencies, power supply offers very low-impedance paths between its terminals. However, as higher frequency currents propagate through power traces, the source is often incapable of maintaining a low-impedance path to ground. Bypass capacitors are used to address this shortcoming. Usually, large bypass capacitors (10 μF to 1000 μF) at the board level do a good job up into the kHz range. Due to their size and length of their leads, large capacitors tend to have large inductance values at the switching frequencies. To solve this problem, smaller capacitors (in the nF to μF range) must be installed locally next to the integrated circuit.

Multilayer ceramic chip or surface-mount capacitors (size 0603 or 0805) minimize lead inductances of bypass capacitors in high-speed environments, because their lead inductance is about 1 nH. For comparison purposes, a typical capacitor with leads has a lead inductance around 5 nH.

The value of the bypass capacitors used locally with M-LVDS chips can be determined by 方程式 1 and 方程式 2, according to *High Speed Digital Design – A Handbook of Black Magic* by Howard Johnson and Martin Graham (1993). A conservative rise time of 4 ns and a worst-case change in supply current of 100 mA covers the whole range of M-LVDS devices offered by Texas Instruments. In this example, the maximum power supply noise tolerated is 100 mV; however, this figure varies depending on the noise budget available for the design.

$$C_{chip} = \left(\frac{\Delta I_{\text{Maximum Step Change Supply Current}}}{\Delta V_{\text{Maximum Power Supply Noise}}} \right) \times T_{\text{Rise Time}} \quad (1)$$

$$C_{MLVDS} = \left(\frac{100\ \text{mA}}{100\ \text{mV}} \right) \times 4\,\text{ns} = 0.004\ \mu\text{F} \quad (2)$$

图 9-2 shows a configuration that lowers lead inductance and covers intermediate frequencies between the board-level capacitor (>10 μF) and the value of capacitance found above (0.004 μF). Place the smallest value of capacitance as close as possible to the chip.

图 9-2. Recommended M-LVDS Bypass Capacitor Layout

9.2.3.3 Driver Input Voltage

The input stage accepts LVTTL signals. The driver operates with a decision threshold of approximately 1.4 V.

9.2.3.4 Driver Output Voltage

The driver outputs a steady state common mode voltage of 1 V with a differential signal of 540 mV under nominal conditions.

9.2.3.5 Termination Resistors

As shown earlier, an M-LVDS communication channel employs a current source driving a transmission line which is terminated with two resistive loads. These loads serve to convert the transmitted current into a voltage at the receiver input. To ensure good signal integrity, the termination resistors should be matched to the characteristic impedance of the transmission line. The designer should ensure that the termination resistors are within 10% of the nominal media characteristic impedance. If the transmission line is targeted for 100-Ω impedance, the termination resistors should be between 90 Ω and 110 Ω. The line termination resistors are typically placed at the ends of the transmission line.

9.2.3.6 Receiver Input Signal

The M-LVDS receivers herein comply with the M-LVDS standard and correctly determine the bus state. These devices have Type-1 and Type-2 receivers that detect the bus state with as little as 50 mV of differential voltage over the common mode range of –1 V to 3.4 V.

9.2.3.7 Receiver Input Threshold (Failsafe)

The MLVDS standard defines a Type-1 and Type-2 receiver. Type-1 receivers have their differential input voltage thresholds near zero volts. Type-2 receivers have their differential input voltage thresholds offset from 0 V to detect the absence of a voltage difference. The impact to receiver output by the offset input can be seen in 表 9-2 and 图 9-3.

表 9-2. Receiver Input Voltage Threshold Requirements

RECEIVER TYPE	OUTPUT LOW	OUTPUT HIGH
Type 1	$-2.4\ V \leqslant V_{ID} \leqslant -0.05\ V$	$0.05\ V \leqslant V_{ID} \leqslant 2.4\ V$
Type 2	$-2.4\ V \leqslant V_{ID} \leqslant 0.05\ V$	$0.15\ V \leqslant V_{ID} \leqslant 2.4\ V$

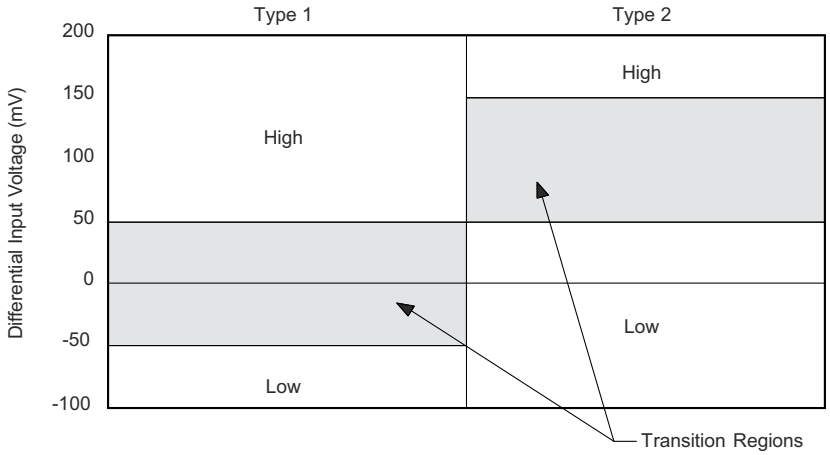


图 9-3. Expanded Graph of Receiver Differential Input Voltage Showing Transition Region

9.2.3.8 Receiver Output Signal

Receiver outputs comply with LVTTL output voltage standards when the supply voltage is within the range of 3 V to 3.6 V.

9.2.3.9 Interconnecting Media

The physical communication channel between the driver and the receiver may be any balanced paired metal conductors meeting the requirements of the M-LVDS standard, the key points which will be included here. This media may be a twisted pair, twinax, flat ribbon cable, or PCB traces.

The nominal characteristic impedance of the interconnect should be between 100 Ω and 120 Ω with variation no more than 10% (90 Ω to 132 Ω).

9.2.3.10 PCB Transmission Lines

As per SNLA187, 图 9-4 depicts several transmission line structures commonly used in printed-circuit boards (PCBs). Each structure consists of a signal line and a return path with uniform cross-section along its length. A microstrip is a signal trace on the top (or bottom) layer, separated by a dielectric layer from its return path in a ground or power plane. A stripline is a signal trace in the inner layer, with a dielectric layer in between a ground plane above and below the signal trace. The dimensions of the structure along with the dielectric material properties determine the characteristic impedance of the transmission line (also called controlled-impedance transmission line).

When two signal lines are placed close by, they form a pair of coupled transmission lines. 图 9-4 shows examples of edge-coupled microstrips, and edge-coupled or broad-side-coupled striplines. When excited by differential signals, the coupled transmission line is referred to as a differential pair. The characteristic impedance of each line is called odd-mode impedance. The sum of the odd-mode impedances of each line is the differential impedance of the differential pair. In addition to the trace dimensions and dielectric material properties, the spacing between the two traces determines the mutual coupling and impacts the differential impedance. When the two lines are immediately adjacent; for example, if S is less than 2 × W, the differential pair is called a tightly-coupled differential pair. To maintain constant differential impedance along the length, it is important to keep the trace width and spacing uniform along the length, as well as maintain good symmetry between the two lines.

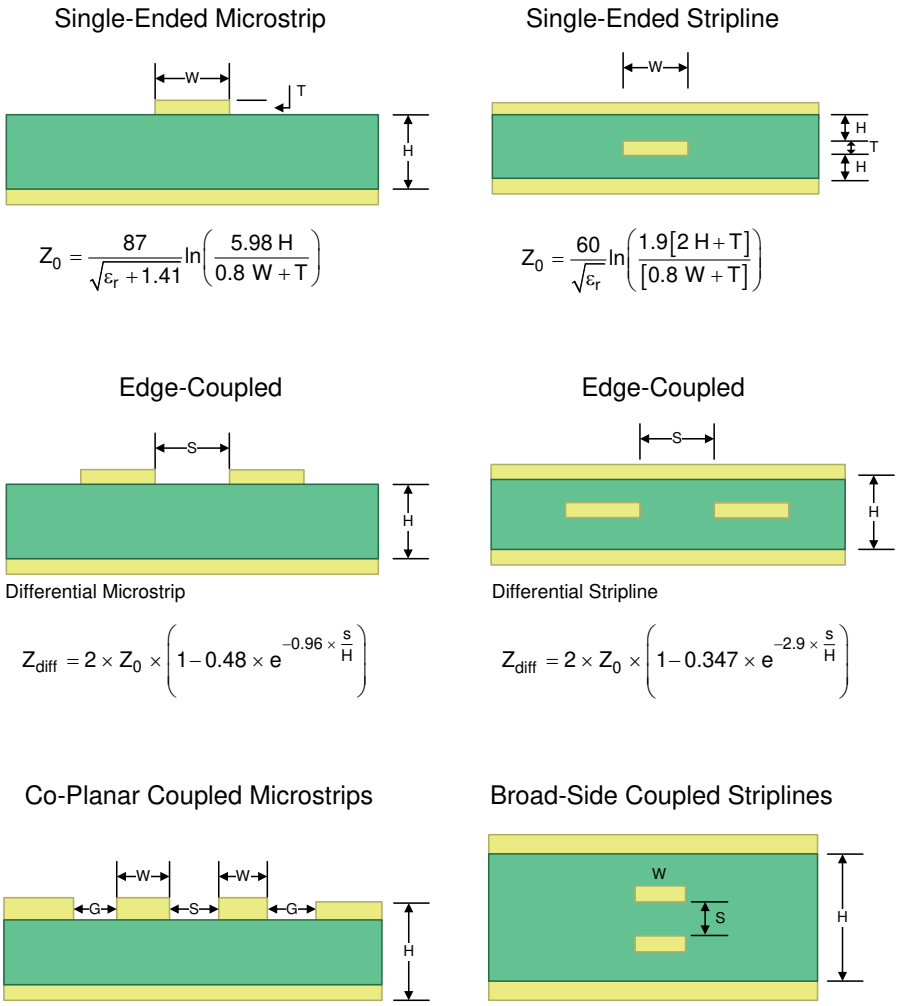
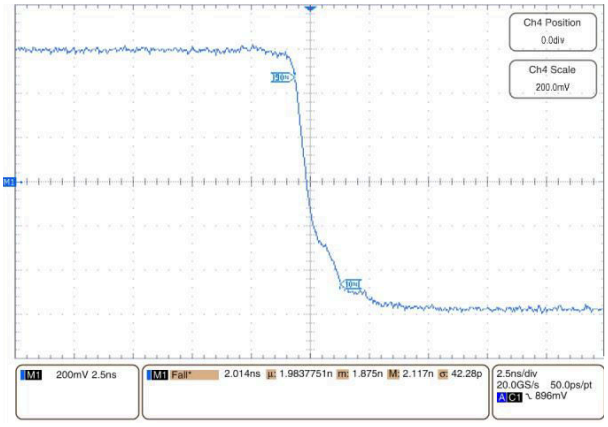


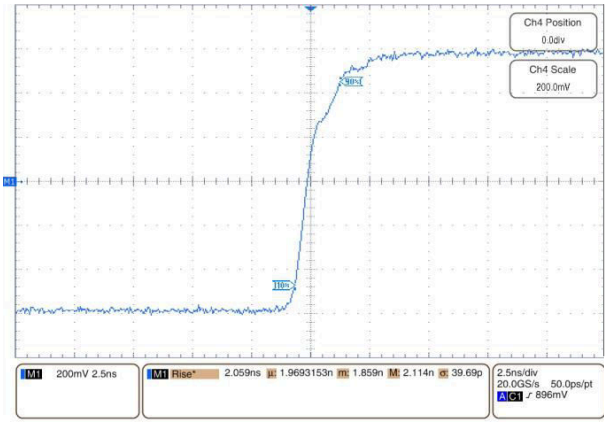
图 9-4. Controlled-Impedance Transmission Lines

9.2.4 Application Curves



V_{CC} = 3.3 V T_A = 25°C

图 9-5. Driver Fall Time



V_{CC} = 3.3 V T_A = 25°C

图 9-6. Driver Rise Time

9.3 Power Supply Recommendations

The M-LVDS driver and receivers in this data sheet are designed to operate from a single power supply. Both drivers and receivers operate with supply voltages in the range of 3 V to 3.6 V. In a typical application, a driver and a receiver may be on separate boards, or even separate equipment. In these cases, separate supplies would be used at each location. The expected ground potential difference between the driver power supply and the receiver power supply would be less than ±1 V. Board level and local device level bypass capacitance should be used and are covered Supply Bypass Capacitance.

9.4 Layout

9.4.1 Layout Guidelines

9.4.1.1 Microstrip vs. Stripline Topologies

As per SLLD009, printed-circuit boards usually offer designers two transmission line options: Microstrip and stripline. Microstrips are traces on the outer layer of a PCB, as shown in 图 9-7.

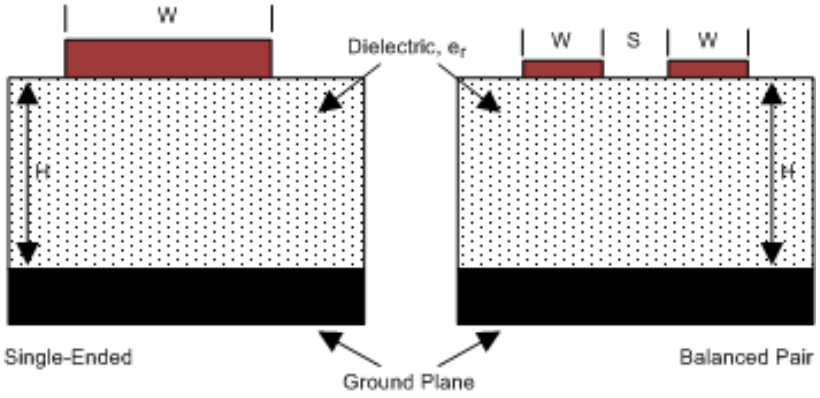


图 9-7. Microstrip Topology

On the other hand, striplines are traces between two ground planes. Striplines are less prone to emissions and susceptibility problems because the reference planes effectively shield the embedded traces. However, from the standpoint of high-speed transmission, juxtaposing two planes creates additional capacitance. TI recommends routing M-LVDS signals on microstrip transmission lines if possible. The PCB traces allow designers to specify the necessary tolerances for Z_O based on the overall noise budget and reflection allowances. Footnotes 1[2], 2[3], and 3[4] provide formulas for Z_O and t_{PD} for differential and single-ended traces. [2] [3] [4]

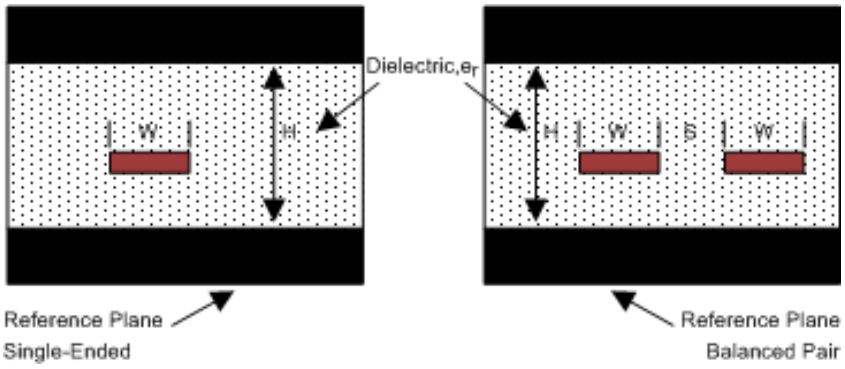


图 9-8. Stripline Topology

[2] Howard Johnson & Martin Graham.1993. High Speed Digital Design – A Handbook of Black Magic. Prentice Hall PRT. ISBN number 013395724.
[3] Mark I. Montrose. 1996. Printed Circuit Board Design Techniques for EMC Compliance. IEEE Press. ISBN number 0780311310.
[4] Clyde F. Coombs, Jr. Ed, Printed Circuits Handbook, McGraw Hill, ISBN number 0070127549.

9.4.1.2 Dielectric Type and Board Construction

The speeds at which signals travel across the board dictates the choice of dielectric. FR-4, or equivalent, usually provides adequate performance for use with M-LVDS signals. If rise or fall times of TTL/CMOS signals are less than 500 ps, empirical results indicate that a material with a dielectric constant near 3.4, such as Rogers™ 4350 or Nelco N4000-13 is better suited. Once the designer chooses the dielectric, there are several parameters pertaining to the board construction that can affect performance. The following set of guidelines were developed experimentally through several designs involving M-LVDS devices:

- Copper weight: 15 g or 1/2 oz start, plated to 30 g or 1 oz
- All exposed circuitry should be solder-plated (60/40) to 7.62 μm or 0.0003 in (minimum).
- Copper plating should be 25.4 μm or 0.001 in (minimum) in plated-through-holes.
- Solder mask over bare copper with solder hot-air leveling

9.4.1.3 Recommended Stack Layout

Following the choice of dielectrics and design specifications, you must decide how many levels to use in the stack. To reduce the TTL/CMOS to M-LVDS crosstalk, it is a good practice to have at least two separate signal planes as shown in 图 9-9.

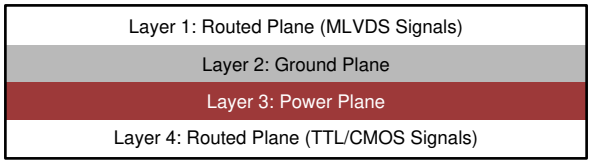


图 9-9. Four-Layer PCB Board

备注

The separation between layers 2 and 3 should be 127 μm (0.005 in). By keeping the power and ground planes tightly coupled, the increased capacitance acts as a bypass for transients.

One of the most common stack configurations is the six-layer board, as shown in 图 9-10.

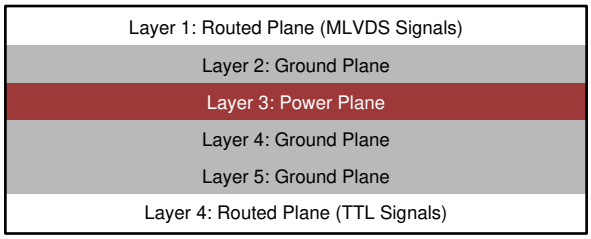


图 9-10. Six-Layer PCB Board

In this particular configuration, it is possible to isolate each signal layer from the power plane by at least one ground plane. The result is improved signal integrity; however, fabrication is more expensive. Using the 6-layer board is preferable, because it offers the layout designer more flexibility in varying the distance between signal layers and referenced planes, in addition to ensuring reference to a ground plane for signal layers 1 and 6.

9.4.1.4 Separation Between Traces

The separation between traces depends on several factors; however, the amount of coupling that can be tolerated usually dictates the actual separation. Low noise coupling requires close coupling between the differential pair of an M-LVDS link to benefit from the electromagnetic field cancellation. The traces should be 100-Ω differential and thus coupled in the manner that best fits this requirement. In addition, differential pairs should have the same electrical length to ensure that they are balanced, thus minimizing problems with skew and signal reflection.

In the case of two adjacent single-ended traces, one should use the 3-W rule, which stipulates that the distance between two traces must be greater than two times the width of a single trace, or three times its width measured from trace center to trace center. This increased separation effectively reduces the potential for crosstalk. The same rule should be applied to the separation between adjacent M-LVDS differential pairs, whether the traces are edge-coupled or broad-side-coupled.

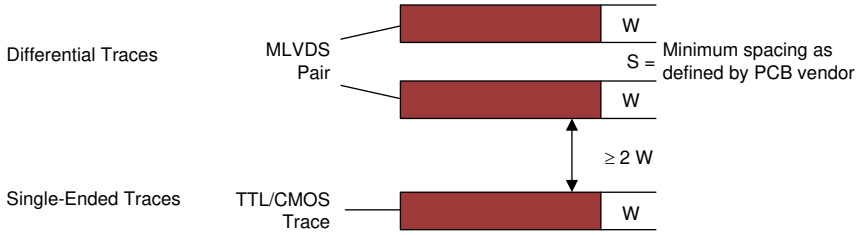


图 9-11. 3-W Rule for Single-Ended and Differential Traces (Top View)

You should exercise caution when using autorouters, because they do not always account for all factors affecting crosstalk and signal reflection. For instance, it is best to avoid sharp 90° turns to prevent discontinuities in the signal path. Using successive 45° turns tends to minimize reflections.

9.4.1.5 Crosstalk and Ground Bounce Minimization

To reduce crosstalk, it is important to provide a return path to high-frequency currents that is as close as possible to its originating trace. A ground plane usually achieves this. Because the returning currents always choose the path of lowest inductance, they are most likely to return directly under the original trace, thus minimizing crosstalk. Lowering the area of the current loop lowers the potential for crosstalk. Traces kept as short as possible with an uninterrupted ground plane running beneath them emit the minimum amount of electromagnetic field strength. Discontinuities in the ground plane increase the return path inductance and should be avoided.

9.4.1.6 Decoupling

Each power or ground lead of a high-speed device should be connected to the PCB through a low inductance path. For best results, one or more vias are used to connect a power or ground pin to the nearby plane. Ideally, via placement is immediately adjacent to the pin to avoid adding trace inductance. Placing a power plane closer to the top of the board reduces the effective via length and its associated inductance.

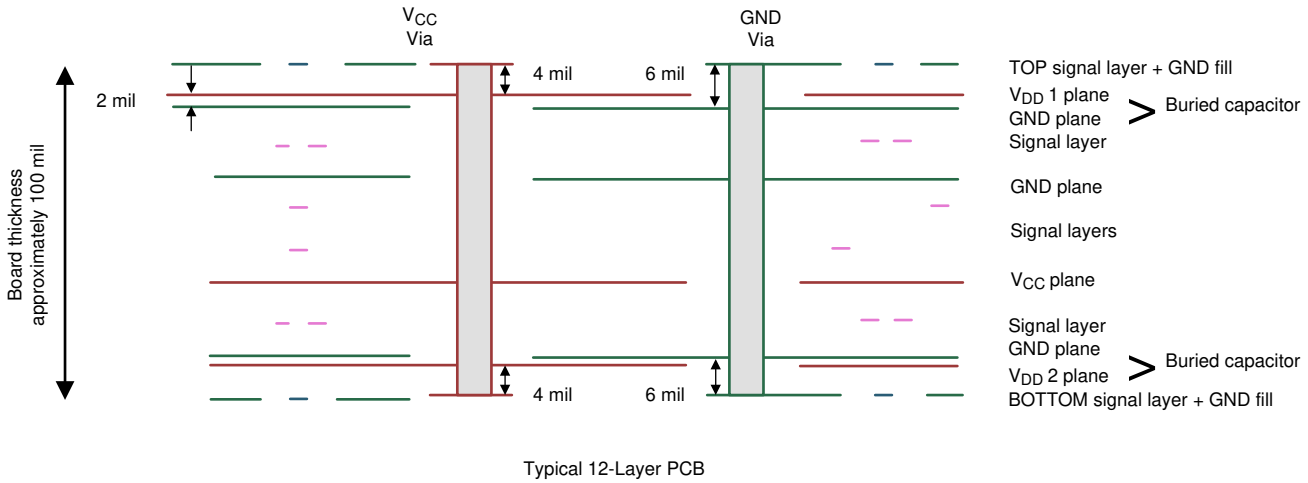
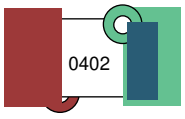


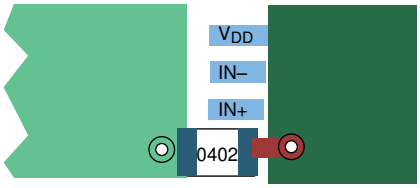
图 9-12. Low Inductance, High-Capacitance Power Connection

Bypass capacitors should be placed close to V_{DD} pins. They can be placed conveniently near the corners or underneath the package to minimize the loop area. This extends the useful frequency range of the added capacitance. Small-physical-size capacitors, such as 0402, 0201, or X7R surface-mount capacitors should be used to minimize body inductance of capacitors. Each bypass capacitor is connected to the power and ground plane through vias tangent to the pads of the capacitor as shown in 图 9-13(a).

An X7R surface-mount capacitor of size 0402 has about 0.5 nH of body inductance. At frequencies above 30 MHz or so, X7R capacitors behave as low-impedance inductors. To extend the operating frequency range to a few hundred MHz, an array of different capacitor values like 100 pF, 1 nF, 0.03 μF, and 0.1 μF are commonly used in parallel. The most effective bypass capacitor can be built using sandwiched layers of power and ground at a separation of 2 to 3 mils. With a 2-mil FR4 dielectric, there is approximately 500 pF per square inch of PCB. Many high-speed devices provide a low-inductance GND connection on the backside of the package. This center pad must be connected to a ground plane through an array of vias. The via array reduces the effective inductance to ground and enhances the thermal performance of the small Surface Mount Technology (SMT) package. Placing vias around the perimeter of the pad connection ensures proper heat spreading and the lowest possible die temperature. Placing high-performance devices on opposing sides of the PCB using two GND planes (as shown in 图 9-4) creates multiple paths for heat transfer. Often thermal PCB issues are the result of one device adding heat to another, resulting in a very high local temperature. Multiple paths for heat transfer minimize this possibility. In many cases the GND pad makes the optimal decoupling layout impossible to achieve due to insufficient pad-to-pad spacing as shown in 图 9-13(b). When this occurs, placing the decoupling capacitor on the backside of the board keeps the extra inductance to a minimum. It is important to place the V_{DD} via as close to the device pin as possible while still allowing for sufficient solder mask coverage. If the via is left open, solder may flow from the pad and into the via barrel. This will result in a poor solder connection.



Typical Decoupling Capacitor Layouts(a)



Typical Decoupling Capacitor Layouts(b)

9.4.2 Layout Example

At least two or three times the width of an individual trace should separate single-ended traces and differential pairs to minimize the potential for crosstalk. Single-ended traces that run in parallel for less than the wavelength of the rise or fall times usually have negligible crosstalk. Increase the spacing between signal paths for long parallel runs to reduce crosstalk. Boards with limited real estate can benefit from the staggered trace layout, as shown in 图 9-13.

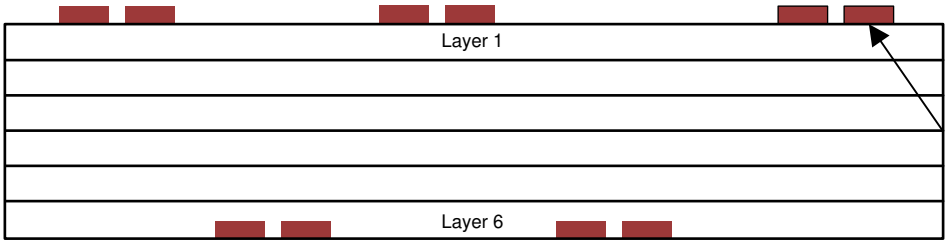


图 9-13. Staggered Trace Layout

This configuration lays out alternating signal traces on different layers; thus, the horizontal separation between traces can be less than 2 or 3 times the width of individual traces. To ensure continuity in the ground signal path, TI recommends having an adjacent ground via for every signal via, as shown in 图 9-14. Note that vias create additional capacitance. For example, a typical via has a lumped capacitance effect of 1/2 pF to 1 pF in FR4.

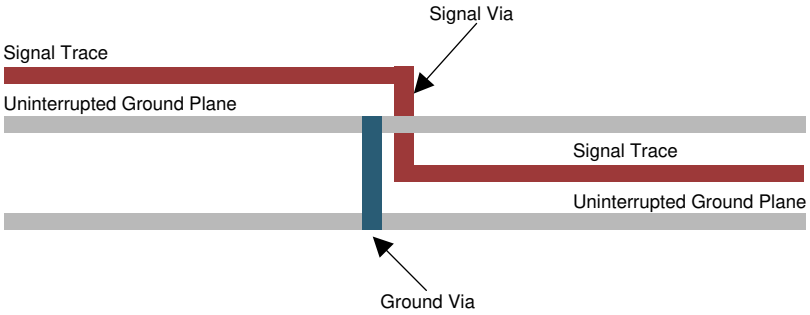


图 9-14. Ground Via Location (Side View)

Short and low-impedance connection of the device ground pins to the PCB ground plane reduces ground bounce. Holes and cutouts in the ground planes can adversely affect current return paths if they create discontinuities that increase returning current loop areas.

To minimize EMI problems, TI recommends avoiding discontinuities below a trace (for example, holes, slits, and so on) and keeping traces as short as possible. Zoning the board wisely by placing all similar functions in the same area, as opposed to mixing them together, helps reduce susceptibility issues.

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For releated documentation, see the following:

1. Howard Johnson & Martin Graham.1993. High Speed Digital Design – A Handbook of Black Magic. Prentice Hall PRT. ISBN number 013395724.
2. Mark I. Montrose. 1996. Printed Circuit Board Design Techniques for EMC Compliance. IEEE Press. ISBN number 0780311310.
3. Clyde F. Coombs, Jr. Ed, Printed Circuits Handbook, McGraw Hill, ISBN number 0070127549.

10.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

10.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

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10.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65MLVD203BRUMR	ACTIVE	WQFN	RUM	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MLVD 203B	Samples
SN65MLVD203BRUMT	ACTIVE	WQFN	RUM	16	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MLVD 203B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

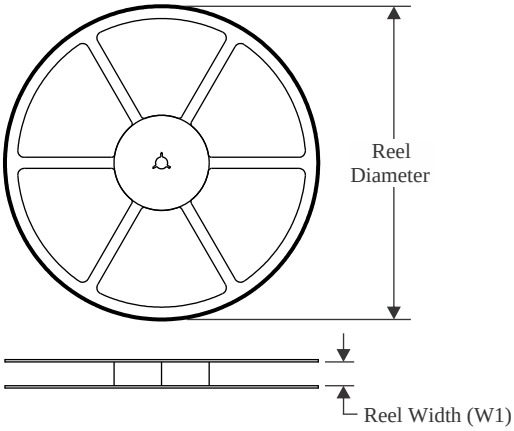
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

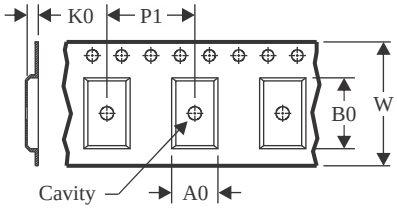
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

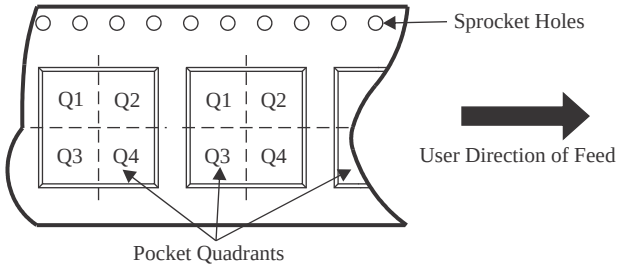


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

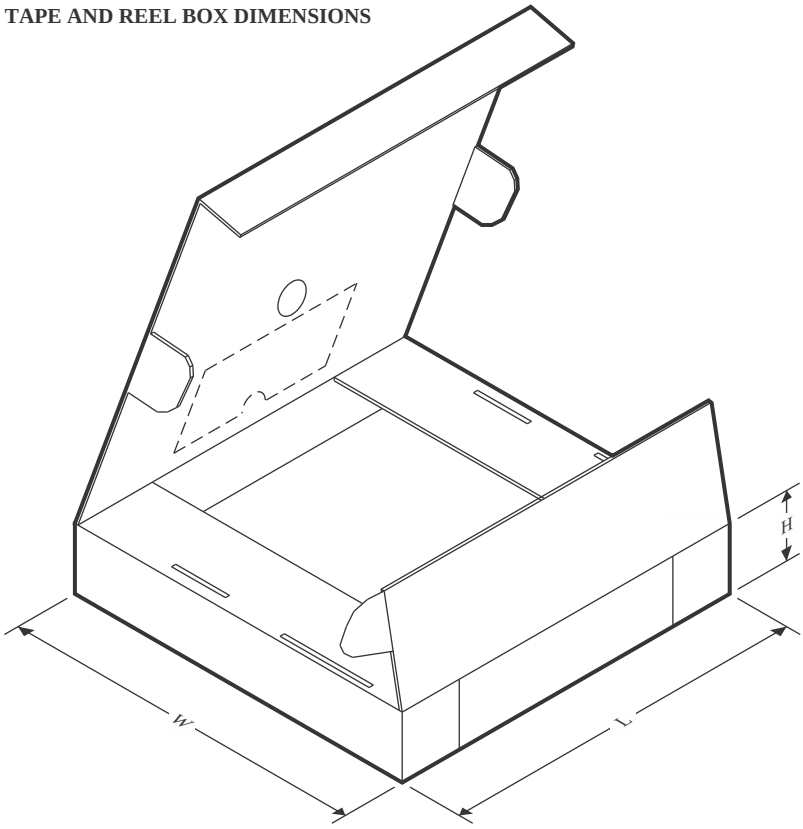
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65MLVD203BRUMR	WQFN	RUM	16	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
SN65MLVD203BRUMT	WQFN	RUM	16	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65MLVD203BRUMR	WQFN	RUM	16	3000	367.0	367.0	35.0
SN65MLVD203BRUMT	WQFN	RUM	16	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

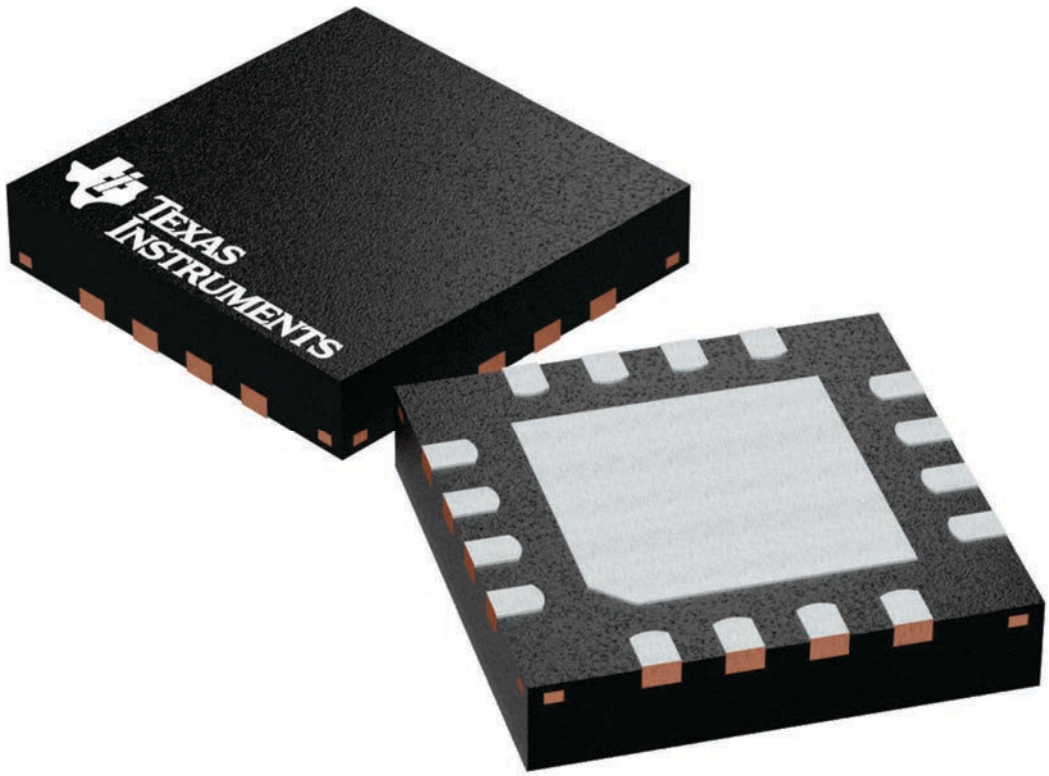
RUM 16

WQFN - 0.8 mm max height

4 x 4, 0.65 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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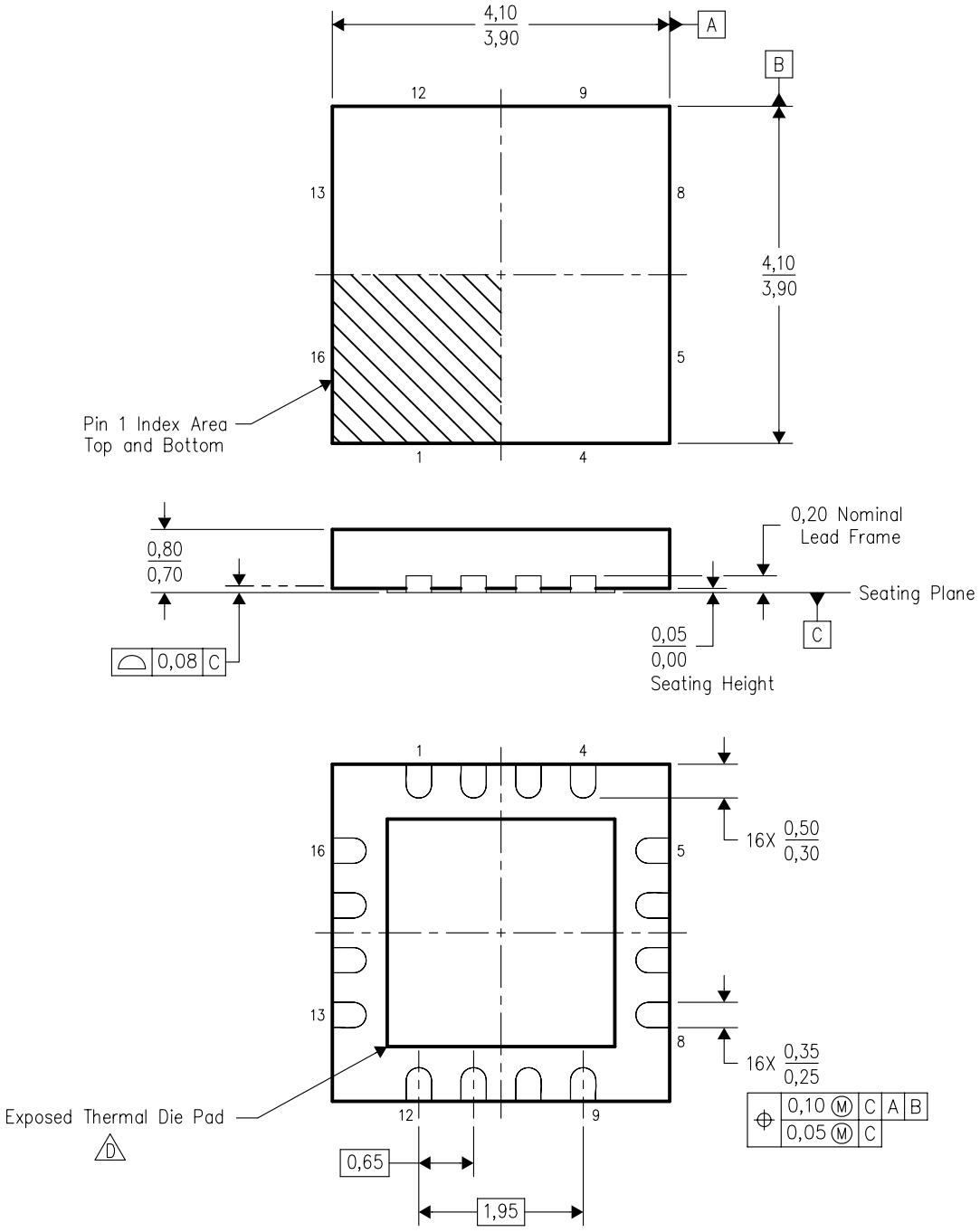
RUM (S–PQFP–N16) PLASTIC QUAD FLATPACK



4209092/A 10/2007

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Package complies to JEDEC MO–220 variation WGGC–3.

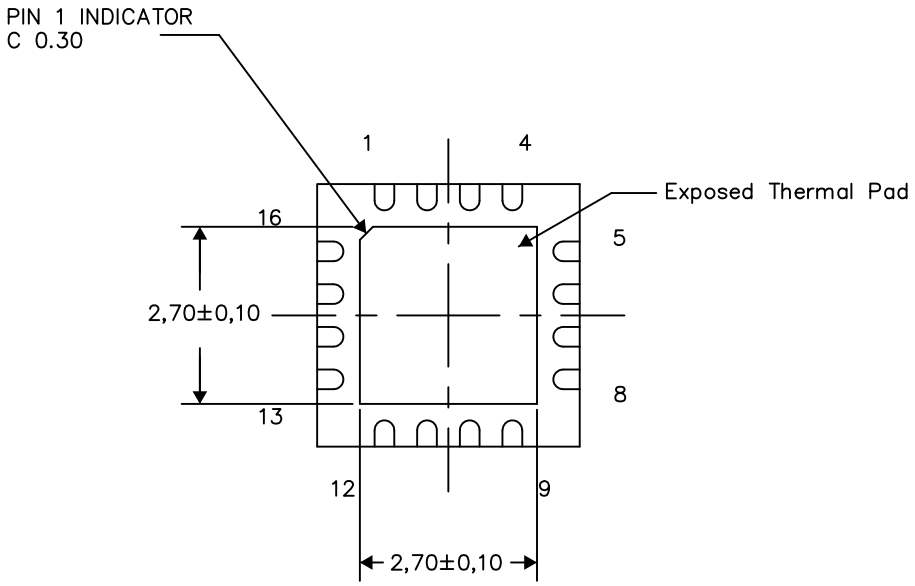
RUM (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



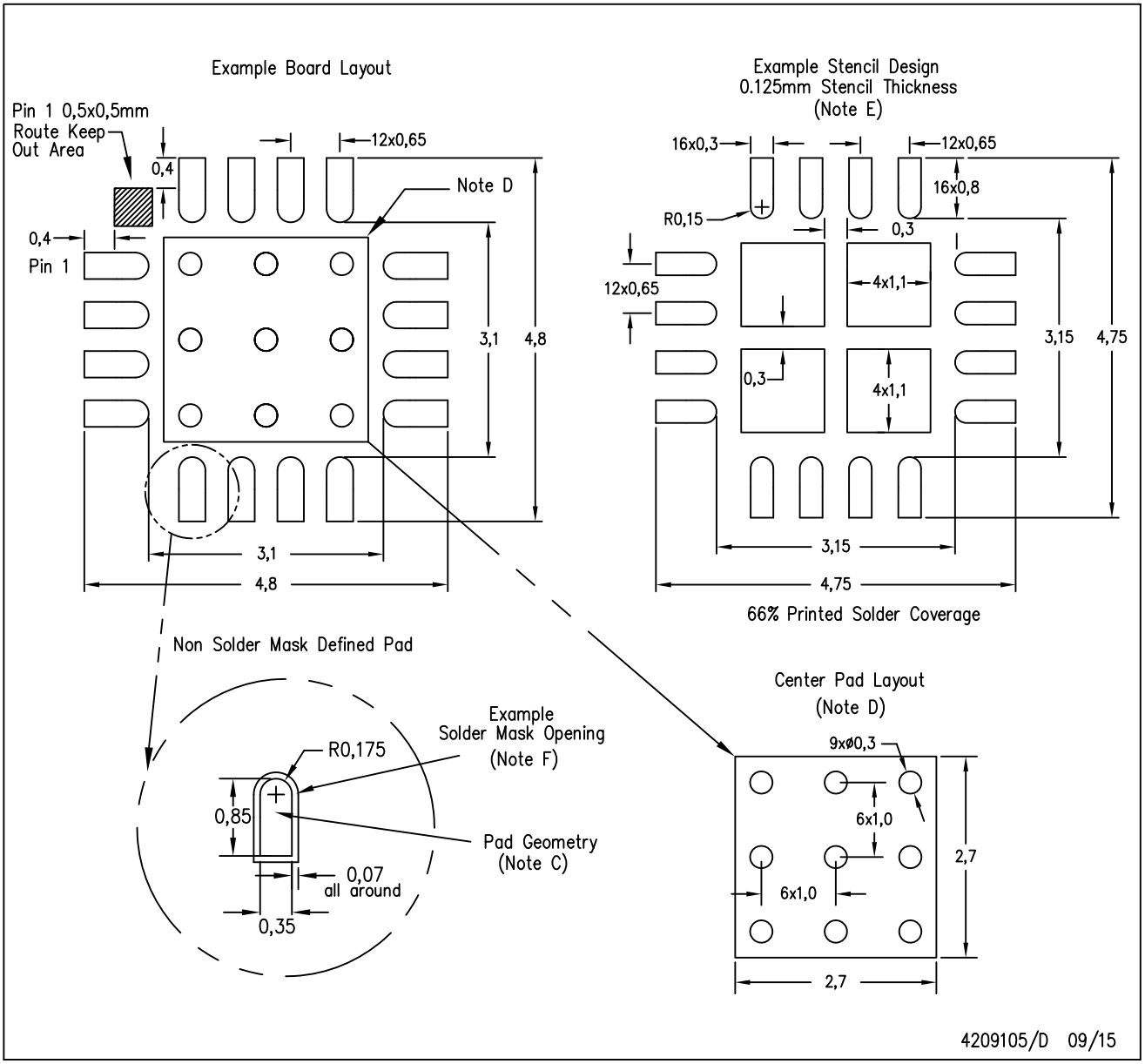
Bottom View

Exposed Thermal Pad Dimensions

4209093–2/F 09/15

NOTES: All linear dimensions are in millimeters

RUM (S–PWQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

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