SNx4ACT08 四通道双输入正与门

1 特性

- 4.5V 至 5.5V V_{CC} 运行
- 输入电压高达 5.5V
- t_{pd} 最大值为 10ns（5V 时）
- 输入兼容 TTL 电压

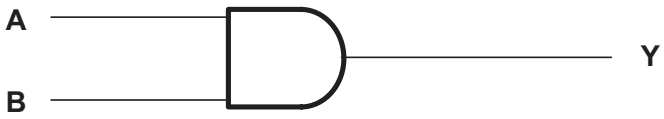
2 说明

’ACT08 器件是四通道 2 输入正与门。这些器件以正逻辑执行布尔函数 $Y = A \cdot B$ 或 $Y = \overline{A} + \overline{B}$。

器件信息

器件型号	封装(1)	封装尺寸(2)	本体尺寸(3)
SNx4ACT08	N（PDIP，14）	19.3mm × 9.4mm	19.3mm × 6.35mm
	NS（SOP，14）	12.60mm × 7.8mm	12.60mm × 5.30mm
	DB（SSOP，14）	6.20mm × 7.8mm	6.20mm × 5.30mm
	PW（TSSOP，14）	5.00mm × 6.4mm	5.00mm × 4.40mm
	D（SOIC，14）	8.65mm × 6mm	8.65mm × 3.91mm
	J（CDIP，14）	19.56mm × 7.9mm	19.56mm × 6.67mm
	W（CFP，14）	9.21mm x 9mm	9.21mm × 6.3mm
	FK（LCCC，20）	8.9mm × 8.9mm	8.9mm × 8.9mm

(1) 如需了解更多信息，请参阅机械、封装和可订购信息。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。
(3) 本体尺寸（长 × 宽）为标称值，不包括引脚。



逻辑图，每个逻辑门（正逻辑）

内容

3 引脚配置和功能

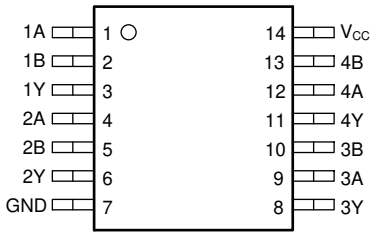


图 3-1. SN54ACT08 J 或 W 封装，14 引脚 CDIP 或 CFP；SN74ACT08 D、DB、N、NS 和 PW；14 引脚 SOIC、SSOP、PDIP、SOP 和 TSSOP

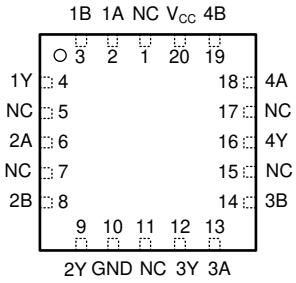


图 3-2. FK 封装，20 引脚 LCCC

引脚功能

引脚		I/O	说明
名称	编号		
1A	1	输入	通道 1，输入 A
1B	2	输入	通道 1，输入 B
1Y	3	输出	通道 1，输出 Y
2A	4	输入	通道 2，输入 A
2B	5	输入	通道 2，输入 B
2Y	6	输出	通道 2，输出 Y
GND	7	—	接地
3Y	8	输出	通道 3，输出 Y
3A	9	输入	通道 3，输入 A
3B	10	输入	通道 3，输入 B
4Y	11	输出	通道 4，输出 Y
4A	12	输入	通道 4，输入 A
4B	13	输入	通道 4，输入 B
V_{CC}	14	—	正电源
散热焊盘(1)		—	散热焊盘可连接到 GND 或悬空。请勿连接到任何其他信号或电源

(1) 信号类型：I = 输入，O = 输出，I/O = 输入或输出。

4 规格

4.1 绝对最大额定值

在自然通风条件下的工作温度范围内测得（除非另有说明）(1)

			最小值	最大值	单位
V_{CC}	电源电压范围		-0.5	7	V
V_I	输入电压范围(2)		-0.5	V_{CC} + 0.5	V
V_O	输出电压范围(2)		-0.5	V_{CC} + 0.5	V
I_{IK}	输入钳位电流	V_I < 0 或 V_I > V_{CC}		±20	mA
I_{OK}	输出钳位电流	V_O < 0 或 V_O > V_{CC}		±20	mA
I_O	持续输出电流	V_O = 0 至 V_{CC}		±50	mA
	通过 V_{CC} 或 GND 的持续电流			±200	mA
T_{stg}	贮存温度范围		-65	150	°C

(1) 应力超出“绝对最大额定值”下所列的值可能会对器件造成永久损坏。这些列出的值仅仅是应力额定值，这并不表示器件在这些条件下以及在“建议运行条件”以外的任何其他条件下能够正常运行。长时间处于绝对最大额定条件下可能会影响器件的可靠性。
(2) 如果遵守输入和输出电流额定值，输入和输出电压可超过额定值。

4.2 建议运行条件

		SN54ACT08		SN74ACT08		单位
		最小值	最大值	最小值	最大值	
V_{CC}	电源电压	4.5	5.5	4.5	5.5	V
V_{IH}	高电平输入电压	2		2		V
V_{IL}	低电平输入电压		0.8		0.8	V
V_I	输入电压	0	V_{CC}	0	V_{CC}	V
V_O	输出电压	0	V_{CC}	0	V_{CC}	V
I_{OH}	高电平输出电流		-24		-24	mA
I_{OL}	低电平输出电流		24		24	mA
$\Delta t/\Delta v$	输入转换上升或下降速率		8		8	ns/V
T_A	自然通风条件下的工作温度范围	-55	125	-40	85	°C

4.3 热性能信息

热指标(1)		SN74ACT08					单位
		DB (SSOP)	D (SOIC)	N (PDIP)	NS (PDIP)	PW (TSSOP)	
		14 引脚	14 引脚	14 引脚	14 引脚	14 引脚	
$R_{\theta JA}$	结至环境热阻	96	86	80	76	145.7	°C/W

(1) 有关新旧热指标的更多信息，请参阅（*半导体和 IC 封装热指标*）应用报告。

4.4 电气特性

在自然通风条件下的建议运行温度范围内测得（除非另有说明）

参数	测试条件	V_{CC}	T_A = 25°C			SN54ACT08		SN74ACT08		单位
			最小值	典型值	最大值	最小值	最大值	最小值	最大值	
V_{OH}	I_{OH} = -50μA	4.5V	4.4	4.49		4.4		4.4		V
		5.5V	5.4	5.49		5.4		5.4		
	I_{OH} = -24mA	4.5V	3.86			3.7		3.76		
		5.5V	4.86			4.7		4.76		
	I_{OH} = -50mA(1)	5.5V				3.85				
	I_{OH} = -75mA(1)	5.5V						3.85		
V_{OL}	I_{OL} = 50μA	4.5V		0.001	0.1		0.1		0.1	V
		5.5V		0.001	0.1		0.1		0.1	
	I_{OL} = 24mA	4.5V			0.36		0.5		0.44	
		5.5V			0.36		0.5		0.44	
	I_{OL} = 50mA(1)	5.5V					1.65			
	I_{OL} = 75mA(1)	5.5V							1.65	
I_I	V_I = V_{CC} 或 GND	5.5V			±0.1		±1		±1	μA
I_{CC}	V_I = V_{CC} 或 GND，I_O = 0	5.5V			2		80		20	μA
ΔI_{CC} (2)	一个输入电压为 3.4V，其他输入电压为 GND 或 V_{CC}	5.5V		0.6			1.6		1.5	mA
C_i	V_I = V_{CC} 或 GND	5V		4.5						pF

(1) 一次不应测试超过一个输出，且测试持续时间不应超过 2ms。
(2) 这是每个输入在指定 TTL 电压电平之一而不是 0V 或 V_{CC} 时电源电流的增加情况。

4.5 开关特性

在自然通风条件下的建议工作温度范围内测得，V_{CC} = 5V ± 0.5V（除非另有说明）（请参阅负载电路和电压波形）

参数	从（输入）	至（输出）	T_A = 25°C			SN54ACT08		SN74ACT08		单位
			最小值	典型值	最大值	最小值	最大值	最小值	最大值	
t_{PLH}	A 或 B	Y	1	6.5	9	1	10	1	10	ns
t_{PHL}			1	6.5	9	1	10	1	10	

4.6 工作特性

V_{CC} = 5V，T_A = 25°C

参数		测试条件		典型值	单位
C_{pd}	功率耗散电容	C_L = 50pF，	f = 1MHz	20	pF

4.7 典型特性

T_A = 25°C（除非另外注明）

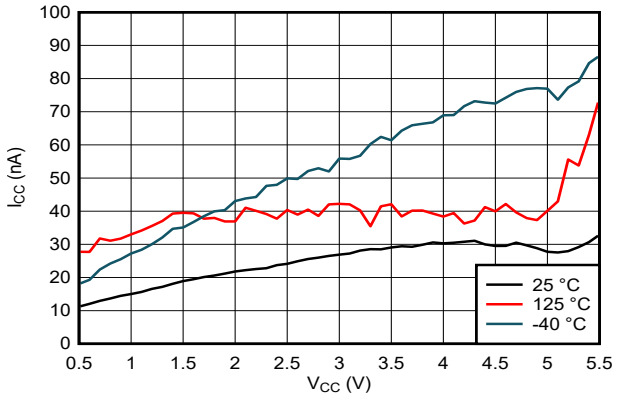


图 4-1. 电源电流与电源电压的关系

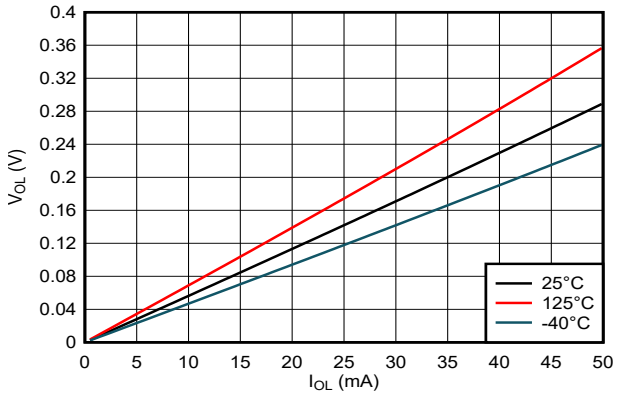
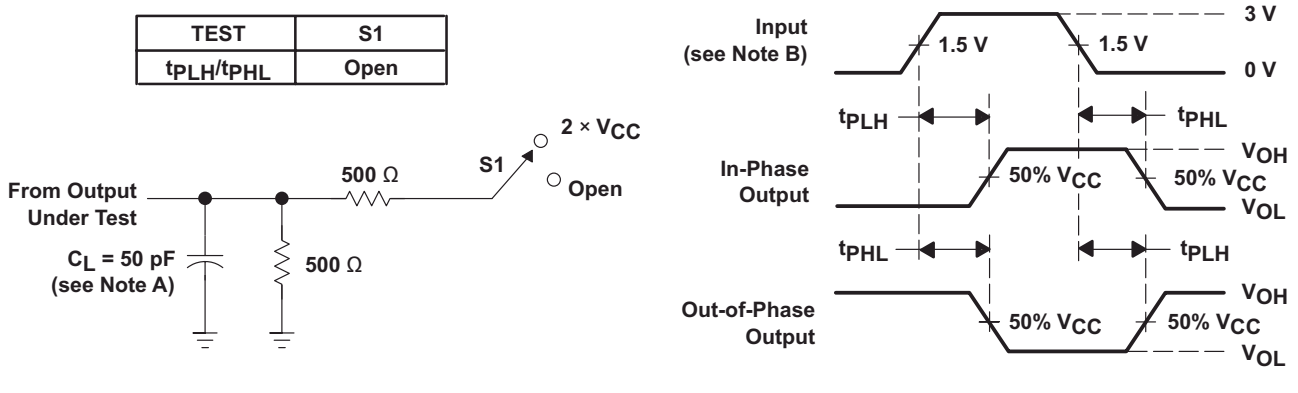


图 4-2. 低电平状态下输出电压与电流间的关系；5V 电源

5 参数测量信息



LOAD CIRCUIT　　VOLTAGE WAVEFORMS

A. C_L 包括探针和夹具电容。

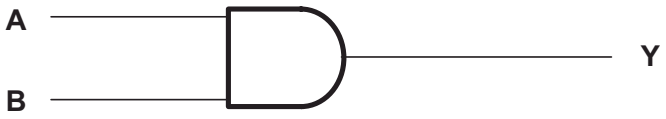
B. 所有输入脉冲均由具有以下特性的发生器提供：PRR ≤1MHz，Z_O = 50Ω，t_r 2.5ns，t_f 2.5ns。

C. 一次测量一个输出，每次测量一个输入转换。

图 5-1. 负载电路和电压波形

6 详细说明

6.1 功能方框图



逻辑图，每个逻辑门（正逻辑）

6.2 器件功能模式

功能表
（每个逻辑门）

输入		输出
A	B	Y
H	H	H
L	X	L
X	L	L

7 应用和实施

备注

以下应用部分中的信息不属于 TI 元件规格，TI 不担保其准确性和完整性。TI 的客户负责确定元件是否适合其用途，以及验证和测试其设计实现以确认系统功能。

7.1 电源相关建议

电源可以是*建议运行条件*表中最小和最大电源电压额定值之间的任何电压。

每个 V_{CC} 引脚应具有一个良好的旁路电容器，以防止功率干扰。对于单电源器件，建议使用 0.1 µF；如果有多个 V_{CC} 引脚，则建议每个电源引脚使用 0.01 µF 或 0.022 µF 电容。可以并联多个旁路电容器以抑制不同的噪声频率。0.1 µF 和 1 µF 通常并联使用。为了获得更佳效果，旁路电容器应尽可能靠近电源引脚安装。

7.2 布局

7.2.1 布局指南

当使用多位逻辑器件时，输入不应悬空。在许多情况下，数字逻辑器件的功能或部分功能未被使用。例如，在仅使用三输入与门的两个输入，或仅使用 4 个缓冲门中的 3 个时。此类输入引脚不应悬空，因为外部连接处的未定义电压会导致未定义的运行状态。节 7.2.2 指定了在所有情况下都必须遵守的规则。数字逻辑器件的所有未使用输入必须连接至一个高或低偏置以防止悬空。应根据器件的功能为任何特定未使用的输入施加逻辑电平。通常，将这些输入连接到 GND 或 V_{CC}，具体取决于哪种更合理或更方便。使输出悬空是可以接受的，除非该器件是收发器。如果该收发器有一个输出使能引脚，它会在置为有效时禁用该器件的输出部分。这不会禁用 I/O 的输入部分，因此输入在禁用后也无法悬空。

7.2.2 布局示例

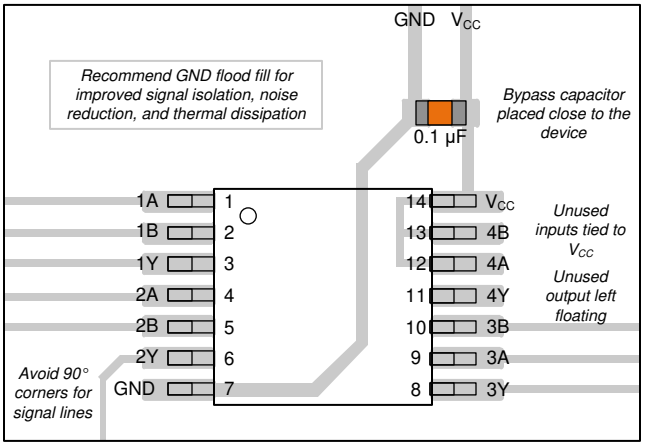


图 7-1. SN74ACT08 的示例布局

8 器件和文档支持

TI 提供广泛的开发工具。下面列出了用于评估器件性能、生成代码和开发解决方案的工具和软件。

8.1 文档支持

8.1.1 相关文档

8.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.3 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

8.4 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.5 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

9 修订历史记录

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision C (October 2003) to Revision D (August 2024)	Page
• 添加了*器件信息* 表、*引脚功能* 表、*热性能信息* 表、*器件功能模式*、”应用和实施“部分、*器件和文档支持* 部分以及*机械、封装和订购信息* 部分	1
• 更新了 R θ JA 值：PW = 113 至 145.7，所有值均以 °C/W 为单位	4

10 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件可用的最新数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。有关此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-89547022A	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-89547022A SNJ54ACT 08FK	Samples
5962-8954702CA	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8954702CA SNJ54ACT08J	Samples
5962-8954702DA	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8954702DA SNJ54ACT08W	Samples
SN74ACT08D	OBSOLETE	SOIC	D	14		TBD	Call TI	Call TI	-40 to 85	ACT08	
SN74ACT08DBR	ACTIVE	SSOP	DB	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AD08	Samples
SN74ACT08DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	ACT08	Samples
SN74ACT08DRG3	ACTIVE	SOIC	D	14	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 85	ACT08	Samples
SN74ACT08DRG4	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT08	Samples
SN74ACT08N	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74ACT08N	Samples
SN74ACT08NSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ACT08	Samples
SN74ACT08PW	OBSOLETE	TSSOP	PW	14		TBD	Call TI	Call TI	-40 to 85	AD08	
SN74ACT08PWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AD08	Samples
SN74ACT08PWRG4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	AD08	Samples
SNJ54ACT08FK	ACTIVE	LCCC	FK	20	55	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-89547022A SNJ54ACT 08FK	Samples
SNJ54ACT08J	ACTIVE	CDIP	J	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8954702CA SNJ54ACT08J	Samples
SNJ54ACT08W	ACTIVE	CFP	W	14	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8954702DA SNJ54ACT08W	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF SN54ACT08, SN74ACT08 :

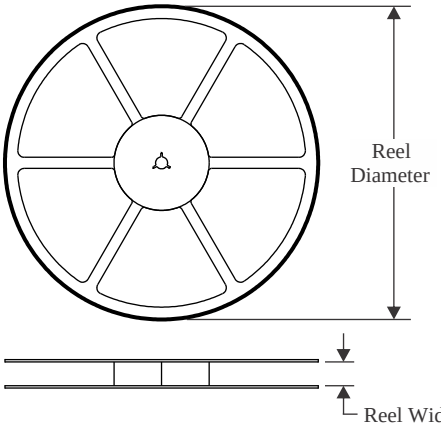
- Catalog : SN74ACT08
- Automotive : SN74ACT08-Q1, SN74ACT08-Q1
- Enhanced Product : SN74ACT08-EP, SN74ACT08-EP
- Military : SN54ACT08

NOTE: Qualified Version Definitions:

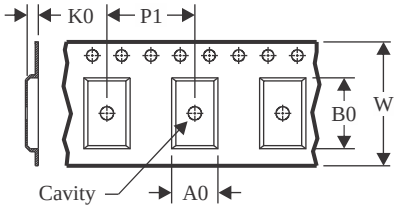
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

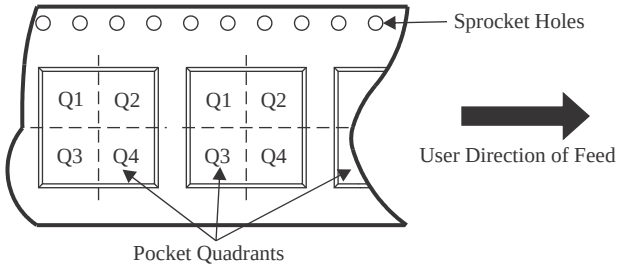


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

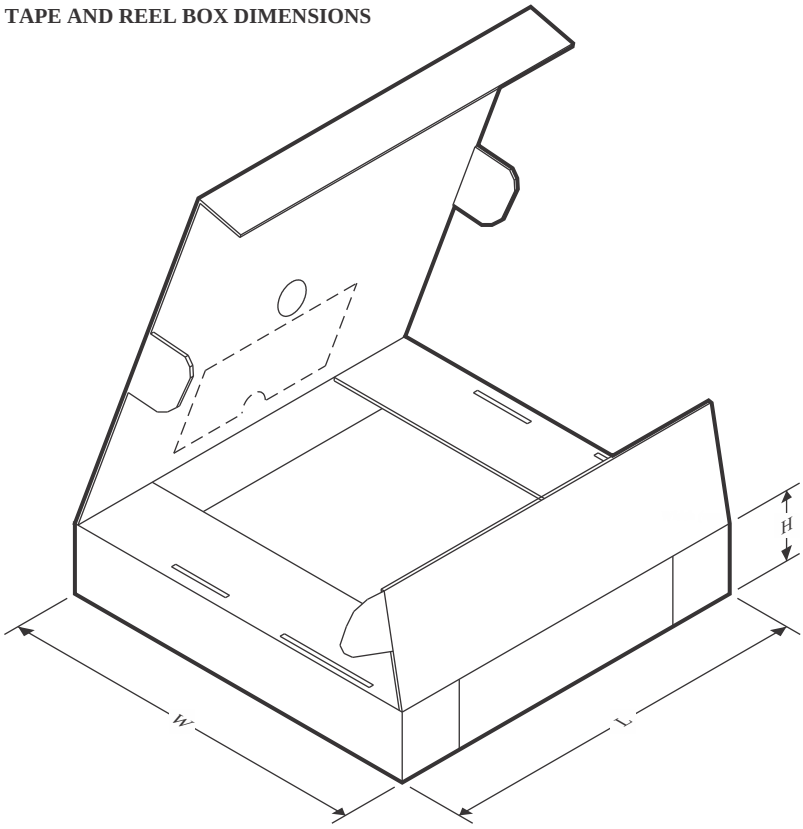
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74ACT08DBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74ACT08DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74ACT08DRG3	SOIC	D	14	2500	330.0	16.8	6.5	9.5	2.1	8.0	16.0	Q1
SN74ACT08DRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74ACT08DRG4	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74ACT08NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74ACT08PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74ACT08PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74ACT08PWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74ACT08PWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

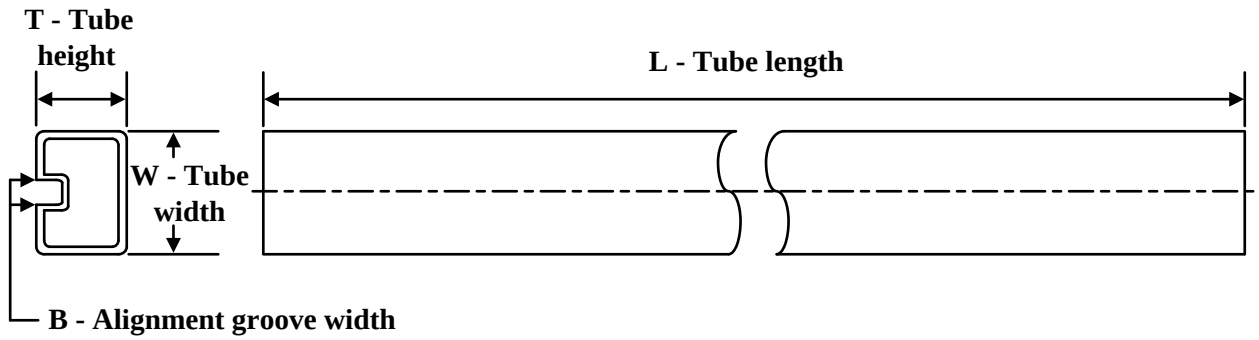
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

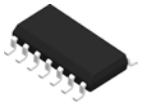
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74ACT08DBR	SSOP	DB	14	2000	356.0	356.0	35.0
SN74ACT08DR	SOIC	D	14	2500	353.0	353.0	32.0
SN74ACT08DRG3	SOIC	D	14	2500	364.0	364.0	27.0
SN74ACT08DRG4	SOIC	D	14	2500	340.5	336.1	32.0
SN74ACT08DRG4	SOIC	D	14	2500	356.0	356.0	35.0
SN74ACT08NSR	SO	NS	14	2000	356.0	356.0	35.0
SN74ACT08PWR	TSSOP	PW	14	2000	353.0	353.0	32.0
SN74ACT08PWR	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74ACT08PWRG4	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74ACT08PWRG4	TSSOP	PW	14	2000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962-89547022A	FK	LCCC	20	55	506.98	12.06	2030	NA
5962-8954702DA	W	CFP	14	25	506.98	26.16	6220	NA
SN74ACT08N	N	PDIP	14	25	506	13.97	11230	4.32
SN74ACT08N	N	PDIP	14	25	506	13.97	11230	4.32
SNJ54ACT08FK	FK	LCCC	20	55	506.98	12.06	2030	NA
SNJ54ACT08W	W	CFP	14	25	506.98	26.16	6220	NA

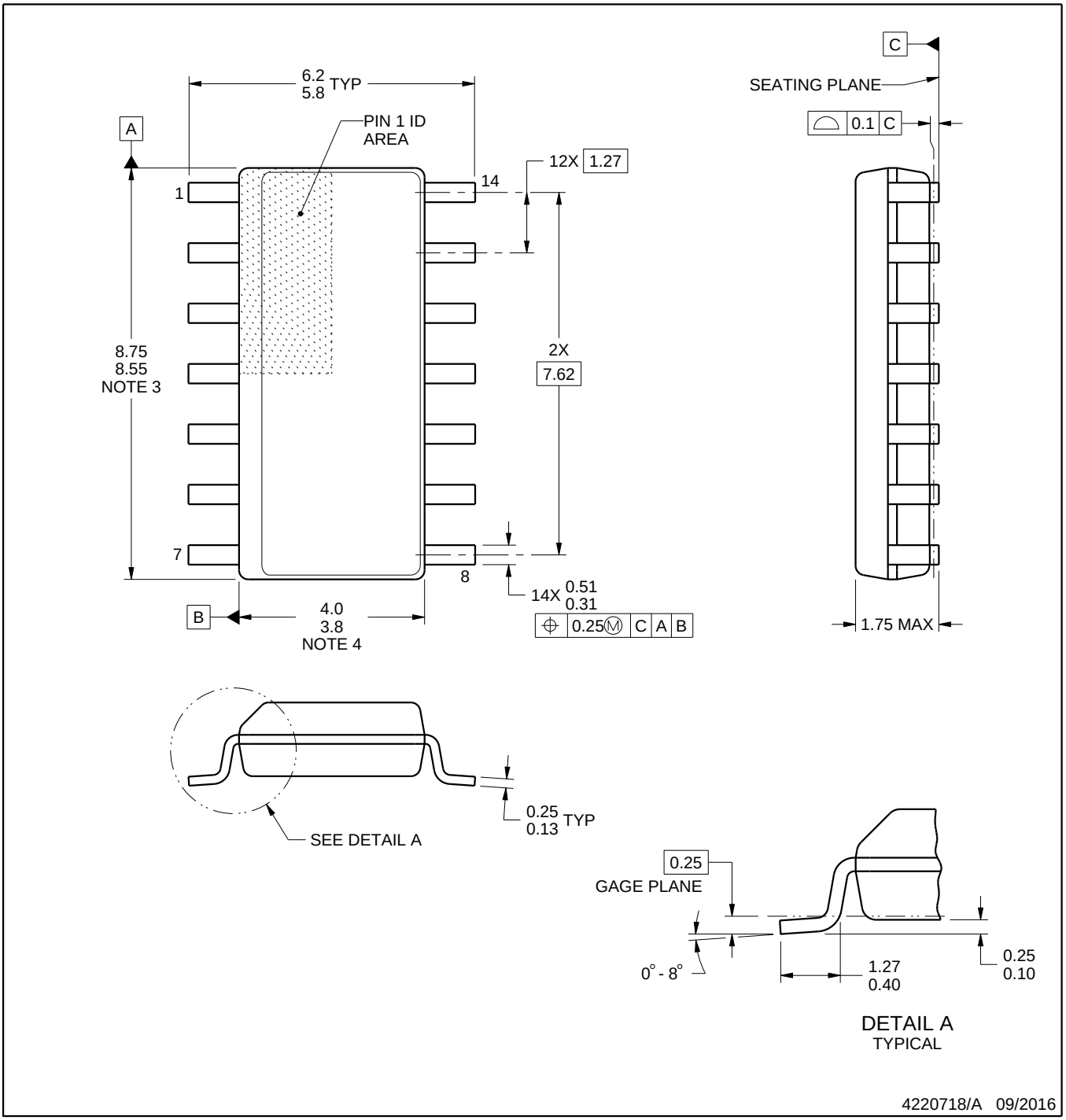


PACKAGE OUTLINE

D0014A

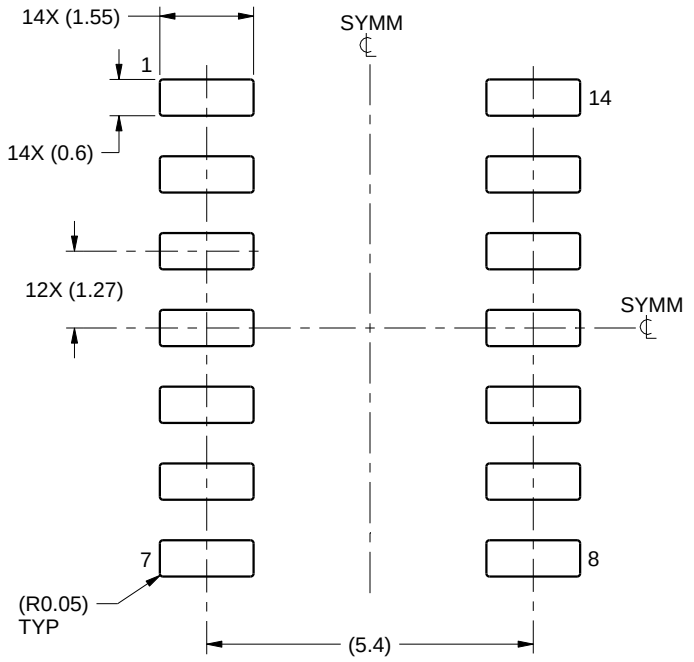
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

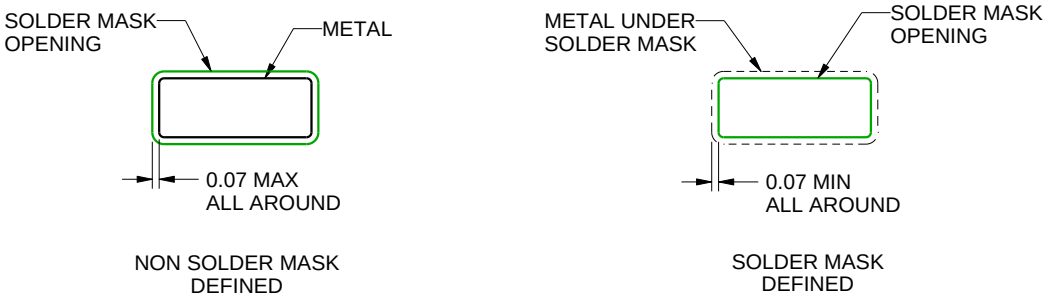


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

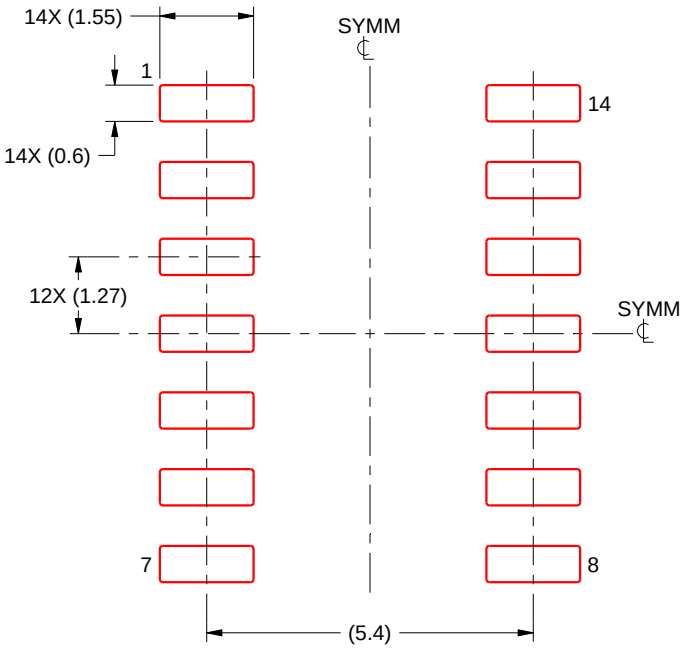
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

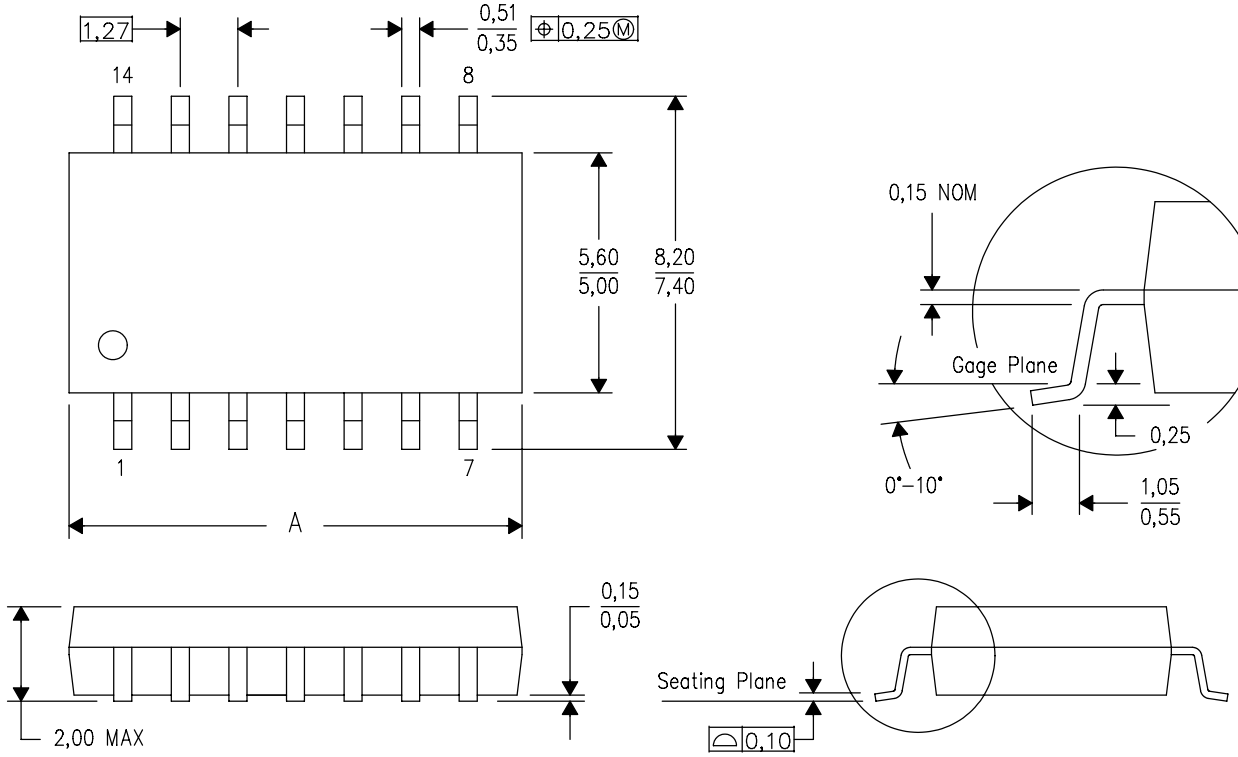
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN

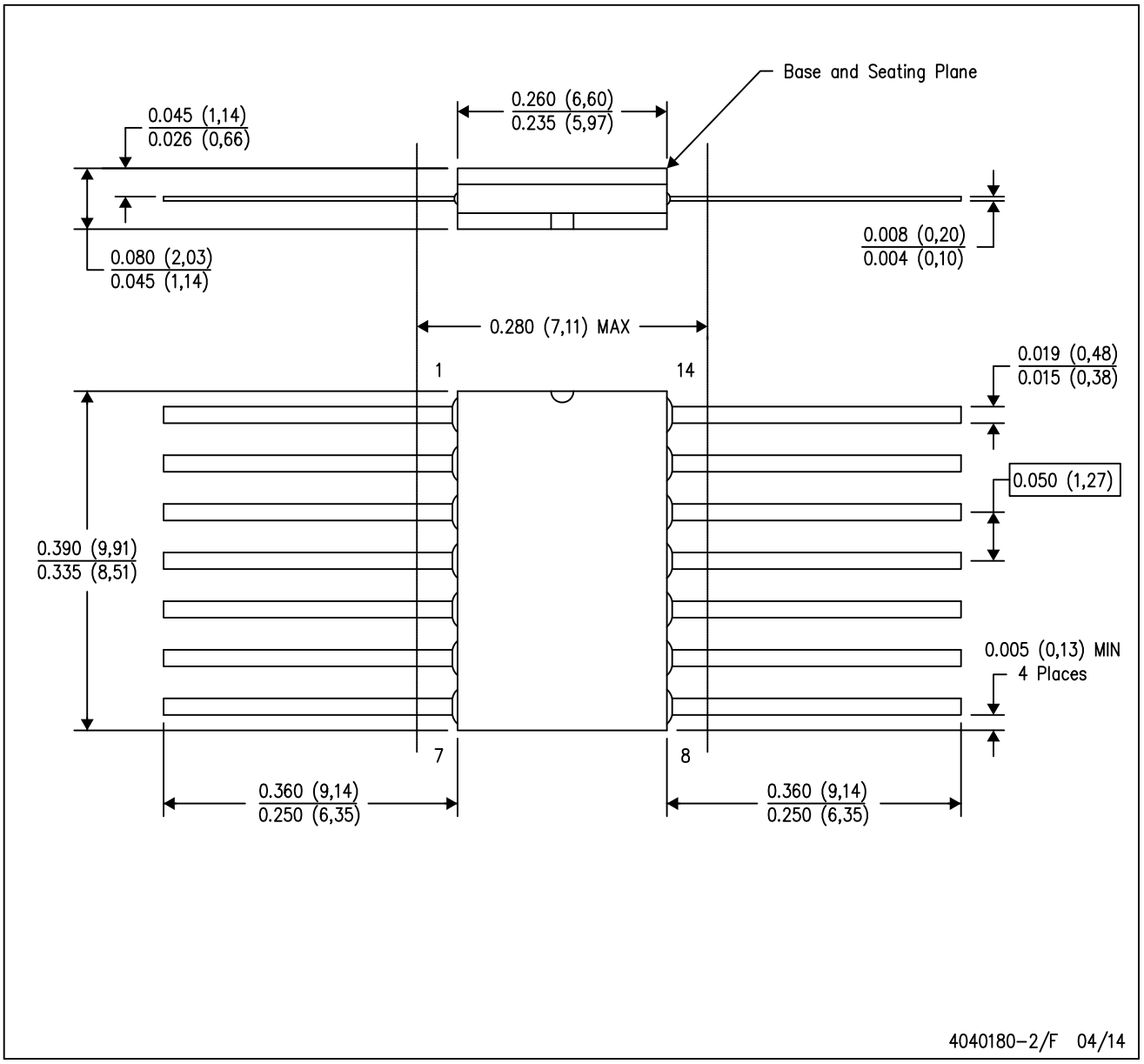


DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

W (R–GDFP–F14) CERAMIC DUAL FLATPACK



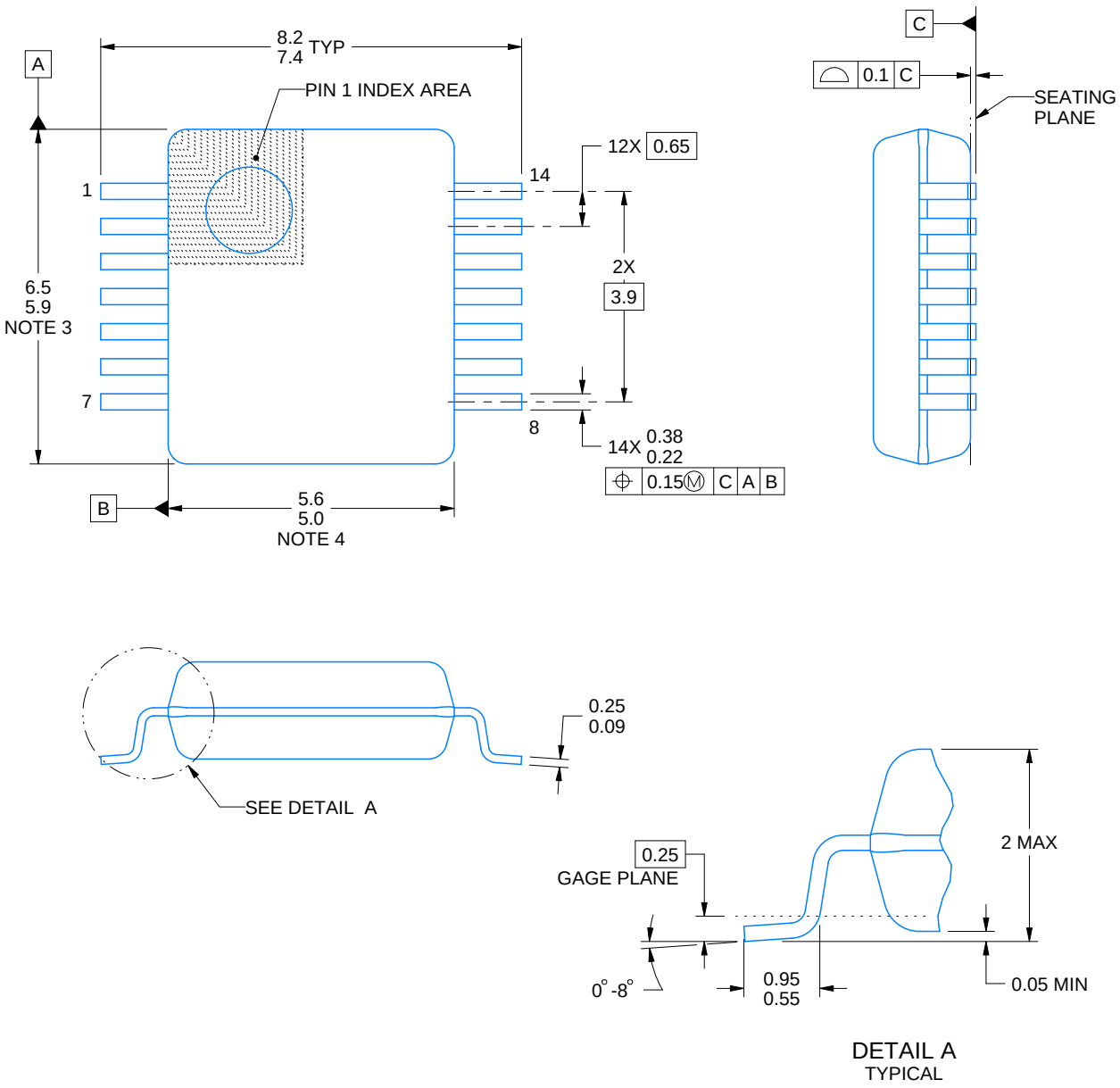
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within MIL STD 1835 GDFP1–F14

PACKAGE OUTLINE

DB0014A

SSOP - 2 mm max height

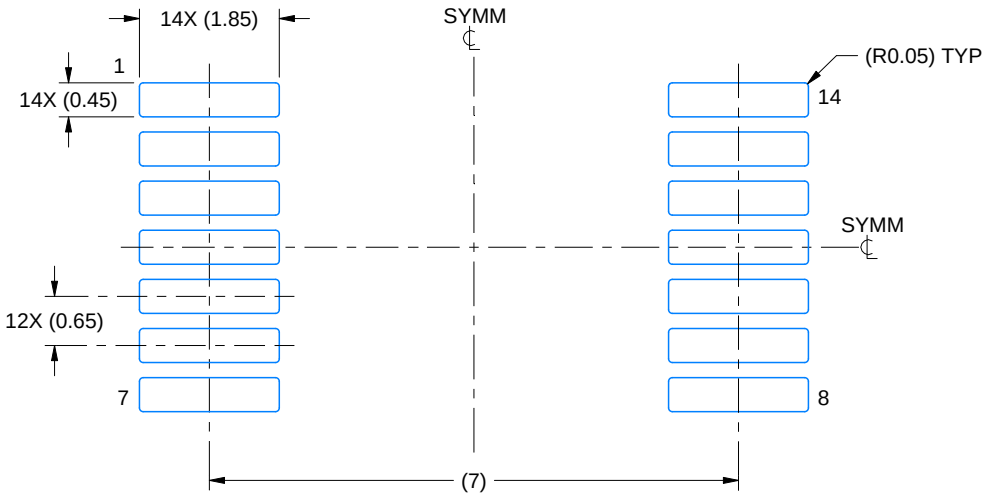
SMALL OUTLINE PACKAGE



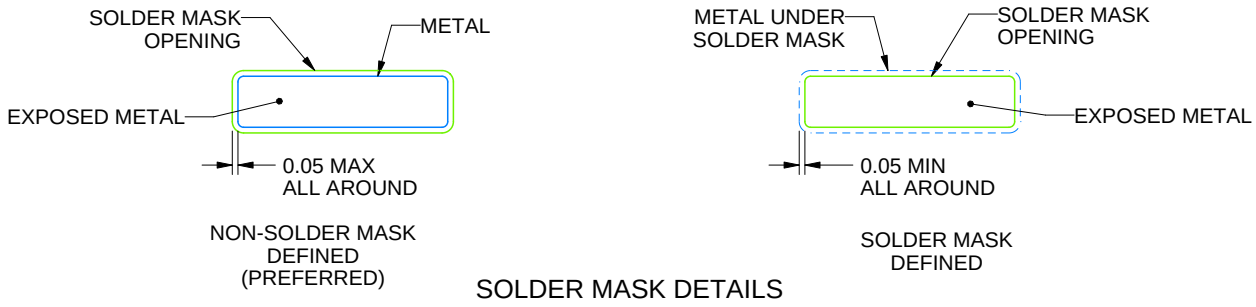
4220762/A 05/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

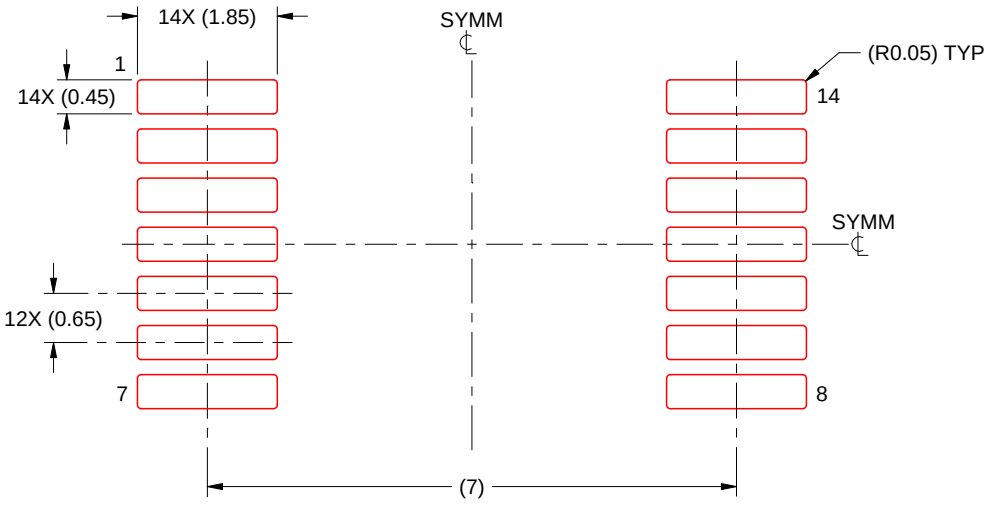


SOLDER MASK DETAILS

4220762/A 05/2024

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220762/A 05/2024

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

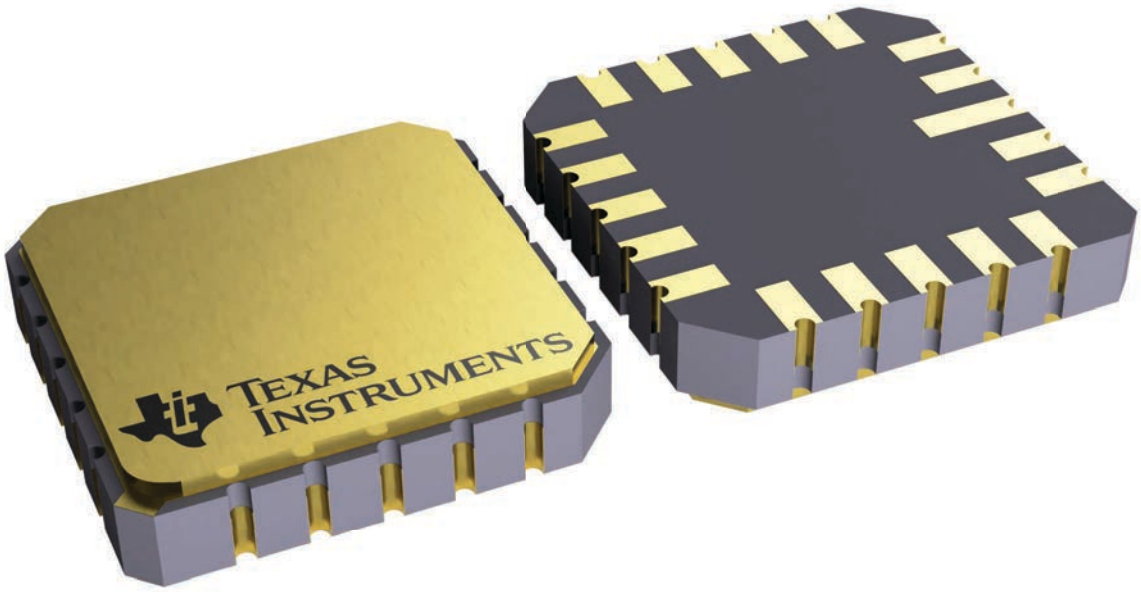
FK 20

LCCC - 2.03 mm max height

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

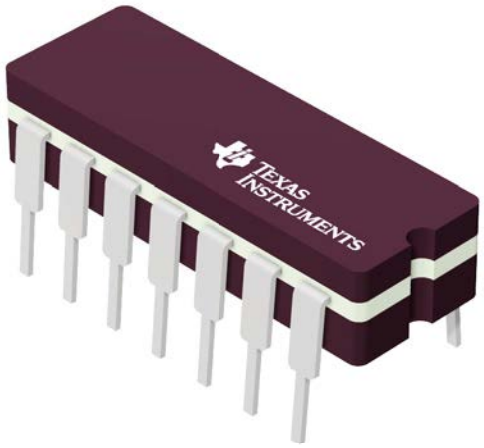


4229370VA\

GENERIC PACKAGE VIEW

J 14 CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

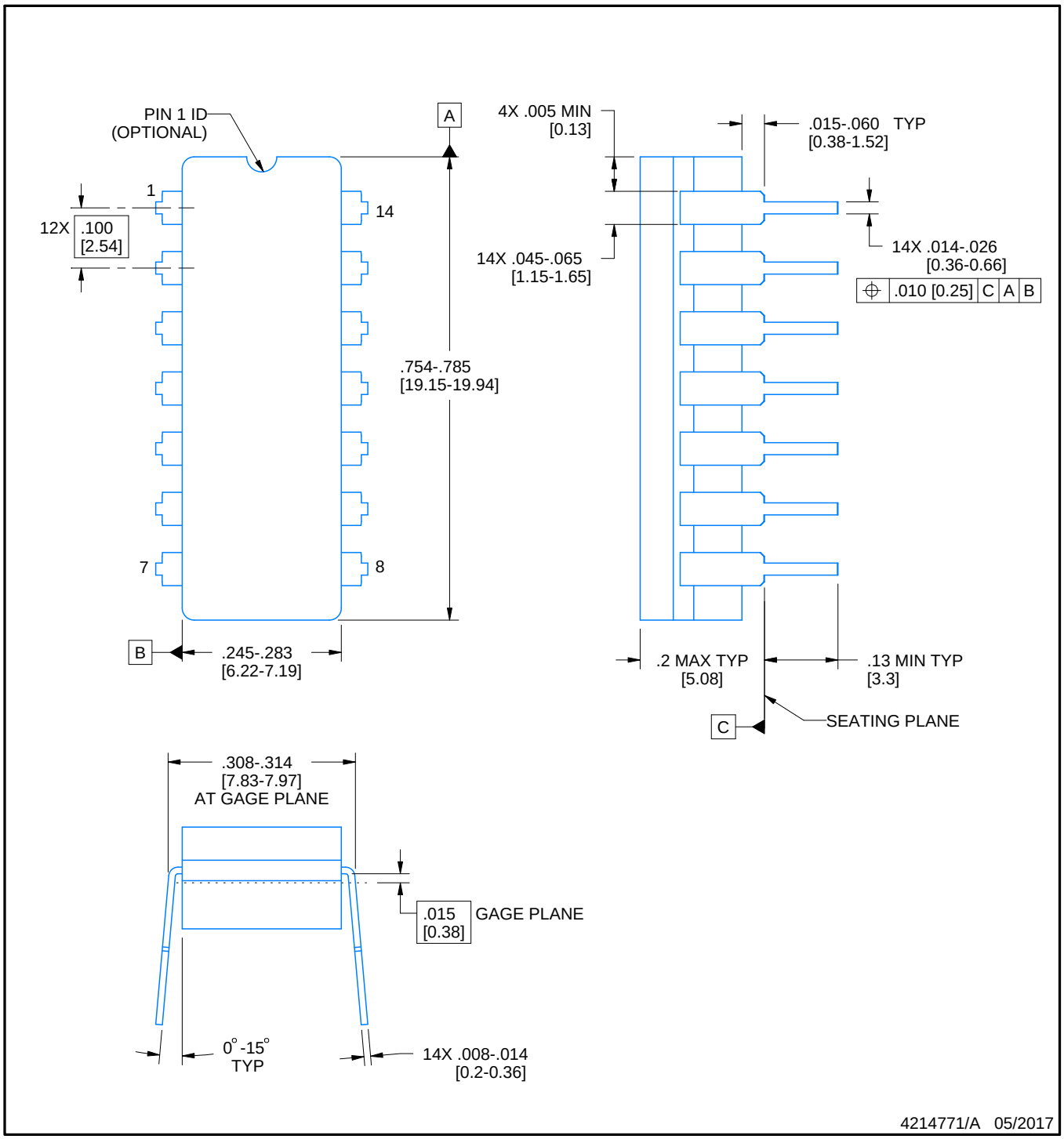
4040083-5/G

PACKAGE OUTLINE

J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



NOTES:

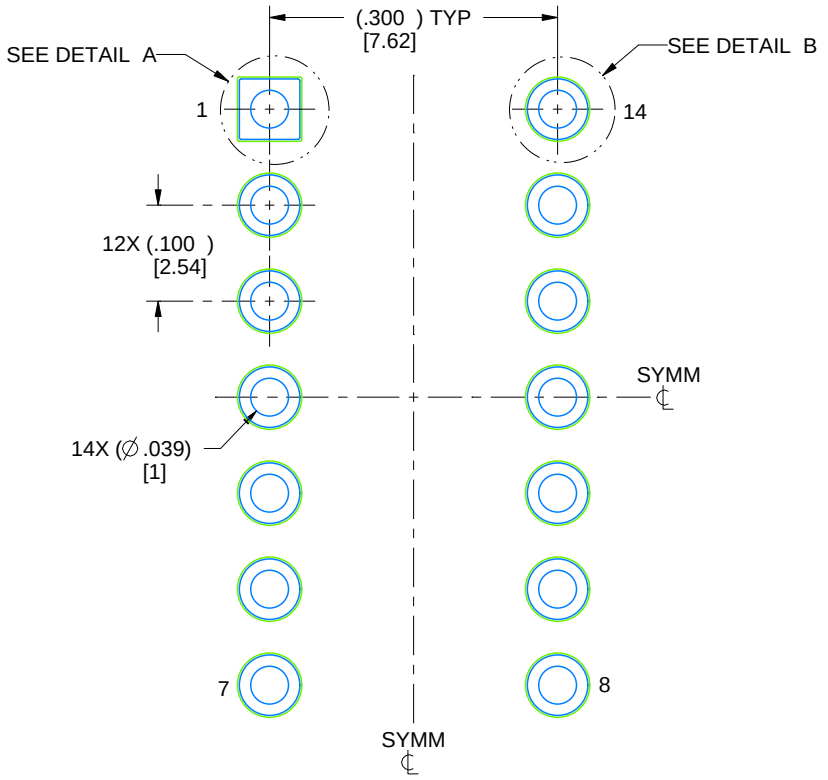
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermitically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.

EXAMPLE BOARD LAYOUT

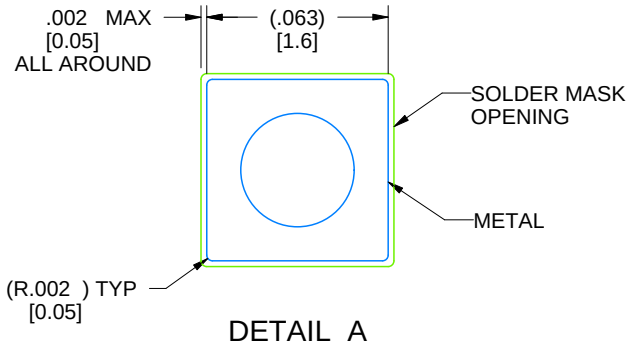
J0014A

CDIP - 5.08 mm max height

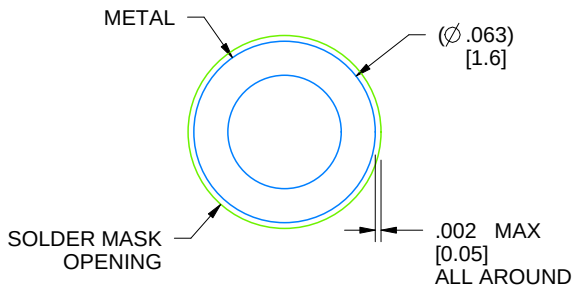
CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X



DETAIL A
SCALE: 15X



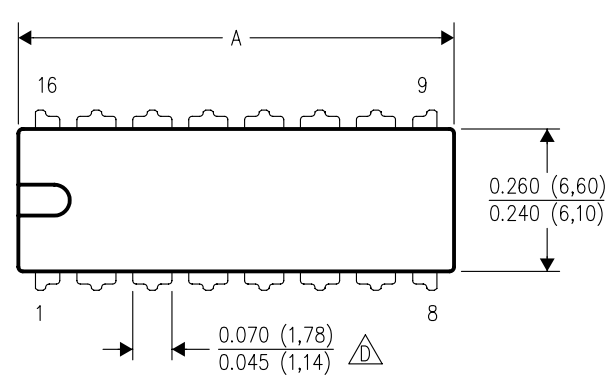
DETAIL B
13X, SCALE: 15X

4214771/A 05/2017

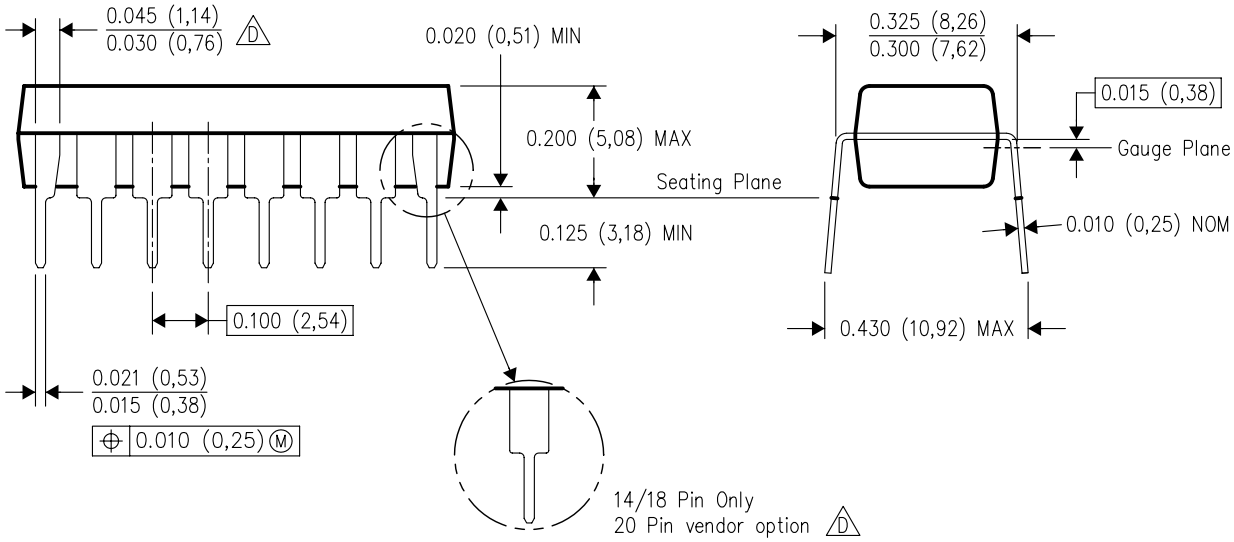
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

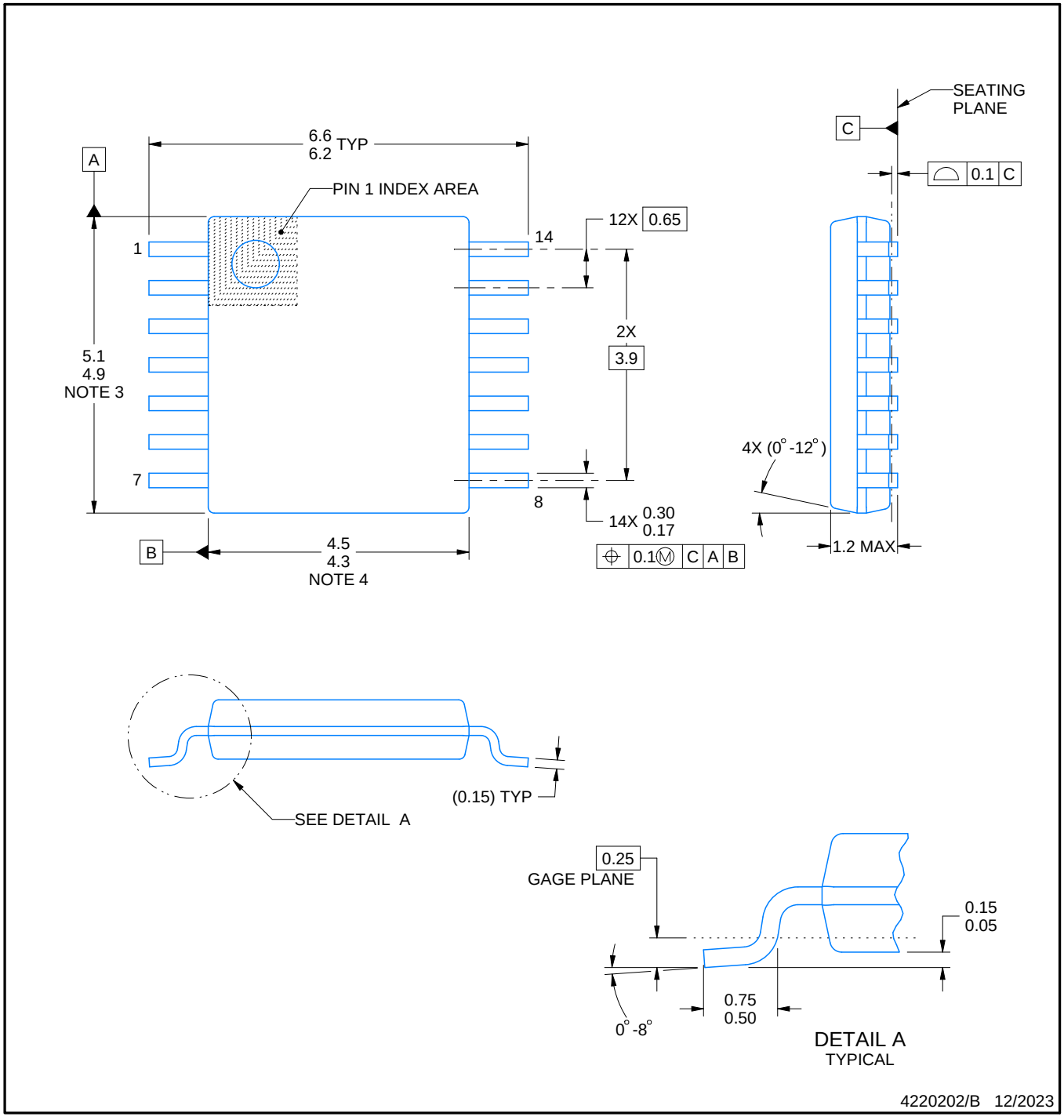
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

PACKAGE OUTLINE

PW0014A

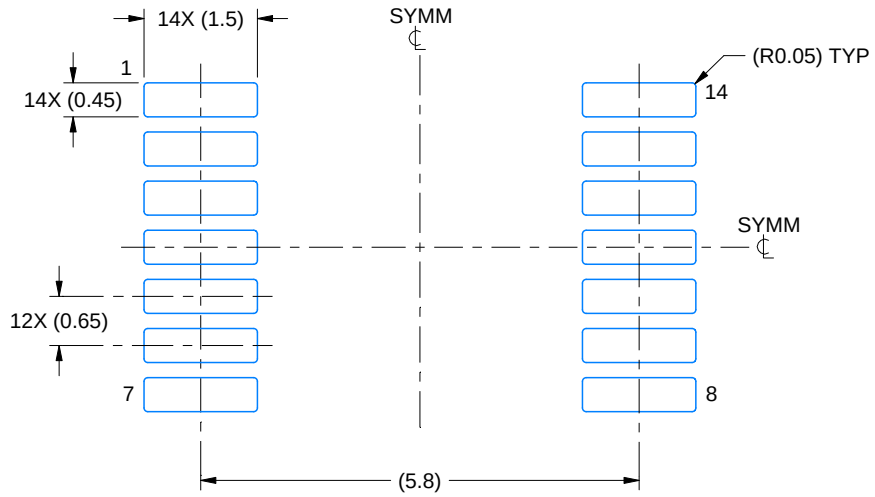
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

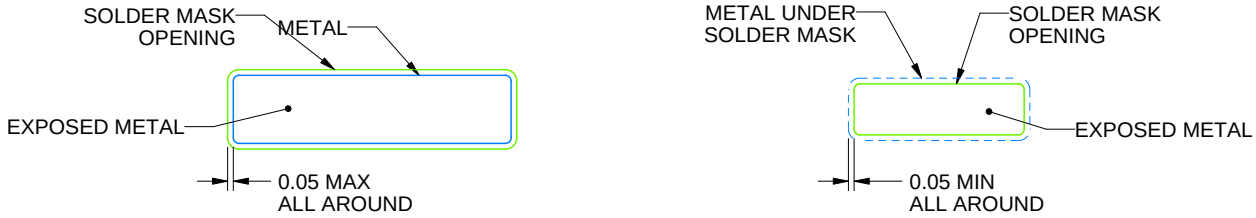


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

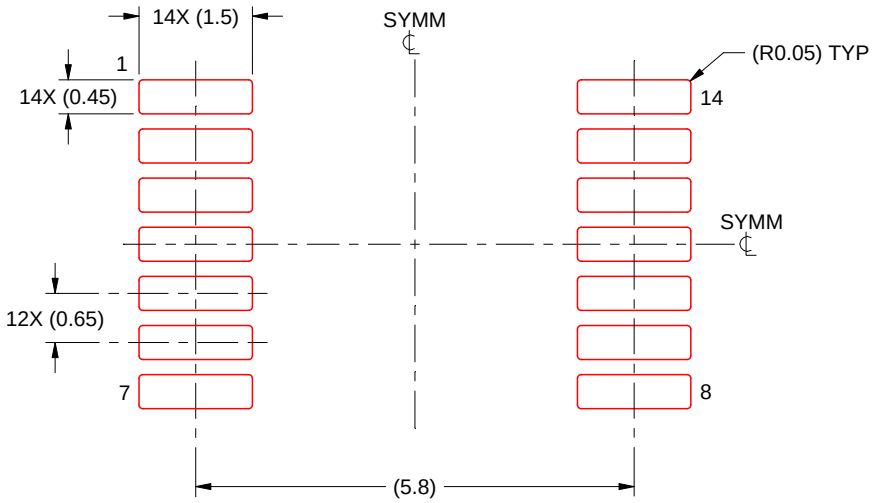


SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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