

# SN74AHC02-Q1 汽车类四路双输入正或非门

## 1 特性

- 符合汽车应用要求
- 工作电压范围为 2V 至 5.5V V<sub>CC</sub>

## 2 说明

SN74AHC02 包含四个独立的双输入或非门，这些门以正逻辑执行布尔函数  $Y = \overline{A \cdot B}$  或  $Y = \overline{A + B}$ 。

### 封装信息

器件型号	封装 <sup>1</sup>	封装尺寸 <sup>2</sup>
SN74AHC02-Q1	PW ( TSSOP , 14 )	5.00 mm x 6.4 mm
	BQA ( WQFN , 14 )	3mm x 2.5mm

- 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。
- 封装尺寸 ( 长 x 宽 ) 为标称值，并包括引脚 ( 如适用 )。

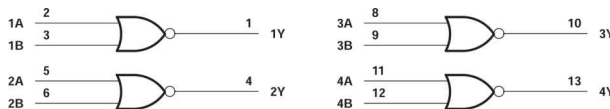


图 2-1. 逻辑图 ( 正逻辑 )



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### 3 Revision History

注：以前版本的页码可能与当前版本的页码不同

<b>Changes from Revision B (April 2008) to Revision C (June 2023)</b>	<b>Page</b>
• 添加了封装信息表、引脚功能表、ESD 等级表、热信息表、器件功能模式、器件和文档支持部分以及机械、封装和可订购信息部分.....	<b>1</b>
• 向封装信息表中添加了 BQA 封装.....	<b>1</b>
• Updated thermal values for PW package from $R^{\theta} JA = 113$ to $147.7$ , all values in $^{\circ}\text{C}/\text{W}$ .....	<b>5</b>
• Added thermal value for $R^{\theta} JA$ : BQA = $88.3$ , all values in $^{\circ}\text{C}/\text{W}$ .....	<b>5</b>

## 4 Pin Configuration and Functions

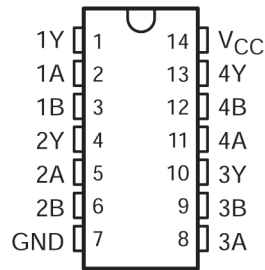


图 4-1. PW Package (Top View)

表 4-1. Pin Functions

NAME	PIN		TYPE <sup>(1)</sup>	DESCRIPTION
	SN74AHC02-Q1			
	D, DB, DGV, N, NS, PW, RGY, BQA			
1A	2		I	1A Input
1B	3		I	1B Input
1Y	1		O	1Y Output
2A	5		I	2A Input
2B	6		I	2B Input
2Y	4		O	2Y Output
3A	8		I	3A Input
3B	9		I	3B Input
3Y	10		O	3Y Output
4A	11		I	4A Input
4B	12		I	4B Input
4Y	13		O	4Y Output
GND	7		—	Ground Pin
NC	—		—	No Connection
V <sub>CC</sub>	14		—	Power Pin

(1) I = input, O = output

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage range	-0.5	7	V
$V_I$ <sup>1</sup>	Input voltage range	-0.5	7	V
$V_O$ <sup>1</sup>	Output voltage range	-0.5	$V_{CC} + 0.5$	V
$I_{IK}$	Input clamp current		-20	mA
				( $V_I < 0$ )
$I_{OK}$	Output clamp current		±20	mA
				( $V_O < 0$ or $V_O > V_{CC}$ )
$I_O$	Continuous output current		±25	mA
				( $V_O = 0$ to $V_{CC}$ )
	Continuous current through $V_{CC}$ or GND		±50	mA
$T_{stg}$	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 5.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM) <sup>1</sup>	±1000 V

- (1) AEC Q100-002 indicates that HBM stressing must be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 5.3 Recommended Operating Conditions

see over recommended operating free-air temperature range (unless otherwise noted)<sup>1</sup>

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	2	5.5	V
$V_{IH}$	High-level input voltage	$V_{CC} = 2\text{ V}$	1.5	V
		$V_{CC} = 3\text{ V}$	2.1	
		$V_{CC} = 5.5\text{ V}$	3.85	
$V_{IL}$	Low-level input voltage	$V_{CC} = 2\text{ V}$	0.5	V
		$V_{CC} = 3\text{ V}$	0.9	
		$V_{CC} = 5.5\text{ V}$	1.65	
$V_I$	Input voltage	0	5.5	V
$V_O$	Output voltage	0	$V_{CC}$	V
$I_{OH}$	High-level output current	$V_{CC} = 2\text{ V}$	-50	mA
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	-4	mA
		$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$	-8	mA
$I_{OL}$	Low-level output current	$V_{CC} = 2\text{ V}$	50	mA
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	4	mA
		$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$	8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	100	ns/V
		$V_{CC} = 5\text{ V} \pm 0.5\text{ V}$	20	
$T_A$	Operating free-air temperature	-40	125	°C

- (1) All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## 5.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		SN74AHC02-Q1		UNIT
		PW (TSSOP)	BQA (WQFN)	
		14 PINS	14 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	147.7	88.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

## 5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V <sub>OH</sub>	I <sub>OH</sub> = -50 μA	2 V	1.9	2		1.9	V	
		3 V	2.9	3		2.9		
		4.5 V	4.4	4.5		4.4		
	I <sub>OH</sub> = -4 mA	3 V	2.58			2.48		
	I <sub>OH</sub> = -8 mA	4.5 V	3.94			3.8		
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	2 V			0.1	0.1	V	
		3 V			0.1	0.1		
		4.5 V			0.1	0.1		
	I <sub>OL</sub> = 4 mA	3 V			0.36	0.5		
	I <sub>OL</sub> = 8 mA	4.5 V			0.36	0.5		
I <sub>I</sub>	V <sub>I</sub> = 5.5 V or GND	0 V to 5.5 V			±0.1	±1	μA	
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V			2	20	μA	
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5 V		4	10		pF	

## 5.6 Switching Characteristics, V<sub>CC</sub> = 3.3 V ± 0.3 V

over recommended operating free-air temperature range, V<sub>CC</sub> = 3.3 V ± 0.3 V (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t <sub>PLH</sub>	A or B	Y	C <sub>L</sub> = 15 pF		5.6	7.9	1	9.5	ns
t <sub>PHL</sub>					5.6	7.9	1	9.5	
t <sub>PLH</sub>	A or B	Y	C <sub>L</sub> = 50 pF		8.1	11.4	1	13	ns
t <sub>PHL</sub>					8.1	11.4	1	13	

## 5.7 Switching Characteristics, V<sub>CC</sub> = 5 V ± 0.5 V

over recommended operating free-air temperature range, V<sub>CC</sub> = 5 V ± 0.5 V (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t <sub>PLH</sub>	A or B	Y	C <sub>L</sub> = 15 pF		3.6	5.5	1	6.5	ns
t <sub>PHL</sub>					3.6	5.5	1	6.5	
t <sub>PLH</sub>	A or B	Y	C <sub>L</sub> = 50 pF		5.1	7.5	1	8.5	ns
t <sub>PHL</sub>					5.1	7.5	1	8.5	

## 5.8 Noise Characteristics

$V_{CC} = 5\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$ <sup>1</sup>

PARAMETER		MIN	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic $V_{OL}$		0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic $V_{OL}$		-0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic $V_{OH}$	4.9		V
$V_{IH(D)}$	High-level dynamic input voltage	3.5		V
$V_{IL(D)}$	Low-level dynamic input voltage		1.5	V

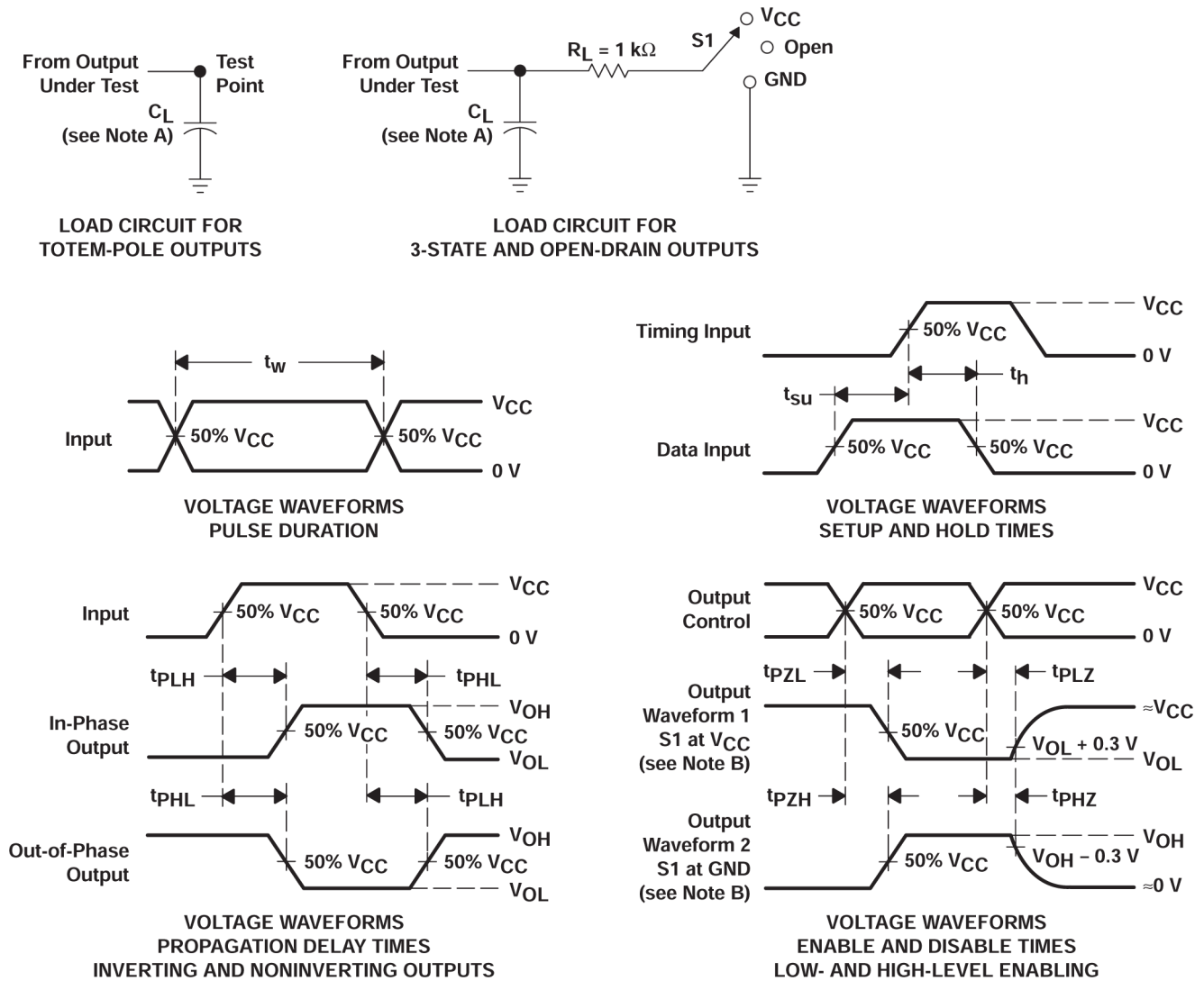
(1) Characteristics are for surface-mount packages only.

## 5.9 Operating Characteristics

$V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS		TYP	UNIT
$C_{pd}$	Power dissipation capacitance	No load,	$f = 1\text{ MHz}$	15	pF

## 6 Parameter Measurement Information



- A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 3$  ns,  $t_f \leq 3$  ns.
- D. The outputs are measured one at a time with one input transition per measurement.
- E. All parameters and waveforms are not applicable to all devices.

图 6-1. Load Circuit and Voltage Waveforms

TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$V_{CC}$
$t_{PHZ}/t_{PZH}$	GND
Open Drain	$V_{CC}$

## 7 Detailed Description

### 7.1 Functional Block Diagram

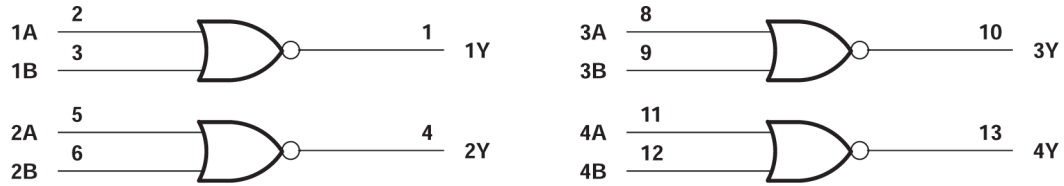


图 7-1. Logic Diagram (Positive Logic)

### 7.2 Device Functional Modes

表 7-1. Function Table (Each Gate)

INPUTS		OUTPUT Y
A	B	
H	X	L
X	H	L
L	L	H



## 8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 8.1 Documentation Support

#### 8.1.1 Related Documentation

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**表 8-1. Related Links**

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN74AHC02-Q1	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

### 8.2 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](http://ti.com) 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 8.3 支持资源

[TI E2E™ 支持论坛](#) 是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《[使用条款](#)》。

### 8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

### 8.5 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 8.6 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

## 9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AHC02QPWRG4Q1	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC02Q1	<a href="#">Samples</a>
SN74AHC02QPWRQ1	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC02Q1	<a href="#">Samples</a>
SN74AHC02QWBQARQ1	ACTIVE	WQFN	BQA	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC02Q	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN74AHC02-Q1 :**

- Catalog : [SN74AHC02](#)
- Enhanced Product : [SN74AHC02-EP](#)
- Military : [SN54AHC02](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC02QPWRG4Q1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC02QPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AHC02QWBQARQ1	WQFN	BQA	14	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**

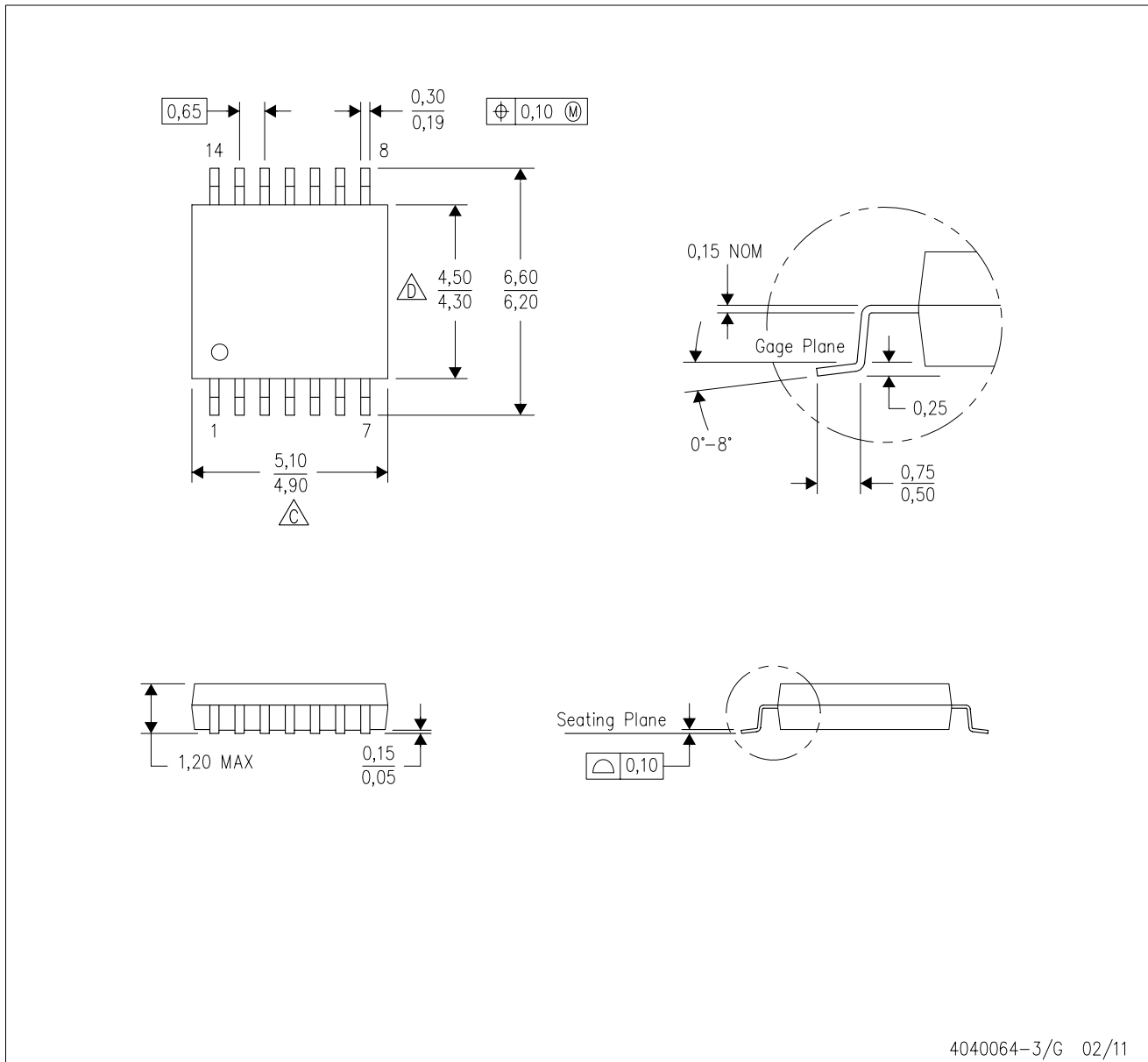

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC02QPWRG4Q1	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74AHC02QPWRQ1	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74AHC02QWBQARQ1	WQFN	BQA	14	3000	210.0	185.0	35.0

**MECHANICAL DATA**

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040064-3/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  -  Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211284-2/G 08/15

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



## GENERIC PACKAGE VIEW

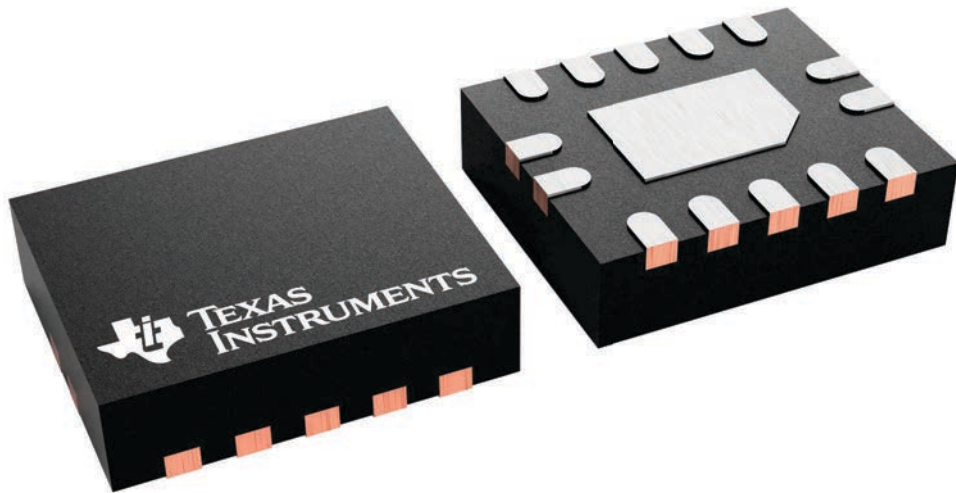
**BQA 14**

**WQFN - 0.8 mm max height**

2.5 x 3, 0.5 mm pitch

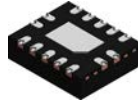
PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4227145/A

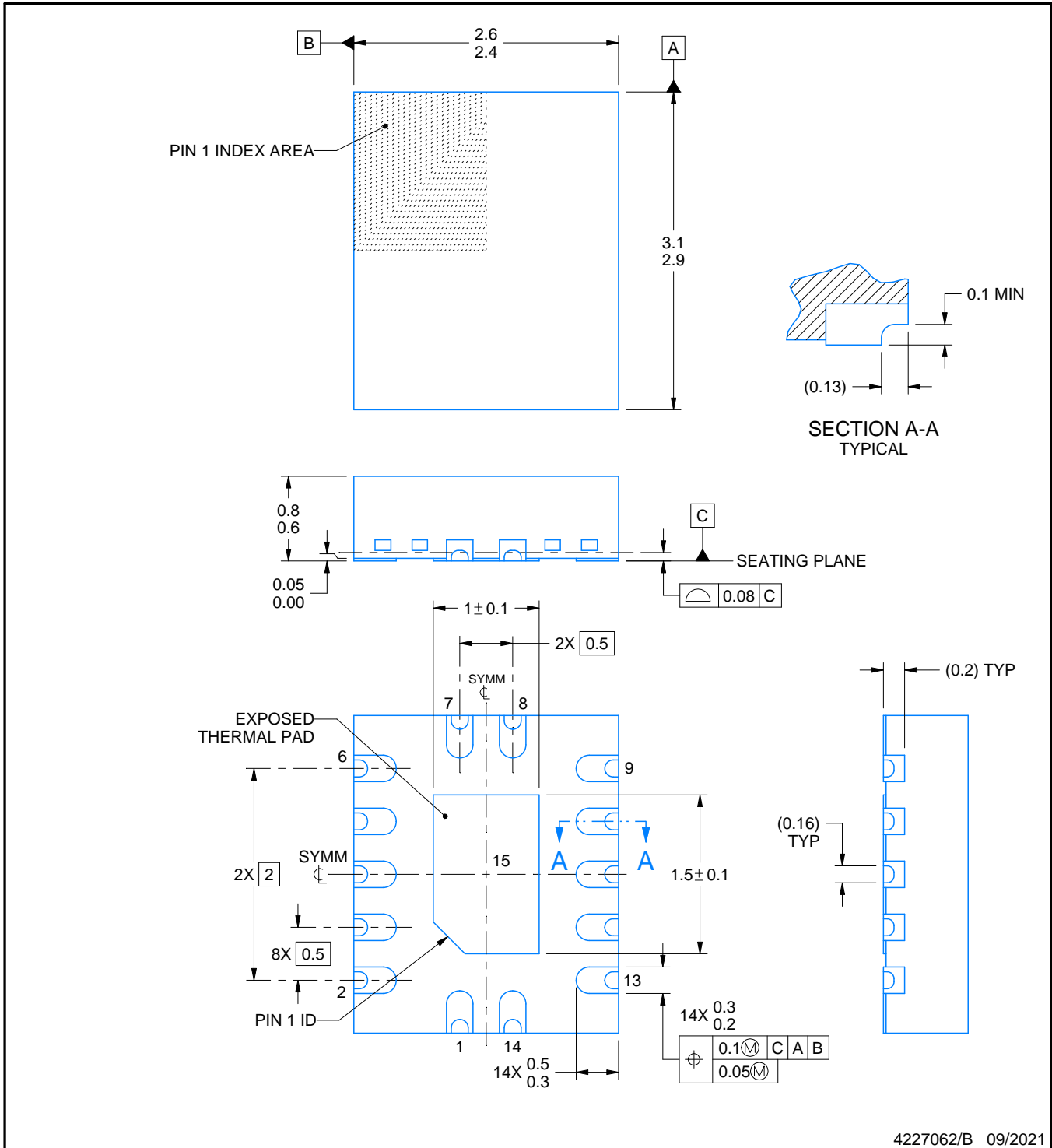
# BQA0014B



## PACKAGE OUTLINE

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



**NOTES:**

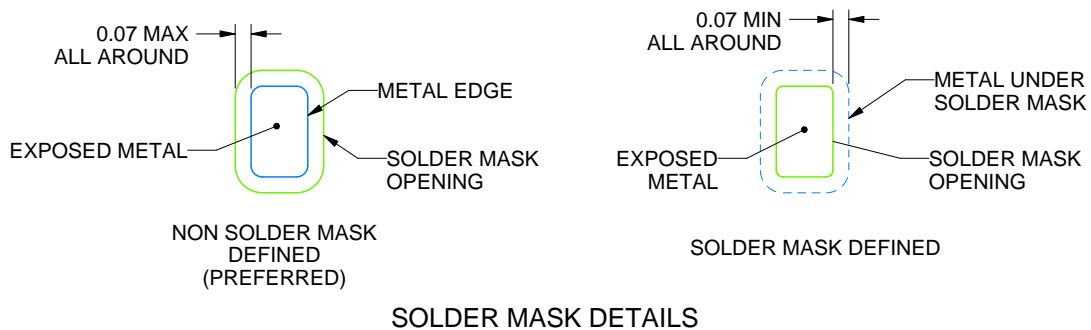
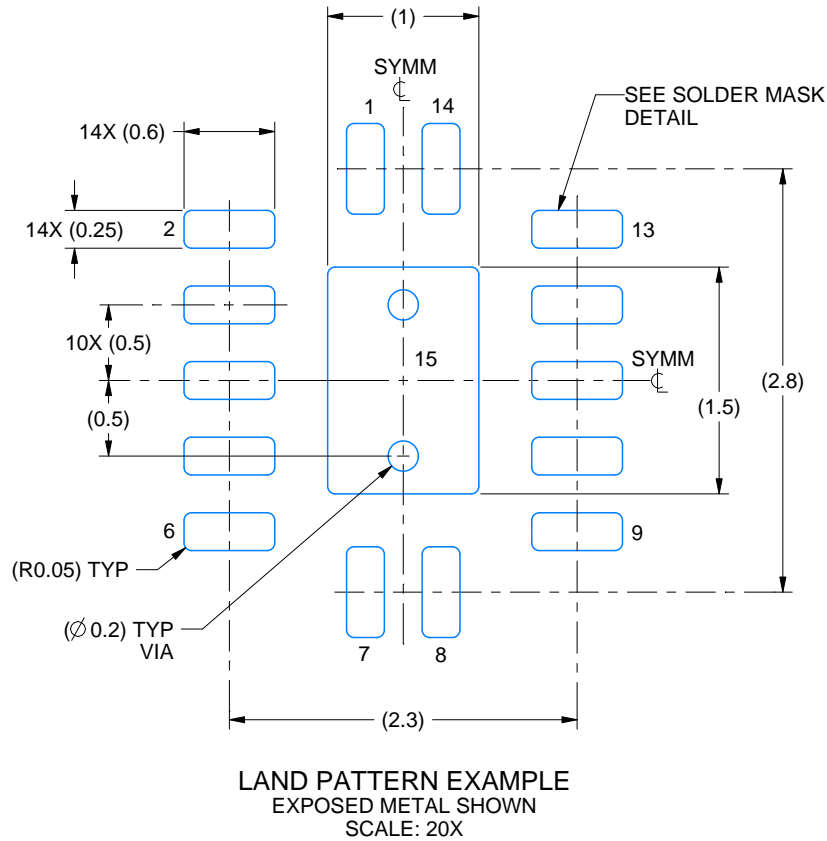
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

**BQA0014B**

**WQFN - 0.8 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



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NOTES: (continued)

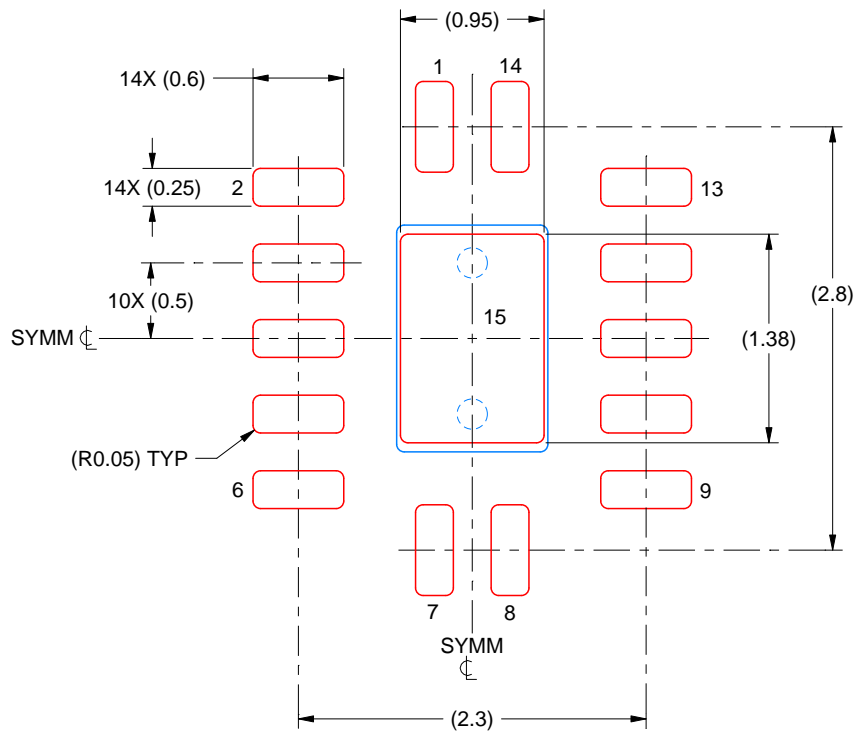
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

BQA0014B

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 MM THICK STENCIL  
SCALE: 20X

EXPOSED PAD 15  
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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