

SN74AVC2T45 具有可配置电平转换和电压转换的 2 位双电源总线收发器

1 特性

- 采用德州仪器 (TI) NanoFree™ 封装
- V_{CC} 隔离特性：如果任何一个 V_{CC} 输入接地 (GND)，那么两个端口都处于高阻抗状态
- 双电源轨设计
- I/O 可承受 4.6V 过压
- I_{off} 支持局部断电模式运行
- 最大数据速率
 - 500Mbps (1.8V 至 3.3V)
 - 320Mbps (<1.8V 至 3.3V)
 - 320Mbps (电平转换至 2.5V 或 1.8V)
 - 280Mbps (电平转换至 1.5V)
 - 240Mbps (电平转换至 1.2V)
- 闩锁性能超过 100mA，符合 JESD 78 II 类规范的要求
- ESD 保护性能超过 JESD 22 规范要求

2 应用

- 智能手机
- 服务器
- 台式计算机和笔记本电脑
- 其他便携式设备

3 说明

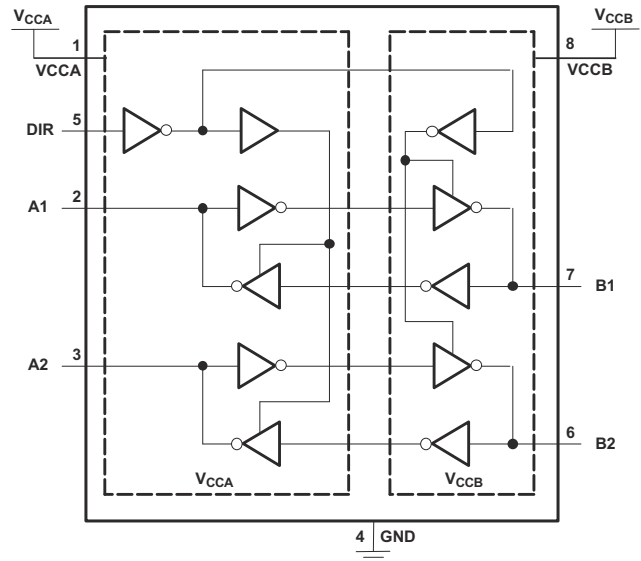
这款 2 位同相总线收发器使用两个独立的可配置电源轨。A 端口用于跟踪 V_{CCA} ，可支持 1.2V 至 3.6V 范围内的任何电源电压。B 端口用于跟踪 V_{CCB} ，可支持 1.2V 至 3.6V 范围内的任何电源电压。因此可在 1.2V、1.5V、1.8V、2.5V 和 3.3V 电压节点之间进行通用的低压双向转换和电平转换。

SN74AVC2T45 旨在实现两条数据总线间的异步通信。方向控制 (DIR 引脚) 输入的逻辑电平会激活 B 端口或 A 端口输出。当 B 端口输出被激活时，此器件将数据从 A 总线发送到 B 总线，而当 A 端口输出被激活时，此器件将数据从 B 总线发送到 A 总线。A 端口和 B 端口上的输入电路一直处于活动状态并且必须施加一个逻辑高或低电平，从而防止内部 CMOS 结构上产生过大的漏电流。

封装信息

器件型号	封装 ⁽¹⁾	封装尺寸 (标称值)
SN74AVC2T45DCT	DCT (SSOP , 8)	2.95mm × 2.80mm
SN74AVC2T45DCU	DCU (VSSOP , 8)	2.30mm × 2.00mm
SN74AVC2T45YZP	YZP (DSBGA , 8)	1.89mm × 0.89mm
SN74AVC2T45DDF	DDF (SOT-23 , 8)	2.90mm × 1.60mm

(1) 有关所有可用封装，请参阅节 11。



A. 引脚编号仅适用于 DCT 和 DCU 封装。

逻辑图 (正逻辑)



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4 Pin Configuration and Functions

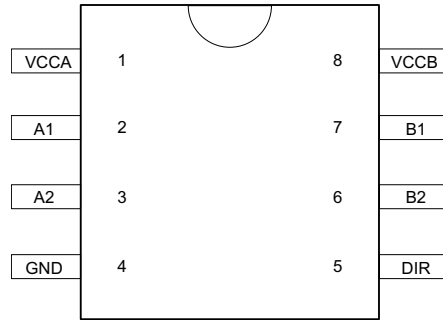


图 4-1. DCT or DCU Package 8-Pin SM8 or VSSOP Top View

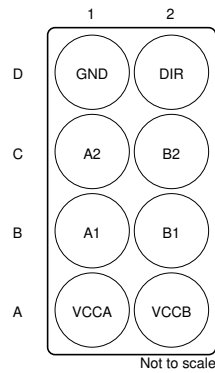


图 4-2. YZP Package 8-Pin DSBGA Bottom View

Pin Functions

NAME	PIN		TYPE ⁽¹⁾	DESCRIPTION
	NO. (SM8, VSSOP)	NO. (DSBGA)		
VCCA	1	A1	—	Supply Voltage A
VCCB	8	A2	—	Supply Voltage B
GND	4	D1	—	Ground
A1	2	B1	I/O	Output or input depending on state of DIR. Output level depends on V_{CCA} .
A2	3	C1	I/O	Output or input depending on state of DIR. Output level depends on V_{CCA} .
B1	7	B2	I/O	Output or input depending on state of DIR. Output level depends on V_{CCB} .
B2	6	C2	I/O	Output or input depending on state of DIR. Output level depends on V_{CCB} .
DIR	5	D2	I	Direction Pin, Connect to GND or to VCCA

(1) I = Input; O = Output; I/O = Input or Output

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT	
V_{CCA} V_{CCB}	Supply voltage	- 0.5	4.6	V	
V_I	Input voltage ⁽²⁾	IO ports (A port)	- 0.5	4.6	V
		IO ports (B port)	- 0.5	4.6	
		Control inputs	- 0.5	4.6	
V_O	Voltage applied to any output in the high-impedance or power-off state ⁽²⁾	A port	- 0.5	4.6	V
		B port	- 0.5	4.6	
V_O	Voltage applied to any output in the high or low state ^{(2) (3)}	A port	- 0.5	$V_{CCA} + 0.5$	V
		B port	- 0.5	$V_{CCB} + 0.5$	
I_{IK}	Input clamp current	$V_I < 0$	- 50	mA	
I_{OK}	Output clamp current	$V_O < 0$	- 50	mA	
I_O	Continuous output current		±50	mA	
	Continuous current through V_{CCA} , V_{CCB} , or GND		±100	mA	
T_J	Junction temperature		150	°C	
T_{stg}	Storage temperature	- 65	150	°C	

- (1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) The input negative-voltage and output voltage ratings can be exceeded if the input and output current ratings are observed.
- (3) The output positive-voltage rating can be exceeded up to 4.6 V maximum if the output current ratings are observed.

5.2 ESD Ratings

		VALUE	UNIT	
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±8000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000	
		Machine Model (MM), Per JEDEC specification JESD22-A115-A	±200	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

See (3) (4) (5)

		$V_{CCI}^{(1)}$	$V_{CCO}^{(2)}$	MIN	MAX	UNIT
V_{CCA}	Supply voltage			1.2	3.6	V
V_{CCB}	Supply voltage			1.2	3.6	V
V_{IH}	High-level input voltage	Data inputs ⁽⁴⁾	1.2 V to 1.95 V	$V_{CCI}^{(1)} \times 0.65$		V
			1.95 V to 2.7 V	1.6		
			2.7 V to 3.6 V	2		
V_{IL}	Low-level input voltage	Data inputs ⁽⁴⁾	1.2 V to 1.95 V	$V_{CCI}^{(1)} \times 0.35$		V
			1.95 V to 2.7 V	0.7		
			2.7 V to 3.6 V	0.8		
V_{IH}	High-level input voltage	DIR (referenced to V_{CCA}) ⁽⁵⁾	1.2 V to 1.95 V	$V_{CCA} \times 0.65$		V
			1.95 V to 2.7 V	1.6		
			2.7 V to 3.6 V	2		
V_{IL}	Low-level input voltage	DIR (referenced to V_{CCA}) ⁽⁵⁾	1.2 V to 1.95 V	$V_{CCA} \times 0.35$		V
			1.95 V to 2.7 V	0.7		
			2.7 V to 3.6 V	0.8		
V_I	Input voltage			0	3.6	V
V_O	Output voltage	Active state		0	$V_{CCO}^{(2)}$	V
		3-state		0	3.6	
I_{OH}	High-level output current		1.2 V	-3		mA
			1.4 V to 1.6 V	-6		
			1.65 V to 1.95 V	-8		
			2.3 V to 2.7 V	-9		
			3 V to 3.6 V	-12		
I_{OL}	Low-level output current		1.2 V	3		mA
			1.4 V to 1.6 V	6		
			1.65 V to 1.95 V	8		
			2.3 V to 2.7 V	9		
			3 V to 3.6 V	12		
$\Delta t / \Delta v$	Input transition rise or fall rate				5	ns/V
T_A	Operating free-air temperature			-40	85	°C

(1) V_{CCI} is the voltage associated with the input port supply V_{CCA} or V_{CCB} .

(2) V_{CCO} is the voltage associated with the output port supply V_{CCA} or V_{CCB} .

(3) All unused data inputs of the device must be held at V_{CCI} or GND to provide proper device operation. See [Implications of Slow or Floating CMOS Inputs](#), SCBA004.

(4) For V_{CCI} values not specified in the data sheet, $V_{IH} \text{ min} = V_{CCI} \times 0.7 \text{ V}$, $V_{IL} \text{ max} = V_{CCI} \times 0.3 \text{ V}$.

(5) For V_{CCI} values not specified in the data sheet, $V_{IH} \text{ min} = V_{CCA} \times 0.7 \text{ V}$, $V_{IL} \text{ max} = V_{CCA} \times 0.3 \text{ V}$.

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		SN74AVC2T45				UNIT
		DCT (SM8)	DCU (VSSOP)	DDF (SOT-23)	YZP (DSBGA)	
		8 PINS	8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	194.4	199.3	203.2	105.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	124.7	76.2	121.5	1.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	106.8	80.6	99.8	10.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	49.8	7.1	21.4	3.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	105.8	80.1	99.5	10.8	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application note.

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)^{(1) (2)}

PARAMETER	TEST CONDITIONS	V_{CCA}	V_{CCB}	$T_A = 25^\circ\text{C}$			$-40^\circ\text{C to } +85^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	
$V_{OH}^{(3)}$	$I_{OH} = -100 \mu\text{A}$ $I_{OH} = -3 \text{ mA}$ $I_{OH} = -6 \text{ mA}$ $I_{OH} = -8 \text{ mA}$ $I_{OH} = -9 \text{ mA}$ $I_{OH} = -12 \text{ mA}$	$V_I = V_{IH}$	1.2 V to 3.6 V	1.2 V to 3.6 V			$V_{CCO} - 0.2 \text{ V}$		V
			1.2 V	1.2 V	0.95				
			1.4 V	1.4 V			1.05		
			1.65 V	1.65 V			1.2		
			2.3 V	2.3 V			1.75		
			3 V	3 V			2.3		
$V_{OL}^{(3)}$	$I_{OL} = 100 \mu\text{A}$ $I_{OL} = 3 \text{ mA}$ $I_{OL} = 6 \text{ mA}$ $I_{OL} = 8 \text{ mA}$ $I_{OL} = 9 \text{ mA}$ $I_{OL} = 12 \text{ mA}$	$V_I = V_{IL}$	1.2 V to 3.6 V	1.2 V to 3.6 V			0.2		V
			1.2 V	1.2 V	0.25				
			1.4 V	1.4 V			0.35		
			1.65 V	1.65 V			0.45		
			2.3 V	2.3 V			0.55		
			3 V	3 V			0.7		
I_I	DIR	$V_I = V_{CCA}$ or GND	1.2 V to 3.6 V	1.2 V to 3.6 V	± 0.025	± 0.25		± 1	μA
I_{off}	A port	V_I or $V_O = 0$ to 3.6 V	0 V	0 to 3.6 V	± 0.1	± 1		± 5	μA
	B port		0 to 3.6 V	0 V	± 0.1	± 1		± 5	
$I_{OZ}^{(3)}$	B port	$V_O = V_{CCO}$ or GND, $V_I = V_{CCI}$ or GND	0 V	3.6 V	± 0.5	± 2.5		± 5	μA
	A port		3.6 V	0 V	± 0.5	± 2.5		± 5	
$I_{CCA}^{(3)}$		$V_I = V_{CCI}$ or GND, $I_O = 0$	1.2 V to 3.6 V	1.2 V to 3.6 V				10	μA
			0 V	3.6 V				-2	
			3.6 V	0 V				10	
$I_{CCB}^{(3)}$		$V_I = V_{CCI}$ or GND, $I_O = 0$	1.2 V to 3.6 V	1.2 V to 3.6 V				10	μA
			0 V	3.6 V				10	
			3.6 V	0 V				-2	
$I_{CCA} + I_{CCB}$ (see 表 5-1)		$V_I = V_{CCI}$ or GND, $I_O = 0$	1.2 V to 3.6 V	1.2 V to 3.6 V				20	μA
C_i	Control inputs	$V_I = 3.3 \text{ V}$ or GND	3.3 V	3.3 V	2.5				pF
C_{io}	A or B port	$V_O = 3.3 \text{ V}$ or GND	3.3 V	3.3 V	6				pF

(1) V_{CCO} is the voltage associated with the output port supply V_{CCA} or V_{CCB} .

(2) V_{CCI} is the voltage associated with the input port supply V_{CCA} or V_{CCB} .

(3) V_{OH} : Output High Voltage; V_{OL} : Output Low Voltage; I_{OZ} : Hi-Z Output Current; I_{CCA} : Supply A Current; I_{CCB} : Supply B Current

5.6 Switching Characteristics: $V_{CCA} = 1.2\text{ V}$

over recommended operating free-air temperature range, $V_{CCA} = 1.2\text{ V}$ (see 图 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.2\text{ V}$	$V_{CCB} = 1.5\text{ V}$	$V_{CCB} = 1.8\text{ V}$	$V_{CCB} = 2.5\text{ V}$	$V_{CCB} = 3.3\text{ V}$	UNIT
			TYP	TYP	TYP	TYP	TYP	
$t_{PLH}^{(2)}$	A	B	3.1	2.6	2.4	2.2	2.2	ns
$t_{PHL}^{(2)}$			3.1	2.6	2.4	2.2	2.2	
$t_{PLH}^{(2)}$	B	A	3.4	3.1	3	2.9	2.9	ns
$t_{PHL}^{(2)}$			3.4	3.1	3	2.9	2.9	
$t_{PHZ}^{(2)}$	DIR	A	5.2	5.2	5.1	5	4.8	ns
$t_{PLZ}^{(2)}$			5.2	5.2	5.1	5	4.8	
$t_{PHZ}^{(2)}$	DIR	B	5	4	3.8	2.8	3.2	ns
$t_{PLZ}^{(2)}$			5	4	3.8	2.8	3.2	
$t_{PZH}^{(2)(1)}$	DIR	A	8.4	7.1	6.8	5.7	6.1	ns
$t_{PZL}^{(2)(1)}$			8.4	7.1	6.8	5.7	6.1	
$t_{PZH}^{(2)(1)}$	DIR	B	8.3	7.8	7.5	7.2	7	ns
$t_{PZL}^{(2)(1)}$			8.3	7.8	7.5	7.2	7	

- (1) The enable time is a calculated value, derived using the formula shown in the 节 8.2.2.1 section.
(2) t_{PLH} : Low-to-high Propagation Delay; t_{PHL} : High-to-Low Propagation Delay; t_{PHZ} : High-to-Hi-Z Propagation Delay; t_{PLZ} : Low-to-Hi-Z Propagation Delay; t_{PZH} : Hi-Z-to-High Propagation Delay; t_{PZL} : Hi-Z-to-Low Propagation Delay

5.7 Switching Characteristics: $V_{CCA} = 1.5\text{ V} \pm 0.1\text{ V}$

over recommended operating free-air temperature range, $V_{CCA} = 1.5\text{ V} \pm 0.1\text{ V}$ (see 图 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.2\text{ V}$	$V_{CCB} = 1.5\text{ V} \pm 0.1\text{ V}$		$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$		$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$t_{PLH}^{(2)}$	A	B	2.8	0.7	5.4	0.5	4.6	0.4	3.7	0.3	3.5	ns
$t_{PHL}^{(2)}$			2.8	0.7	5.4	0.5	4.6	0.4	3.7	0.3	3.5	
$t_{PLH}^{(2)}$	B	A	2.7	0.8	5.4	0.7	5.2	0.6	4.9	0.5	4.7	ns
$t_{PHL}^{(2)}$			2.7	0.8	5.4	0.7	5.2	0.6	4.9	0.5	4.7	
$t_{PHZ}^{(2)}$	DIR	A	3.9	1.3	8.5	1.3	7.8	1.1	7.7	1.4	7.6	ns
$t_{PLZ}^{(2)}$			3.9	1.3	8.5	1.3	7.8	1.1	7.7	1.4	7.6	
$t_{PHZ}^{(2)}$	DIR	B	4.7	1.1	7	1.4	6.9	1.2	6.9	1.7	7.1	ns
$t_{PLZ}^{(2)}$			4.7	1.1	7	1.4	6.9	1.2	6.9	1.7	7.1	
$t_{PZH}^{(2)(1)}$	DIR	A	7.4		12.4		12.1		11.8		11.8	ns
$t_{PZL}^{(2)(1)}$			7.4		12.4		12.1		11.8		11.8	
$t_{PZH}^{(2)(1)}$	DIR	B	6.7		13.9		12.4		11.4		11.1	ns
$t_{PZL}^{(2)(1)}$			6.7		13.9		12.4		11.4		11.1	

- (1) The enable time is a calculated value, derived using the formula shown in the 节 8.2.2.1 section.
(2) t_{PLH} : Low-to-high Propagation Delay; t_{PHL} : High-to-Low Propagation Delay; t_{PHZ} : High-to-Hi-Z Propagation Delay; t_{PLZ} : Low-to-Hi-Z Propagation Delay; t_{PZH} : Hi-Z-to-High Propagation Delay; t_{PZL} : Hi-Z-to-Low Propagation Delay

5.8 Switching Characteristics: $V_{CCA} = 1.8 \text{ V} \pm 0.15 \text{ V}$

over recommended operating free-air temperature range, $V_{CCA} = 1.8 \text{ V} \pm 0.15 \text{ V}$ (see 图 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.2 \text{ V}$		$V_{CCB} = 1.5 \text{ V} \pm 0.1 \text{ V}$		$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$		$V_{CCB} = 2.5 \text{ V} \pm 0.2 \text{ V}$		$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	
$t_{PLH}^{(2)}$	A	B	2.7	0.5	5.2	0.4	4.3	0.2	3.4	0.2	3.1	ns	
$t_{PHL}^{(2)}$			2.7	0.5	5.2	0.4	4.3	0.2	3.4	0.2	3.1		
$t_{PLH}^{(2)}$	B	A	2.4	0.7	4.7	0.5	4.4	0.5	4	0.4	3.8	ns	
$t_{PHL}^{(2)}$			2.4	0.7	4.7	0.5	4.4	0.5	4	0.4	3.8		
$t_{PHZ}^{(2)}$	DIR	A	3.7	1.3	8.1	0.7	6.9	1.4	5.3	1.1	5.2	ns	
$t_{PLZ}^{(2)}$			3.7	1.3	8.1	0.7	6.9	1.4	5.3	1.1	5.2		
$t_{PHZ}^{(2)}$	DIR	B	4.4	1.3	5.8	1.3	5.9	0.8	5.7	1.5	5.9	ns	
$t_{PLZ}^{(2)}$			4.4	1.3	5.8	1.3	5.9	0.8	5.7	1.5	5.9		
$t_{PZH}^{(2)(1)}$	DIR	A	6.8		10.5		10.3		9.7		9.7	ns	
$t_{PZL}^{(2)(1)}$			6.8		10.5		10.3		9.7		9.7		
$t_{PZH}^{(2)(1)}$	DIR	B	6.4		13.3		11.2		8.7		8.3	ns	
$t_{PZL}^{(2)(1)}$			6.4		13.3		11.2		8.7		8.3		

(1) The enable time is a calculated value, derived using the formula shown in the 节 8.2.2.2.1 section.

(2) t_{PLH} : Low-to-high Propagation Delay; t_{PHL} : High-to-Low Propagation Delay; t_{PHZ} : High-to-Hi-Z Propagation Delay; t_{PLZ} : Low-to-Hi-Z Propagation Delay; t_{PZH} : Hi-Z-to-High Propagation Delay; t_{PZL} : Hi-Z-to-Low Propagation Delay

5.9 Switching Characteristics: $V_{CCA} = 2.5 \text{ V} \pm 0.2 \text{ V}$

over recommended operating free-air temperature range, $V_{CCA} = 2.5 \text{ V} \pm 0.2 \text{ V}$ (see 图 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.2 \text{ V}$		$V_{CCB} = 1.5 \text{ V} \pm 0.1 \text{ V}$		$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$		$V_{CCB} = 2.5 \text{ V} \pm 0.2 \text{ V}$		$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	
$t_{PLH}^{(2)}$	A	B	2.6	0.4	4.9	0.2	4	0.2	3	0.2	2.6	ns	
$t_{PHL}^{(2)}$			2.6	0.4	4.9	0.2	4	0.2	3	0.2	2.6		
$t_{PLH}^{(2)}$	B	A	2.1	0.6	3.8	0.5	3.4	0.4	3	0.3	2.8	ns	
$t_{PHL}^{(2)}$			2.1	0.6	3.8	0.5	3.4	0.4	3	0.3	2.8		
$t_{PHZ}^{(2)}$	DIR	A	2.4	0.7	7.9	0.8	6.4	0.8	5	0.5	4.3	ns	
$t_{PLZ}^{(2)}$			2.4	0.7	7.9	0.8	6.4	0.8	5	0.5	4.3		
$t_{PHZ}^{(2)}$	DIR	B	3.8	1	4.3	0.6	4.3	0.5	4.2	1.1	4.1	ns	
$t_{PLZ}^{(2)}$			3.8	1	4.3	0.6	4.3	0.5	4.2	1.1	4.1		
$t_{PZH}^{(2)(1)}$	DIR	A	5.9		8.5		7.7		7.2		6.9	ns	
$t_{PZL}^{(2)(1)}$			5.9		8.5		7.7		7.2		6.9		
$t_{PZH}^{(2)(1)}$	DIR	B	5		12.8		10.4		8		6.9	ns	
$t_{PZL}^{(2)(1)}$			5		12.8		10.4		8		6.9		

(1) The enable time is a calculated value, derived using the formula shown in the 节 8.2.2.2.1 section.

(2) t_{PLH} : Low-to-high Propagation Delay; t_{PHL} : High-to-Low Propagation Delay; t_{PHZ} : High-to-Hi-Z Propagation Delay; t_{PLZ} : Low-to-Hi-Z Propagation Delay; t_{PZH} : Hi-Z-to-High Propagation Delay; t_{PZL} : Hi-Z-to-Low Propagation Delay

5.10 Switching Characteristics: $V_{CCA} = 3.3\text{ V} \pm 0.3\text{ V}$

over recommended operating free-air temperature range, $V_{CCA} = 3.3\text{ V} \pm 0.3\text{ V}$ (see 图 6-1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.2\text{ V}$		$V_{CCB} = 1.5\text{ V} \pm 0.1\text{ V}$		$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$		$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	
$t_{PLH}^{(2)}$	A	B	2.5	0.3	4.7	0.2	3.8	0.2	2.8	0.2	2.4	ns	
$t_{PHL}^{(2)}$			2.5	0.3	4.7	0.2	3.8	0.2	2.8	0.2	2.4		
$t_{PLH}^{(2)}$	B	A	2.1	0.6	3.6	0.4	3.1	0.3	2.6	0.3	2.4	ns	
$t_{PHL}^{(2)}$			2.1	0.6	3.6	0.4	3.1	0.3	2.6	0.3	2.4		
$t_{PHZ}^{(2)}$	DIR	A	2.9	1.1	8	1	6.5	1.3	4.7	1.2	4	ns	
$t_{PLZ}^{(2)}$			2.9	1.1	8	1	6.5	1.3	4.7	1.2	4		
$t_{PHZ}^{(2)}$	DIR	B	3.4	0.5	6.6	0.3	5.6	0.3	4.6	1.1	4.2	ns	
$t_{PLZ}^{(2)}$			3.4	0.5	6.6	0.3	5.6	0.3	4.6	1.1	4.2		
$t_{PZH}^{(2)(1)}$	DIR	A	5.5		10.2		8.7		7.2		6.6	ns	
$t_{PZL}^{(2)(1)}$			5.5		10.2		8.7		7.2		6.6		
$t_{PZH}^{(2)(1)}$	DIR	B	5.4		12.7		10.3		7.5		6.4	ns	
$t_{PZL}^{(2)(1)}$			5.4		12.7		10.3		7.5		6.4		

(1) The enable time is a calculated value, derived using the formula shown in the section

(2) t_{PLH} : Low-to-high Propagation Delay; t_{PHL} : High-to-Low Propagation Delay; t_{PHZ} : High-to-Hi-Z Propagation Delay; t_{PLZ} : Low-to-Hi-Z Propagation Delay; t_{PZH} : Hi-Z-to-High Propagation Delay; t_{PZL} : Hi-Z-to-Low Propagation Delay

5.11 Operating Characteristics

$T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	$V_{CCA} =$ $V_{CCB} = 1.2\text{ V}$	$V_{CCA} =$ $V_{CCB} = 1.5\text{ V}$	$V_{CCA} =$ $V_{CCB} = 1.8\text{ V}$	$V_{CCA} =$ $V_{CCB} = 2.5\text{ V}$	$V_{CCA} =$ $V_{CCB} = 3.3\text{ V}$	UNIT
			TYP	TYP	TYP	TYP	TYP	
$C_{pdA}^{(1)}$	A-port input, B-port output	$C_L = 0,$ $f = 10\text{ MHz},$ $t_r^{(2)} = t_f^{(2)} = 1\text{ ns}$	3	3	3	3	4	pF
	B-port input, A-port output		12	13	13	14	15	
$C_{pdB}^{(1)}$	A-port input, B-port output	$C_L = 0,$ $f = 10\text{ MHz},$ $t_r^{(2)} = t_f^{(2)} = 1\text{ ns}$	12	13	13	14	15	pF
	B-port input, A-port output		3	3	3	3	4	

(1) Power-dissipation capacitance per transceiver

(2) t_r : Rise time; t_f : Fall time

5.12 Typical Characteristics

表 5-1. Typical Total Static Power Consumption ($I_{CCA} + I_{CCB}$)

V_{CCB}	V_{CCA}						UNIT
	0 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
0 V	0	<0.5	<0.5	<0.5	<0.5	<0.5	μA
1.2 V	<0.5	<1	<1	<1	<1	1	
1.5 V	<0.5	<1	<1	<1	<1	1	
1.8 V	<0.5	<1	<1	<1	<1	<1	
2.5 V	<0.5	1	<1	<1	<1	<1	
3.3 V	<0.5	1	<1	<1	<1	<1	

5.12.1 Typical Propagation Delay (A to B) vs Load Capacitance, $T_A = 25^\circ\text{C}$, $V_{CCA} = 1.2\text{ V}$

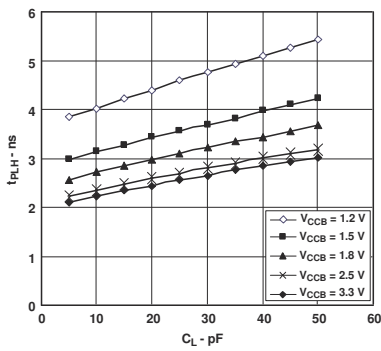


图 5-1. Typical A-to-B Propagation Delay, Low to High

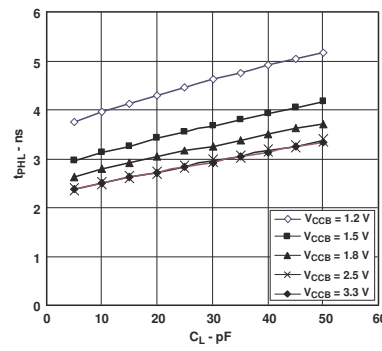


图 5-2. Typical A-to-B Propagation Delay, High to Low

5.12.2 Typical Propagation Delay (A to B) vs Load Capacitance, $T_A = 25^\circ\text{C}$, $V_{CCA} = 1.5\text{ V}$

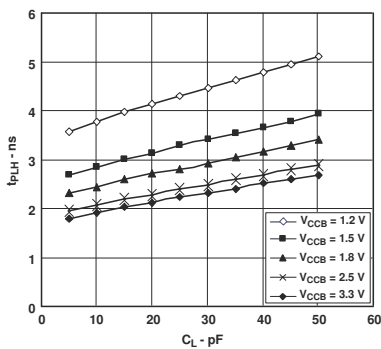


图 5-3. Typical A-to-B Propagation Delay, Low to High

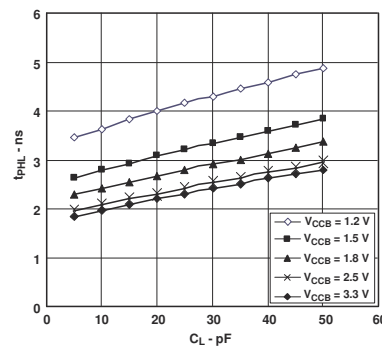


图 5-4. Typical A-to-B Propagation Delay, High to Low

5.12.3 Typical Propagation Delay (A-to-B) vs Load Capacitance, $T_A = 25^\circ\text{C}$, $V_{CCA} = 1.8\text{ V}$

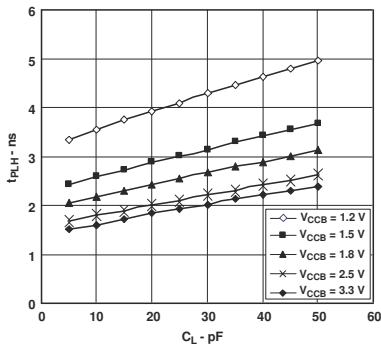


图 5-5. Typical A-to-B Propagation Delay, Low to High

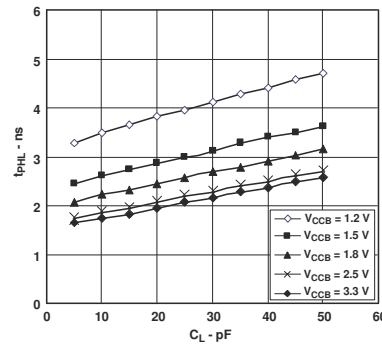


图 5-6. Typical A-to-B Propagation Delay, High to Low

5.12.4 Typical Propagation Delay (A to B) vs Load Capacitance, $T_A = 25^\circ\text{C}$, $V_{CCA} = 2.5\text{ V}$

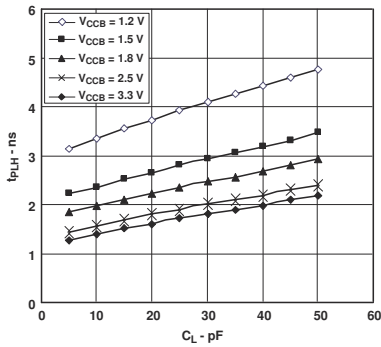


图 5-7. Typical A-to-B Propagation Delay, Low to High

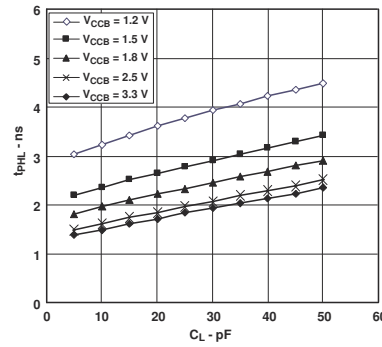


图 5-8. Typical A-to-B Propagation Delay, High to Low

5.12.5 Typical Propagation Delay (A to B) vs Load Capacitance, $T_A = 25^\circ\text{C}$, $V_{CCA} = 3.3\text{ V}$

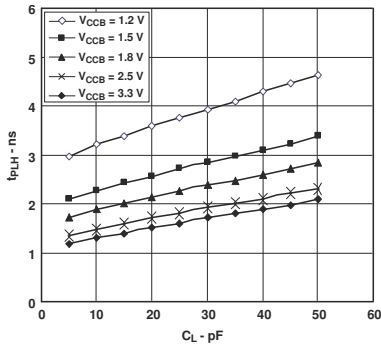


图 5-9. Typical A-to-B Propagation Delay, Low to High

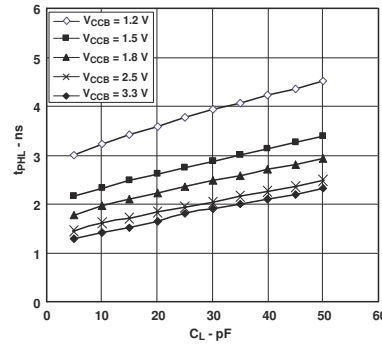
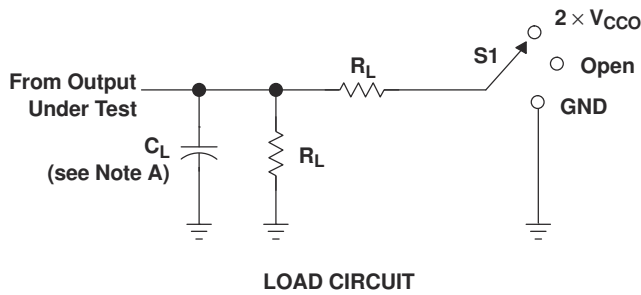


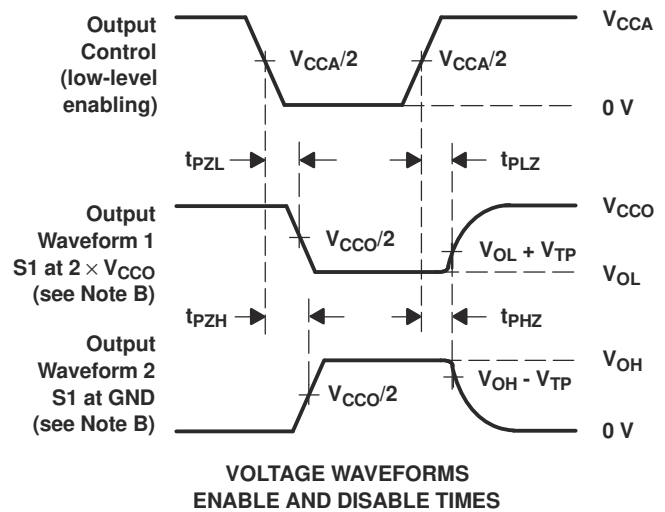
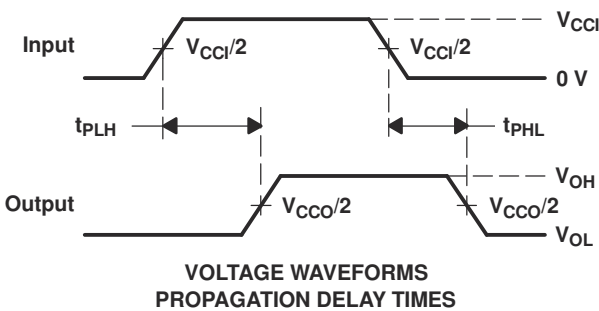
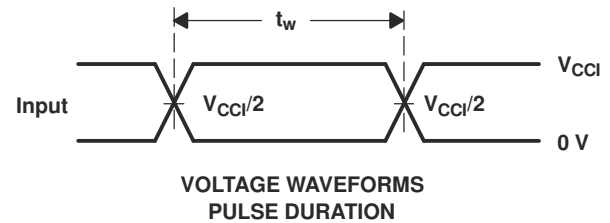
图 5-10. Typical A-to-B Propagation Delay, High to Low

6 Parameter Measurement Information



TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CCO}$
t_{PHZ}/t_{PZH}	GND

V_{CCO}	C_L	R_L	V_{TP}
1.2 V	15 pF	2 k Ω	0.1 V
1.5 V \pm 0.1 V	15 pF	2 k Ω	0.1 V
1.8 V \pm 0.15 V	15 pF	2 k Ω	0.15 V
2.5 V \pm 0.2 V	15 pF	2 k Ω	0.15 V
3.3 V \pm 0.3 V	15 pF	2 k Ω	0.3 V



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $dv/dt \geq 1$ V/ns.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .
 - V_{CC1} is the V_{CC} associated with the input port.
 - V_{CCO} is the V_{CC} associated with the output port.

图 6-1. Load Circuit and Voltage Waveforms

7 Detailed Description

7.1 Overview

This dual-bit noninverting bus transceiver uses two separate configurable power-supply rails. The A port is designed to track V_{CCA} and accepts any supply voltage from 1.2 V to 3.6 V. The B port is designed to track V_{CCB} and accepts any supply voltage from 1.2 V to 3.6 V. This allows for universal low-voltage bidirectional translation and level-shifting between any of the 1.2 V, 1.5 V, 1.8 V, 2.5 V, and 3.3 V voltage nodes.

The device is designed for asynchronous communication between two data buses. The logic levels of the direction-control (DIR) input activate either the B-port outputs or the A-port outputs. The device transmits data from the A bus to the B bus when the B-port outputs are activated and from the B bus to the A bus when the A-port outputs are activated. The input circuitry on both A and B ports always is active and must have a logic HIGH or LOW level applied to prevent excess internal leakage of the CMOS.

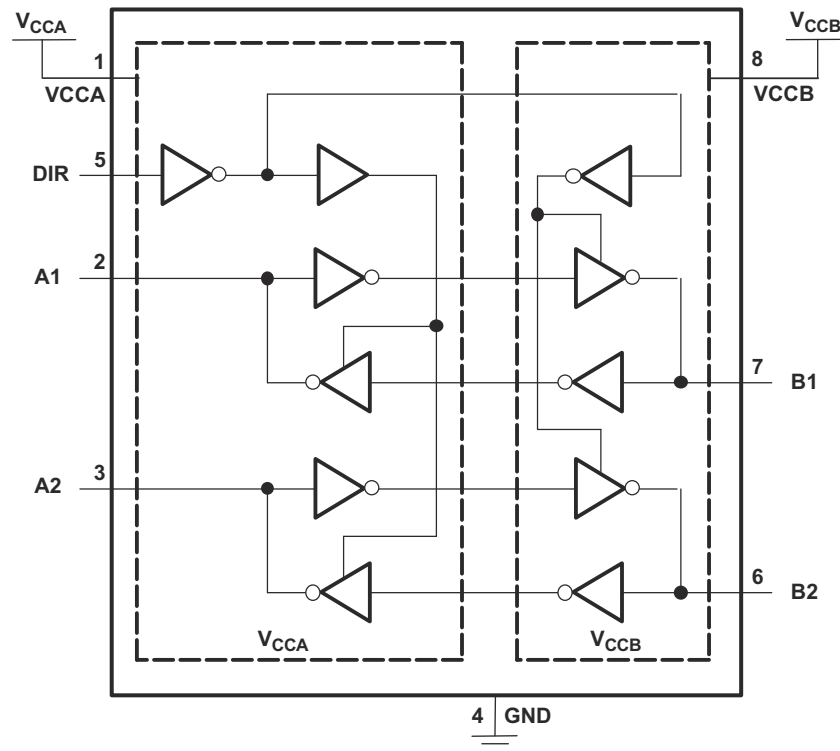
The device is designed so that the DIR input is powered by supply voltage from V_{CCA} .

This device is fully specified for partial-power-down applications using off output current (I_{off}). The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when powered down.

The V_{CC} isolation feature makes sure that if either VCC input is at GND, both ports are put in a high-impedance state. This action prevents a false high or low logic being presented at the output.

NanoFree package technology is a major breakthrough in IC packaging concepts, using the die as the package.

7.2 Functional Block Diagram



Pin numbers are for the DCT and DCU packages only.

7.3 Feature Description

7.3.1 VCC Isolation

The V_{CC} isolation feature make sure that if either V_{CCA} or V_{CCB} are at GND, both ports are in a high-impedance state (I_{OZ} shown in [Electrical Characteristics](#)). This action prevents false logic levels from being presented to either bus.

7.3.2 2-Rail Design

Fully configurable 2-rail design allows each port to operate over the full 1.2 V to 3.6 V power-supply range.

7.3.3 IO Ports are 4.6-V Tolerant

The IO ports are up to 4.6 V tolerant.

7.3.4 Partial-Power-Down Mode

This device is fully specified for partial-power-down applications using off output current (I_{off}). The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when the device is powered down.

7.4 Device Functional Modes

表 7-1 shows the functional modes of the SN74AVC2T45-Q1.

**表 7-1. Function Table
(Each Transceiver)**

INPUT DIR	OPERATION
L	B data to A bus
H	A data to B bus

8 Application and Implementation

备注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The SN74AVC2T45 is used to shift IO voltage levels from one voltage domain to another. Bus A and bus B have independent power supplies, and a direction pin is used to control the direction of data flow. Unused data ports must not be floating; tie the unused port input and output to ground directly.

8.2 Typical Applications

8.2.1 Unidirectional Logic Level-Shifting Application

图 8-1 is an example circuit of the SN74AVC2T45 used in a unidirectional logic level-shifting application.

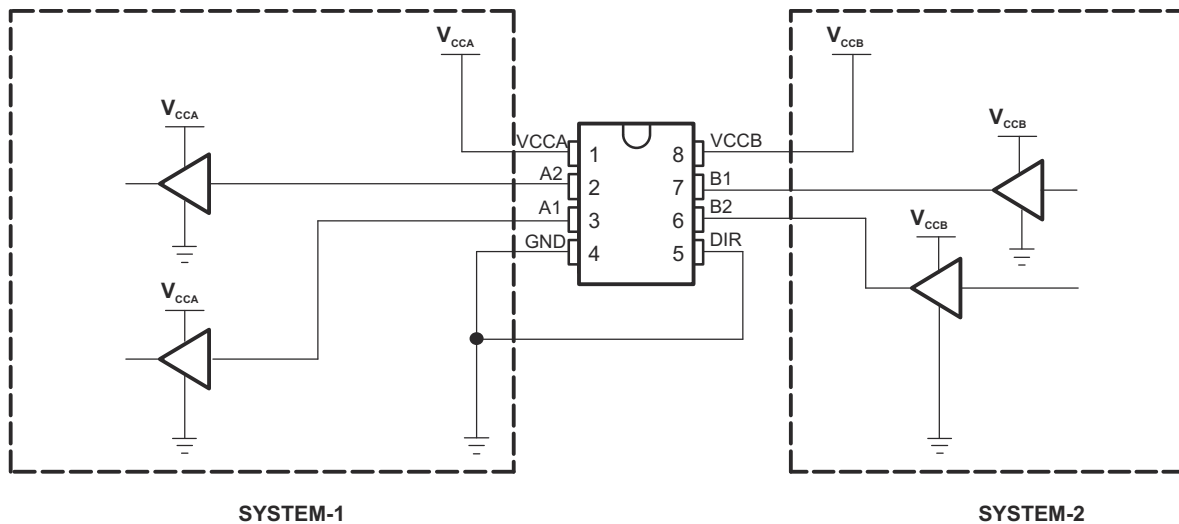


图 8-1. Unidirectional Logic Level-Shifting Application

8.2.1.1 Design Requirements

表 8-1 lists the pins and pin descriptions of the SN74AVC2T45 connections with SYSTEM-1 and SYSTEM-2.

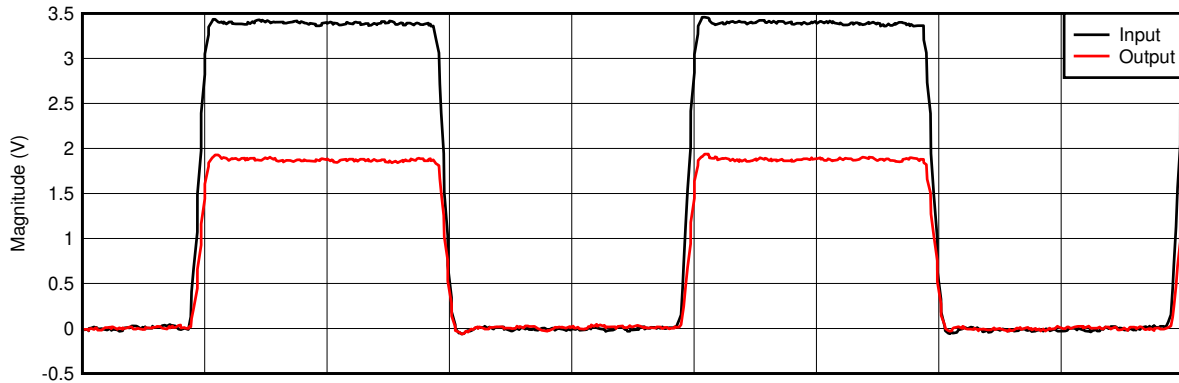
表 8-1. SN74AVC2T45 Pin Connections With SYSTEM-1 and SYSTEM-2

PIN	NAME	DESCRIPTION
1	VCCA	SYSTEM-1 supply voltage (1.2 V to 3.6 V)
2	A1	Output level depends on V_{CCA} .
3	A2	Output level depends on V_{CCA} .
4	GND	Device GND
5	DIR	The GND (low-level) determines B-port to A-port direction.
6	B2	Input threshold value depends on V_{CCB} .
7	B1	Input threshold value depends on V_{CCB} .
8	VCCB	SYSTEM-2 supply voltage (1.2 V to 3.6 V)

8.2.1.2 Detailed Design Procedure

This device uses drivers which are enabled depending on the state of the DIR pin. The designer must know the intended flow of data and take care not to violate any of the high or low logic levels. Unused data inputs must not be floating, as this can cause excessive internal leakage on the input CMOS structure. Make sure to tie any unused input and output ports directly to ground.

8.2.1.3 Application Curve



D001

图 8-2. 3.3 V to 1.8 V Level-Shifting With 1-MHz Square Wave

8.2.2 Bidirectional Logic Level-Shifting Application

图 8-3 shows the SN74AVC2T45 used in a bidirectional logic level-shifting application.

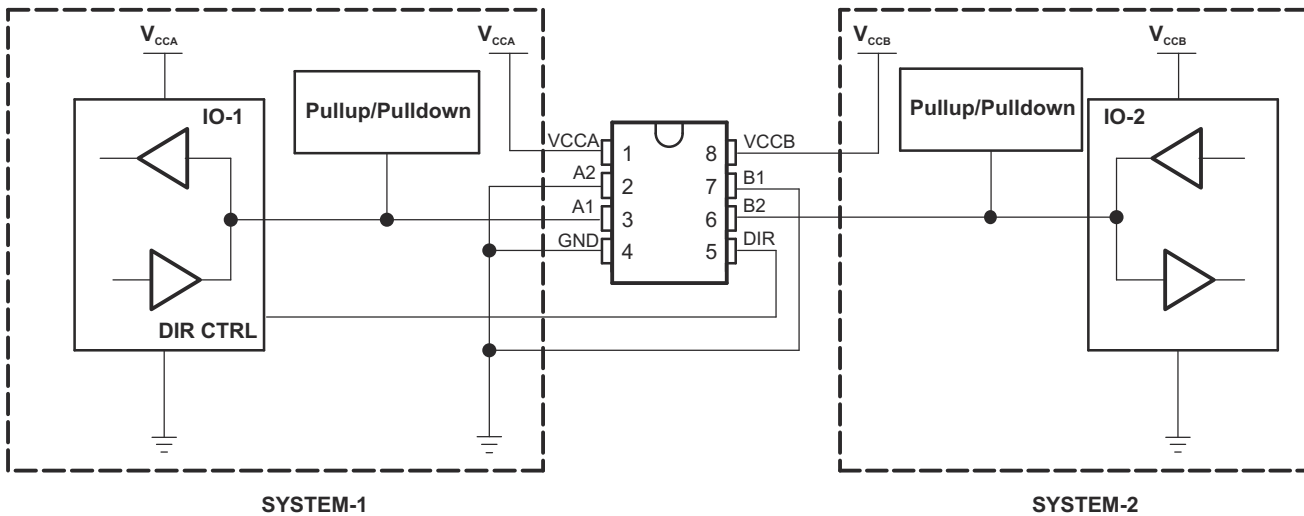


图 8-3. Bidirectional Logic Level-Shifting Application

8.2.2.1 Design Requirements

The SN74AVC2T45 does not have an output-enable (OE) pin, the system designer must take precautions to avoid bus contention between SYSTEM-1 and SYSTEM-2 when changing directions.

8.2.2.2 Detailed Design Procedure

表 8-2 shows a sequence that illustrates data transmission from SYSTEM-1 to SYSTEM-2 and then from SYSTEM-2 to SYSTEM-1.

表 8-2. Data Transmission Sequence

STATE	DIR CTRL	IO-1	IO-2	DESCRIPTION
1	H	Output	Input	SYSTEM-1 data to SYSTEM-2
2	H	Hi-Z	Hi-Z	SYSTEM-2 is getting ready to send data to SYSTEM-1. IO-1 and IO-2 are disabled. The bus-line state depends on pullup or pulldown. ⁽¹⁾
3	L	Hi-Z	Hi-Z	DIR bit is flipped. IO-1 and IO-2 still are disabled. The bus-line state depends on pullup or pulldown. ⁽¹⁾
4	L	Input	Output	SYSTEM-2 data to SYSTEM-1

(1) SYSTEM-1 and SYSTEM-2 must use the same conditions, that is, both pullup or both pulldown.

8.2.2.2.1 Enable Times

Calculate the enable times for the SN74AVC2T45 using the following formulas:

- $t_{PZH} \text{ (DIR to A)} = t_{PLZ} \text{ (DIR to B)} + t_{PLH} \text{ (B to A)}$
- $t_{PZL} \text{ (DIR to A)} = t_{PHZ} \text{ (DIR to B)} + t_{PHL} \text{ (B to A)}$
- $t_{PZH} \text{ (DIR to B)} = t_{PLZ} \text{ (DIR to A)} + t_{PLH} \text{ (A to B)}$
- $t_{PZL} \text{ (DIR to B)} = t_{PHZ} \text{ (DIR to A)} + t_{PHL} \text{ (A to B)}$

In a bidirectional application, these enable times provide the maximum delay from the time the DIR bit is switched until an output is expected. For example, if the SN74AVC2T45 initially is transmitting from A to B, then the DIR bit is switched; the B port of the device must be disabled before presenting the device with an input. After the B port has been disabled, an input signal applied to the port appears on the corresponding A port after the specified propagation delay.

8.3 Power Supply Recommendations

A proper power-up sequence must always be followed to avoid excessive current on the supply pin, bus contention, oscillations, or other anomalies. To guard against such power-up problems, take the following precautions:

1. Connect ground before any supply voltage is applied.
2. Power up V_{CCA} .
3. V_{CCB} can be ramped up along with or after V_{CCA} .

8.4 Layout

8.4.1 Layout Guidelines

To verify the reliability of the device, follow common printed-circuit board layout guidelines.

- Bypass capacitors can be used on power supplies. Place the capacitors as close as possible to the VCCA, VCCB pin and GND pin.
- Short trace lengths can be used to avoid excessive loading.

8.4.2 Layout Example

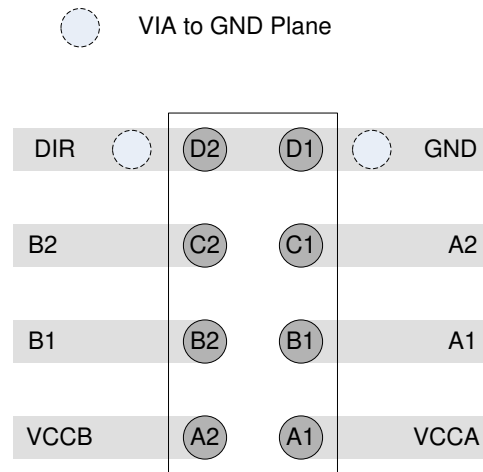


图 8-4. Layout Example for YZP Package

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation see the following:

[Implications of Slow or Floating CMOS Inputs](#), SCBA004

9.2 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](https://www.ti.com) 上的器件产品文件夹。点击 [通知](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.3 支持资源

[TI E2E™ 中文支持论坛](#) 是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.6 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

10 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision L (May 2017) to Revision M (September 2024)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式.....	1
• 添加了 DDF 封装.....	1
• Deleted the <i>Community Resources</i> section	19
• Added the <i>Support Resources, Receiving Notification of Documentation Updates, Electrostatic Discharge Statement, and Glossary</i> sections.....	19

Changes from Revision K (April 2015) to Revision L (May 2017)	Page
• 更改了数据表标题.....	1
• Changed YZP package pinout diagram to bottom view.....	3
• Added Type column to <i>Pin Functions</i> table	3
• Added Junction temperature, T _J	4

Changes from Revision J (June 2007) to Revision K (April 2015)

Page

- 添加了引脚配置和功能部分、ESD 等级表、特性说明部分、器件功能模式、应用和实施部分、电源相关建议部分、布局部分、器件和文档支持部分以及机械、封装和可订购信息部分.....1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AVC2T45DCTR	ACTIVE	SSOP	DCT	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DT2 Z	Samples
SN74AVC2T45DCTRE4	ACTIVE	SSOP	DCT	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DT2 Z	Samples
SN74AVC2T45DCTT	ACTIVE	SSOP	DCT	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DT2 Z	Samples
SN74AVC2T45DCUR	ACTIVE	VSSOP	DCU	8	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 85	(DT2R, T2) DZ	Samples
SN74AVC2T45DCURG4	ACTIVE	VSSOP	DCU	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DT2R	Samples
SN74AVC2T45DCUT	ACTIVE	VSSOP	DCU	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DT2R	Samples
SN74AVC2T45DCUTG4	ACTIVE	VSSOP	DCU	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	DT2R	Samples
SN74AVC2T45DDFR	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	A2T45	Samples
SN74AVC2T45YZPR	ACTIVE	DSBGA	YZP	8	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TDN	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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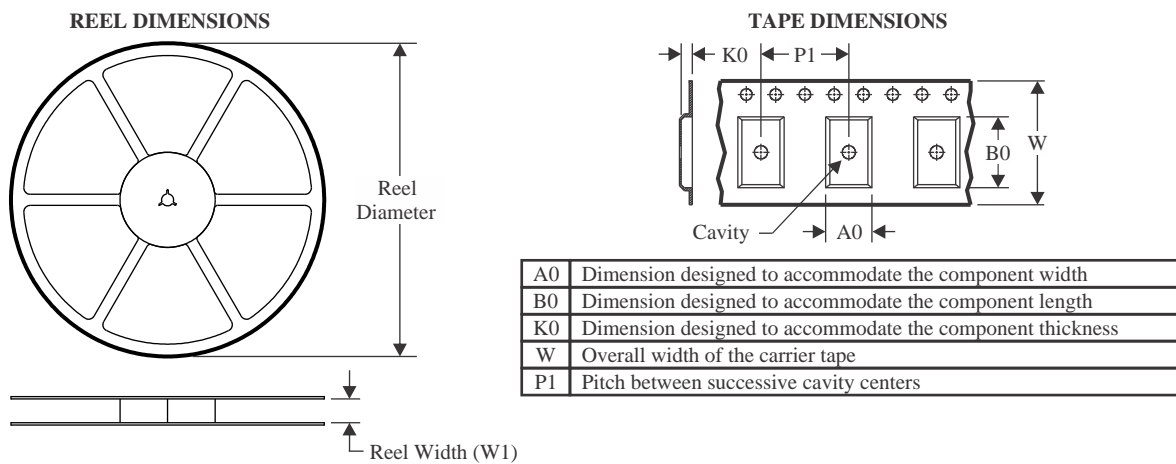
OTHER QUALIFIED VERSIONS OF SN74AVC2T45 :

- Automotive : [SN74AVC2T45-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



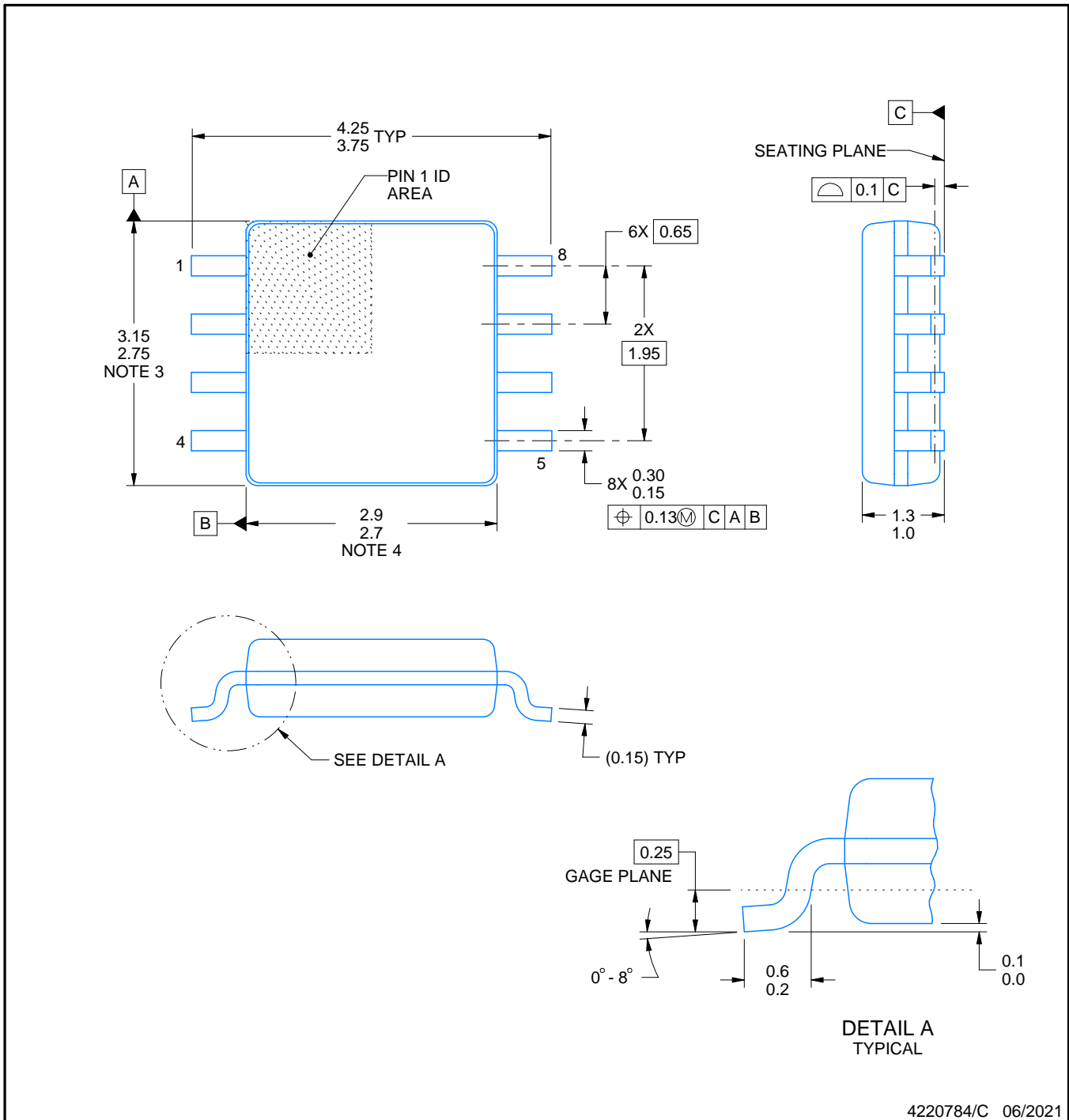
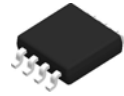
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AVC2T45DCTR	SSOP	DCT	8	3000	180.0	13.0	3.35	4.5	1.55	4.0	12.0	Q3
SN74AVC2T45DCTT	SSOP	DCT	8	250	180.0	13.0	3.35	4.5	1.55	4.0	12.0	Q3
SN74AVC2T45DCUR	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74AVC2T45DCUR	VSSOP	DCU	8	3000	180.0	9.0	2.25	3.4	1.0	4.0	8.0	Q3
SN74AVC2T45DCURG4	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74AVC2T45DCUTG4	VSSOP	DCU	8	250	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74AVC2T45DDFR	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.1	1.25	4.0	8.0	Q3
SN74AVC2T45YZPR	DSBGA	YZP	8	3000	178.0	9.2	1.02	2.02	0.63	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AVC2T45DCTR	SSOP	DCT	8	3000	182.0	182.0	20.0
SN74AVC2T45DCTT	SSOP	DCT	8	250	182.0	182.0	20.0
SN74AVC2T45DCUR	VSSOP	DCU	8	3000	202.0	201.0	28.0
SN74AVC2T45DCUR	VSSOP	DCU	8	3000	182.0	182.0	20.0
SN74AVC2T45DCURG4	VSSOP	DCU	8	3000	202.0	201.0	28.0
SN74AVC2T45DCUTG4	VSSOP	DCU	8	250	202.0	201.0	28.0
SN74AVC2T45DDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
SN74AVC2T45YZPR	DSBGA	YZP	8	3000	220.0	220.0	35.0



4220784/C 06/2021

NOTES:

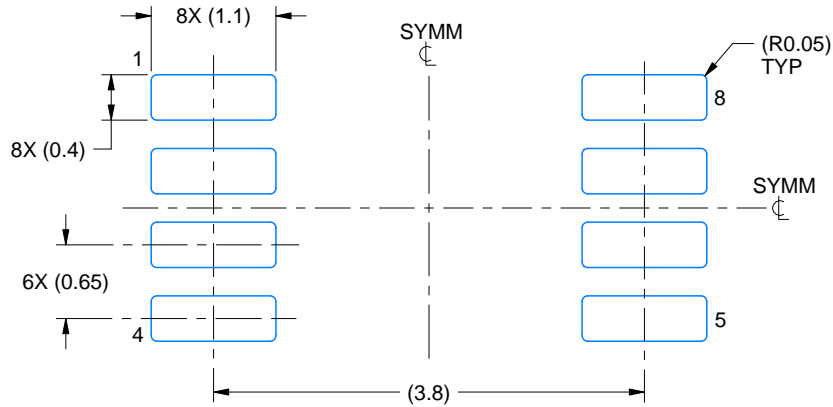
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.

EXAMPLE BOARD LAYOUT

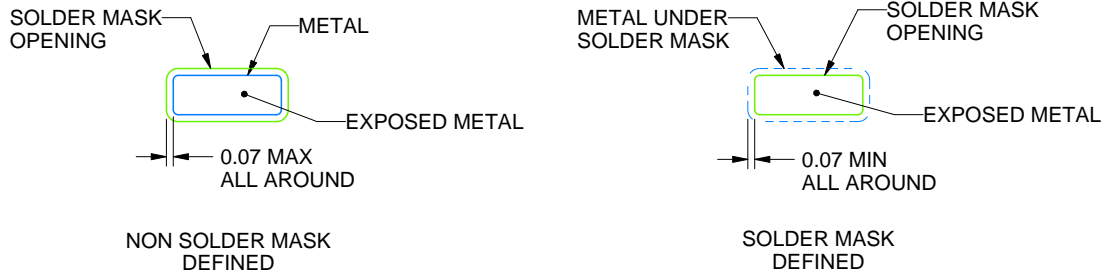
DCT0008A

SSOP - 1.3 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4220784/C 06/2021

NOTES: (continued)

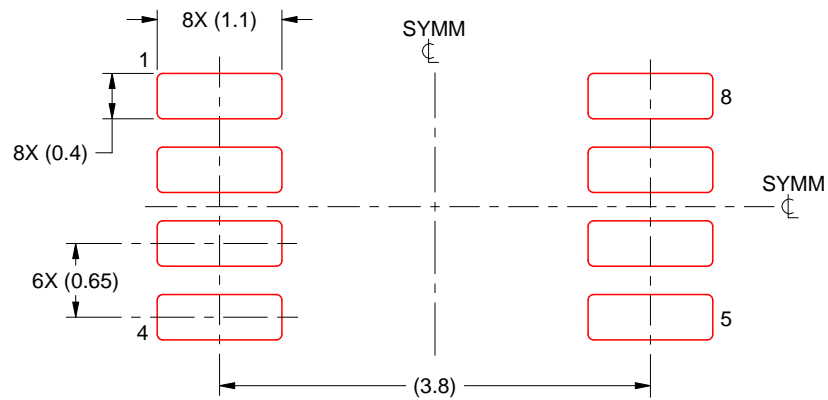
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DCT0008A

SSOP - 1.3 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4220784/C 06/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

DDF0008A



PACKAGE OUTLINE

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



4222047/E 07/2024

NOTES:

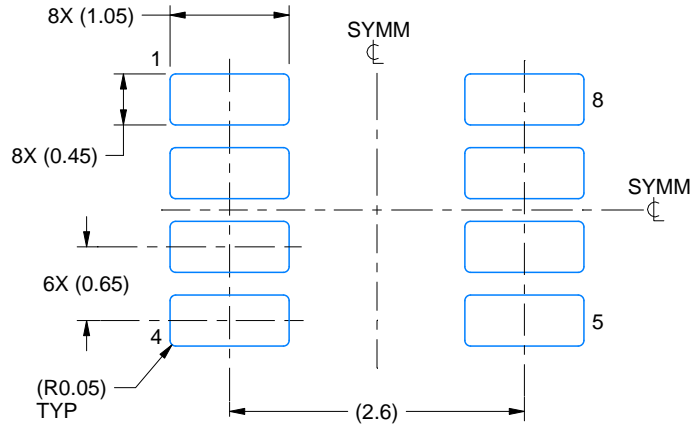
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

EXAMPLE BOARD LAYOUT

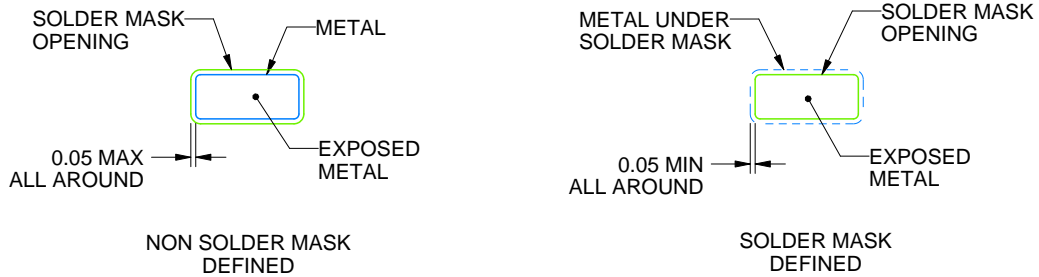
DDF0008A

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4222047/E 07/2024

NOTES: (continued)

- 4. Publication IPC-7351 may have alternate designs.
- 5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DDF0008A

SOT-23-THIN - 1.1 mm max height

PLASTIC SMALL OUTLINE



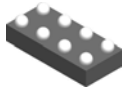
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/E 07/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

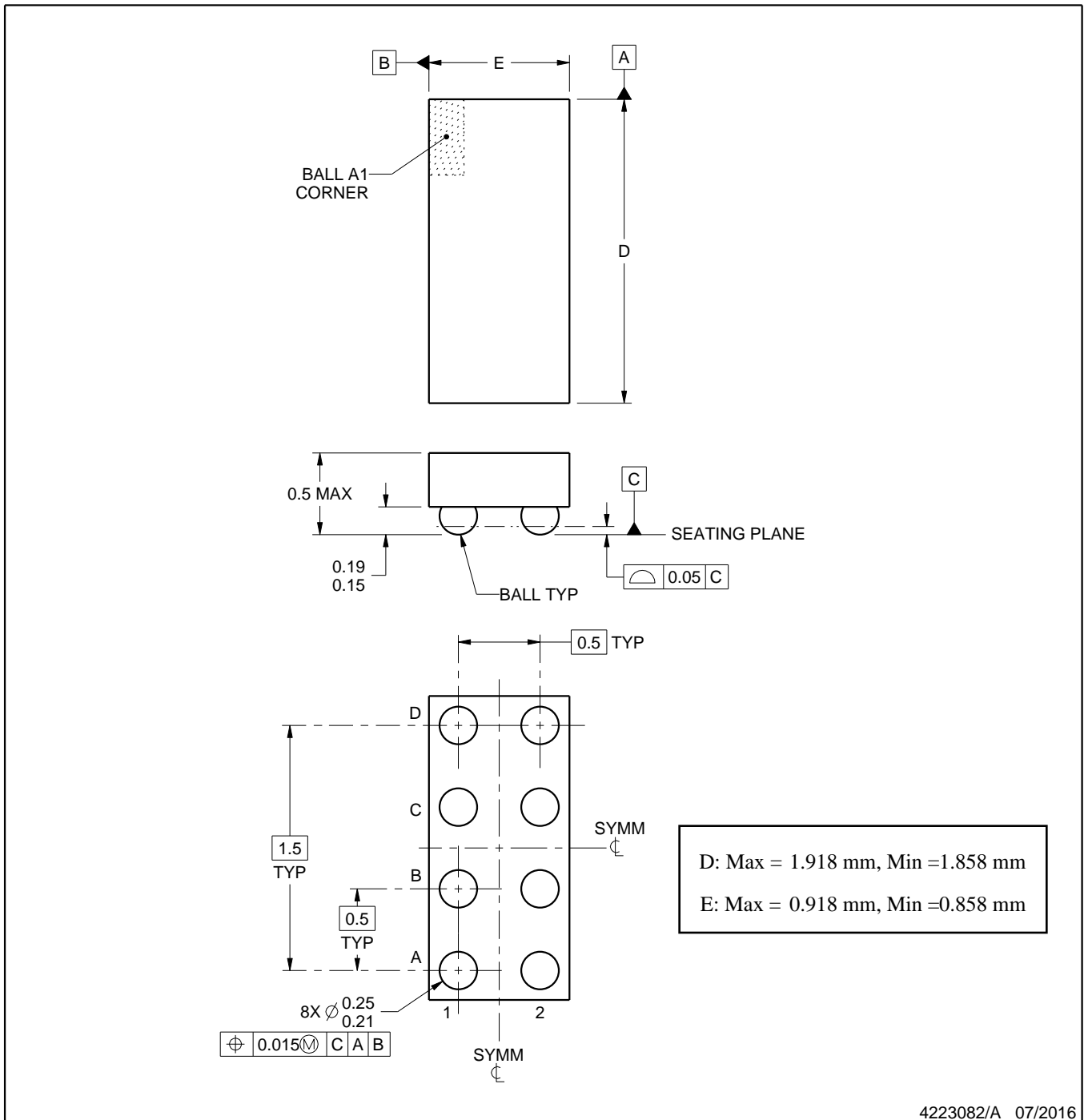
YZP0008



PACKAGE OUTLINE

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



4223082/A 07/2016

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

YZP0008

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:40X



SOLDER MASK DETAILS
NOT TO SCALE

4223082/A 07/2016

NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YZP0008

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:40X

4223082/A 07/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

DCU0008A



PACKAGE OUTLINE

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE



4225266/A 09/2014

NOTES:

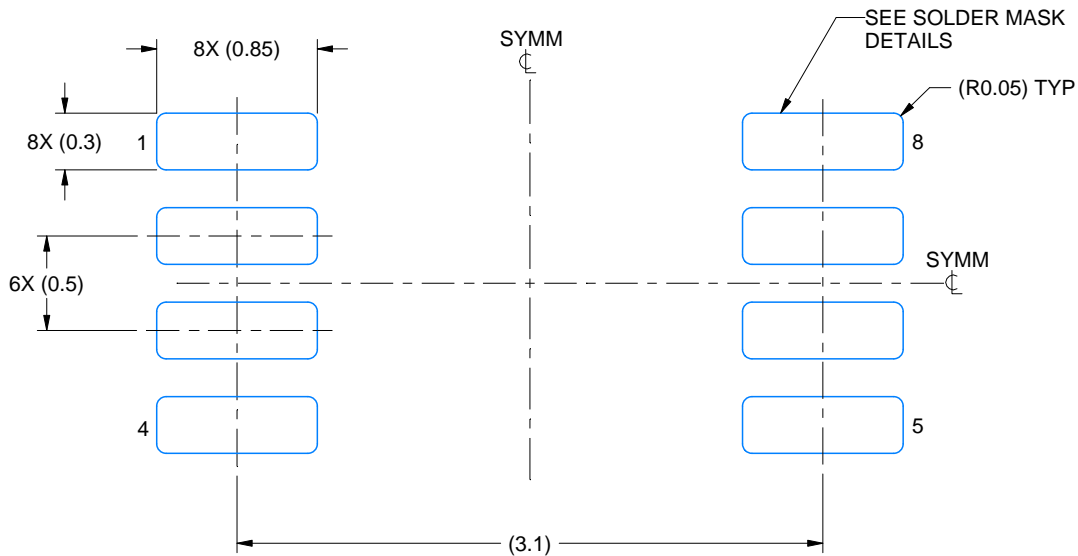
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-187 variation CA.

EXAMPLE BOARD LAYOUT

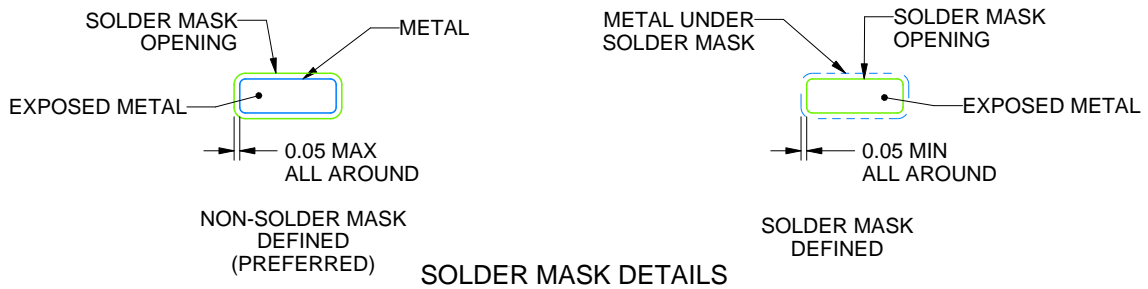
DCU0008A

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X



4225266/A 09/2014

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DCU0008A

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 25X

4225266/A 09/2014

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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