

## SNx4LVC157A 四通道 2 线至 1 线数据选择器/多路复用器

### 1 特性

- 工作电压范围为 1.65V 至 3.6V
- 额定温度范围为 -40°C 至 85°C、  
-40°C 至 125°C 以及 -55°C 至 125°C
- 输入电压高达 5.5V
- 电压为 3.3V 时， $t_{pd}$  最大值为 5.2ns
- $V_{OLP}$  (输出接地反弹) 典型值  
<0.8V ( $V_{CC} = 3.3V$ 、 $T_A = 25^\circ C$ )
- $V_{OHV}$  (输出  $V_{OH}$  下冲) 典型值  
>2V ( $V_{CC} = 3.3V$ 、 $T_A = 25^\circ C$ )
- 闩锁性能超过 250mA，  
符合 JESD 17 规范
- ESD 保护性能超过 JESD 22 规范要求
  - 2000V 人体放电模型 (A114-A)
  - 1000V 充电器件模型 (C101)

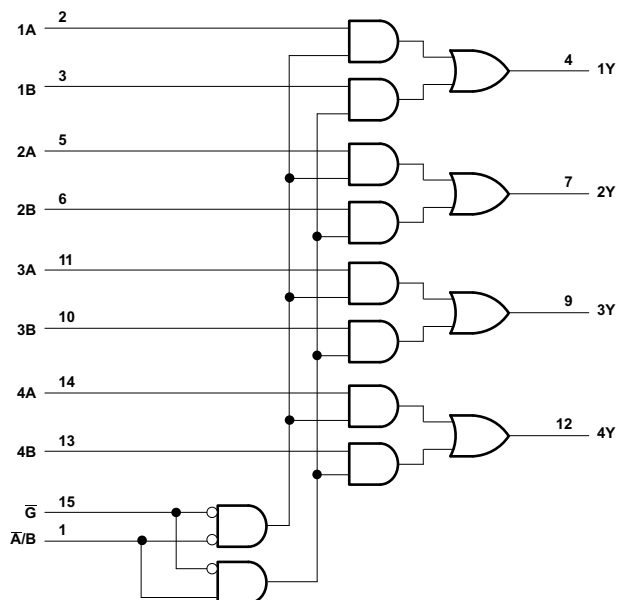
### 2 说明

这些四通道 2 线至 1 线数据选择器/多路复用器可在 1.65V 至 3.6V  $V_{CC}$  下运行。

#### 器件信息

器件型号	封装 <sup>(1)</sup>	封装尺寸 <sup>(2)</sup>	本体尺寸 <sup>(3)</sup>
SNx4LVC157A	BQB (WQFN, 16)	3.5mm × 2.5mm	3.5mm × 2.5mm
	D (SOIC, 16)	9.90mm × 6mm	9.90mm × 3.90mm
	DB (SSOP, 16)	6.20mm × 7.8mm	6.20mm × 5.30mm
	NS (SOP, 16)	5mm × 6.4mm	5mm × 4.4mm
	PW (TSSOP, 16)	5.00mm × 6.4mm	5.00mm × 4.40mm
	RGY (VQFN, 16)	4mm × 3.5mm	4mm × 3.5mm

- (1) 如需了解更多信息，请参阅机械、封装和可订购信息。
- (2) 封装尺寸 (长 × 宽) 为标称值，并包括引脚 (如适用)。
- (3) 本体尺寸 (长 × 宽) 为标称值，不包括引脚。



逻辑图 (正逻辑)



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### 3 Pin Configuration and Functions

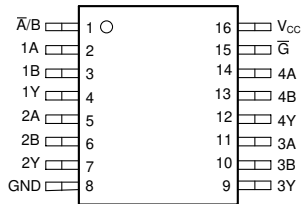


图 3-1. SN54LVC157A J or W Package, 16-Pin CDIP or CFP; SN74LVC157A D, DB, NS, or, PW Package, 16-Pin SOIC, SSOP, SOP, or TSSOP (Top View)

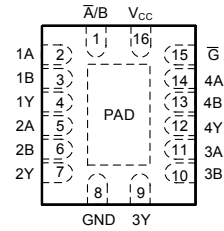


图 3-2. SN74LVC157A BQB or RGY Package, 16-Pin WQFN or VQFN (Top View)

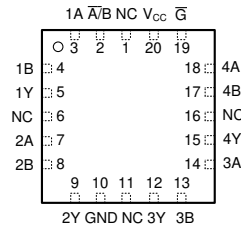


图 3-3. SN54LVC157A FK Package, 16-Pin LCCC (Top View)

表 3-1. Pin Functions

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
A/B	1	I	Address select
1A	2	I	Channel 1, data input A
1B	3	I	Channel 1, data input B
1Y	4	O	Channel 1, data output
2A	5	I	Channel 2, data input A
2B	6	I	Channel 2, data input B
2Y	7	O	Channel 2, data output
GND	8	G	Ground
3Y	9	O	Channel 3, data output
3B	10	I	Channel 3, data input B
3A	11	I	Channel 3, data input A
4Y	12	O	Channel 4, data output
4B	13	I	Channel 4, data input B
4A	14	I	Channel 4, data input A
G-bar	15	I	Output strobe, active low
V <sub>CC</sub>	16	P	Positive supply
Thermal pad <sup>(2)</sup>		—	The thermal pad can be connected to GND or left floating. Do not connect to any other signal or supply.

(1) Signal Types: I = Input, O = Output, I/O = Input or Output, P = Power, G = Ground.

(2) WBQB package only.

## 4 Specifications

### 4.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT	
V <sub>CC</sub>	Supply voltage range	- 0.5	6.5	V	
V <sub>I</sub>	Input voltage range <sup>(1)</sup>	- 0.5	6.5	V	
V <sub>O</sub>	Output voltage range <sup>(1) (2)</sup>	- 0.5	V <sub>CC</sub> + 0.5	V	
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0	- 50	mA	
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0	- 50	mA	
I <sub>O</sub>	Continuous output current		±50	mA	
	Continuous current through V <sub>CC</sub> or GND		±100	mA	
T <sub>stg</sub>	Storage temperature range	- 65	150	°C	
P <sub>tot</sub>	Power dissipation <sup>(3) (4)</sup>	T <sub>A</sub> = - 40°C to 125°C		500	mW

(1) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.

(2) The value of V<sub>CC</sub> is provided in the recommended operating conditions table.

(3) For the D package, above 70°C the value of P<sub>tot</sub> derates linearly with 8 mW/K.

(4) For the DB, NS, and PW packages, above 60°C the value of P<sub>tot</sub> derates linearly with 5.5 mW/K.

### 4.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000
		Charged device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1000

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

### 4.3 Recommended Operating Conditions, SN54LVC157A

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		SN54LVC157A		UNIT
		- 55 TO 125°C		
		MIN	MAX	
V <sub>CC</sub>	Supply voltage	Operating	2	3.6
		Data retention only	1.5	
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 2.7V to 3.6V		V
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 2.7V to 3.6V		0.8
V <sub>I</sub>	Input voltage	0	5.5	V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 2.7V	- 12	mA
		V <sub>CC</sub> = 3V	- 24	
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 2.7V	12	mA
		V <sub>CC</sub> = 3V	24	

(1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

#### 4.4 Recommended Operating Conditions, SN74LVC157A

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

			SN74LVC157A						UNIT
			T <sub>A</sub> = 25°C		- 40 TO 85°C		- 40 TO 125°C		
			MIN	MAX	MIN	MAX	MIN	MAX	
V <sub>CC</sub>	Supply voltage	Operating	1.65	3.6	1.65	3.6	1.65	3.6	V
		Data retention only	1.5		1.5		1.5		
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 1.65V to 1.95V	0.65 × V <sub>CC</sub>		0.65 × V <sub>CC</sub>		0.65 × V <sub>CC</sub>		V
		V <sub>CC</sub> = 2.3V to 2.7V	1.7		1.7		1.7		
		V <sub>CC</sub> = 2.7V to 3.6V	2		2		2		
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 1.65V to 1.95V	0.35 × V <sub>CC</sub>		0.35 × V <sub>CC</sub>		0.35 × V <sub>CC</sub>		V
		V <sub>CC</sub> = 2.3V to 2.7V	0.7		0.7		0.7		
		V <sub>CC</sub> = 2.7V to 3.6V	0.8		0.8		0.8		
V <sub>I</sub>	Input voltage	0	5.5	0	5.5	0	5.5	V	
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	0	V <sub>CC</sub>	0	V <sub>CC</sub>	V	
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 1.65V	- 4		- 4		- 4		mA
		V <sub>CC</sub> = 2.3V	- 8		- 8		- 8		
		V <sub>CC</sub> = 2.7V	- 12		- 12		- 12		
		V <sub>CC</sub> = 3V	- 24		- 24		- 24		
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 1.65V	4		4		4		mA
		V <sub>CC</sub> = 2.3V	8		8		8		
		V <sub>CC</sub> = 2.7V	12		12		12		
		V <sub>CC</sub> = 3V	24		24		24		
$\frac{\Delta t}{\Delta v}$	Input transition rise and fall rate		10		10		10	ns/V	

(1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

#### 4.5 Thermal Information

THERMAL METRIC <sup>(1)</sup>		SN74LVC157A						UNIT
		BQB (WQFN)	D (SOIC)	DB (SSOP)	NS (SOP)	PW (TSSOP)	RGY (VQFN)	
		16						
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	98.8	73	82	64	108	39	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.

#### 4.6 Electrical Characteristics, SN54LVC157A

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	SN54LVC157A		UNIT
			- 55 TO 125°C		
			MIN	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = - 100μA	2.7V to 3.6V	V <sub>CC</sub> - 0.2		V
	I <sub>OH</sub> = - 12mA	2.7V	2.2		
		3V	2.4		
		3V	2.2		

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	SN54LVC157A		UNIT
			- 55 TO 125°C		
			MIN	MAX	
V <sub>OL</sub>	I <sub>OL</sub> = 100µA	2.7V to 3.6V	0.2		V
	I <sub>OL</sub> = 12mA	2.7V	0.4		
	I <sub>OL</sub> = 24mA	3V	0.55		
I <sub>I</sub>	All inputs V <sub>I</sub> = 5.5V or GND	3.6V	±5		µA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND I <sub>O</sub> = 0	3.6V	10		µA
Δ I <sub>CC</sub>	One input at V <sub>CC</sub> - 0.6V, Other inputs at V <sub>CC</sub> or GND	2.7V to 3.6V	500		µA

#### 4.7 Electrical Characteristics, SN74LVC157A

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	SN74LVC157A						UNIT	
			T <sub>A</sub> = 25°C			- 40 TO 85°C		- 40 TO 125°C		
			MIN	TYP	MAX	MIN	MAX	MIN		MAX
V <sub>OH</sub>	I <sub>OH</sub> = - 100µA	1.65V to 3.6V	V <sub>CC</sub> - 0.2			V <sub>CC</sub> - 0.2		V <sub>CC</sub> - 0.3		V
	I <sub>OH</sub> = - 4mA	1.65V	1.29			1.2		1.05		
	I <sub>OH</sub> = - 8mA	2.3V	1.9			1.7		1.55		
	I <sub>OH</sub> = - 12mA	2.7V	2.2			2.2		2.05		
		3V	2.4			2.4		2.25		
I <sub>OH</sub> = - 24mA	3V	2.3			2.2		2			
V <sub>OL</sub>	I <sub>OL</sub> = 100µA	1.65V to 3.6V				0.1		0.2		V
	I <sub>OL</sub> = 4mA	1.65V				0.24		0.45		
	I <sub>OL</sub> = 8mA	2.3V				0.3		0.7		
	I <sub>OL</sub> = 12mA	2.7V				0.4		0.4		
	I <sub>OL</sub> = 24mA	3V				0.55		0.55		
I <sub>I</sub>	All inputs V <sub>I</sub> = 5.5V or GND	3.6V				±1		±5		µA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND I <sub>O</sub> = 0	3.6V				1		10		µA
Δ I <sub>CC</sub>	One input at V <sub>CC</sub> - 0.6V, Other inputs at V <sub>CC</sub> or GND	2.7V to 3.6V				500		500		µA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3V				5				pF

#### 4.8 Switching Characteristics, SN54LVC157A

over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	SN54LVC157A		UNIT
				- 55 TO 125°C		
				MIN	MAX	
t <sub>pd</sub>	A or B	Y	2.7V	6.2		ns
			3.3V ± 0.3V	0.8	5.4	
	A/B		2.7V	8.2		
			3.3V ± 0.3V	0.8	7	
	G		2.7V	7.8		
			3.3V ± 0.3V	0.8	6.5	

#### 4.9 Switching Characteristics, SN74LVC157A

over recommended operating free-air temperature range (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	SN74LVC157A						UNIT	
				T <sub>A</sub> = 25°C			- 40 TO 85°C		- 40 TO 125°C		
				MIN	TYP	MAX	MIN	MAX	MIN		MAX
t <sub>pd</sub>	A or B	Y	1.8V ± 0.15V	1	5.5	13.5	1	14	1	15.5	ns
			2.5V ± 0.2V	1	3.2	7.4	1	7.9	1	10	
			2.7V	1	3.6	5.7	1	5.9	1	7.4	
			3.3V ± 0.3V	1	3	5	1	5.2	1	6.4	
	A/B		1.8V ± 0.15V	1	6	15.5	1	16	1	17.5	
			2.5V ± 0.2V	1	3.7	9.6	1	10.1	1	12.2	
			2.7V	1	4.1	7.9	1	8.1	1	10	
			3.3V ± 0.3V	1	3.4	6.6	1	6.8	1	8.4	
	G		1.8V ± 0.15V	1	5.9	13.5	1	14	1	15.5	
			2.5V ± 0.2V	1	3.5	9.3	1	9.8	1	11.9	
			2.7V	1	3.9	7.6	1	7.8	1	9.3	
			3.3V ± 0.3V	1	3.3	6.3	1	6.5	1	7.9	
t <sub>sk(o)</sub>			1.8V ± 0.15V					2	2.5	ns	
			3.3V ± 0.3V					1	1.5		

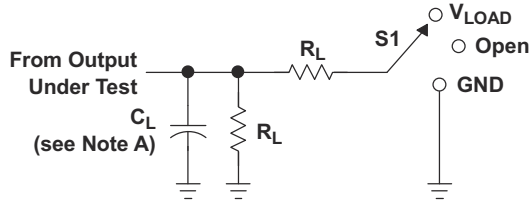
#### 4.10 Operating Characteristics

T<sub>A</sub> = 25°C

PARAMETER		TEST CONDITIONS	V <sub>CC</sub>	TYP	UNIT
C <sub>pd</sub>	Power dissipation capacitance	f = 10 MHz	1.8V	14 <sup>(1)</sup>	pF
			2.5V	15 <sup>(1)</sup>	
			3.3V	16	

(1) On products compliant to MIL-PRF-38535, this parameter does not apply.

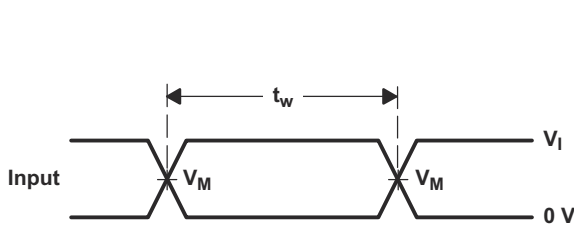
### 5 Parameter Measurement Information



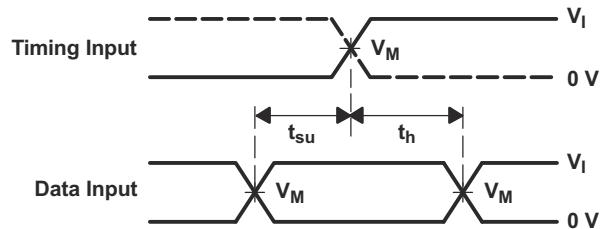
LOAD CIRCUIT

TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$V_{LOAD}$
$t_{PHZ}/t_{PZH}$	GND

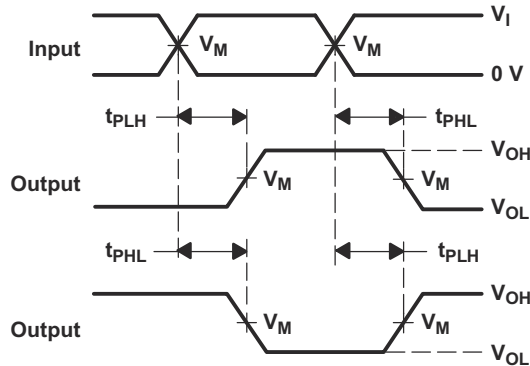
$V_{CC}$	INPUTS		$V_M$	$V_{LOAD}$	$C_L$	$R_L$	$V_{\Delta}$
	$V_I$	$t_r/t_f$					
$1.8\text{ V} \pm 0.15\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 kW	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 W	0.15 V
2.7 V	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 W	0.3 V
$3.3\text{ V} \pm 0.3\text{ V}$	2.7 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 W	0.3 V



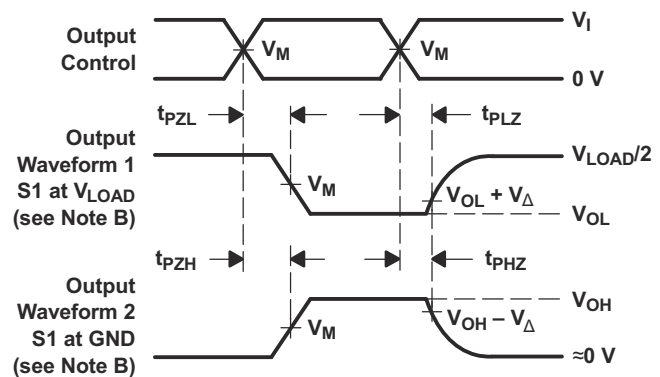
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ .
  - D. The outputs are measured one at a time, with one transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
  - H. All parameters and waveforms are not applicable to all devices.

图 5-1. Load Circuit and Voltage Waveforms



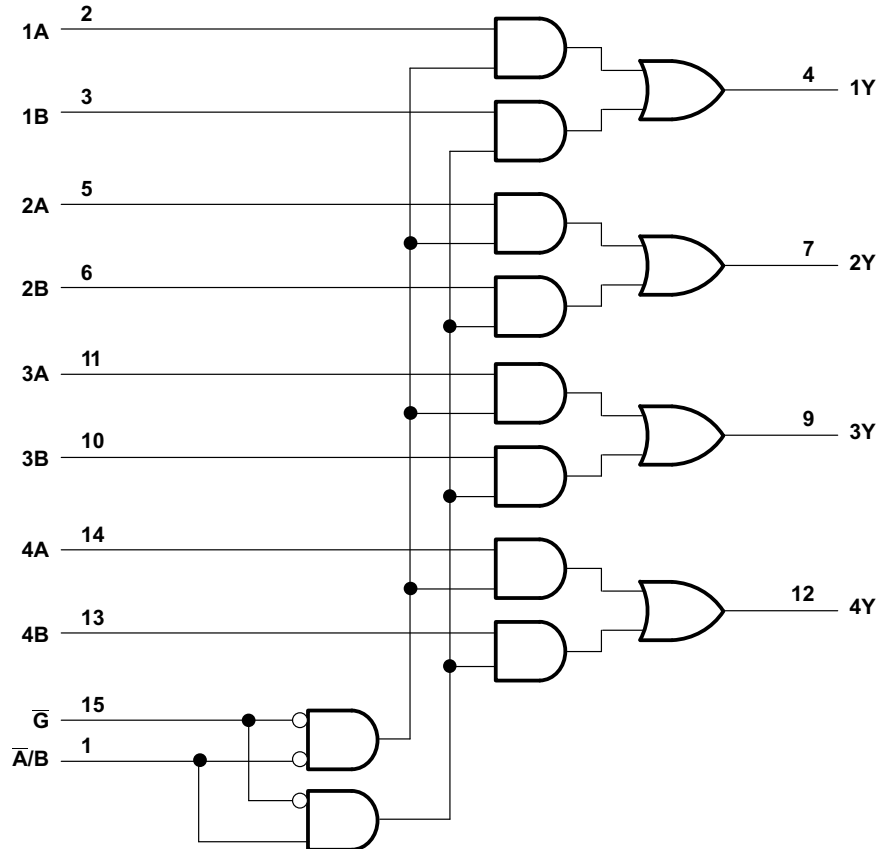
## 6 Detailed Description

### 6.1 Overview

The 'LVC157A devices feature a common strobe ( $\bar{G}$ ) input. When  $\bar{G}$  is high, all outputs are low. When  $\bar{G}$  is low, a 4-bit word is selected from one of two sources and is routed to the four outputs. The 'LVC157A devices provide true data.

Inputs can be driven from either 3.3V or 5V devices. This feature allows the use of these devices as translators in a mixed 3.3V/5V system environment.

### 6.2 Functional Block Diagram



Pin numbers shown are for the D, DB, DGV, J, N, NS, PW, RGY, and W packages.

图 6-1. Logic Diagram (Positive Logic)

### 6.3 Device Functional Modes

Function Table

INPUTS				OUTPUT Y
$\bar{G}$	$\bar{A}/\bar{B}$	A	B	
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

## 7 Application and Implementation

### 备注

以下应用部分中的信息不属于 TI 元件规格，TI 不承担其准确性和完整性。TI 的客户负责确定元件是否适合其用途，以及验证和测试其设计实现以确认系统功能。

### 7.1 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the [表 4.4](#) table.

Each  $V_{CC}$  pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply,  $0.1\ \mu\text{f}$  is recommended; if there are multiple  $V_{CC}$  pins, then  $0.01\ \mu\text{f}$  or  $0.022\ \mu\text{f}$  is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A  $0.1\ \mu\text{f}$  and a  $1\ \mu\text{f}$  are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

### 7.2 Layout

#### 7.2.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified in Layout Diagram are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or  $V_{CC}$ , whichever makes more sense or is more convenient. It is acceptable to float outputs unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the outputs section of the part when asserted. This will not disable the input section of the I/Os so they also cannot float when disabled.

#### 7.2.2 Layout Example

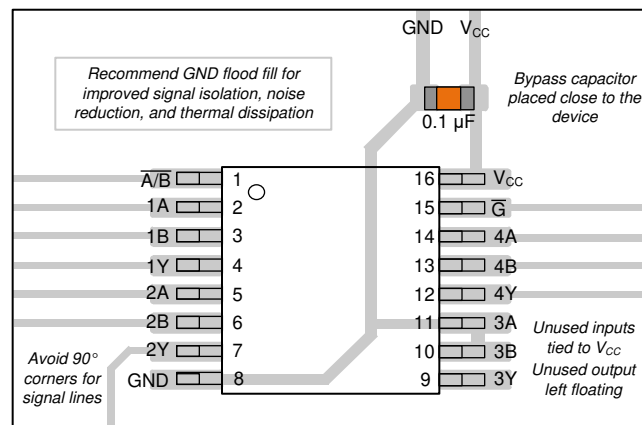


图 7-1. Example Layout for the SN74LVC157A

## 8 Device and Documentation Support

### 8.1 Documentation Support (Analog)

#### 8.1.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 8-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN54LVC157A	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
SN74LVC157A	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

### 8.2 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](http://ti.com) 上的器件产品文件夹。点击 [通知](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 8.3 支持资源

[TI E2E™ 中文支持论坛](#) 是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 [使用条款](#)。

### 8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.  
所有商标均为其各自所有者的财产。

### 8.5 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 8.6 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

## 9 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision Q (December 2010) to Revision R (May 2024)	Page
• 向 <a href="#">封装信息表</a> 、 <a href="#">引脚配置和功能</a> 部分以及 <a href="#">热性能信息表</a> 中添加了 BQA 封装.....	1
• 添加了 <a href="#">器件信息表</a> 、 <a href="#">引脚功能表</a> 、 <a href="#">ESD 等级表</a> 、 <a href="#">热性能信息表</a> 、 <a href="#">器件功能模式</a> 、“应用和实施”部分、 <a href="#">器件和文档支持</a> 部分以及 <a href="#">机械、封装和可订购信息</a> 部分.....	1
• 删除了 <a href="#">特性</a> 中的机器放电模型.....	1

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-0050601QEA	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-0050601QE A SNJ54LVC157AJ	<a href="#">Samples</a>
5962-0050601QFA	ACTIVE	CFP	W	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-0050601QF A SNJ54LVC157AW	<a href="#">Samples</a>
SN74LVC157ABQBR	ACTIVE	WQFN	BQB	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC157A	<a href="#">Samples</a>
SN74LVC157AD	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC157A	<a href="#">Samples</a>
SN74LVC157ADBR	ACTIVE	SSOP	DB	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC157A	<a href="#">Samples</a>
SN74LVC157ADG4	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC157A	<a href="#">Samples</a>
SN74LVC157ADR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	LVC157A	<a href="#">Samples</a>
SN74LVC157ADRE4	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC157A	<a href="#">Samples</a>
SN74LVC157ADRG3	ACTIVE	SOIC	D	16	2500	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	LVC157A	<a href="#">Samples</a>
SN74LVC157ADRG4	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC157A	<a href="#">Samples</a>
SN74LVC157ADT	ACTIVE	SOIC	D	16	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC157A	<a href="#">Samples</a>
SN74LVC157ANSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC157A	<a href="#">Samples</a>
SN74LVC157ANSRE4	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LVC157A	<a href="#">Samples</a>
SN74LVC157APW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC157A	<a href="#">Samples</a>
SN74LVC157APWE4	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC157A	<a href="#">Samples</a>
SN74LVC157APWG4	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC157A	<a href="#">Samples</a>
SN74LVC157APWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	LC157A	<a href="#">Samples</a>
SN74LVC157APWRE4	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC157A	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVC157APWRG4	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC157A	<a href="#">Samples</a>
SN74LVC157APWT	ACTIVE	TSSOP	PW	16	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LC157A	<a href="#">Samples</a>
SN74LVC157ARGYR	ACTIVE	VQFN	RGY	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	LC157A	<a href="#">Samples</a>
SNJ54LVC157AJ	ACTIVE	CDIP	J	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-0050601QE A SNJ54LVC157AJ	<a href="#">Samples</a>
SNJ54LVC157AW	ACTIVE	CFP	W	16	25	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-0050601QF A SNJ54LVC157AW	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN54LVC157A, SN74LVC157A :**

- Catalog : [SN74LVC157A](#)
- Automotive : [SN74LVC157A-Q1](#), [SN74LVC157A-Q1](#)
- Enhanced Product : [SN74LVC157A-EP](#), [SN74LVC157A-EP](#)
- Military : [SN54LVC157A](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC157ADBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74LVC157ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LVC157ADRG3	SOIC	D	16	2500	330.0	16.8	6.5	10.3	2.1	8.0	16.0	Q1
SN74LVC157ADRG4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74LVC157ANSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LVC157APWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC157APWRG4	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC157APWT	TSSOP	PW	16	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LVC157ARGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC157ADBR	SSOP	DB	16	2000	356.0	356.0	35.0
SN74LVC157ADR	SOIC	D	16	2500	340.5	336.1	32.0
SN74LVC157ADRG3	SOIC	D	16	2500	364.0	364.0	27.0
SN74LVC157ADRG4	SOIC	D	16	2500	340.5	336.1	32.0
SN74LVC157ANSR	SO	NS	16	2000	356.0	356.0	35.0
SN74LVC157APWR	TSSOP	PW	16	2000	356.0	356.0	35.0
SN74LVC157APWRG4	TSSOP	PW	16	2000	356.0	356.0	35.0
SN74LVC157APWT	TSSOP	PW	16	250	356.0	356.0	35.0
SN74LVC157ARGYR	VQFN	RGY	16	3000	356.0	356.0	35.0



**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-0050601QFA	W	CFP	16	25	506.98	26.16	6220	NA
SN74LVC157AD	D	SOIC	16	40	507	8	3940	4.32
SN74LVC157ADG4	D	SOIC	16	40	507	8	3940	4.32
SN74LVC157APW	PW	TSSOP	16	90	530	10.2	3600	3.5
SN74LVC157APWE4	PW	TSSOP	16	90	530	10.2	3600	3.5
SN74LVC157APWG4	PW	TSSOP	16	90	530	10.2	3600	3.5
SNJ54LVC157AW	W	CFP	16	25	506.98	26.16	6220	NA

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# DB0016A



# PACKAGE OUTLINE

## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4220763/A 05/2022

### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

# EXAMPLE BOARD LAYOUT

DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220763/A 05/2022

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



# EXAMPLE STENCIL DESIGN

DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220763/A 05/2022

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

## GENERIC PACKAGE VIEW

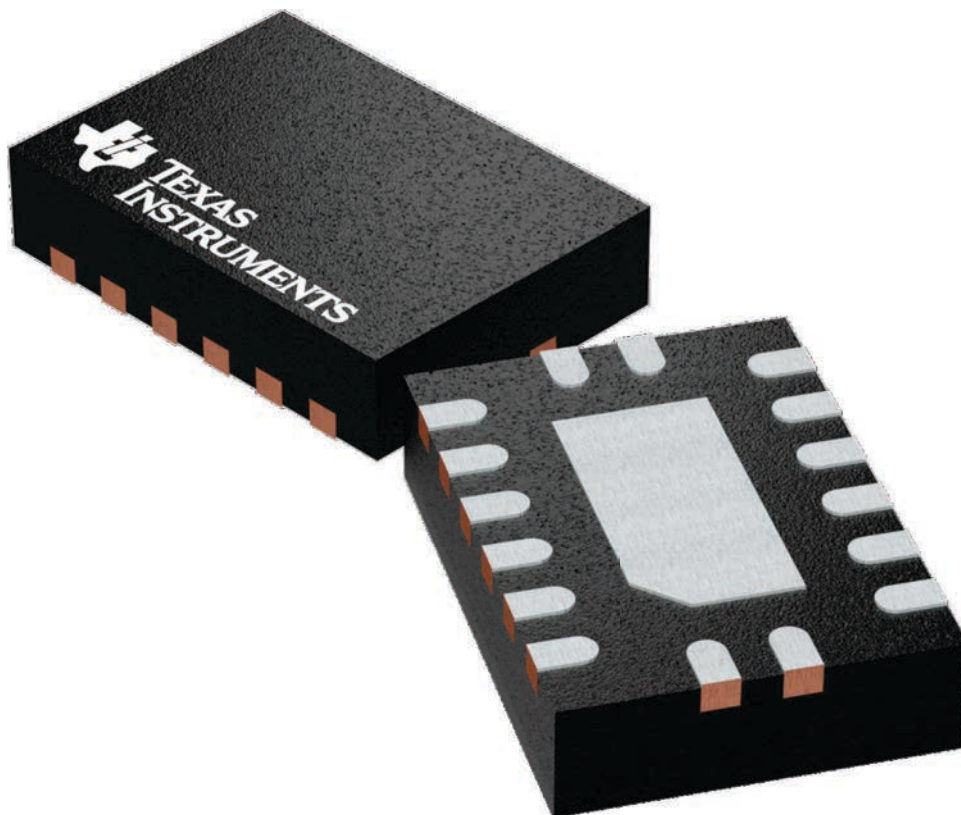
**BQB 16**

**WQFN - 0.8 mm max height**

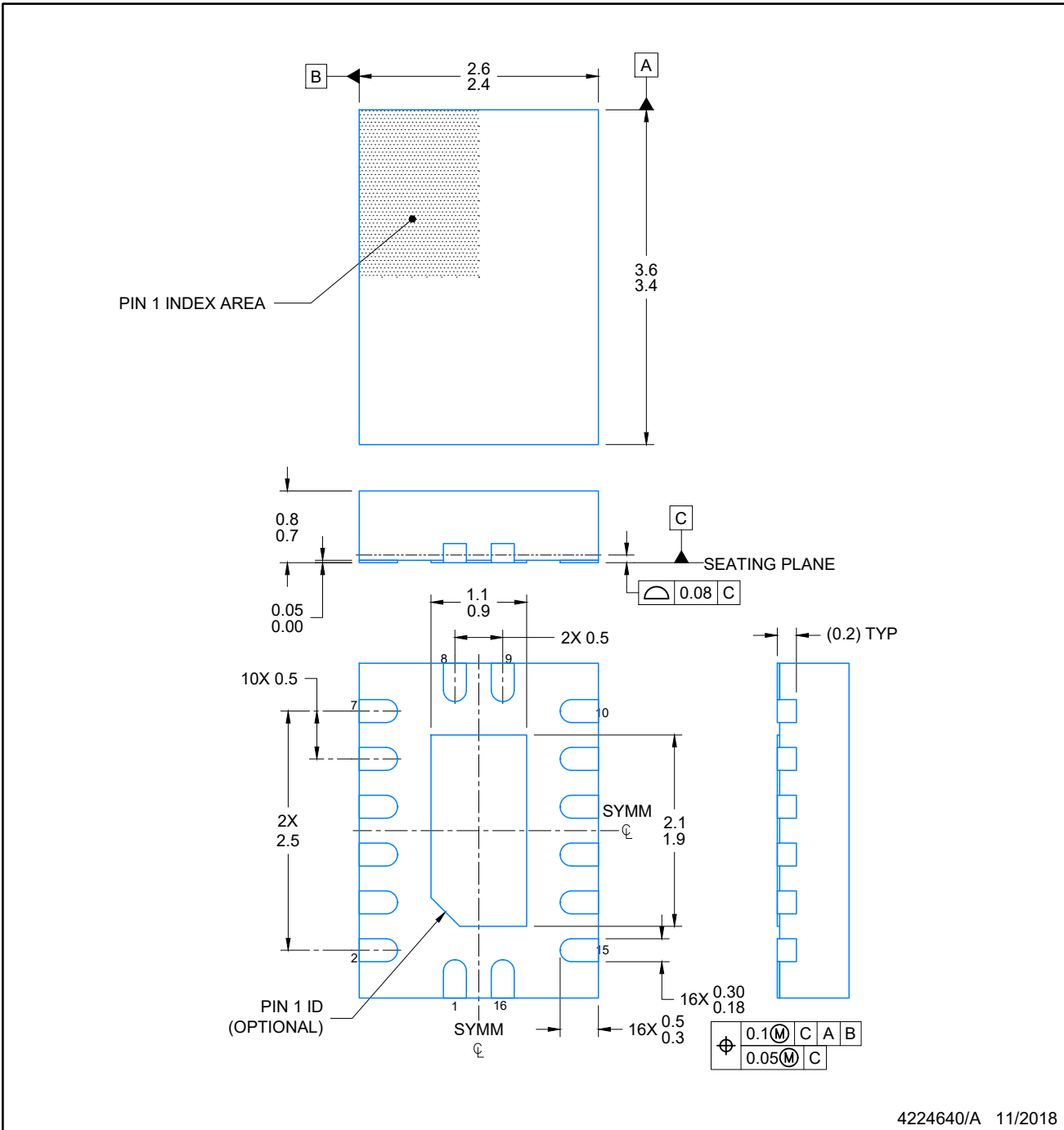
2.5 x 3.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4226161/A



**NOTES:**

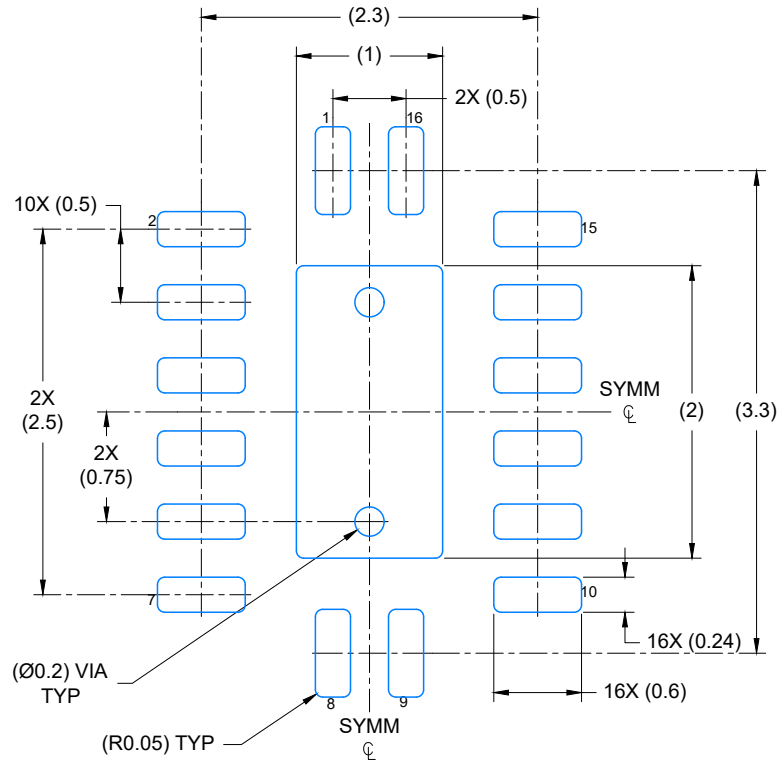
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

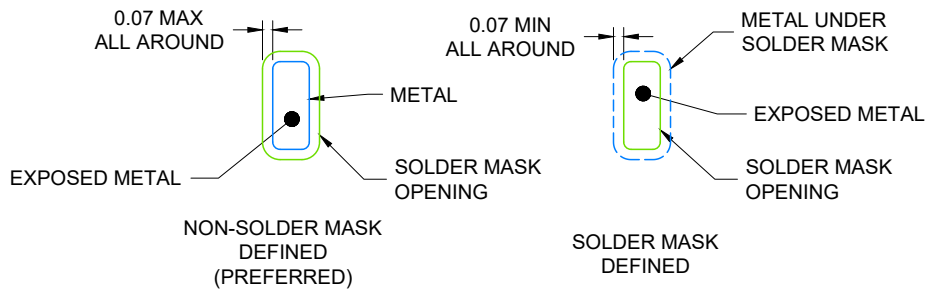
**BQB0016A**

**WQFN - 0.8 mm max height**

PLASTIC QUAD FLAT PACK-NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 20X



4224640/A 11/2018

NOTES: (continued)

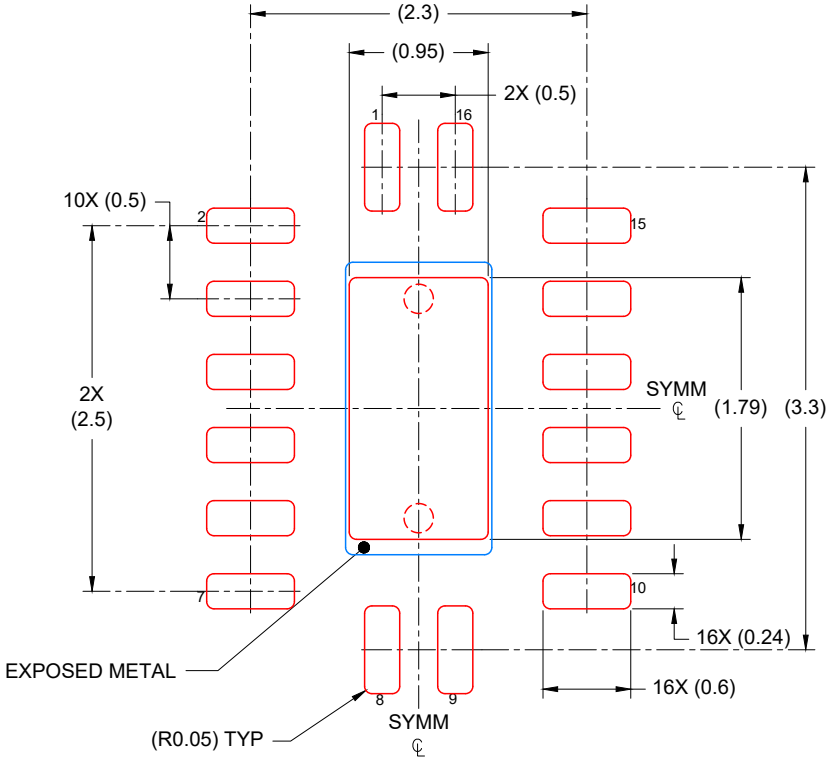
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

**BQB0016A**

**WQFN - 0.8 mm max height**

PLASTIC QUAD FLAT PACK-NO LEAD



**SOLDER PASTE EXAMPLE**  
 BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD  
 85% PRINTED COVERAGE BY AREA  
 SCALE: 20X

4224640/A 11/2018

NOTES: (continued)

- 6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within MIL STD 1835 GDFP2-F16

J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



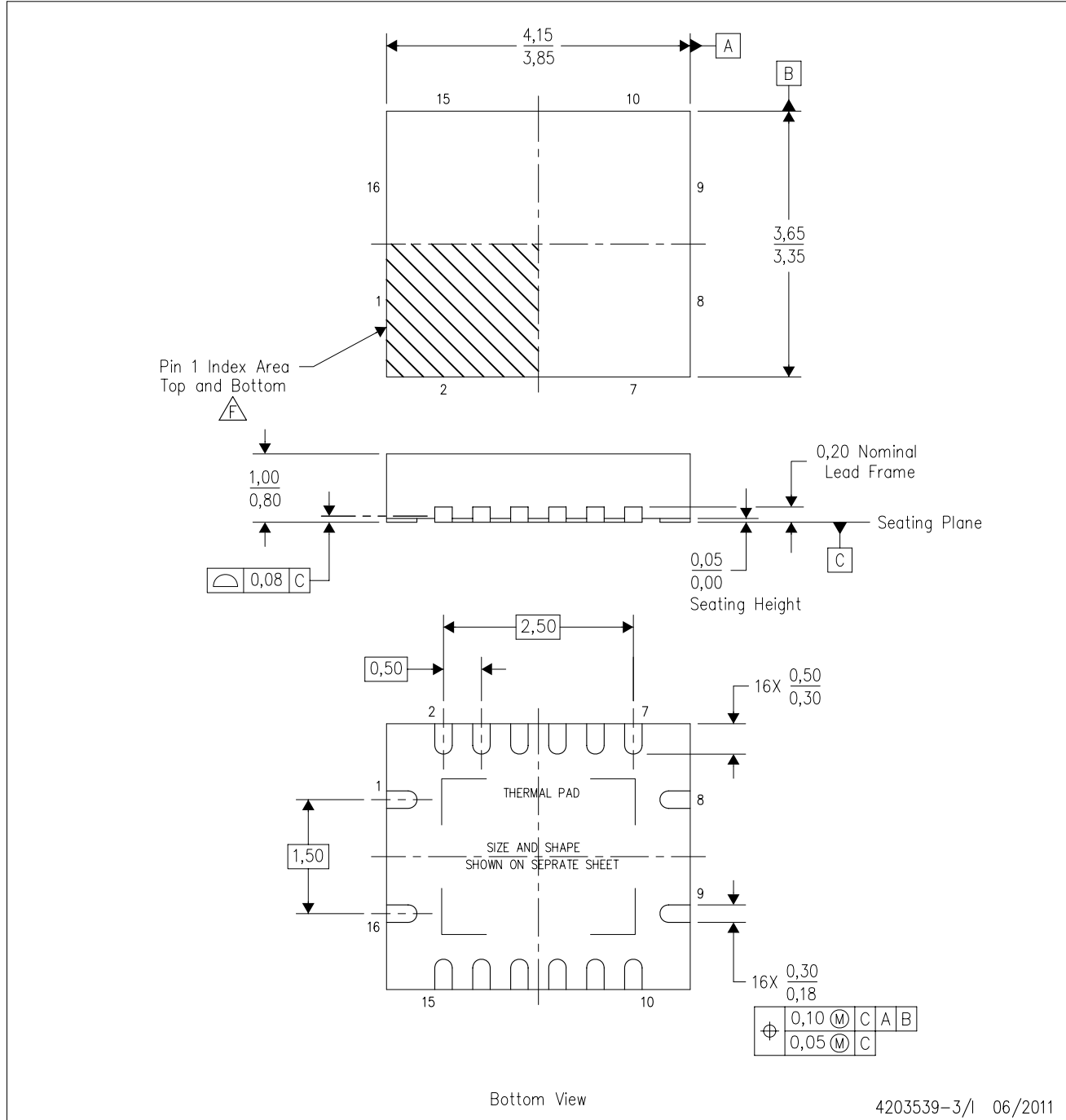
4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.



RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. QFN (Quad Flatpack No-Lead) package configuration.
  - D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
  - F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
  - G. Package complies to JEDEC MO-241 variation BA.

RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD

**THERMAL INFORMATION**

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at [www.ti.com](http://www.ti.com).

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206353-3/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (R-PVQFN-N16)

PLASTIC QUAD FLATPACK NO-LEAD



4208122-3/P 03/14

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at [www.ti.com](http://www.ti.com) <<http://www.ti.com>>.
  - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
  - F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.



# PACKAGE OUTLINE

## NS0016A

### SOP - 2.00 mm max height

SOP



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#### NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



# EXAMPLE STENCIL DESIGN

NS0016A

SOP - 2.00 mm max height

SOP



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:7X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

## 重要声明和免责声明

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