SN74LVC4245A 具有三态输出的八路总线收发器和 3.3V 至 5V 移位器

1 特性

- 双向电压转换器
- A 端口的电压为 5.5V，B 端口的电压范围为 2.7V 至 3.6V
- 控制输入 V_{IH}/V_{IL} 电平以 V_{CCA} 电压为基准
- 闩锁性能超过 250mA，符合 JESD 17 规范
- ESD 保护性能超过 JESD 22 规范要求
  - 2000V 人体模型
  - 1000V 充电器件模型

2 应用

- ATCA 解决方案
- CPAP 呼吸机
- 摄像头：监控模拟
- 化学或气体传感器
- CT 扫描仪
- DLP 3D 机器视觉和光纤网络
- 数字标牌
- ECG：心电图
- 现场变送器：压力传感器和温度传感器
- 高速数据采集和生成
- HMI（人机界面）
- RF4CE 远程控制
- 服务器主板
- 软件定义无线电 (SDR)
- 无线 LAN 卡和数据访问卡
- X 射线：医疗、牙科和行李扫描仪

3 说明

这款 8 位（八路）同相总线收发器包含两个独立的电源轨；B 端口具有 V_{CCB}，设置为 3.3V；A 端口具有 V_{CCA}，设置为 5V。这样可实现从 3.3V 到 5V 的环境转换，反之亦然。

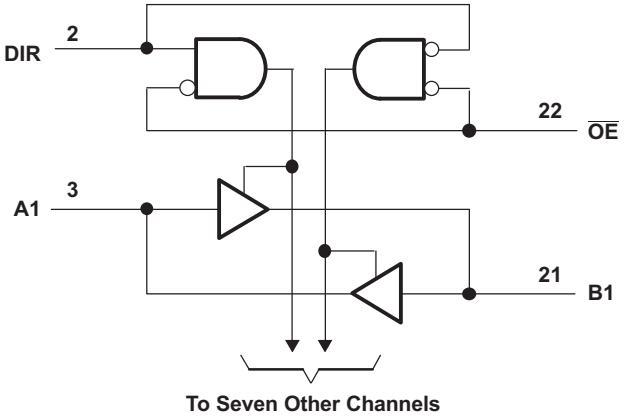
SN74LVC4245A 器件旨在实现数据总线之间的异步通信。根据方向控制 (DIR) 输入上的逻辑电平，此器件将数据从 A 总线发送至 B 总线，或者将数据从 B 总线发送至 A 总线。输出使能 ($\overline{OE}$) 输入可用于禁用器件，这样可有效隔离总线。控制电路（DIR，$\overline{OE}$）由 V_{CCA} 供电。

设计人员可将 SN74LVC4245A 器件端子输出切换到正常的全 3.3V 或全 5V 20 端子 SN74LVC4245 器件，而无需重新布局电路板。设计人员可使用 SN74LVC4245A 器件的 2 到 11 和 14 到 23 引脚的数据路径来与传统的 245 端子输出保持一致。

封装信息(1)

器件型号	封装	封装尺寸（标称值）
SN74LVC4245A	DB (SSOP, 24)	8.20mm × 5.30mm
	DW（SOIC，24）	15.40mm × 7.50mm
	PW（TSSOP，24）	7.80mm × 4.40mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



简化原理图

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4 Revision History

Changes from Revision I (January 2015) to Revision J (December 2022)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式	1
• Updated thermals for DB and PW package	5

Changes from Revision H (March 2005) to Revision I (January 2015)	Page
• 添加了*应用*、*器件信息*表、*引脚功能*表、*ESD 等级*表、*热性能信息*表、*典型特性*、*特性说明*部分、*器件功能模式*、*应用和实施*部分、*电源相关建议*部分、*布局*部分、*器件和文档支持*部分以及*机械、封装和可订购信息*部分	1
• 删除了*订购信息*表	1

5 Pin Configuration and Functions

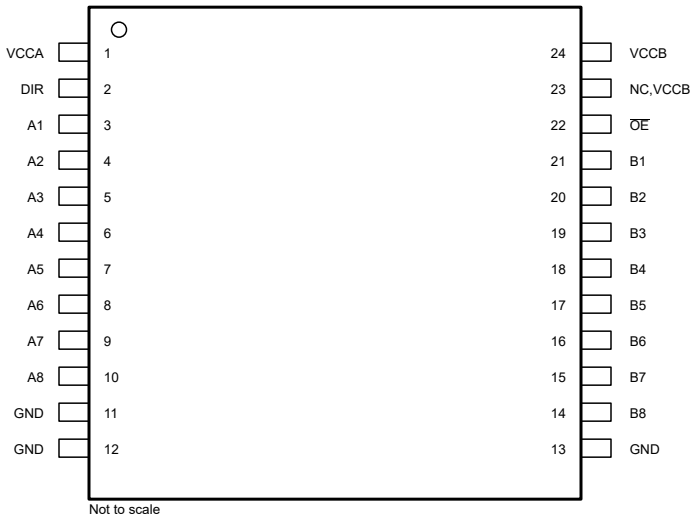


图 5-1. DB, DW, or PW Package, SOP, TSSOP, (Top View)

表 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
V_{CCA}	1	—	Power supply for side A
DIR	2	I	Direction control
A1	3	I/O	Transceiver I/O pin
A2	4	I/O	Transceiver I/O pin
A3	5	I/O	Transceiver I/O pin
A4	6	I/O	Transceiver I/O pin
A5	7	I/O	Transceiver I/O pin
A6	8	I/O	Transceiver I/O pin
A7	9	I/O	Transceiver I/O pin
A8	10	I/O	Transceiver I/O pin
GND	11	—	Ground
GND	12	—	Ground
GND	13	—	Ground
B8	14	I/O	Transceiver I/O pin
B7	15	I/O	Transceiver I/O pin
B6	16	I/O	Transceiver I/O pin
B5	17	I/O	Transceiver I/O pin
B4	18	I/O	Transceiver I/O pin
B3	19	I/O	Transceiver I/O pin
B2	20	I/O	Transceiver I/O pin
B1	21	I/O	Transceiver I/O pin
$\overline{OE}$	22	I	Output Enable
V_{CCB}	23	—	Power supply for side B
V_{CCB}	24	—	Power supply for side B

(1) I = input, O = output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range for V_{CCA} = 4.5 V to 5.5 V (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CCA}	Supply voltage range		– 0.5	6.5	V
V_I	Input voltage range	A port(2)	– 0.5	V_{CCA} + 0.5	V
		Control inputs	– 0.5	6	
V_O	Output voltage range	A port(2)	– 0.5	V_{CCA} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		– 50	mA
I_{OK}	Output clamp current	V_O < 0		– 50	mA
I_O	Continuous output current			±50	mA
	Continuous current through each V_{CCA} or GND			±100	mA
T_{stg}	Storage temperature range		– 65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under 节 6.4 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) This value is limited to 6 V maximum.

6.2 Absolute Maximum Ratings

over operating free-air temperature range for V_{CCB} = 2.7 V to 3.6 V (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CCB}	Supply voltage range		– 0.5	4.6	V
V_I	Input voltage range	B port(2)	– 0.5	V_{CCB} + 0.5	V
V_O	Output voltage range	B port(2)	– 0.5	V_{CCB} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		– 50	mA
I_{OK}	Output clamp current	V_O < 0		– 50	mA
I_O	Continuous output current			±50	mA
	Continuous current through V_{CCB} or GND			±100	mA
T_{stg}	Storage temperature range		– 65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under 节 6.4 is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) This value is limited to 4.6 V maximum.

6.3 ESD Ratings

PARAMETER		DEFINITION	VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.4 Recommended Operating Conditions

for V_{CCA} = 4.5 V to 5.5 V(1)

		MIN	MAX	UNIT
V_{CCA}	Supply voltage	4.5	5.5	V
V_{IH}	High-level input voltage	2		V
V_{IL}	Low-level input voltage		0.8	V
V_{IA}	Input voltage	0	V_{CCA}	V
V_{OA}	Output voltage	0	V_{CCA}	V
I_{OH}	High-level output current		– 24	mA
I_{OL}	Low-level output current		24	mA
T_A	Operating free-air temperature	– 40	85	°C

(1) All unused inputs of the device must be held at the associated V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

6.5 Recommended Operating Conditions

for V_{CCB} = 2.7 V to 3.6 V(1)

			MIN	MAX	UNIT
V_{CCB}	Supply voltage		2.7	3.6	V
V_{IH}	High-level input voltage	V_{CCB} = 2.7 V to 3.6 V	2		V
V_{IL}	Low-level input voltage	V_{CCB} = 2.7 V to 3.6 V		0.8	V
V_{IB}	Input voltage		0	V_{CCB}	V
V_{OB}	Output voltage		0	V_{CCB}	V
I_{OH}	High-level output current	V_{CCB} = 2.7 V		– 12	mA
		V_{CCB} = 3 V		– 24	
I_{OL}	Low-level output current	V_{CCB} = 2.7 V		12	mA
		V_{CCB} = 3 V		24	
T_A	Operating free-air temperature		– 40	85	°C

(1) All unused inputs of the device must be held at the associated V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

6.6 Thermal Information

THERMAL METRIC(1)		SN74LVC4245A		UNIT
		DB	PW	
		24 PINS		
$R_{\theta JA}$	Junction-to-ambient thermal resistance	90.7	100.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	51.9	44.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	49.7	55.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	18.8	6.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	49.3	55.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.7 Electrical Characteristics

over recommended operating free-air temperature range for V_{CCA} = 4.5 V to 5.5 V (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		V_{CCA}	MIN	TYP(2)	MAX	UNIT
V_{OH}		I_{OH} = –100 μA		4.5 V	4.3			V
				5.5 V	5.3			
		I_{OH} = –24 mA		4.5 V	3.7			
				5.5 V	4.7			
V_{OL}		I_{OL} = 100 μA		4.5 V			0.2	V
				5.5 V			0.2	
		I_{OL} = 24 mA		4.5 V			0.55	
				5.5 V			0.55	
I_I	Control inputs	$V_I = V_{CCA}$ or GND		5.5 V			±1	μA
I_{OZ} (3)	A port	$V_O = V_{CCA}$ or GND		5.5 V			±5	μA
I_{CCA}		$V_I = V_{CCA}$ or GND,	I_O = 0	5.5 V			80	μA
ΔI_{CCA} (4)		One input at 3.4 V,	Other inputs at V_{CCA} or GND	5.5 V			1.5	mA
C_i	Control inputs	$V_I = V_{CCA}$ or GND		Open		5		pF
C_{io}	A port	$V_O = V_{CCA}$ or GND		5 V		11		pF

(1) V_{CCB} = 2.7 V to 3.6 V.
(2) All typical values are measured at V_{CC} = 5 V, T_A = 25°C.
(3) For I/O ports, the parameter I_{OZ} includes the input leakage current.
(4) This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or the associated V_{CC}.

6.8 Electrical Characteristics

over recommended operating free-air temperature range for V_{CCB} = 2.7 V to 3.6 V (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS		V_{CCB}	MIN	TYP(4)	MAX	UNIT
V_{OH}		I_{OH} = –100 μA		2.7 V to 3.6 V	V_{CC} – 0.2			V
		I_{OH} = –12 mA		2.7 V	2.2			
				3 V	2.4			
		I_{OH} = –24 mA		3 V	2			
V_{OL}		I_{OL} = 100 μA		2.7 V to 3.6 V			0.2	V
		I_{OL} = 12 mA		2.7 V			0.4	
		I_{OL} = 24 mA		3 V			0.55	
I_{OZ} (2)	B port	$V_O = V_{CCB}$ or GND		3.6 V			±5	μA
I_{CCB}		$V_I = V_{CCB}$ or GND,	I_O = 0	3.6 V			50	μA
ΔI_{CCB} (3)		One input at V_{CCB} – 0.6 V,	Other inputs at V_{CCB} or GND	2.7 V to 3.6 V			0.5	mA
C_{io}	B port	$V_O = V_{CCB}$ or GND		3.3 V		11		pF

(1) V_{CCA} = 5 V ± 0.5 V.
(2) For I/O ports, the parameter I_{OZ} includes the input leakage current.
(3) This is the increase in supply current for each input that is at one of the specified TTL voltage levels, rather than 0 V or the associated V_{CC}.
(4) All typical values are measured at V_{CC} = 3.3 V, T_A = 25°C.

6.9 Switching Characteristics

over recommended operating free-air temperature range, C_L = 50 pF (unless otherwise noted) (see 图 7-1 and 图 7-2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CCA} = 5 V ± 0.5 V, V_{CCB} = 2.7 V to 3.6 V		UNIT
			MIN	MAX	
t_{PHL}	A	B	1	6.3	ns
t_{PLH}			1	6.7	
t_{PHL}	B	A	1	6.1	ns
t_{PLH}			1	5	
t_{PZL}	$\overline{OE}$	A	1	9	ns
t_{PZH}			1	10	
t_{PZL}	$\overline{OE}$	B	1	10.3	ns
t_{PZH}			1	9.8	
t_{PLZ}	$\overline{OE}$	A	1	7	ns
t_{PHZ}			1	5.8	
t_{PLZ}	$\overline{OE}$	B	1	7.7	ns
t_{PHZ}			1	7.8	

6.10 Operating Characteristics

V_{CCA} = 4.5 V to 5.5 V, V_{CCB} = 2.7 V to 3.6 V, T_A = 25°C

PARAMETER			TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance per transceiver	Outputs enabled	C_L = 0,	f = 10 MHz	39.5	pF
		Outputs disabled			5	

6.11 Typical Characteristics

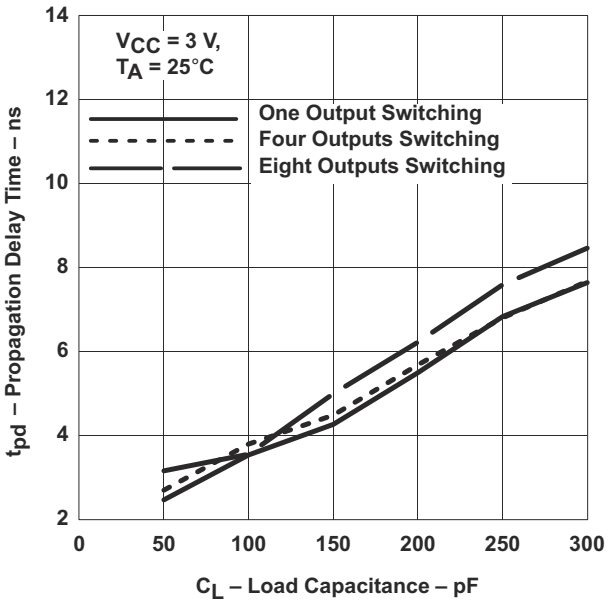


图 6-1. Propagation Delay (Low to High Transition) vs Load Capacitance

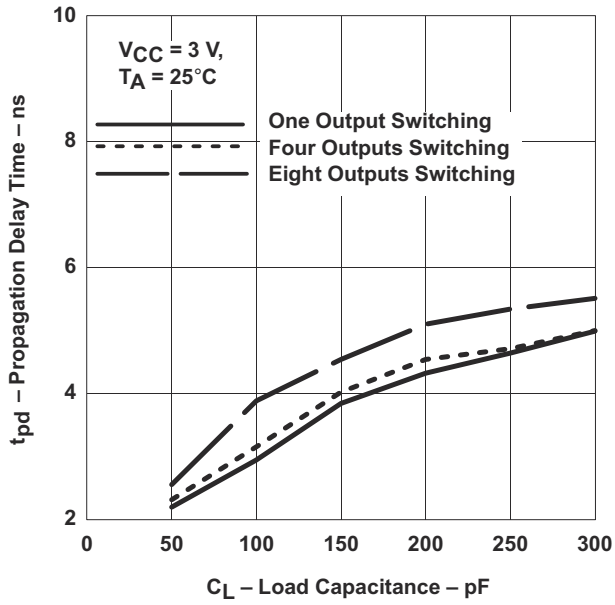
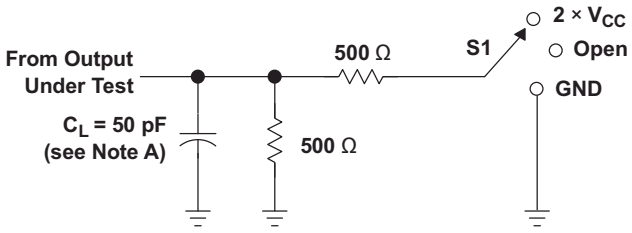


图 6-2. Propagation Delay (High to Low Transition) vs Load Capacitance

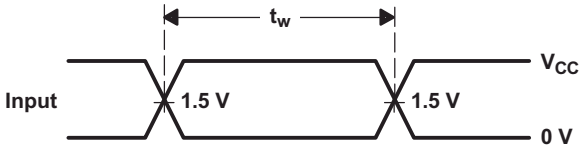
7 Parameter Measurement Information

7.1 A Port

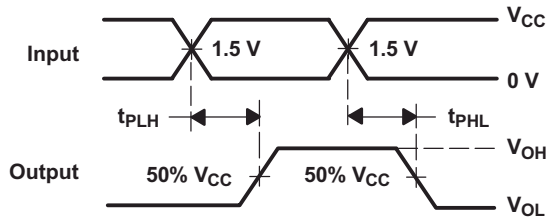


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

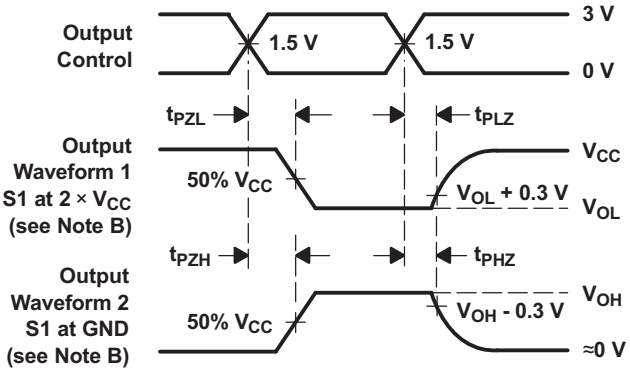
LOAD CIRCUIT



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
NONINVERTING OUTPUTS

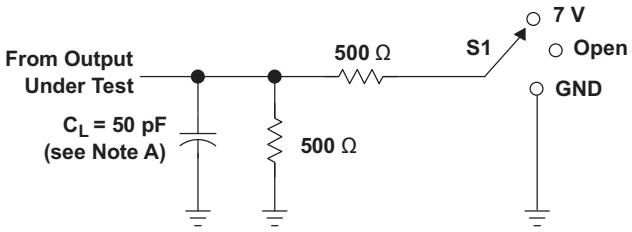


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

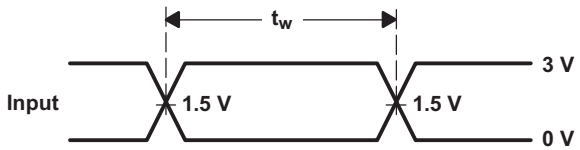
图 7-1. Load Circuit and Voltage Waveforms

7.2 B Port

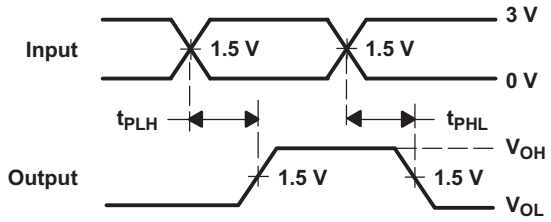


TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	7 V
t_{PHZ}/t_{PZH}	GND

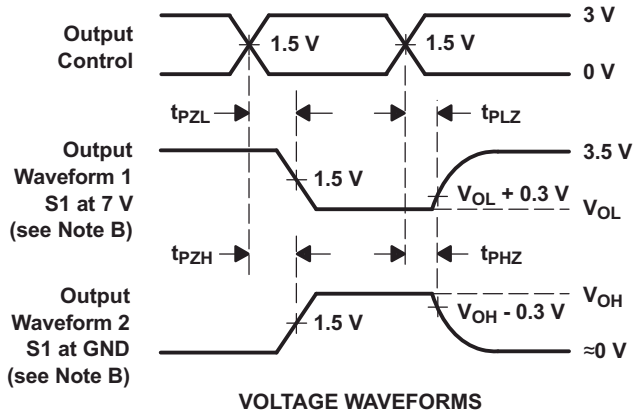
LOAD CIRCUIT



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
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NOTES: A. C_L includes probe and jig capacitance.
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D. The outputs are measured one at a time, with one transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

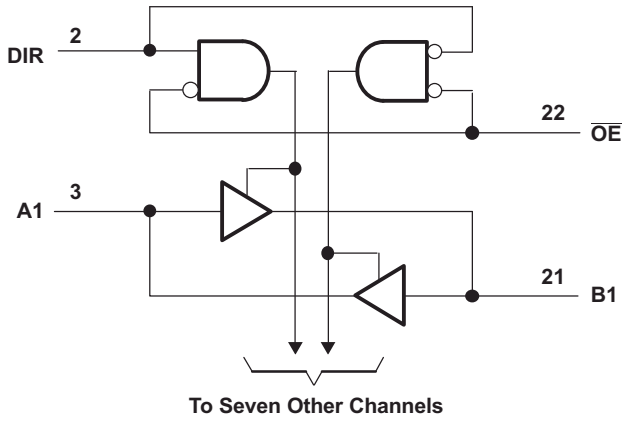
图 7-2. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

SN74LVC4245A is an 8-bit (octal) noninverting bus transceiver contains two separate supply rails; B port has V_{CCB}, which is set at 3.3 V, and A port has V_{CCA}, which is set at 5 V. This allows for translation from a 3.3-V to a 5-V environment, and vice versa, designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the device so the buses are effectively isolated. The control circuitry (DIR, $\overline{OE}$) is powered by V_{CCA}.

8.2 Functional Block Diagram



8.3 Feature Description

- 24 mA drive at 3-V supply
  - Good for heavier loads and longer traces
- Low V_{IH}
  - Allows 3.3-V to 5-V translation

8.4 Device Functional Modes

表 8-1. Function Table

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

9 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

9.1 Application Information

The SN74LVC4245A device pinout allows the designer to switch to a normal all-3.3-V or all-5-V 20-pin '245 device without board re-layout. The designer uses the data paths for pins 2 – 11 and 14 – 23 of the SN74LVC4245A to align with the conventional SN74LVC4245 device's pinout. SN74LVC4245A is a high drive CMOS device that can be used for a multitude of bus interface type applications where output drive or PCB trace length is a concern.

9.2 Typical Application

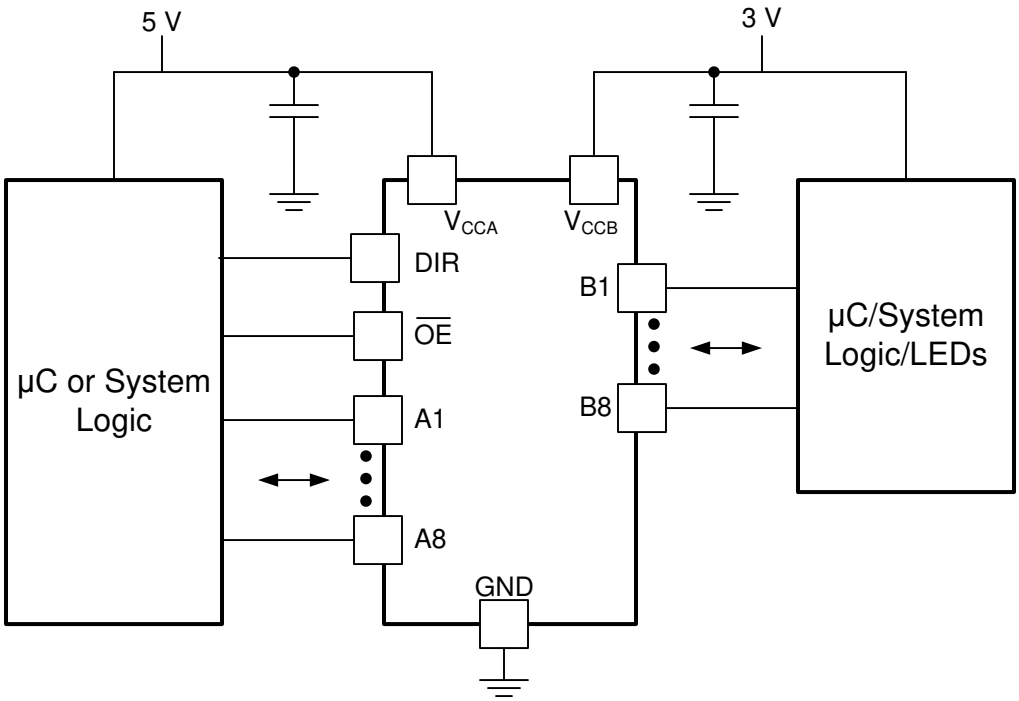


图 9-1. Typical Application Schematic

9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

9.2.2 Detailed Design Procedure

1. Recommended Input Conditions:
   - For rise time and fall time specifcations, see ($\Delta t/\Delta V$) in the 节 6.4 table.
   - For specified high and low levels, see (V_{IH} and V_{IL}) in the 节 6.4 table.
2. Recommend Output Conditions:
   - Load currents should not exceed (I_O max) per output and should not exceed (Continuous current through V_{CC} or GND) total current for the part. These limits are located in the 节 6.1 table.
   - Outputs should not be pulled above V_{CC}.
   - Series resistors on the output may be used if the user desires to slow the output edge signal or limit the output current.

9.2.3 Application Curves

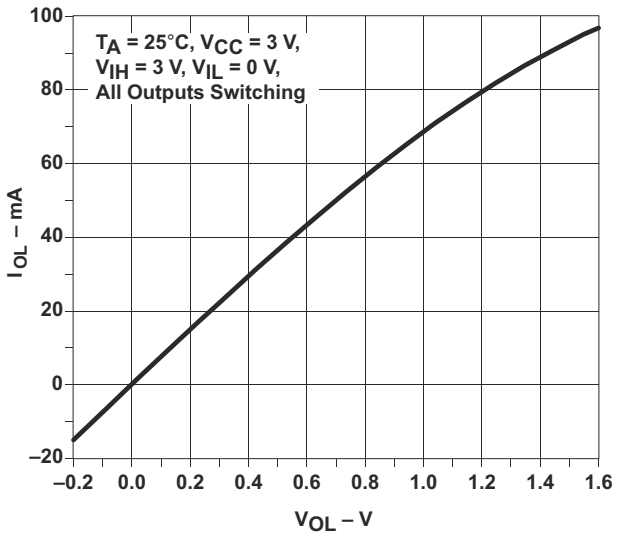


图 9-2. Output Drive Current (I_{OL}) vs LOW-level Output Voltage (V_{OL})

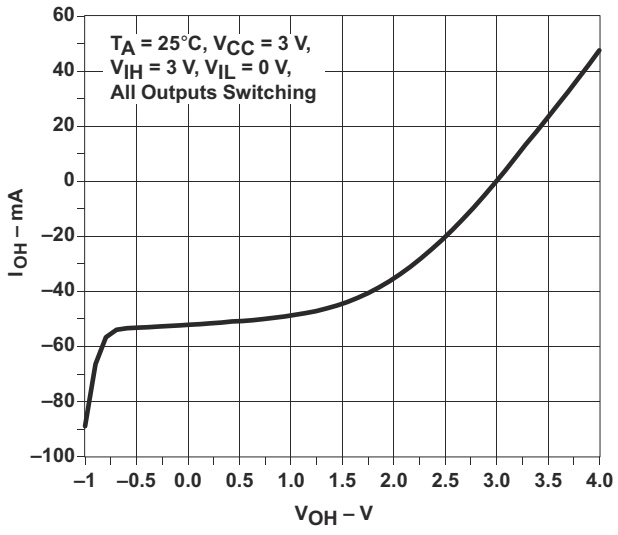


图 9-3. Output Drive Current (I_{OH}) vs HIGH-level Output Voltage (V_{OH})

10 Power Supply Recommendations

10.1 Power-Up Consideration

TI level-translation devices offer an opportunity for successful mixed-voltage signal design. A proper power-up sequence always should be followed to avoid excessive supply current, bus contention, oscillations, or other anomalies caused by improperly biased device terminals. Take these precautions to guard against such power-up problems:

1. Connect ground before any supply voltage is applied.
2. Power up the control side of the device (V_{CCA} for all four of these devices).
3. Tie $\overline{OE}$ to V_{CCA} with a pullup resistor so that it ramps with V_{CCA}.
4. Depending on the direction of the data path, DIR can be high or low. If DIR high is needed (A data to B bus), ramp it with V_{CCA}. Otherwise, keep DIR low.

For more information, refer to the *Voltage-Level-Translation Devices* application note.

11 Layout

11.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in 图 11-1 are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC}, whichever makes more sense or is more convenient.

11.2 Layout Example

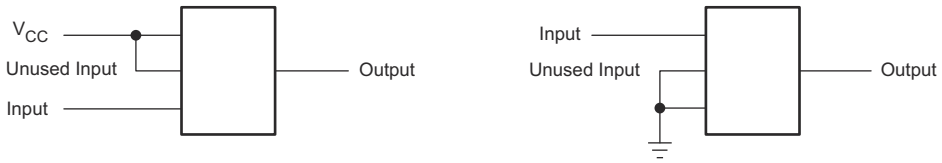


图 11-1. Layout Diagram

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Voltage-Level-Translation Devices* application note

12.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*订阅更新*进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

12.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVC4245ADBR	ACTIVE	SSOP	DB	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LJ245A	Samples
SN74LVC4245ADBRE4	ACTIVE	SSOP	DB	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LJ245A	Samples
SN74LVC4245ADW	ACTIVE	SOIC	DW	24	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC4245A	Samples
SN74LVC4245ADWE4	ACTIVE	SOIC	DW	24	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC4245A	Samples
SN74LVC4245ADWG4	ACTIVE	SOIC	DW	24	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC4245A	Samples
SN74LVC4245ADWR	ACTIVE	SOIC	DW	24	2000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 85	LVC4245A	Samples
SN74LVC4245ADWRE4	ACTIVE	SOIC	DW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC4245A	Samples
SN74LVC4245ADWRG4	ACTIVE	SOIC	DW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVC4245A	Samples
SN74LVC4245APW	ACTIVE	TSSOP	PW	24	60	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LJ245A	Samples
SN74LVC4245APWG4	ACTIVE	TSSOP	PW	24	60	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LJ245A	Samples
SN74LVC4245APWR	ACTIVE	TSSOP	PW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LJ245A	Samples
SN74LVC4245APWRE4	ACTIVE	TSSOP	PW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LJ245A	Samples
SN74LVC4245APWRG4	ACTIVE	TSSOP	PW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LJ245A	Samples
SN74LVC4245APWT	ACTIVE	TSSOP	PW	24	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LJ245A	Samples
SN74LVC4245APWTG4	ACTIVE	TSSOP	PW	24	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LJ245A	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF SN74LVC4245A :

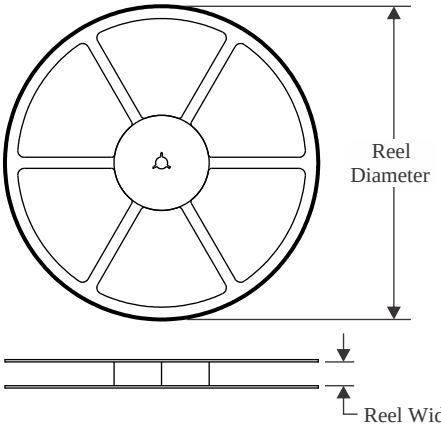
- Enhanced Product : SN74LVC4245A-EP

NOTE: Qualified Version Definitions:

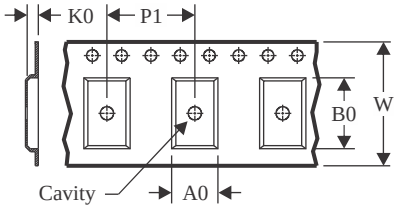
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

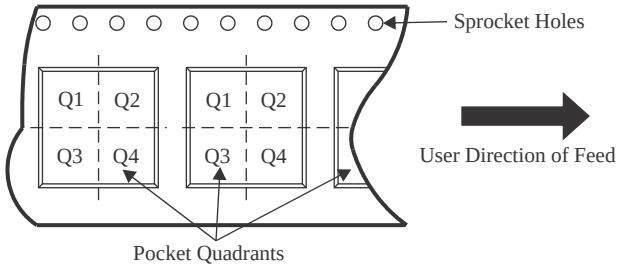


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

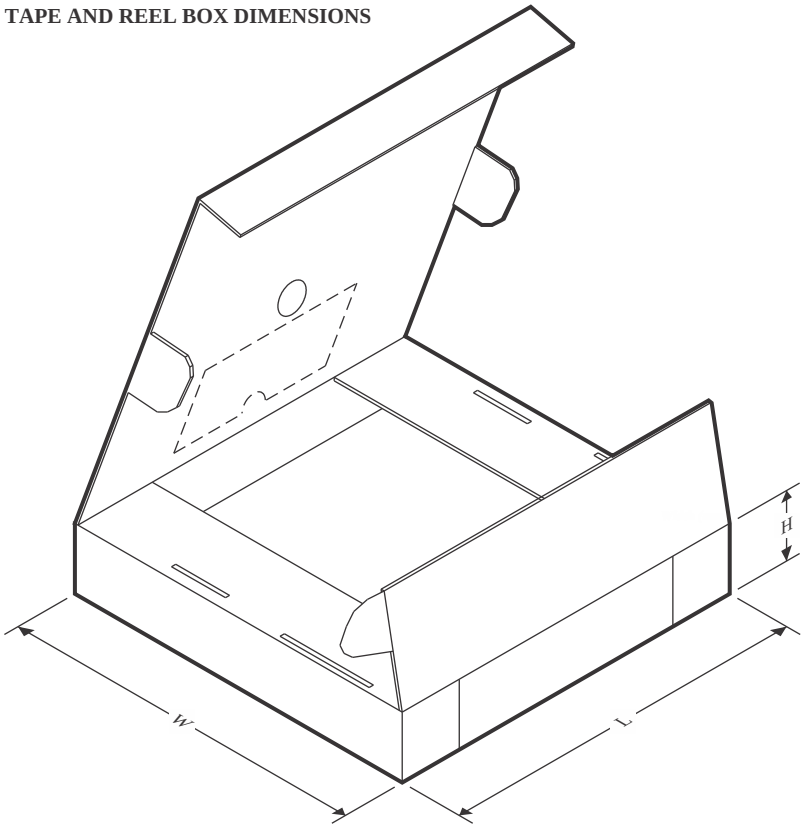
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC4245ADBR	SSOP	DB	24	2000	330.0	16.4	8.2	8.8	2.5	12.0	16.0	Q1
SN74LVC4245ADWR	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
SN74LVC4245ADWRG4	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
SN74LVC4245APWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
SN74LVC4245APWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
SN74LVC4245APWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
SN74LVC4245APWT	TSSOP	PW	24	250	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

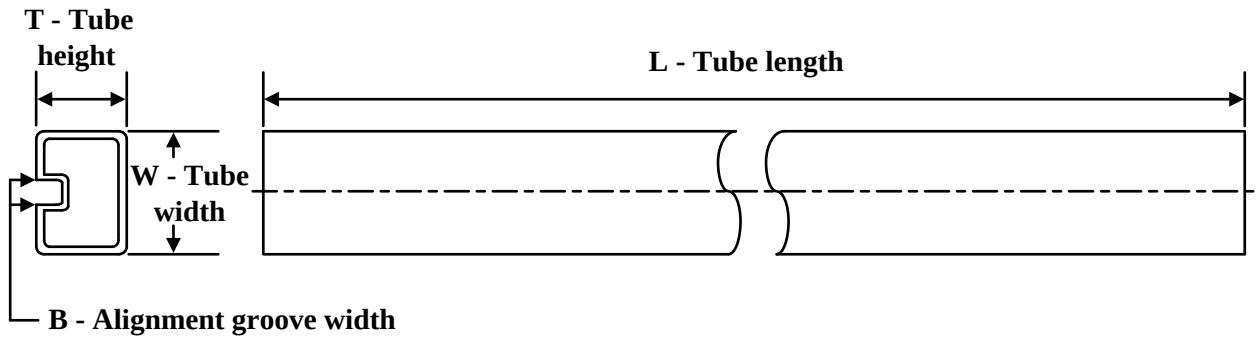
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC4245ADBR	SSOP	DB	24	2000	356.0	356.0	35.0
SN74LVC4245ADWR	SOIC	DW	24	2000	350.0	350.0	43.0
SN74LVC4245ADWRG4	SOIC	DW	24	2000	350.0	350.0	43.0
SN74LVC4245APWR	TSSOP	PW	24	2000	353.0	353.0	32.0
SN74LVC4245APWR	TSSOP	PW	24	2000	356.0	356.0	35.0
SN74LVC4245APWR	TSSOP	PW	24	2000	356.0	356.0	35.0
SN74LVC4245APWT	TSSOP	PW	24	250	356.0	356.0	35.0

TUBE



*All dimensions are nominal

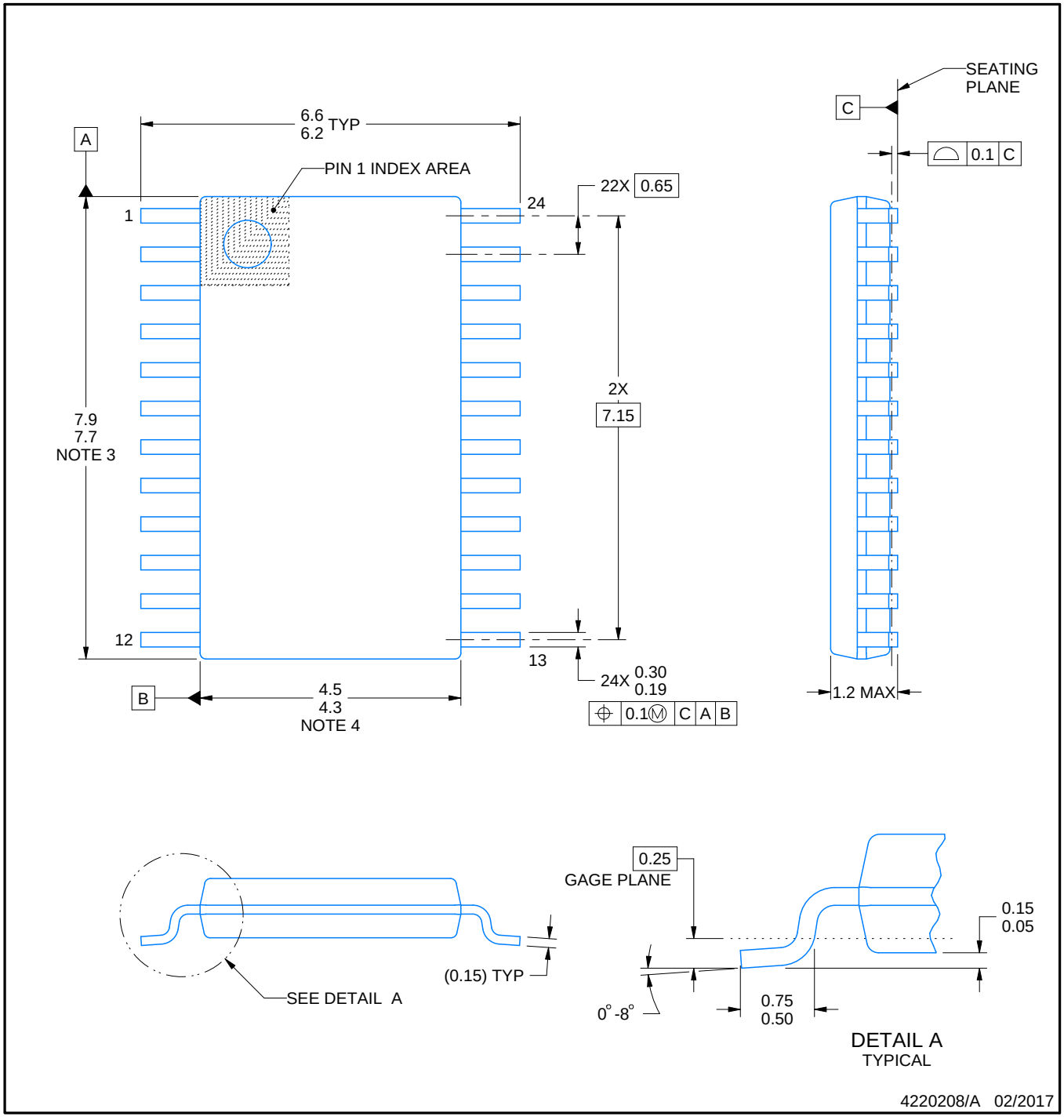
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74LVC4245ADW	DW	SOIC	24	25	506.98	12.7	4826	6.6
SN74LVC4245ADWE4	DW	SOIC	24	25	506.98	12.7	4826	6.6
SN74LVC4245ADWG4	DW	SOIC	24	25	506.98	12.7	4826	6.6
SN74LVC4245APW	PW	TSSOP	24	60	530	10.2	3600	3.5
SN74LVC4245APW	PW	TSSOP	24	60	530	10.2	3600	3.5
SN74LVC4245APWG4	PW	TSSOP	24	60	530	10.2	3600	3.5
SN74LVC4245APWG4	PW	TSSOP	24	60	530	10.2	3600	3.5

PACKAGE OUTLINE

PW0024A

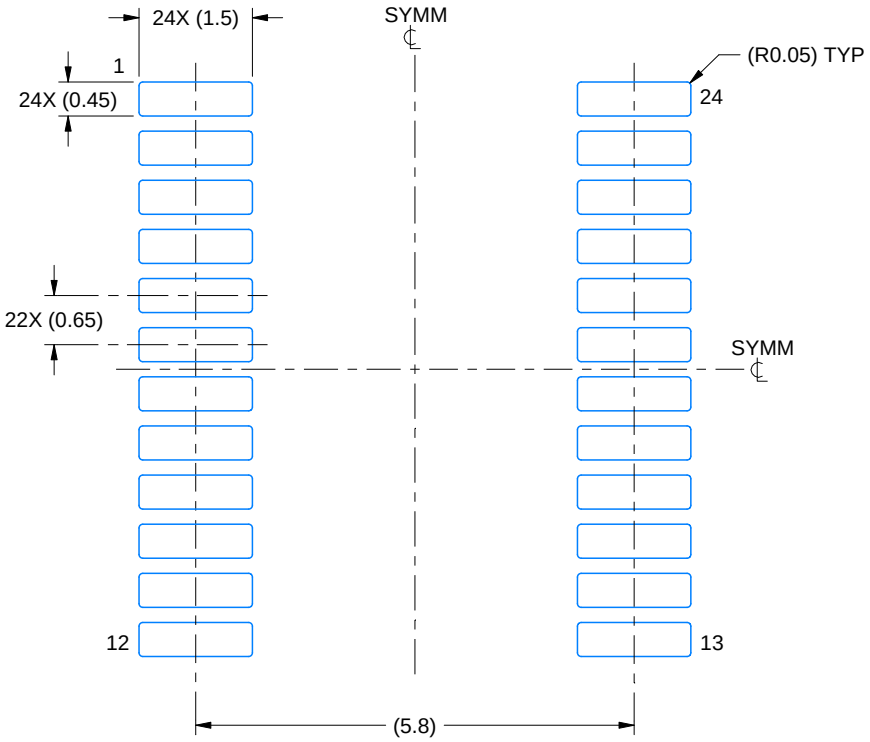
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

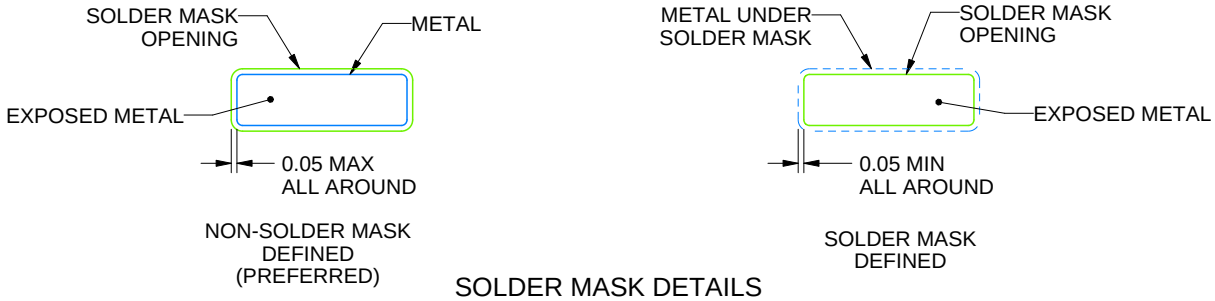


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

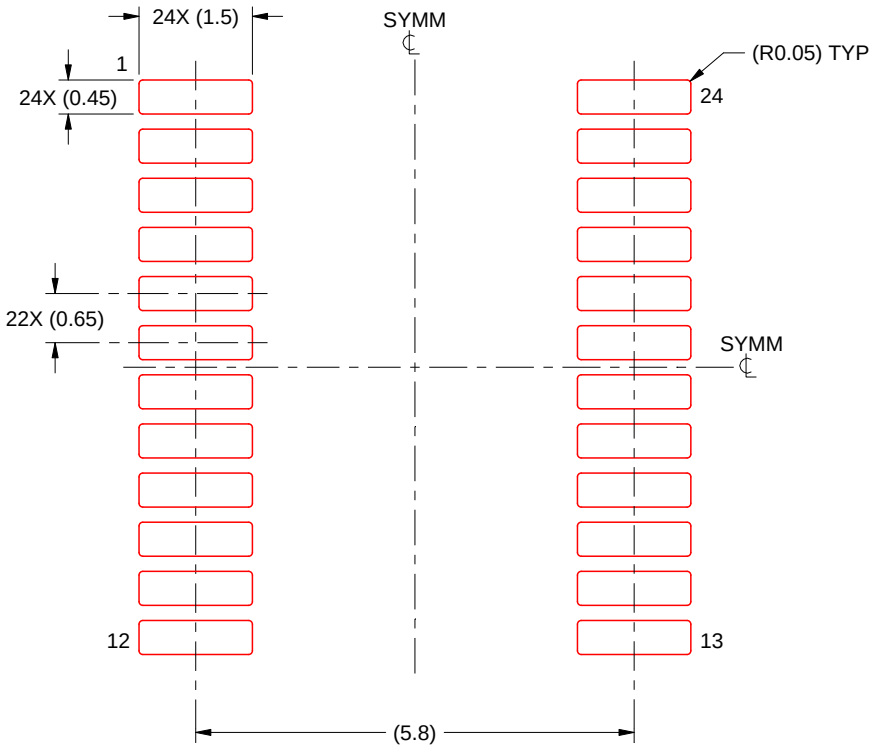


SOLDER MASK DETAILS

4220208/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



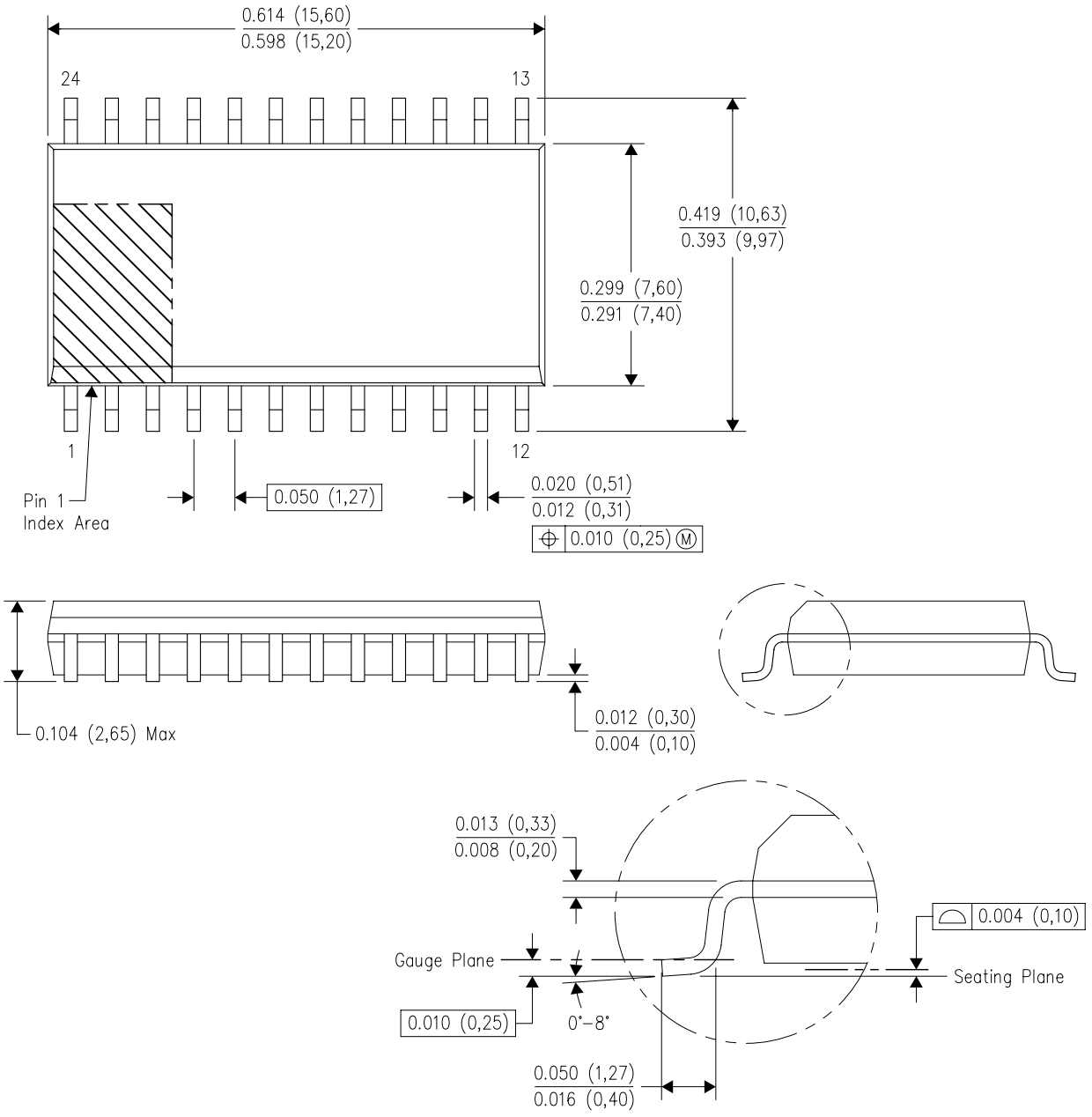
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220208/A 02/2017

NOTES: (continued)

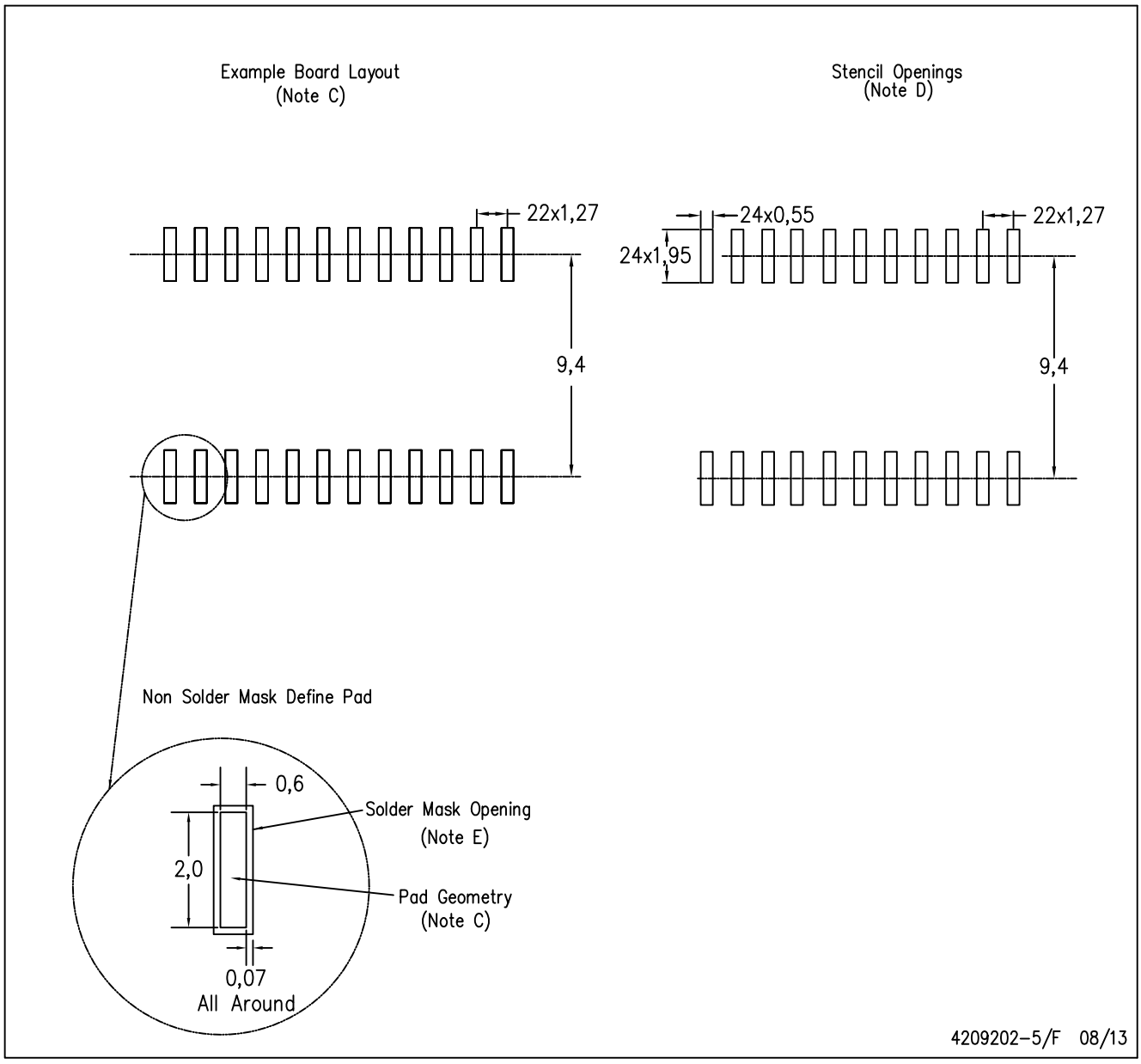
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DW (R–PDSO–G24) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AD.

DW (R–PDSO–G24) PLASTIC SMALL OUTLINE

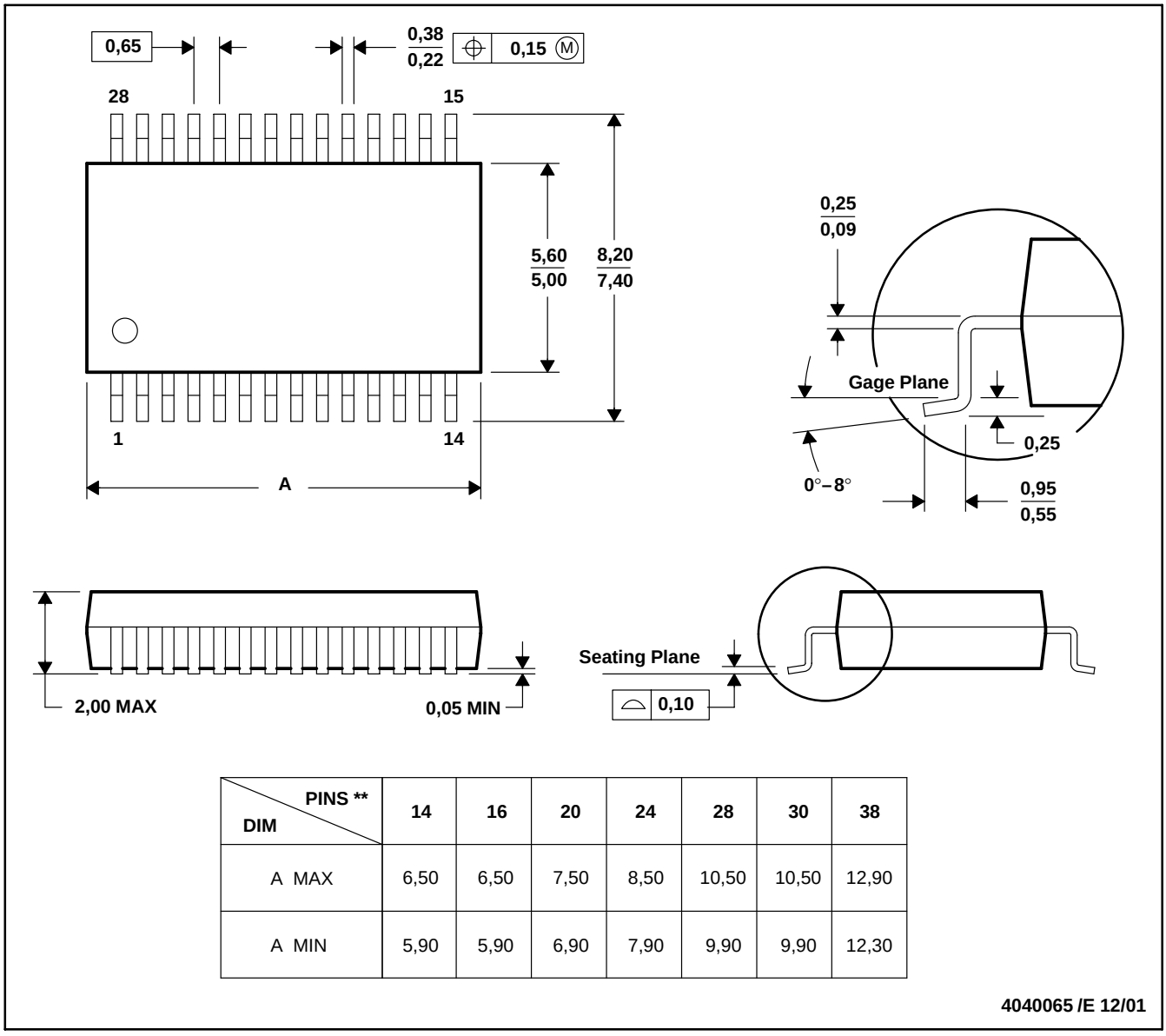


NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Refer to IPC7351 for alternate board design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MSSO002E – JANUARY 1995 – REVISED DECEMBER 2001

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

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