

# SN54LVTH16646, SN74LVTH16646 3.3-V ABT 16-BIT BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

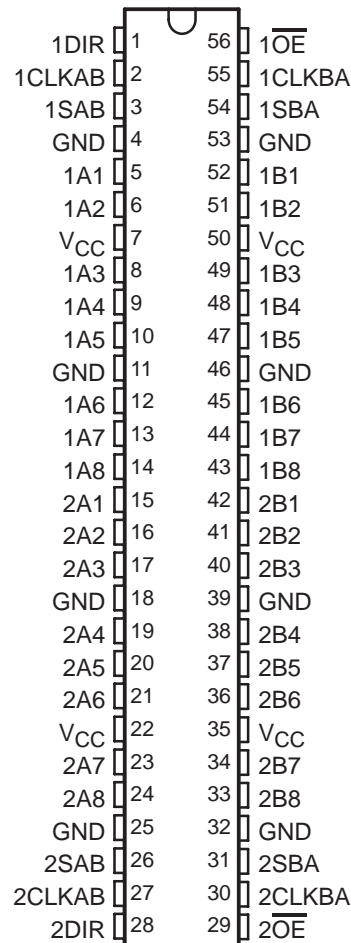
SCBS698G – JULY 1997 – REVISED MAY 2004

- Members of the Texas Instruments Widebus™ Family
- State-of-the-Art Advanced BiCMOS Technology (ABT) Design for 3.3-V Operation and Low Static-Power Dissipation
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V  $V_{CC}$ )
- Support Unregulated Battery Operation Down to 2.7 V
- Typical  $V_{OLP}$  (Output Ground Bounce)  $<0.8$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- $I_{off}$  and Power-Up 3-State Support Hot Insertion
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Distributed  $V_{CC}$  and GND Pin Configuration Minimizes High-Speed Switching Noise
- Flowthrough Architecture Optimizes PCB Layout
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)

## description/ordering information

The 'LVTH16646 devices are 16-bit bus transceivers and registers designed for low-voltage (3.3-V)  $V_{CC}$  operation, but with the capability to provide a TTL interface to a 5-V system environment.

SN54LVTH16646 . . . WD PACKAGE  
SN74LVTH16646 . . . DGG OR DL PACKAGE  
(TOP VIEW)



## ORDERING INFORMATION

$T_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 85°C	SSOP – DL	Tube	SN74LVTH16646DL	LVTH16646
		Tape and reel	SN74LVTH16646DLR	
-55°C to 125°C	TSSOP – DGG	Tape and reel	SN74LVTH16646DGGR	LVTH16646
		CFP – WD	Tube	SNJ54LVTH16646WD

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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 **TEXAS  
INSTRUMENTS**

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# SN54LVTH16646, SN74LVTH16646

## 3.3-V ABT 16-BIT BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SCBS698G – JULY 1997 – REVISED MAY 2004

### description/ordering information (continued)

These devices can be used as two 8-bit transceivers or one 16-bit transceiver. Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the 'LVTH16646 devices.

Output-enable ( $\overline{OE}$ ) and direction-control (DIR) inputs are provided to control the transceiver functions. In the transceiver mode, data present at the high-impedance port may be stored in either register or in both. The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. DIR determines which bus receives data when  $\overline{OE}$  is low. In the isolation mode ( $\overline{OE}$  high), A data can be stored in one register and/or B data can be stored in the other register.

When an output function is disabled, the input function still is enabled and can be used to store and transmit data. Only one of the two buses, A or B, can be driven at a time.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

These devices are fully specified for hot-insertion applications using  $I_{off}$  and power-up 3-state. The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

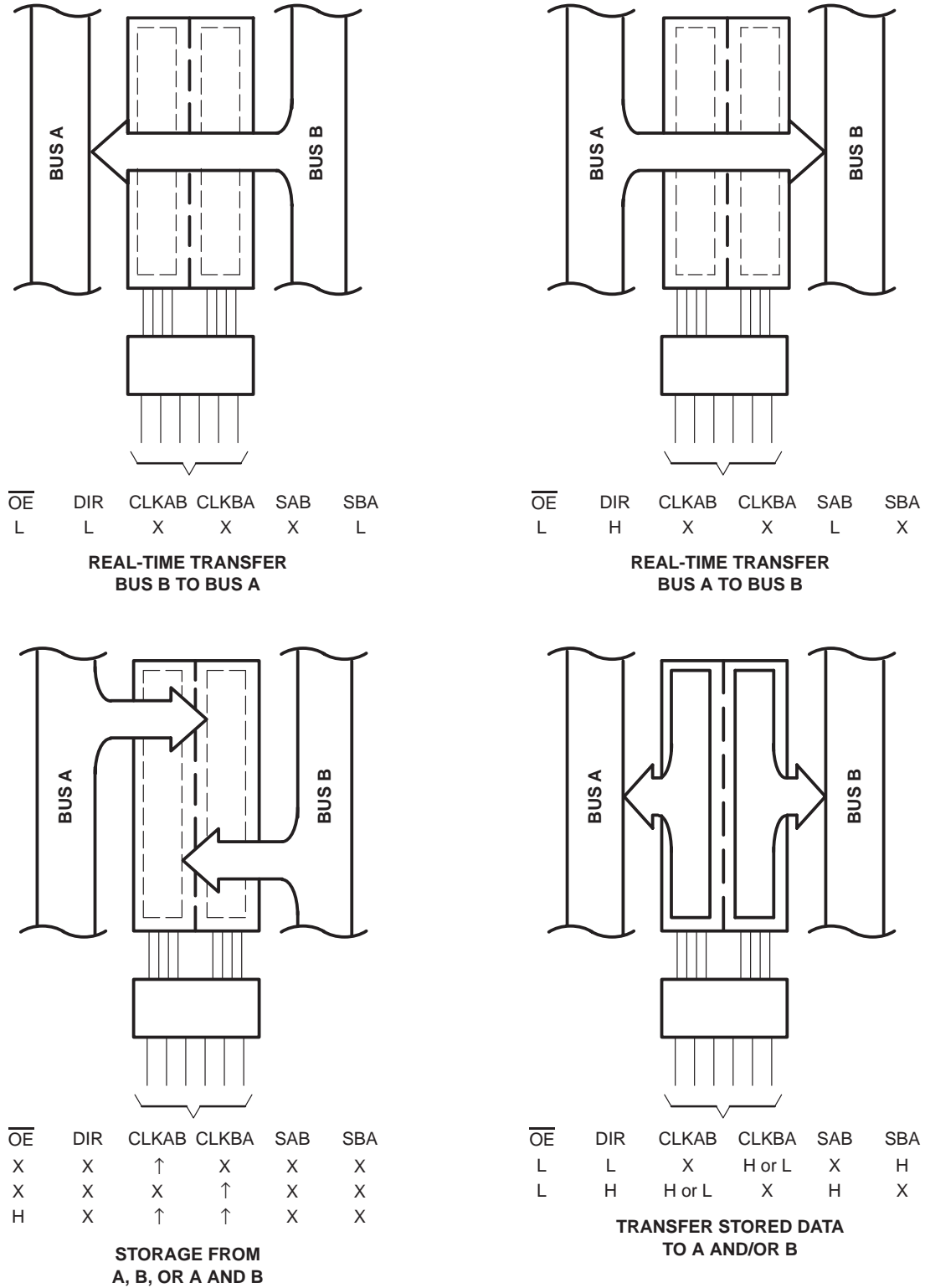
FUNCTION TABLE

INPUTS						DATA I/O		OPERATION OR FUNCTION
$\overline{OE}$	DIR	CLKAB	CLKBA	SAB	SBA	A1-A8	B1-B8	
X	X	↑	X	X	X	Input	Unspecified†	Store A, B unspecified†
X	X	X	↑	X	X	Unspecified†	Input	Store B, A unspecified†
H	X	↑	↑	X	X	Input	Input	Store A and B data
H	X	H or L	H or L	X	X	Input disabled	Input disabled	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
L	H	X	X	L	X	Input	Output	Real-time A data to B Bus
L	H	H or L	X	H	X	Input	Output	Stored A data to bus

† The data-output functions can be enabled or disabled by various signals at  $\overline{OE}$  or DIR. Data-input functions always are enabled, i.e., data at the bus terminals is stored on every low-to-high transition of the clock inputs.

**SN54LVTH16646, SN74LVTH16646**  
**3.3-V ABT 16-BIT BUS TRANSCEIVERS AND REGISTERS**  
**WITH 3-STATE OUTPUTS**

SCBS698G – JULY 1997 – REVISED MAY 2004

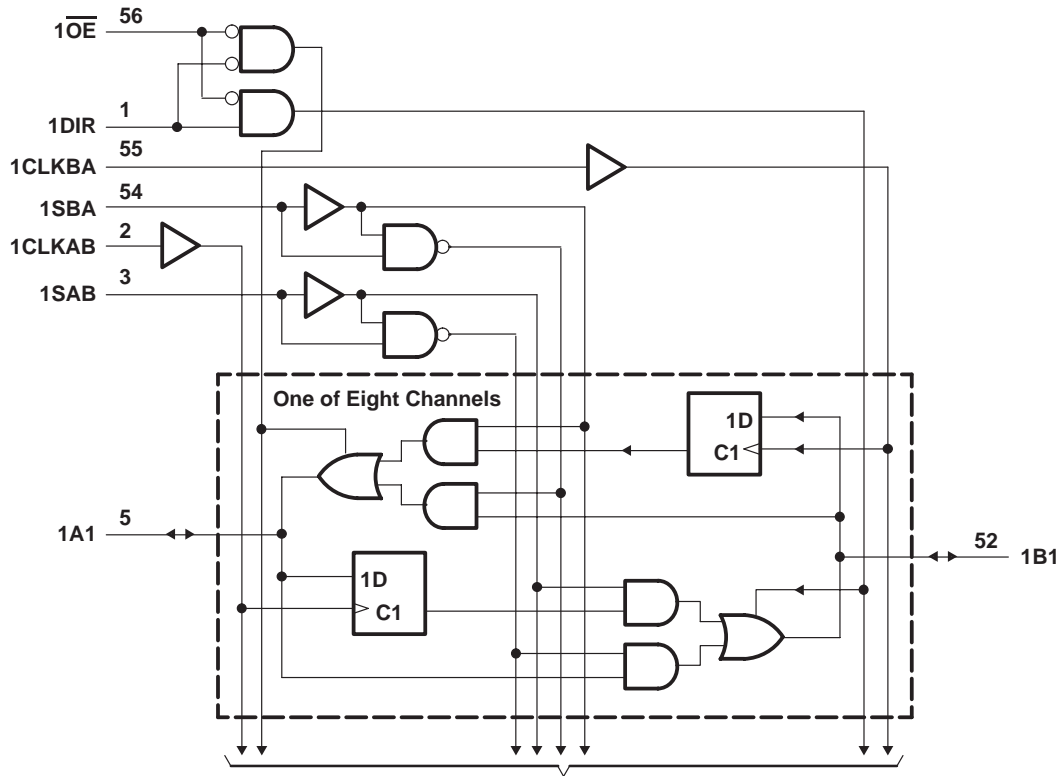


**Figure 1. Bus-Management Functions**

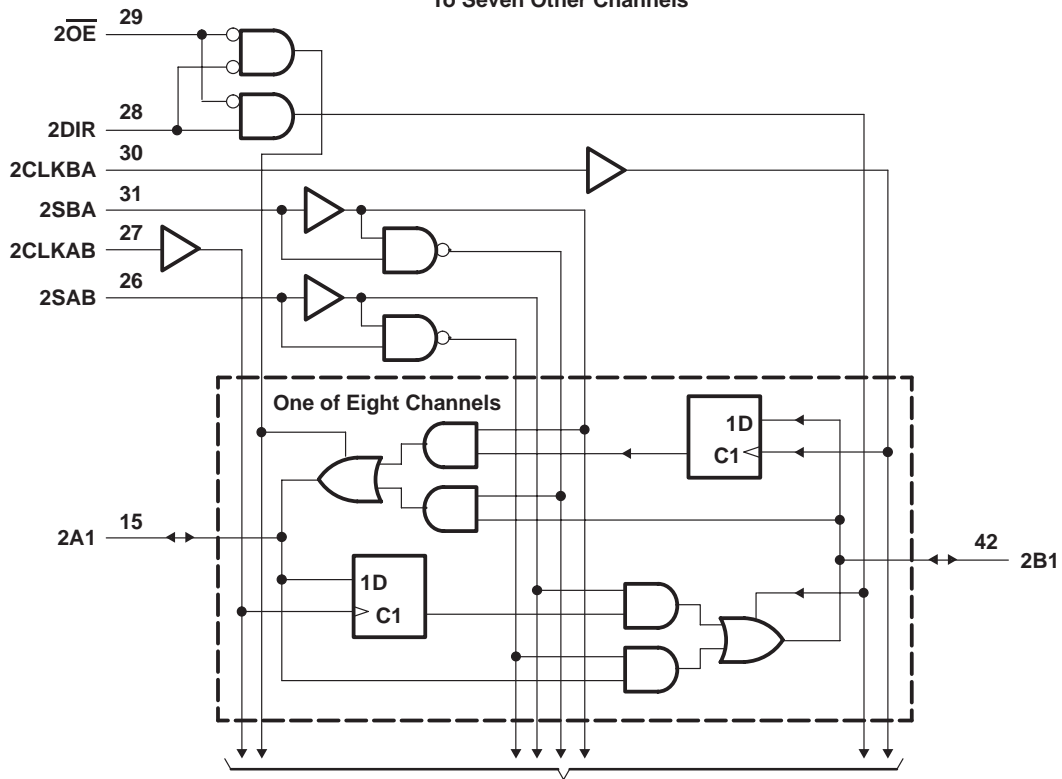
**SN54LVTH16646, SN74LVTH16646**  
**3.3-V ABT 16-BIT BUS TRANSCEIVERS AND REGISTERS**  
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SCBS698G – JULY 1997 – REVISED MAY 2004

**logic diagram (positive logic)**



To Seven Other Channels



To Seven Other Channels



# SN54LVTH16646, SN74LVTH16646 3.3-V ABT 16-BIT BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SCBS698G – JULY 1997 – REVISED MAY 2004

## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ .....	–0.5 V to 4.6 V
Input voltage range, $V_I$ (see Note 1) .....	–0.5 V to 7 V
Voltage range applied to any output in the high-impedance or power-off state, $V_O$ (see Note 1) .....	–0.5 V to 7 V
Voltage range applied to any output in the high state, $V_O$ (see Note 1) .....	–0.5 V to $V_{CC} + 0.5$ V
Current into any output in the low state, $I_O$ : SN54LVTH16646 .....	96 mA
SN74LVTH16646 .....	128 mA
Current into any output in the high state, $I_O$ (see Note 2): SN54LVTH16646 .....	48 mA
SN74LVTH16646 .....	64 mA
Input clamp current, $I_{IK}$ ( $V_I < 0$ ) .....	–50 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ ) .....	–50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 3): DGG package .....	64°C/W
DL package .....	56°C/W
Storage temperature range, $T_{stg}$ .....	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.  
 2. This current flows only when the output is in the high state and  $V_O > V_{CC}$ .  
 3. The package thermal impedance is calculated in accordance with JESD 51–7.

## recommended operating conditions (see Note 4)

		SN54LVTH16646		SN74LVTH16646		UNIT
		MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage	2.7	3.6	2.7	3.6	V
$V_{IH}$	High-level input voltage	2		2		V
$V_{IL}$	Low-level input voltage		0.8		0.8	V
$V_I$	Input voltage		5.5		5.5	V
$I_{OH}$	High-level output current		–24		–32	mA
$I_{OL}$	Low-level output current		48		64	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	Outputs enabled			10	ns/V
$\Delta t/\Delta V_{CC}$	Power-up ramp rate	200		200		μs/V
$T_A$	Operating free-air temperature	–55	125	–40	85	°C

NOTE 4: All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

# SN54LVTH16646, SN74LVTH16646

## 3.3-V ABT 16-BIT BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS

SCBS698G – JULY 1997 – REVISED MAY 2004

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		SN54LVTH16646			SN74LVTH16646			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
$V_{IK}$	$V_{CC} = 2.7\text{ V}$ , $I_I = -18\text{ mA}$		-1.2			-1.2			V
$V_{OH}$	$V_{CC} = 2.7\text{ V to }3.6\text{ V}$ , $I_{OH} = -100\text{ }\mu\text{A}$		$V_{CC}-0.2$			$V_{CC}-0.2$			V
	$V_{CC} = 2.7\text{ V}$ , $I_{OH} = -8\text{ mA}$		2.4			2.4			
	$V_{CC} = 3\text{ V}$	$I_{OH} = -24\text{ mA}$	2						
$I_{OH} = -32\text{ mA}$					2				
$V_{OL}$	$V_{CC} = 2.7\text{ V}$	$I_{OL} = 100\text{ }\mu\text{A}$	0.2			0.2			V
		$I_{OL} = 24\text{ mA}$	0.5			0.5			
	$V_{CC} = 3\text{ V}$	$I_{OL} = 16\text{ mA}$	0.4			0.4			
		$I_{OL} = 32\text{ mA}$	0.5			0.5			
		$I_{OL} = 48\text{ mA}$	0.55						
$I_I$	Control inputs	$V_{CC} = 3.6\text{ V}$ , $V_I = V_{CC}\text{ or GND}$	$\pm 1$			$\pm 1$			$\mu\text{A}$
		$V_{CC} = 0\text{ or }3.6\text{ V}$ , $V_I = 5.5\text{ V}$	10			10			
	A or B ports‡	$V_{CC} = 3.6\text{ V}$ , $V_I = 5.5\text{ V}$	20			20			
		$V_{CC} = 3.6\text{ V}$ , $V_I = 0$	-5			-5			
$I_{off}$	$V_{CC} = 0$ , $V_I\text{ or }V_O = 0\text{ to }4.5\text{ V}$					$\pm 100$			$\mu\text{A}$
$I_{I(\text{hold})}$	A or B ports	$V_{CC} = 3\text{ V}$ , $V_I = 0.8\text{ V}$	75			75			$\mu\text{A}$
		$V_{CC} = 3\text{ V}$ , $V_I = 2\text{ V}$	-75			-75			
	$V_{CC} = 3.6\text{ V}\S$ , $V_I = 0\text{ to }3.6\text{ V}$					$\pm 500$			
$I_{OZPU}$	$V_{CC} = 0\text{ to }1.5\text{ V}$ , $V_O = 0.5\text{ V to }3\text{ V}$ , $OE = \text{don't care}$		$\pm 100^*$			$\pm 100$			$\mu\text{A}$
$I_{OZPD}$	$V_{CC} = 1.5\text{ V to }0$ , $V_O = 0.5\text{ V to }3\text{ V}$ , $OE = \text{don't care}$		$\pm 100^*$			$\pm 100$			$\mu\text{A}$
$I_{CC}$	$V_{CC} = 3.6\text{ V}$ , $I_O = 0$ , $V_I = V_{CC}\text{ or GND}$	Outputs high	0.19			0.19			mA
		Outputs low	5			5			
		Outputs disabled	0.19			0.19			
$\Delta I_{CC}\P$	$V_{CC} = 3\text{ V to }3.6\text{ V}$ , One input at $V_{CC} - 0.6\text{ V}$ , Other inputs at $V_{CC}\text{ or GND}$		0.2			0.2			mA
$C_i$	$V_I = 3\text{ V or }0$		4			4			pF
$C_{io}$	$V_O = 3\text{ V or }0$		10			10			pF

\* On products compliant to MIL-PRF-38535, this parameter is not production tested.

† All typical values are at  $V_{CC} = 3.3\text{ V}$ ,  $T_A = 25^\circ\text{C}$ .

‡ Unused pins at  $V_{CC}$  or GND

§ This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

¶ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than  $V_{CC}$  or GND.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



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SCBS698G – JULY 1997 – REVISED MAY 2004

timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

		SN54LVTH16646				SN74LVTH16646				UNIT
		V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 2.7 V		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency	150		150		150		150		MHz
t <sub>w</sub>	Pulse duration, CLK high or low	3.3		3.3		3.3		3.3		ns
t <sub>su</sub>	Setup time, A or B before CLKAB↑ or CLKBA↑	Data high	1.2	1.5	1.2	1.5	1.2	1.5	ns	
		Data low	2	2.8	2	2.8	2	2.8	ns	
t <sub>h</sub>	Hold time, A or B after CLKAB↑ or CLKBA↑	Data high	0.5	0	0.5	0	0.5	0	ns	
		Data low	0.5	0.5	0.5	0.5	0.5	0.5	ns	

switching characteristics over recommended operating free-air temperature range, C<sub>L</sub> = 50 pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	SN54LVTH16646				SN74LVTH16646				UNIT	
			V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 2.7 V		V <sub>CC</sub> = 3.3 V ± 0.3 V			V <sub>CC</sub> = 2.7 V		
			MIN	MAX	MIN	MAX	MIN	TYP†	MAX	MIN		MAX
f <sub>max</sub>			150		150		150			150	MHz	
t <sub>PLH</sub>	CLKBA or CLKAB	A or B	1.3	4.5	5		1.3	2.8	4.2	4.7		ns
t <sub>PHL</sub>			1.3	4.5	5		1.3	2.8	4.2	4.7		
t <sub>PLH</sub>	A or B	B or A	1	3.6	4.1		1	2.4	3.4	3.9		ns
t <sub>PHL</sub>			1	3.6	4.1		1	2.1	3.4	3.9		
t <sub>PLH</sub>	SBA or SAB‡	A or B	1	4.7	5.6		1	2.8	4.5	5.4		ns
t <sub>PHL</sub>			1	4.7	5.6		1	3	4.5	5.4		
t <sub>PZH</sub>	$\overline{\text{OE}}$	A or B	1	4.5	5.4		1	2.5	4.3	5.2		ns
t <sub>PZL</sub>			1	4.5	5.4		1	2.6	4.3	5.2		
t <sub>PHZ</sub>	$\overline{\text{OE}}$	A or B	2	5.8	6.3		2	4	5.6	6.1		ns
t <sub>PLZ</sub>			2	5.6	6.3		2	3.6	5.4	6.1		
t <sub>PZH</sub>	DIR	A or B	1	4.6	5.5		1	3	4.4	5.3		ns
t <sub>PZL</sub>			1	4.6	5.5		1	3	4.4	5.3		
t <sub>PHZ</sub>	DIR	A or B	1.5	6	7.1		1.5	3.9	5.7	6.8		ns
t <sub>PLZ</sub>			1.5	5.5	6		1.5	3.6	5.2	5.7		

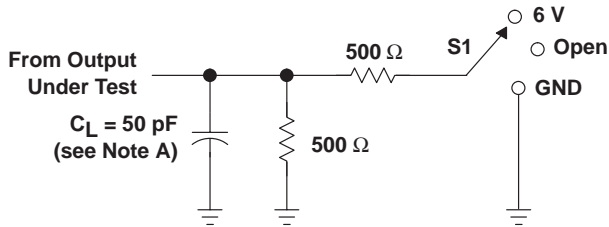
† All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

‡ These parameters are measured with the internal output state of the storage register opposite that of the bus input.

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**WITH 3-STATE OUTPUTS**

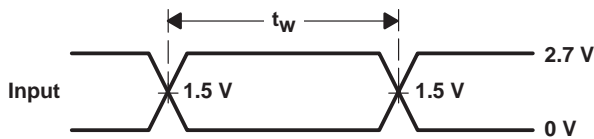
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**PARAMETER MEASUREMENT INFORMATION**

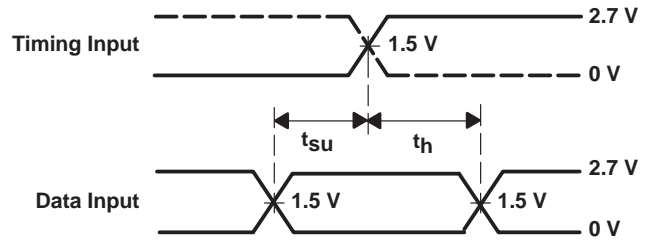


**LOAD CIRCUIT**

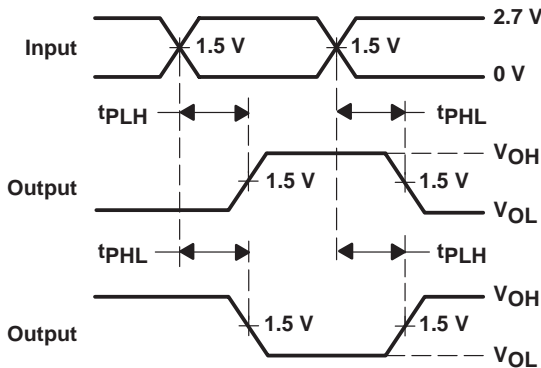
TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	6 V
$t_{PHZ}/t_{PZH}$	GND



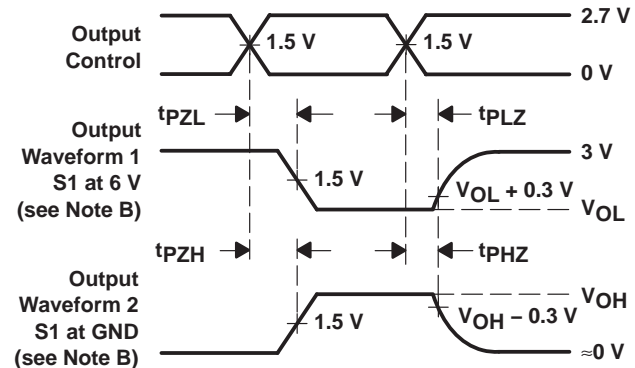
**VOLTAGE WAVEFORMS**  
**PULSE DURATION**



**VOLTAGE WAVEFORMS**  
**SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS**  
**PROPAGATION DELAY TIMES**  
**INVERTING AND NONINVERTING OUTPUTS**



**VOLTAGE WAVEFORMS**  
**ENABLE AND DISABLE TIMES**  
**LOW- AND HIGH-LEVEL ENABLING**

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .  
 D. The outputs are measured one at a time, with one transition per measurement.  
 E. All parameters and waveforms are not applicable to all devices.

**Figure 2. Load Circuit and Voltage Waveforms**



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVTH16646DGGR	ACTIVE	TSSOP	DGG	56	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH16646	<a href="#">Samples</a>
SN74LVTH16646DL	ACTIVE	SSOP	DL	56	20	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH16646	<a href="#">Samples</a>
SN74LVTH16646DLR	ACTIVE	SSOP	DL	56	1000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	LVTH16646	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVTH16646DGGR	TSSOP	DGG	56	2000	330.0	24.4	8.9	14.7	1.4	12.0	24.0	Q1
SN74LVTH16646DLR	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVTH16646DGGR	TSSOP	DGG	56	2000	367.0	367.0	45.0
SN74LVTH16646DLR	SSOP	DL	56	1000	367.0	367.0	55.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74LVTH16646DL	DL	SSOP	56	20	473.7	14.24	5110	7.87

# MECHANICAL DATA

DL (R-PDSO-G56)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MO-118

PowerPAD is a trademark of Texas Instruments.



4222167/A 07/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

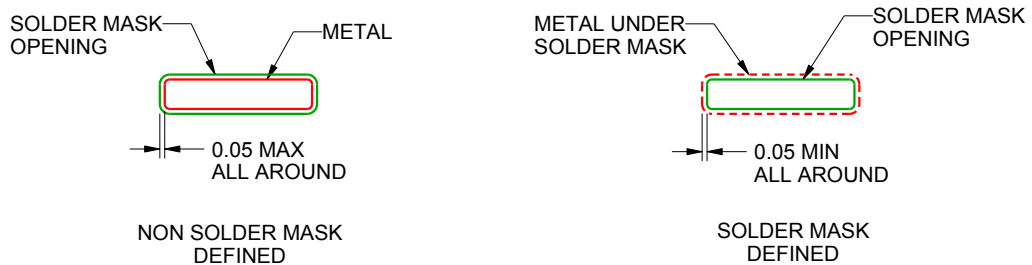
DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4222167/A 07/2015

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



# EXAMPLE STENCIL DESIGN

DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4222167/A 07/2015

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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