SN75ALS192 四路差分线路驱动器

1 特性

- 符合或超出 ANSI 标准 EIA/TIA-422-B 和 ITU 建议 V.11 的要求
- 设计在高达 20Mbaud 的速率下运行
- 与三态 TTL 兼容
- 由 5V 单电源供电运行
- 在断电情况下具有高输出阻抗
- 互补输出使能输入
- 经改进可替代 AM26LS31

2 应用

- 工厂自动化
- ATM 和点钞机
- 智能电网
- 交流和伺服 电机驱动器

3 说明

这些四路差分线路驱动器设计用于双绞线或并行线传输线路上的数据传输。它们符合 ANSI 标准 EIA/TIA-422-B 和 ITU 建议 V.11 的要求，并与三态 TTL 电路兼容。先进的低功耗肖特基技术可提供高速度，但不会导致常见的功率损耗。待机电源电流通常仅为 26mA，而传播延迟时间的典型值小于 10ns。

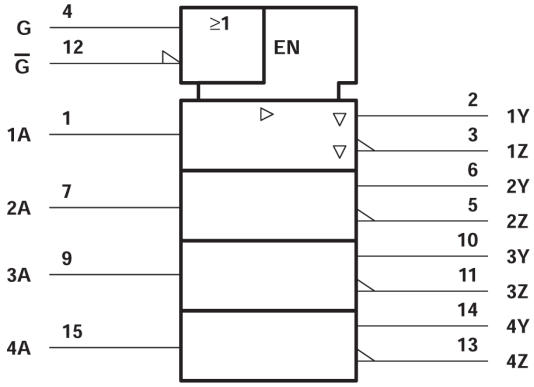
高阻抗输入可保持低输入电流：高电平时小于 μA，低电平时小于 100μA。互补输出使能输入（G 和 $\overline{G}$）允许这些器件在高输入电平或低输入电平下启用。SN75ALS192 支持超过 20Mbit/s 的数据速率，旨在与 SN75ALS193 四路线路接收器配合使用。

SN75ALS192 的工作温度范围是 0°C 至 70°C。

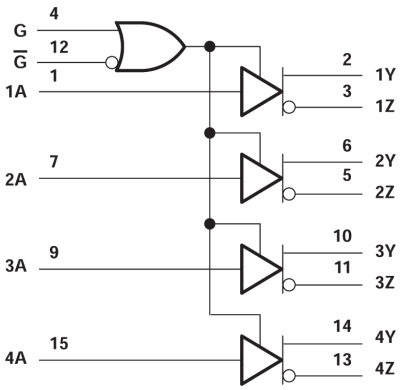
封装信息

器件型号	封装(1)	封装尺寸(2)
SN75ALS192	SOIC（D，16）	9.9mm × 6mm
	SO（NS，16）	10.2mm × 7.8mm

(1) 有关更多信息，请参阅节 10。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。



逻辑符号†



逻辑图（正逻辑）

† 此符号符合 ANSI/IEEE 标准 91-1984 和 IEC 出版物 617-12。

Table of Contents

† Operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied.

4 Pin Configuration and Functions

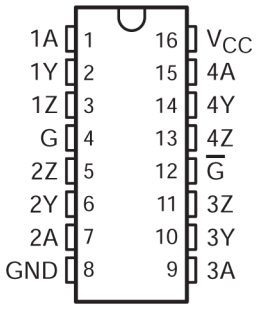


图 4-1. D or NS Package (Top View)

表 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
1A	1	I	Single Ended Data Input for Channel 1
1Y	2	O	Non-Inverting Output for Differential Driver on Channel 1
1Z	3	O	Inverting Output of Differential Driver on Channel 1
G	4	I	Active High Enable Input (OR'd with $\overline{G}$)
2Z	5	O	Inverting Output of Differential Driver on Channel 2
2Y	6	O	Non-Inverting Output for Differential Driver on Channel 2
2A	7	I	Single Ended Data Input for Channel 2
GND	8	GND	Device Ground
3A	9	I	Single Ended Data Input for Channel 3
3Y	10	O	Non-Inverting Output for Differential Driver on Channel 3
3Z	11	O	Inverting Output of Differential Driver on Channel 3
$\overline{G}$	12	I	Active Low Enable Input (OR'd with G)
4Z	13	O	Inverting Output of Differential Driver on Channel 4
4Y	14	O	Non-Inverting Output for Differential Driver on Channel 4
4A	15	I	Single Ended Data Input for Channel 4
V_{CC}	16	P	5V Power Supply Positive Terminal Connection

(1) Signal Types: I = Input, O = Output, I/O = Input or Output, P = Power, GND = Ground.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage (see Note (2))		7	V
V_I	Input voltage		7	V
	Off-state output voltage		6	V
	Continuous total dissipation	See Dissipation Rating Table		
T_{stg}	Storage temperature range	– 65	150	°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values except differential output voltage, $V_{OD,}$ are with respect to network ground terminal.

5.2 Dissipation Rating Table

PACKAGE	$T_A \leqslant$ 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A= 125°C POWER RATING
D	950 mW	7.6 mW/°C	608 mW	N/A
N	1150 mW	9.2 mW/°C	736 mW	N/A

5.3 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
High-level output current, I_{OH}			– 20	mA
Low-level output current, I_{OL}			20	mA
Operating free-air temperature, T_A	0		70	°C

5.4 Thermal Information

THERMAL METRIC(1)		D (SOIC)	NS (SOP)	UNIT
		16-PINS		
$R_{\theta JA}$	Junction-to-ambient thermal resistance	84.6	88.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	43.5	46.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	43.	50.	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.4	13.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	42.8	50.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS(1)		MIN	TYP(2)	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = –18mA			–1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN,	I_{OH} = –20mA	2.5			V
V_{OL}	Low-level output voltage	V_{CC} = MIN,	I_{OL} = 20mA			0.5	V
V_O	Output voltage	V_{CC} = MAX,	I_O = 0	0	6		V
$\|V_{OD1}\|$	Differential output voltage	V_{CC} = MIN,	I_O = 0	1.5	6		V
$\|V_{OD2}\|$	Differential output voltage	R_L = 100Ω,	See 图 6-1	1/2 V_{OD1} or 2(3)			V
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage(4)	R_L = 100Ω,	See 图 6-1			±0.2	V
V_{OC}	Common-mode output voltage(5)	R_L = 100Ω,	See 图 6-1			±3	V
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage(4)	R_L = 100Ω,	See 图 6-1			±0.2	V
I_O	Output current with power off	V_{CC} = 0	V_O = 6V			100	
			V_O = –0.25V			–100	µA
I_{OZ}	Off state (high impedance state) output current	V_{CC} = MAX	V_O = 0.5V			–20	
			V_O = 2.5V			20	µA
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 7V			100	µA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7V			20	µA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4V			–200	µA
I_{OS}	Short-circuit output current(6)	V_{CC} = MAX		–30	–150	mA	
I_{CC}	Supply current (all drivers)	V_{CC} = MAX,	All outputs disabled		26	45	mA

(1) For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
(2) All typical values are at V_{CC} = 5 V and T_A = 25°C.
(3) The minimum V_{OD2} with a 100-Ω load is either 1/2 V_{OD1} or 2 V, whichever is greater.
(4) $|V_{OD}|$ and $|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
(5) In ANSI Standard EIA/TIA-422-B, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.
(6) Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

5.6 Switching Characteristics

V_{CC} = 5 V, T_A = 25°C (see 图 6-2)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	S1 and S2 open,	C_L = 30 pF		6	13	ns
t_{PHL}	Propagation delay time, high-to-low-level output	S1 and S2 open,	C_L = 30 pF		9	14	ns
	Output-to-output skew	S1 and S2 open,	C_L = 30 pF		3	6	ns
t_{PZH}	Output enable time to high level	S1 open and S2 closed			11	15	ns
t_{PZL}	Output enable time to low level	S1 closed and S2 open			16	20	ns
t_{PHZ}	Output disable time from high level	S1 open and S2 closed,	C_L = 10 pF		8	15	ns
t_{PLZ}	Output disable time from low level	S1 and S2 closed,	C_L = 10 pF		18	20	ns

5.7 Typical Characteristics†

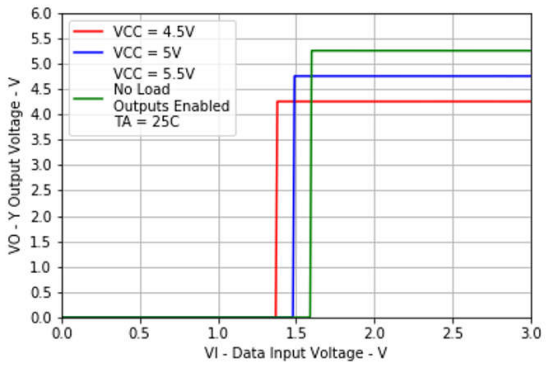


图 5-1. Y Output Voltage vs Data Input Voltage

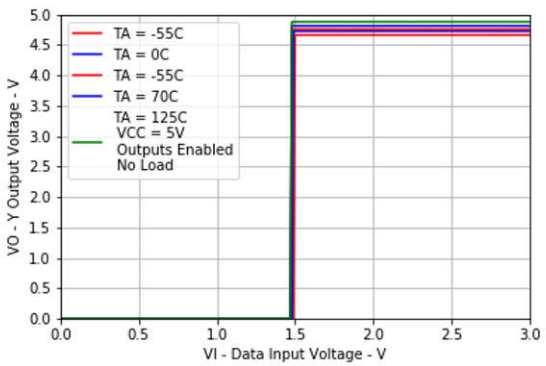
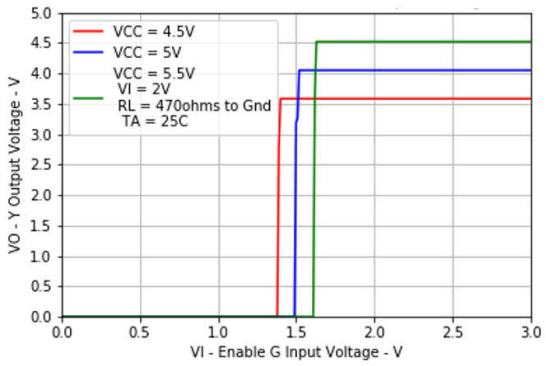
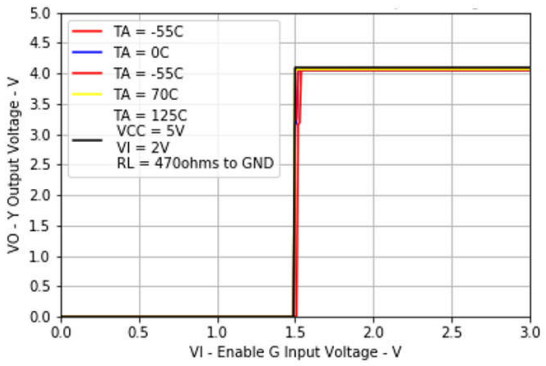


图 5-2. Y Output Voltage vs Data Input Voltage



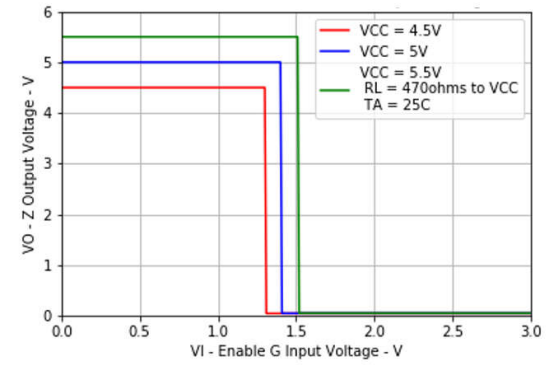
The A input is connected to V_{CC} during the testing of the Y outputs and to ground during the testing of the Z outputs.

图 5-3. Y Output Voltage vs Enable G Input Voltage



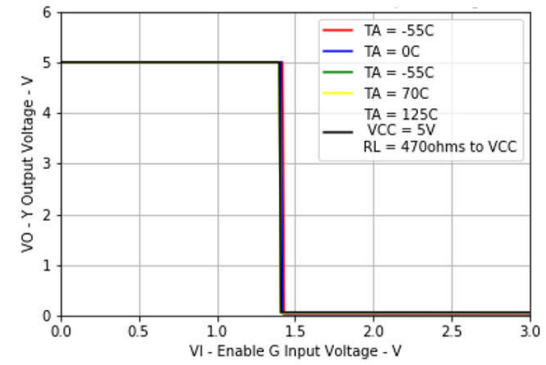
The A input is connected to V_{CC} during the testing of the Y outputs and to ground during the testing of the Z outputs.

图 5-4. Y Output Voltage vs Enable G Input Voltage



The A input is connected to V_{CC} during the testing of the Y outputs and to ground during the testing of the Z outputs.

图 5-5. Z Output Voltage vs Enable G Input Voltage

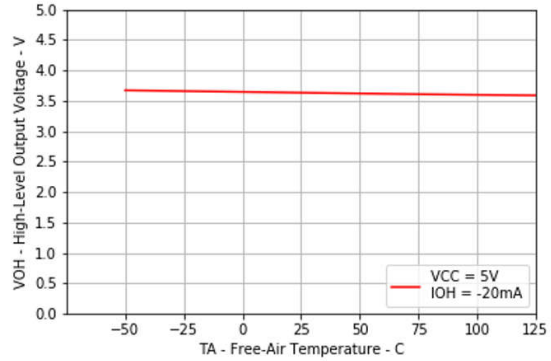


The A input is connected to GND during the testing of the Y outputs and to V_{CC} during the testing of the Z outputs.

图 5-6. Z Output Voltage vs Enable G Input Voltage

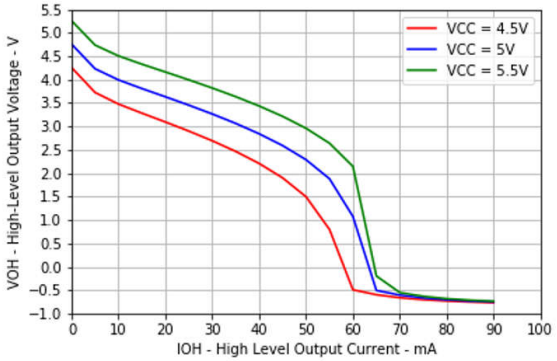
† Operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied.

5.7 Typical Characteristics† (continued)



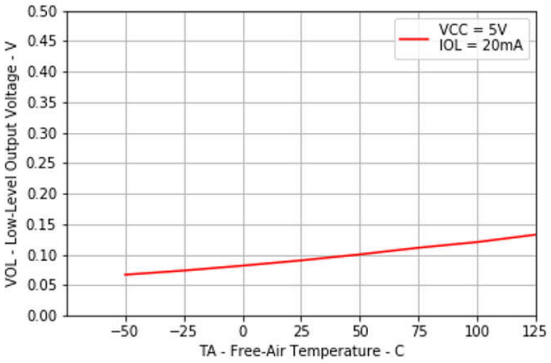
The A input is connected to V_{CC} during the testing of the Y outputs and to ground during the testing of the Z outputs.

图 5-7. High-level Output Voltage vs Free-air Temperature



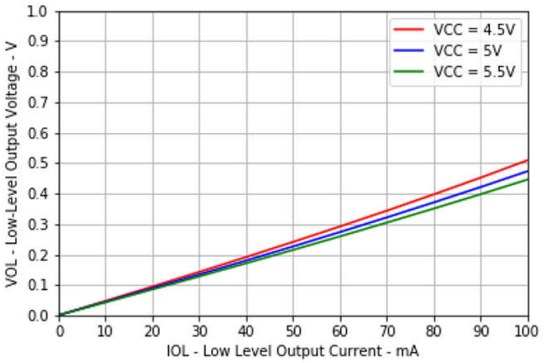
The A input is connected to V_{CC} during the testing of the Y outputs and to ground during the testing of the Z outputs.

图 5-8. High-level Output Voltage vs Output Current



The A input is connected to GND during the testing of the Y outputs and to V_{CC} during the testing of the Z outputs.

图 5-9. Low-level Output Voltage vs Free-air Temperature



The A input is connected to GND during the testing of the Y outputs and to V_{CC} during the testing of the Z outputs.

图 5-10. Low-level Output Voltage vs Low-level Output Current

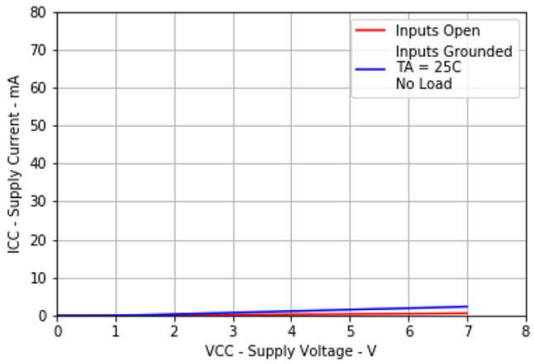


图 5-11. Supply Current vs Supply Voltage

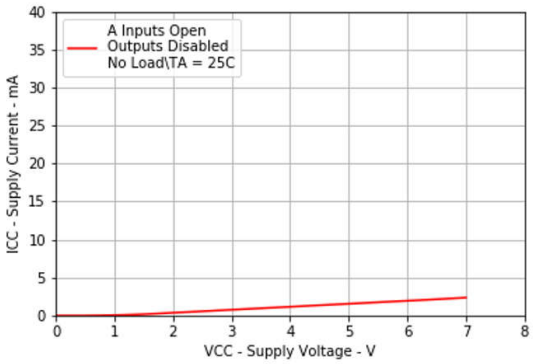


图 5-12. Supply Current vs Supply Voltage

† Operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied.

5.7 Typical Characteristics† (continued)

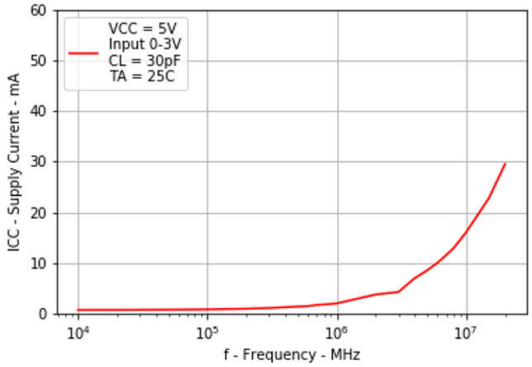


图 5-13. Supply Current vs Frequency

† Operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied.

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† Operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied.

6 Parameter Measurement Information

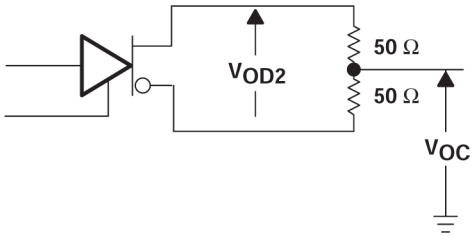
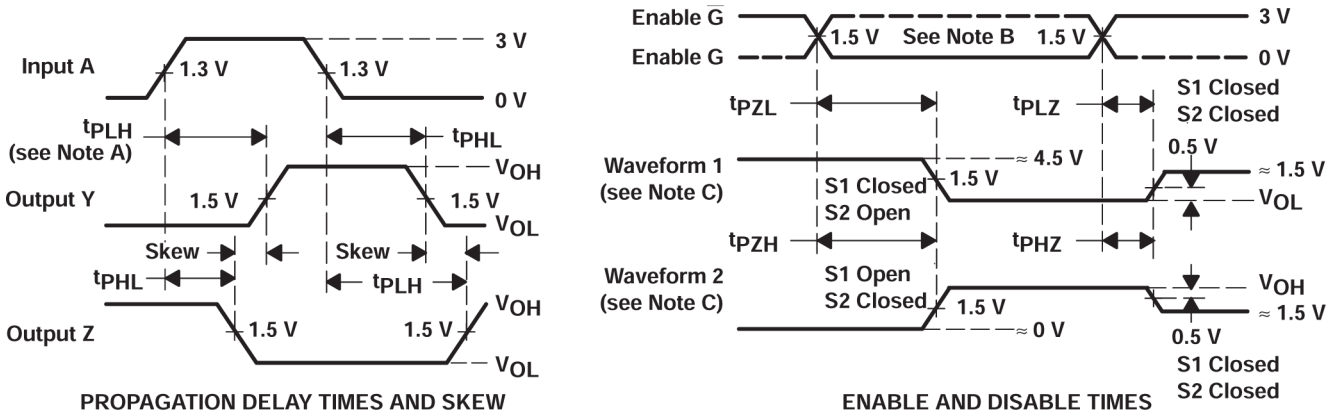
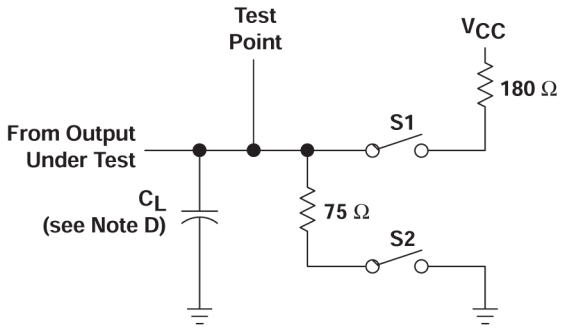


图 6-1. Differential and Common-Mode Output Voltages





A. When measuring propagation delay times and skew, switches S1 and S2 are open.
B. Each enable is tested separately.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. C_L includes probe and jig capacitance.
E. All input pulses are supplied by generators having the following characteristics: PRR ⩽ 1 MHz, Z_O ≈ 50 Ω, t_r ⩽ 15 ns, and t_f ⩽ 6 ns.

图 6-2. Test Circuit and Voltage Waveforms

7 Device Functional Modes

表 7-1. Function Table (Each Driver)

INPUT(1)	ENABLES		OUTPUTS	
A	G	$\overline{G}$	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off)

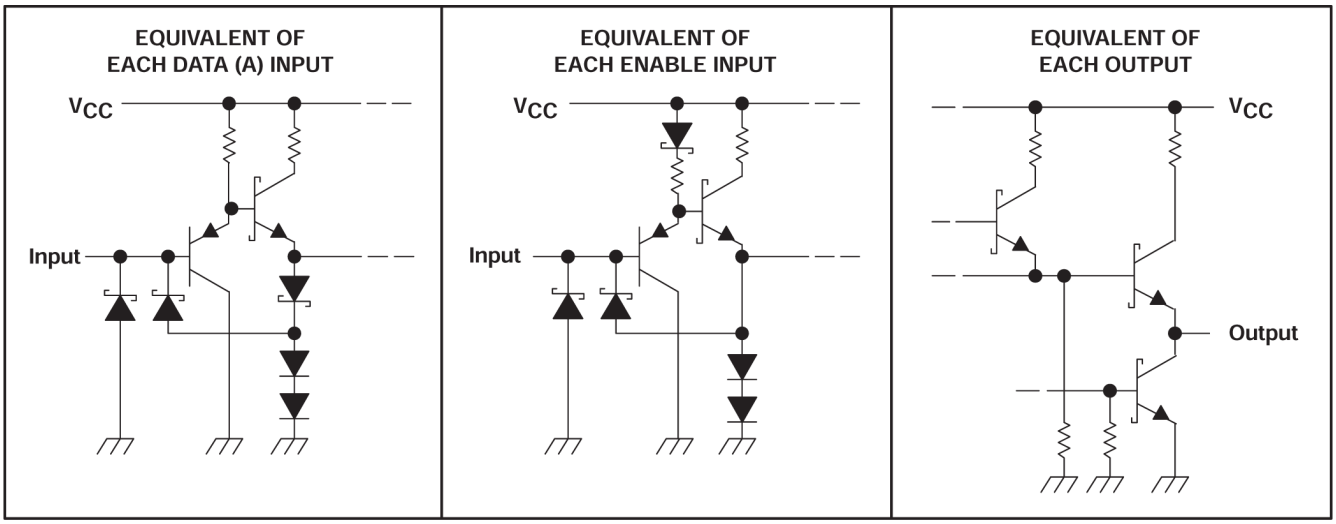


图 7-1. Schematics of Inputs and Outputs

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

8.2 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

8.3 商标

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

8.4 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.5 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

9 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision D (April 1998) to Revision E (March 2024)	Page
• 更改了整个文档中的表格、图和交叉参考的编号格式	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN75ALS192D	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	0 to 70	75ALS192	
SN75ALS192DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS192	Samples
SN75ALS192N	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN75ALS192N	Samples
SN75ALS192NE4	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN75ALS192N	Samples
SN75ALS192NSR	ACTIVE	SO	NS	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75ALS192	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

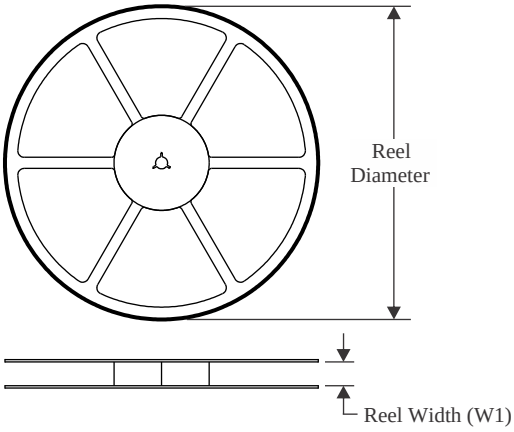
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

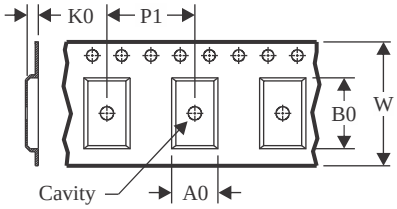
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

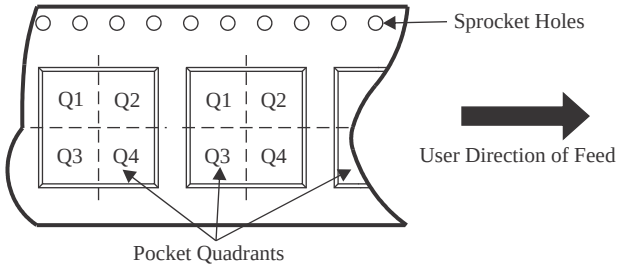


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

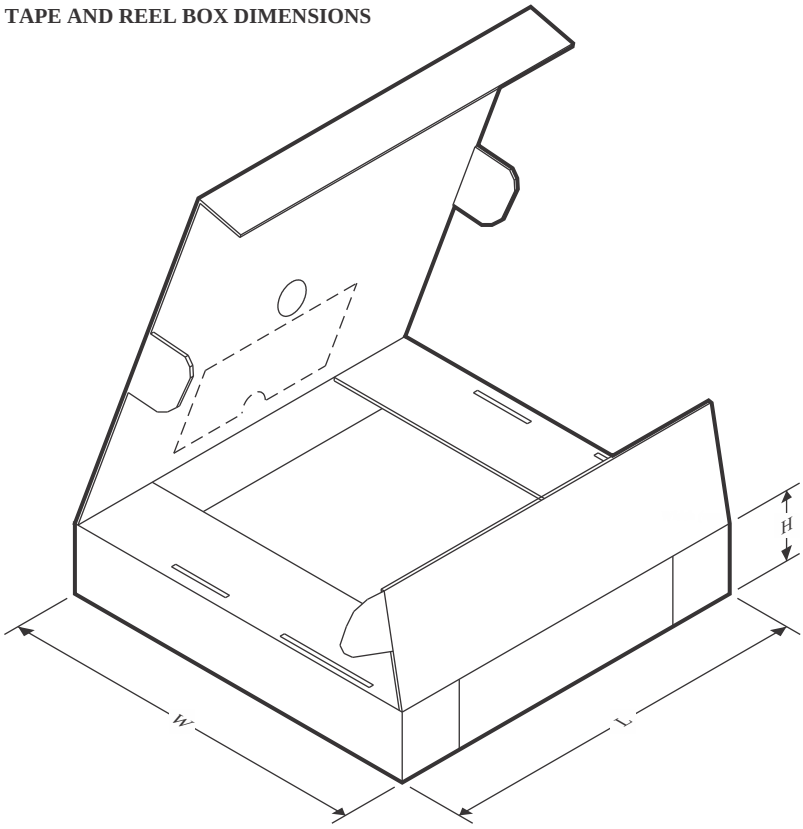
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN75ALS192DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN75ALS192DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN75ALS192NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN75ALS192NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

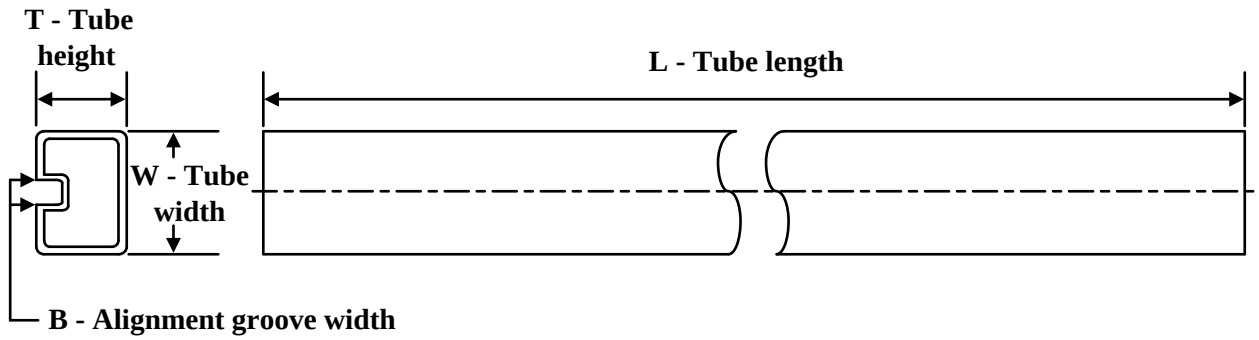
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN75ALS192DR	SOIC	D	16	2500	340.5	336.1	32.0
SN75ALS192DR	SOIC	D	16	2500	353.0	353.0	32.0
SN75ALS192NSR	SO	NS	16	2000	353.0	353.0	32.0
SN75ALS192NSR	SO	NS	16	2000	356.0	356.0	35.0

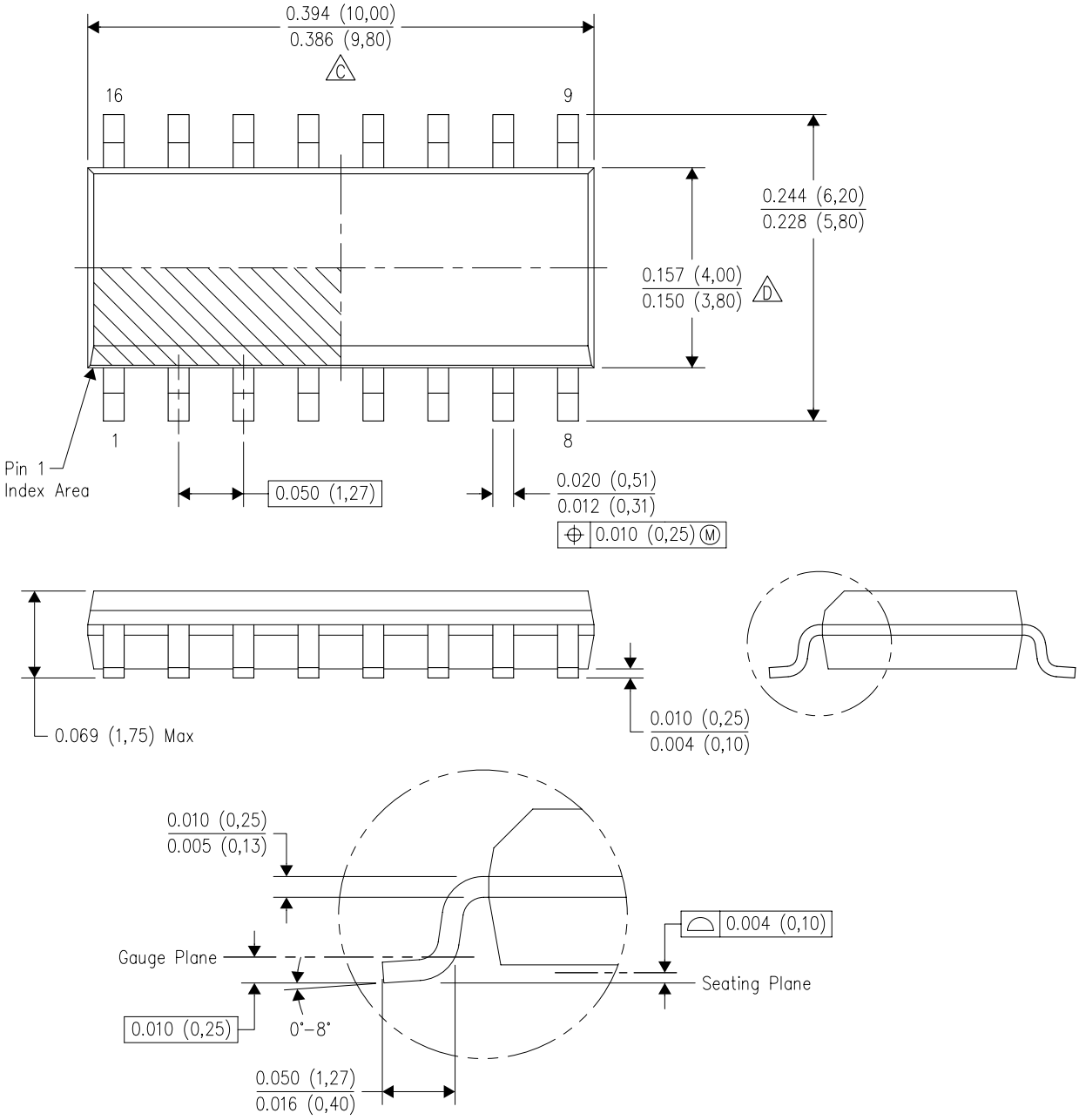
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN75ALS192N	N	PDIP	16	25	506	13.97	11230	4.32
SN75ALS192NE4	N	PDIP	16	25	506	13.97	11230	4.32

D (R–PDSO–G16) PLASTIC SMALL OUTLINE

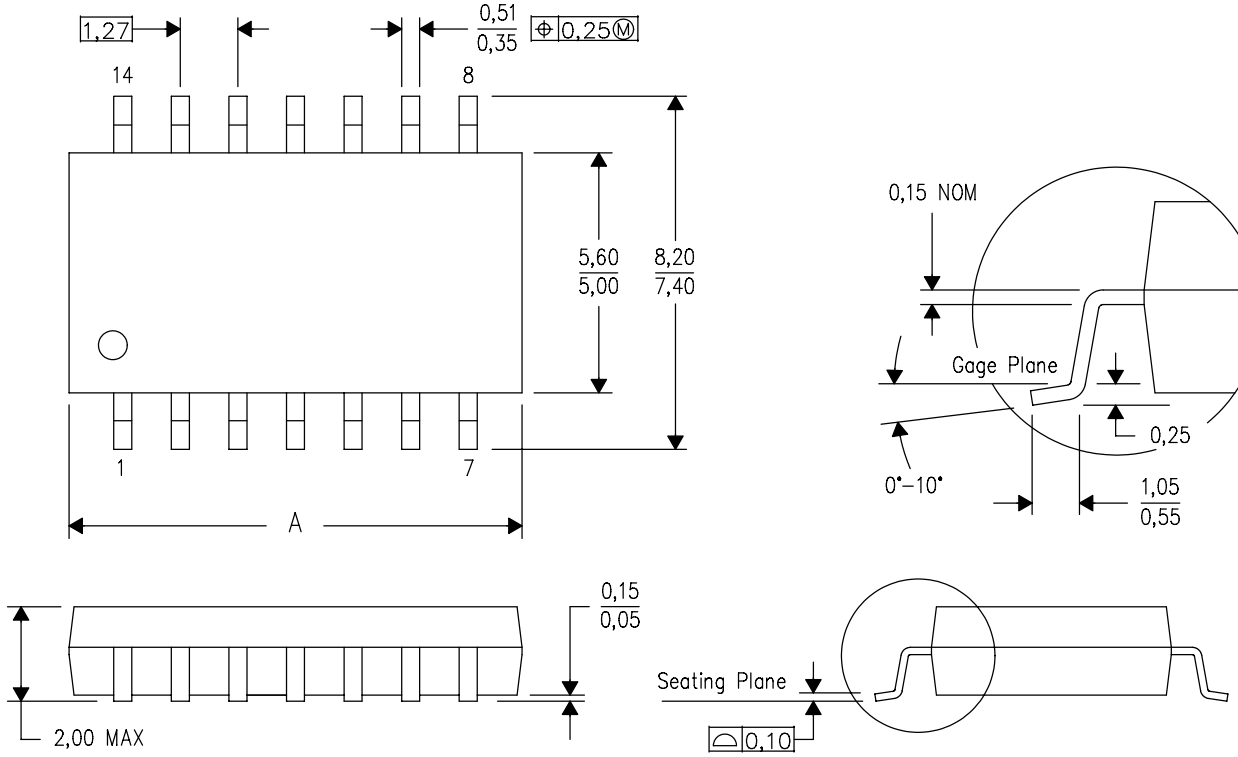


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

MECHANICAL DATA

NS (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

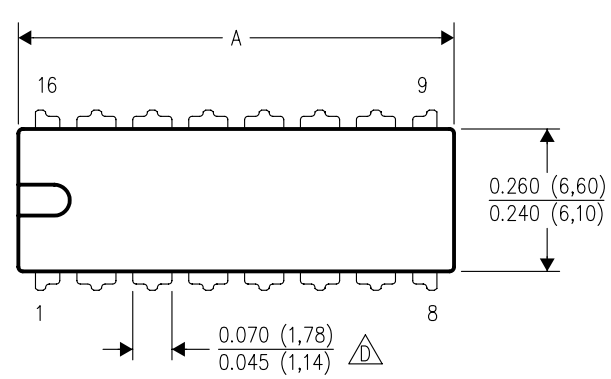
4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

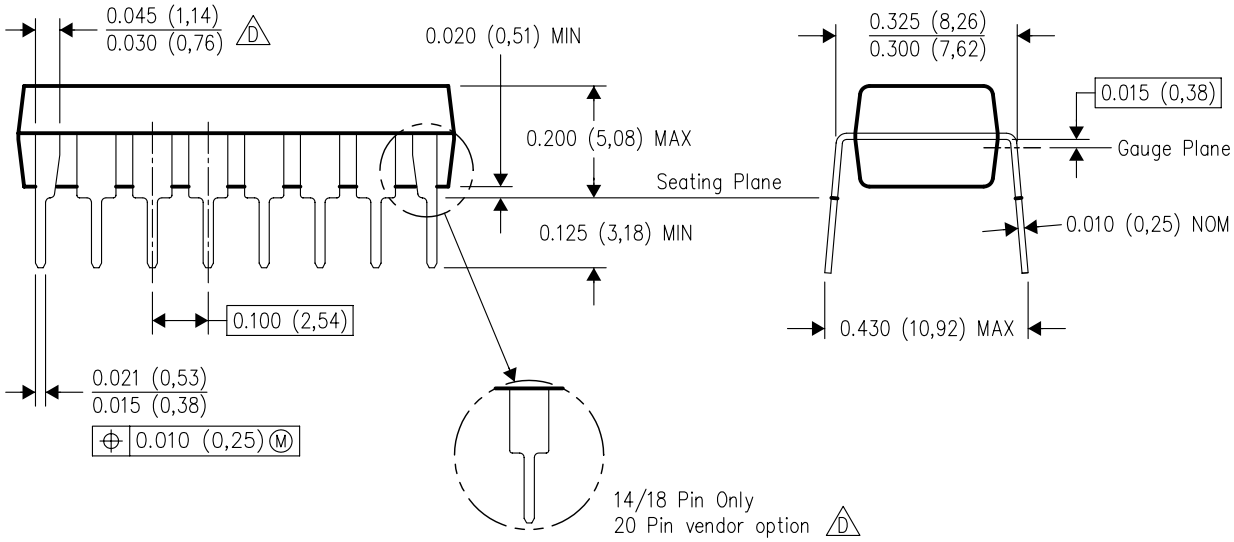
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN

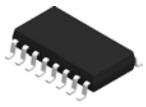


DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

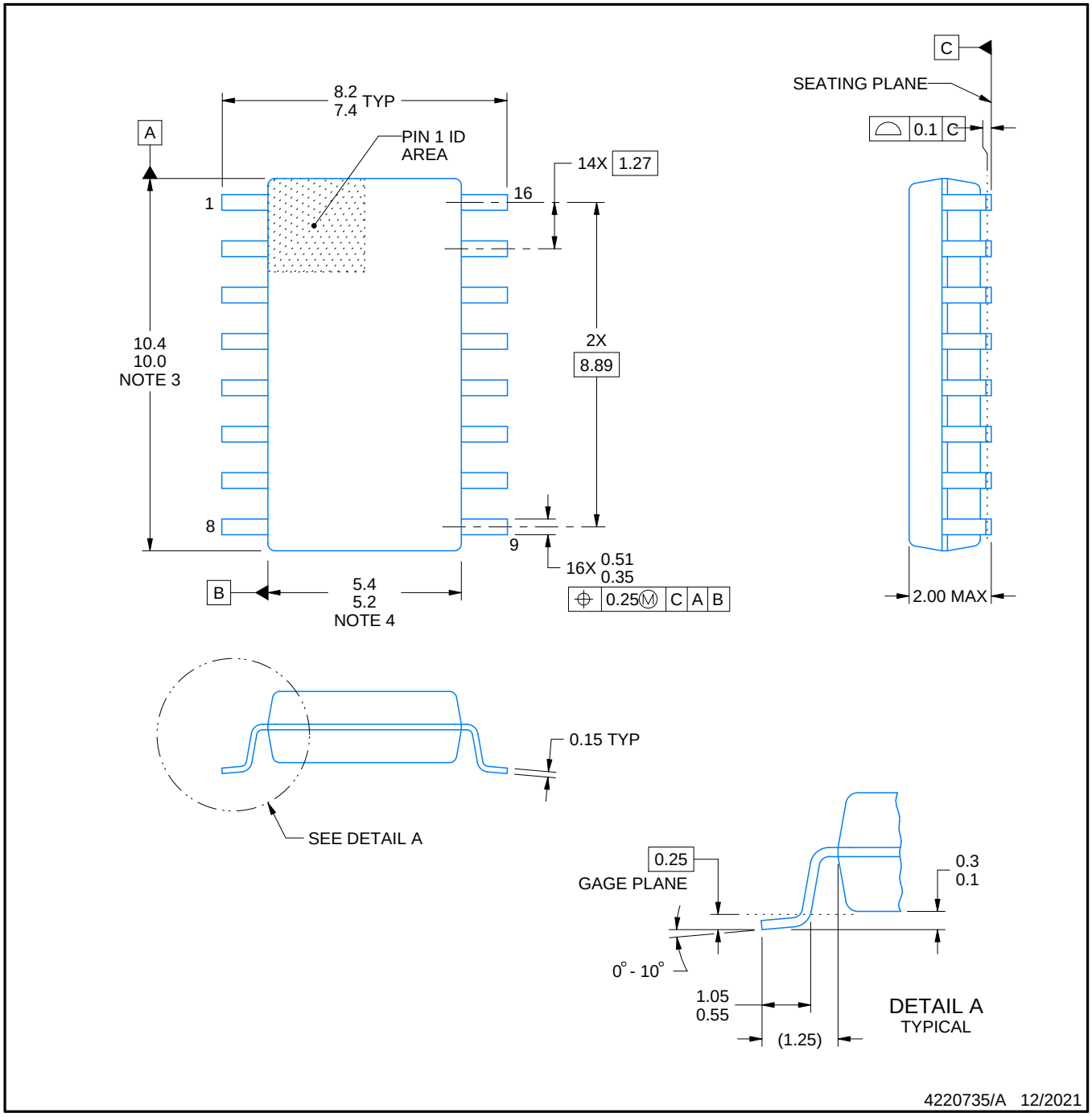


PACKAGE OUTLINE

NS0016A

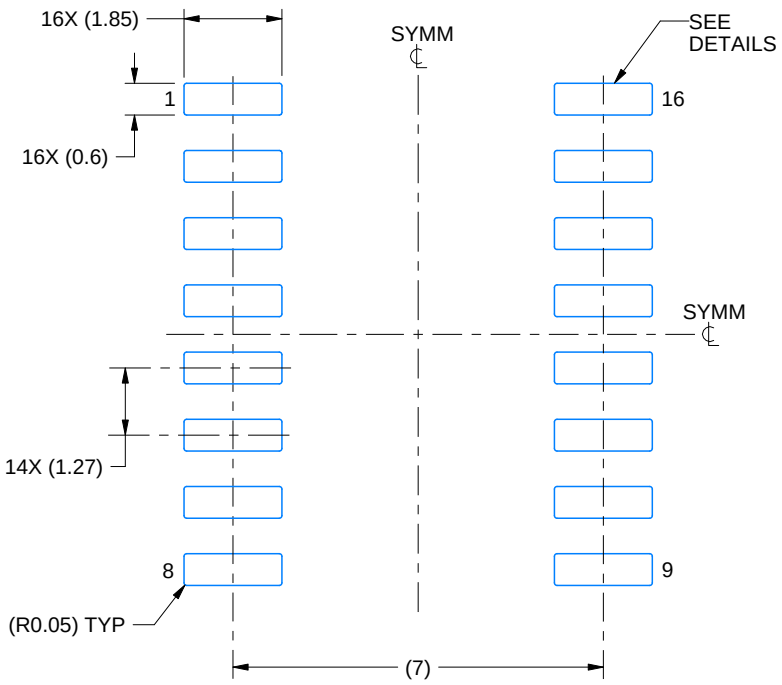
SOP - 2.00 mm max height

SOP

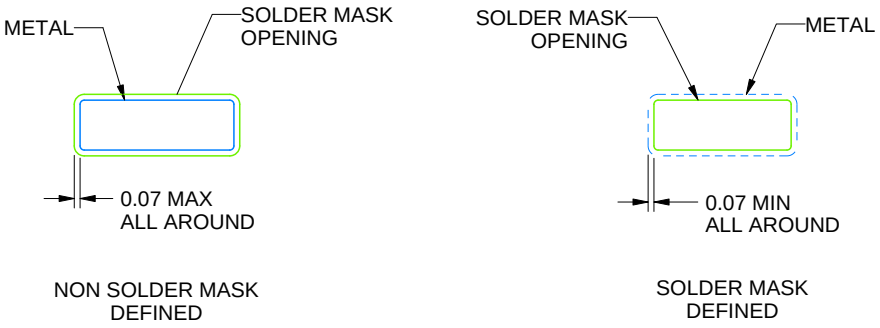


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
SCALE:7X



NON SOLDER MASK
DEFINED

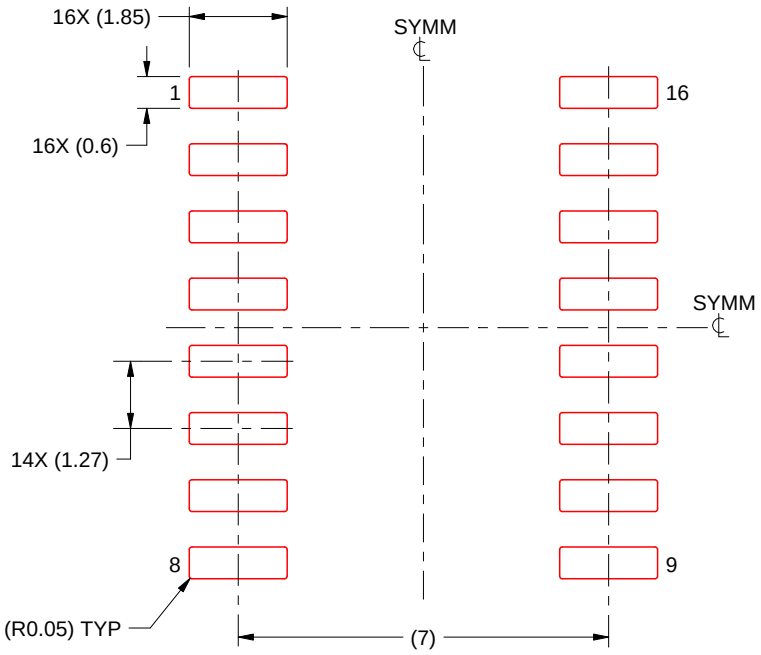
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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