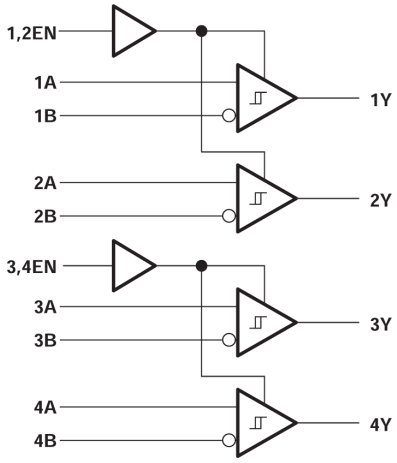
SN65LBC175A、SN75LBC175A 四通道 RS-485 差分线路接收器

1 特性

- 专为 TIA/EIA-485、TIA/EIA-422 和 ISO 8482 应用而设计
- 信号传输速率超过 50Mbps
- 在总线短路、开路和空闲总线情况下提供失效防护
- 为总线输入提供 6kV 的 ESD 保护
- 共模总线电压输入范围：-7V 至 12V
- 传播延迟时间 < 16ns
- 低待机功耗 < 20µA
- 针对 MC3486、DS96F175、LTC489 和 SN75175 进行引脚兼容升级

2 应用

- 工厂自动化
- ATM 和点钞机
- 智能电网
- 交流和伺服电机驱动器



逻辑图 [1]

3 说明

SN65LBC175A 和 SN75LBC175A 是具有三态输出的四通道差分线路接收器，专为 TIA/EIA-485 (RS-485)、TIA/EIA-422 (RS-422) 和 ISO 8482 (Euro RS-485) 应用而设计。

当数据速率高达甚至超过每秒 5000 万位时，该器件针对均衡后的多点总线通信进行了优化。传输介质可采用双绞线电缆、印刷电路板走线或背板。最终数据传输速率和距离取决于介质衰减特性和环境噪声耦合。

每个接收器都可在较宽的正负共模输入电压范围内运行，并具有高达 6kV 的 ESD 保护，使其适用于恶劣环境中的高速多点数据传输应用。这些器件采用 LinBiCMOS™ 进行设计，有助于实现低功耗和固有的稳健性。

两个 EN 输入可实现成对的使能控制，也可在外部将二者连接在一起，用相同的信号使能全部四个驱动器。

SN75LBC175A 可在 0°C 至 70°C 的工作温度范围内运行。SN65LBC175A 可在 -40°C 至 85°C 的温度范围内运行。

封装信息

器件型号	封装(1)	封装尺寸(2)
SN65LBC175A SN75LBC175A	SOIC（D，16）	9.9mm x 6mm
	PDIP（N，16）	19.3mm x 9.4mm

(1) 有关详细信息，请参阅 节 11。
(2) 封装尺寸（长 x 宽）为标称值，并包括引脚（如适用）。

[1] 线路的信号传输速率是每秒进行电压转换的次数，以单位 bps（每秒位数）来表示。

Table of Contents

4 Pin Configuration and Functions

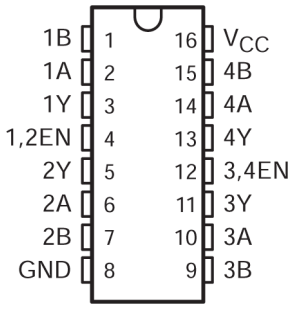


图 4-1. SN65LBC175A (Marked as 65LBC175A)
SN75LBC175A (Marked as 75LBC175A)
D or N Package (Top View)

表 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
1B	1	I	Channel 1 Inverting Differential Input
1A	2	I	Channel 1 Non-Inverting Differential Input
1Y	3	O	Channel 1 Output
1,2 EN	4	I	Channel 1 and 2 Active High Enable
2Y	5	O	Channel 2 Output
2A	6	I	Channel 2 Non-Inverting Differential Input
2B	7	I	Channel 2 Inverting Differential Input
GND	8	GND	Device Ground
3B	9	I	Channel 3 Inverting Differential Input
3A	10	I	Channel 3 Non-Inverting Differential Input
3Y	11	O	Channel 3 Output
3,4 EN	12	I	Channel 3 and 4 Active High Enable
4Y	13	O	Channel 4 Output
4A	14	I	Channel 4 Non-Inverting Differential Input
4B	15	I	Channel 4 Inverting Differential Input
V_{CC}	16	POW	Device Supply

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC} (see (2))	Supply voltage range		−0.3	6	V
	Voltage range at any bus input (steady state)	A and B	−10	15	V
	Voltage range at any bus input	transient pulse through 100 Ω, see 图 6-5	−30	30	V
V_I	Voltage input range at 1,2EN and 3,4EN		−0.5	V_{CC} + 0.5	V
I_O	Receiver output current		±10	mA	
	Electrostatic discharge:				
	Continuous power dissipation		See Power Dissipation Rating Table		

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to GND, and are steady-state (unless otherwise specified).

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	A and B to GND	±6000	V
			All pins	±5000	
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	All pins	±2000	

(1) Tested in accordance with JEDEC Standard 22, Test Method A114-A.
(2) Tested in accordance with JEDEC Standard 22, Test Method C101.

5.3 Dissipation Rating Table

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR(1) ABOVE $T_A = 25°C$	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
D	1080 mW	8.7 mW/°C	690 mW	560 mW
N	1150 mW	9.2 mW/°C	736 mW	598 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

5.4 Thermal Information

THERMAL METRIC(1)		SOIC (D)	PDIP (N)	UNIT
		16 Pins	16 Pins	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	84.6	60.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	43.5	48.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	43.1	40.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	10.4	27.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	42.8	40.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

5.5 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Voltage at any bus terminal	A, B	−7		12	V
High-level input voltage, V_{IH}	EN	2		V_{CC}	V
Low-level input voltage, V_{IL}		0		0.8	mA
Output current	Y	−8		8	
Operating free-air temperature, T_A	SN75LBC175A	0		70	°C
	SN65LBC175A	−40		85	

5.6 Electrical Characteristics

over recommended operating conditions

PARAMETER			TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going differential input voltage threshold		-7 V ⩽ V_{CM} ⩽ 12 V (V_{CM} = (V_A + V_B) / 2)			-80	-10	mV
V_{IT-}	Negative-going differential input voltage threshold					-200	-120	
V_{HYS}	Hysteresis voltage (V_{IT+} - V_{IT-})					-40		mV
V_{IK}	Input clamp voltage		I_I = -18 mA			-1.5	-0.8	V
V_{OH}	High-level output voltage		V_{ID} = 200 mV, I_{OH} = -8 mA	See 图 6-1		2.7	4.8	V
V_{OL}	Low-level output voltage		V_{ID} = -200 mV, I_{OL} = 8 mA			0.2	0.4	
I_{OZ}	High-impedance-state output current		V_O = 0 V to V_{CC}			-1	1	µA
I_I	Line input current		Other input at 0 V, V_{CC} = 0 V or 5 V	V_I = 12 V			0.9	mA
				V_I = -7 V		-0.7		
I_{IH}	High-level input current	Enable inputs					100	µA
I_{IL}	Low-level input current					-100		µA
R_I	Input resistance		A, B			12		kΩ
I_{CC}	Supply current		V_{ID} = 5 V	1,2EN, 3,4EN at 0 V			20	mA
			No load	1,2EN, 3,4EN at V_{CC}		11	16	mA

(1) All typical values are at V_{CC} = 5 V and 25°C.

5.7 Switching Characteristics

over recommended operating conditions

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_r	output rise time			2	4	ns
t_f	output fall time	V_{ID} = -3 V to 3 V, See 图 6-2		2	4	ns
t_{PLH}	Propagation delay time, low-to-high level output			9 12	16	ns
t_{PHL}	Propagation delay time, high-to-low level output			9 12	16	ns
t_{PZH}	Propagation delay time, high-impedance to high-level output	See 图 6-3		27	38	ns
t_{PHZ}	Propagation delay time, high-level to high-impedance output			7	16	ns
t_{PZL}	Propagation delay time, high-impedance to low level output	See 图 6-4		29	38	ns
t_{PLZ}	Propagation delay time, low-level to high-impedance output			12	16	ns
$t_{sk(P)}$	Pulse skew ($\|(t_{PLH} - t_{PHL})\|$)			0.2	1	ns
$t_{sk(o)}$	output skew (see Note 4)				2	ns
$t_{sk(PP)}$	Part-to-part skew (see Note 5)				2	ns

(1) All typical values are at V_{CC} = 5 V and 25°C.
(2) Outputs skew ($t_{sk(o)}$) is the magnitude of the time delay difference between the outputs of a single device with all of the inputs connected together.
(3) Part-to-part skew ($t_{sk(pp)}$) is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same input signals, the same supply voltages, at the same temperature, and have identical packages and test circuits.

5.8 Typical Characteristics

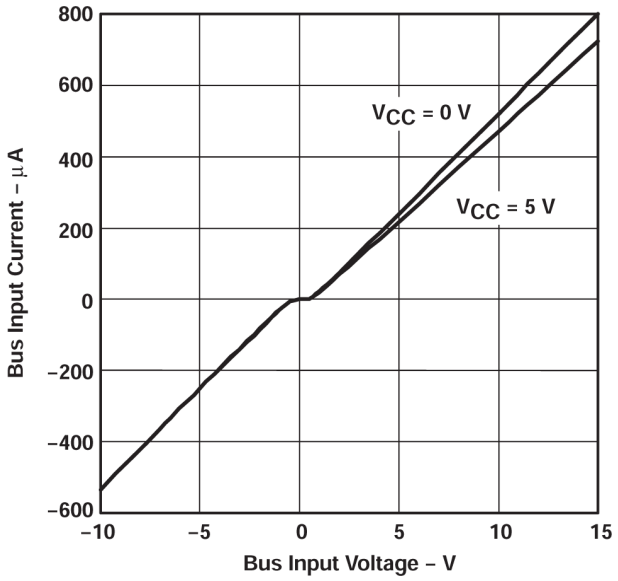


图 5-1. Bus Input Current vs Bus Input Voltage

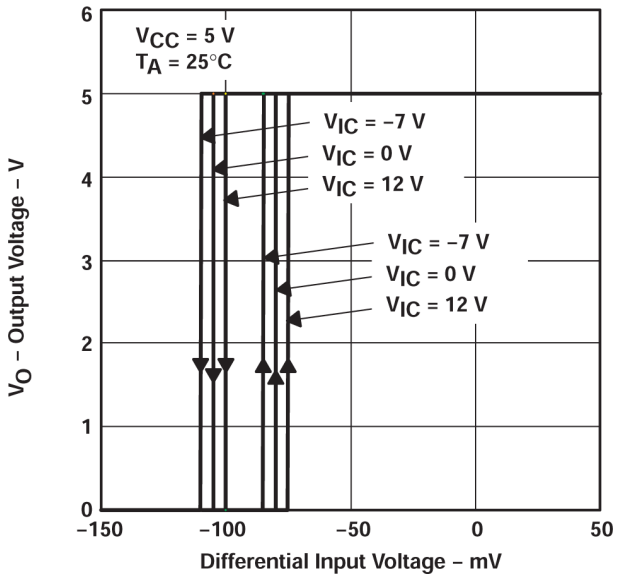


图 5-2. Output Voltage vs Differential Input Voltage

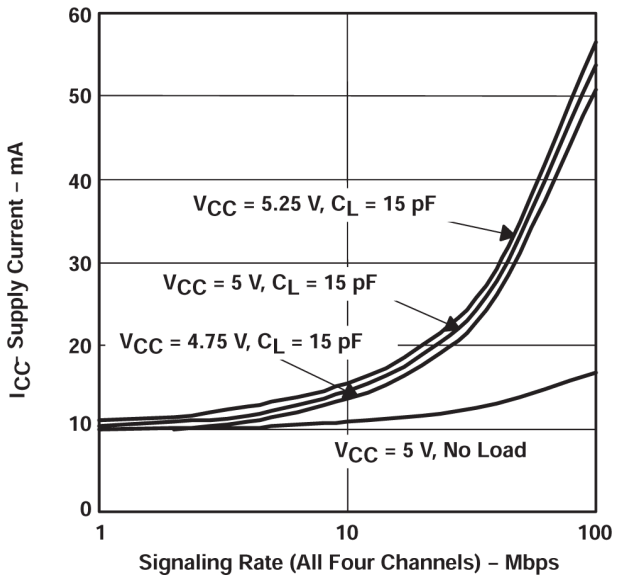


图 5-3. Supply Current vs Signaling Rate (All Four Channels)

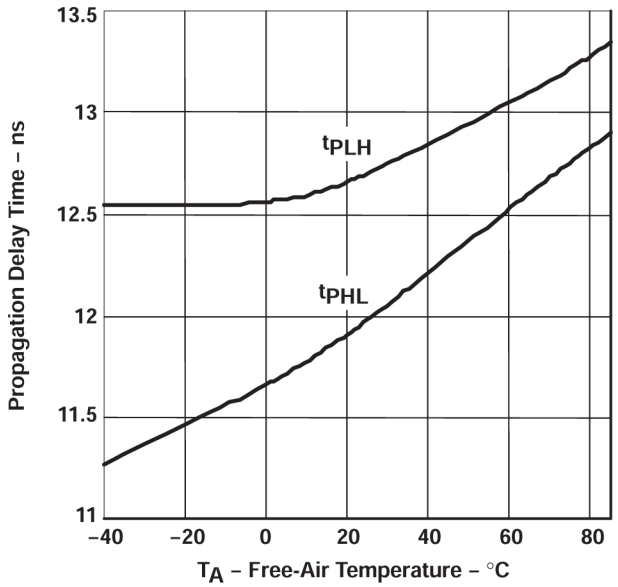


图 5-4. Propagation Delay Time vs Free-air Temperature

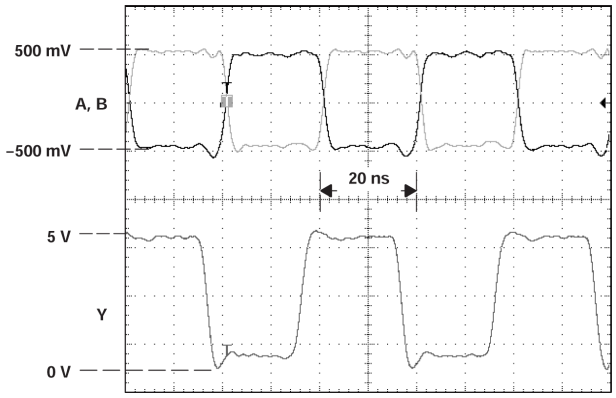


图 5-5. Receiver Inputs and Outputs, 50 Mbps Signaling Rate

6 Parameter Measurement Information

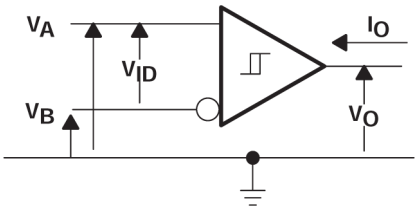
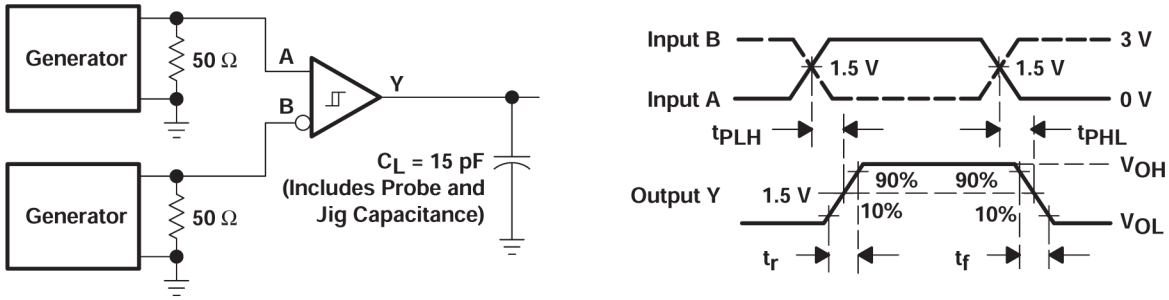
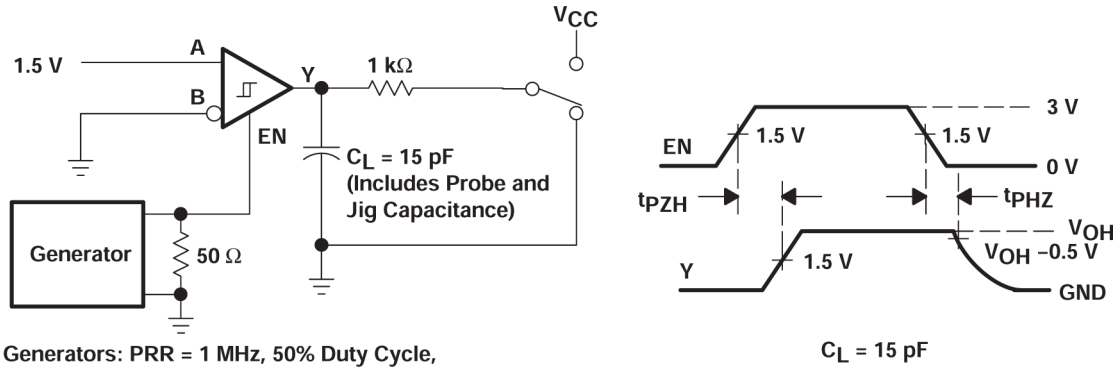


图 6-1. Voltage and Current Definitions



Generators: PRR = 1 MHz, 50% Duty Cycle,
t_r <6 ns, Z_O = 50 Ω

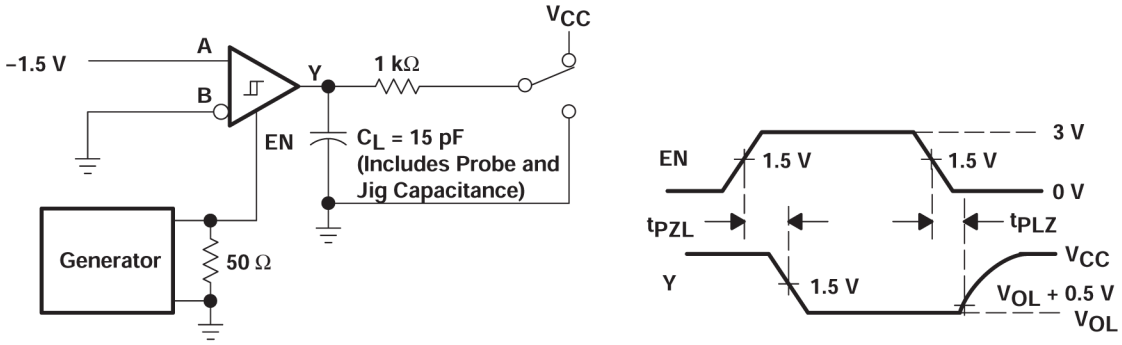
图 6-2. Switching Test Circuit and Waveforms



Generators: PRR = 1 MHz, 50% Duty Cycle,
t_r <6 ns, Z_O = 50 Ω

C_L = 15 pF

图 6-3. Test Circuit Waveforms, t_{PZH} and t_{PHZ}



Generators: PRR = 1 MHz, 50% Duty Cycle,
t_r <6 ns, Z_O = 50 Ω

图 6-4. Test Circuit Waveforms, t_{PZL} and t_{PLZ}

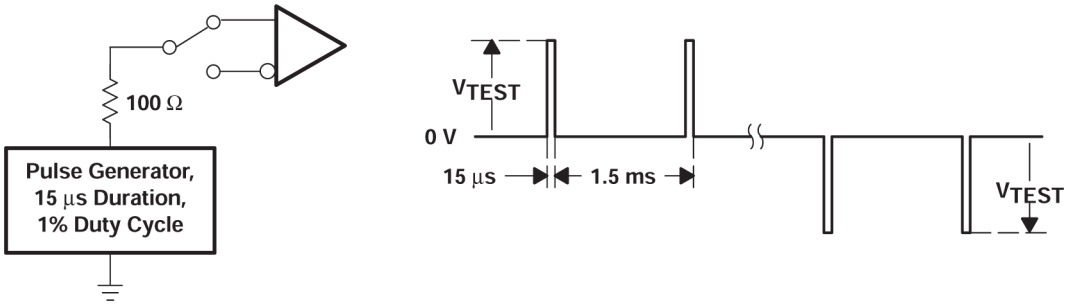


图 6-5. Test Circuit and Waveform, Transient Over-Voltage Test

7 Detailed Description

7.1 Device Functional Modes

表 7-1. Functional Table (Each Receiver)

DIFFERENTIAL INPUTS A – B (V_{ID})	ENABLE EN(1)	OUTPUT Y
$V_{ID} \leqslant -0.2$ V	H	L
-0.2 V < V_{ID} < -0.01 V	H	?
-0.01 V $\leqslant V_{ID}$	H	H
X	L	Z
X	OPEN	Z
Short circuit	H	H
Open circuit	H	H

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), ? = indeterminate

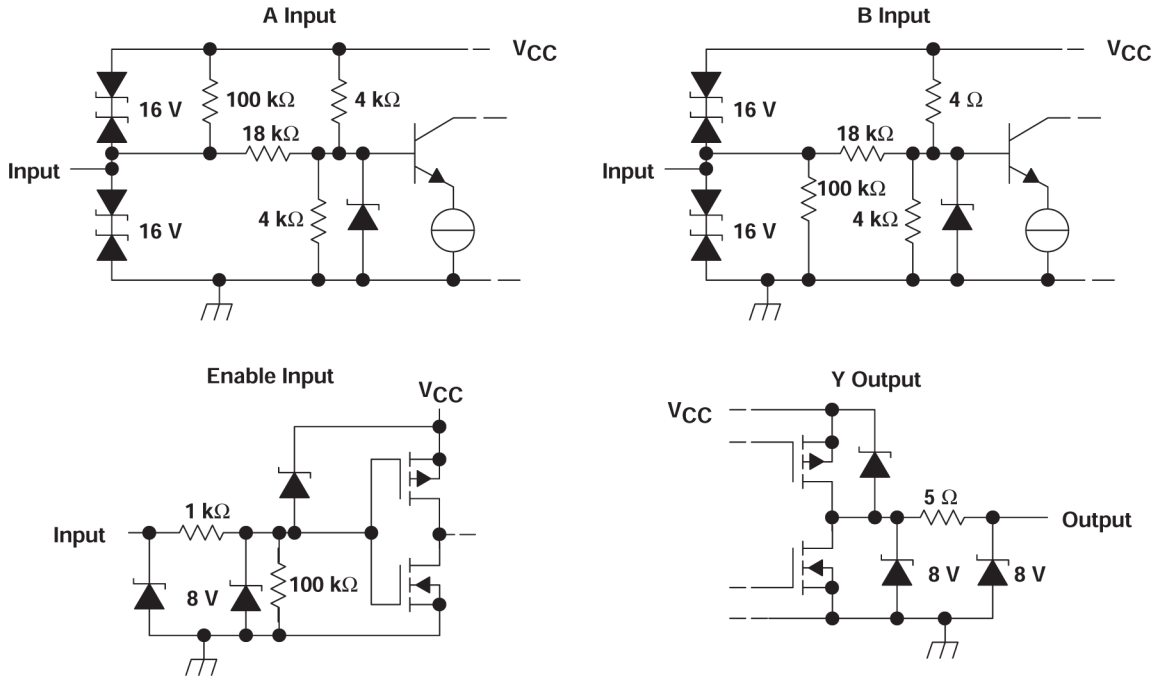


图 7-1. Equivalent Input and Output Schematic Diagrams

8 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Typical Application

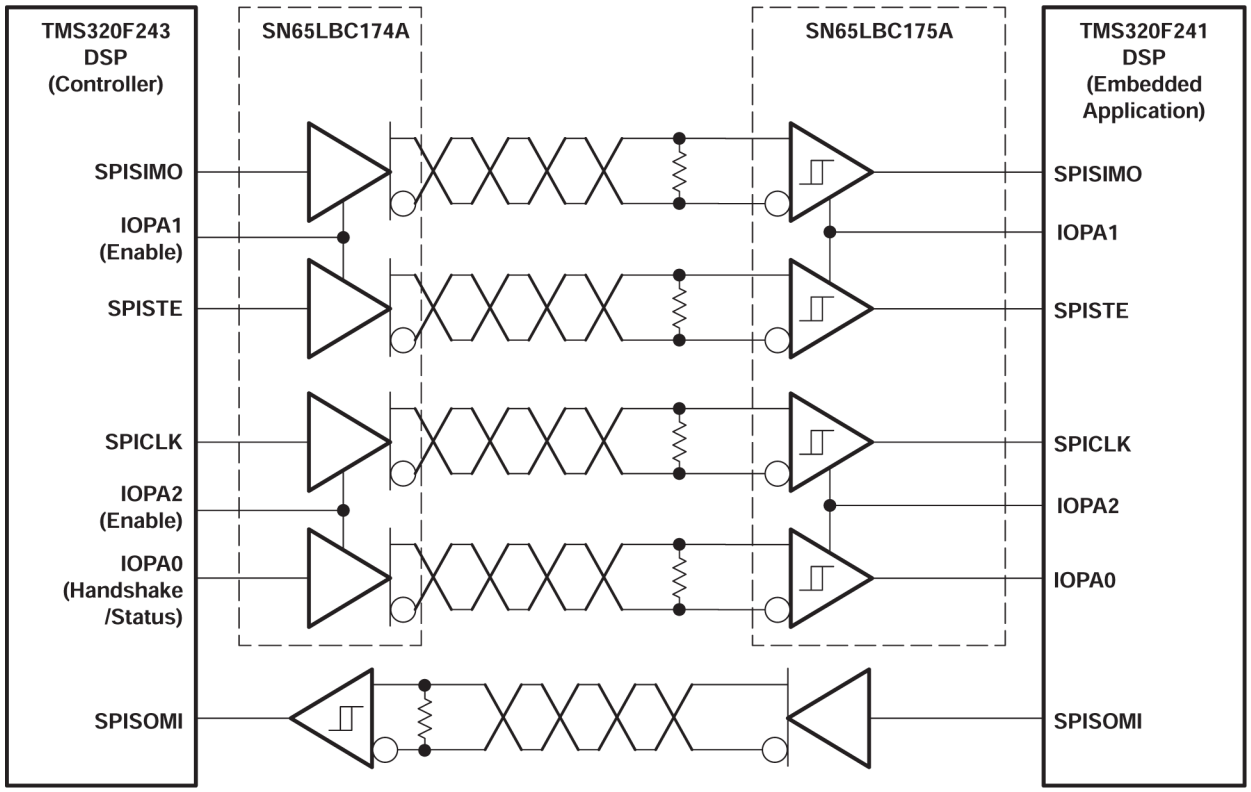


图 8-1. Typical Application Circuit, DSP-to-DSP Link via Serial Peripheral Interface

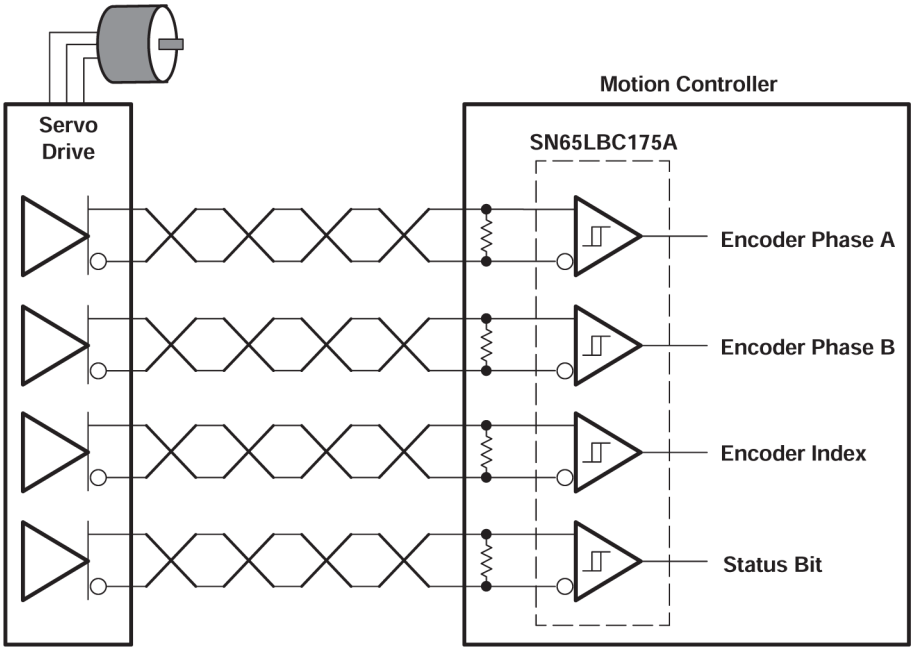


图 8-2. Typical Application Circuit, High-Speed Servomotor Encoder Interface

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.2 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
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9.4 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

9.5 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

10 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision C (March 2009) to Revision D (November 2023)	Page
• 更改了整个文档中的表格、图和交叉参考的编号格式	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65LBC175AD	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	-40 to 85	65LBC175A	
SN65LBC175ADR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	65LBC175A	Samples
SN65LBC175AN	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	65LBC175A	Samples
SN75LBC175AD	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI	0 to 70	75LBC175A	
SN75LBC175AN	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI	0 to 70	75LBC175A	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals.
TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN65LBC175A :

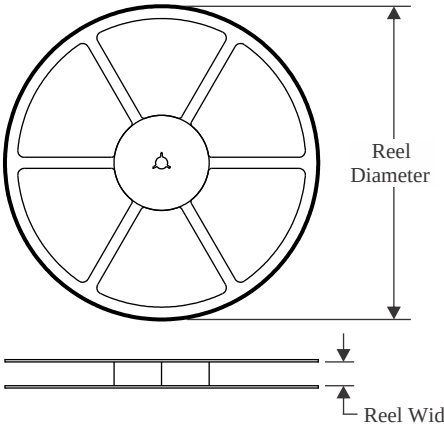
- Enhanced Product : SN65LBC175A-EP

NOTE: Qualified Version Definitions:

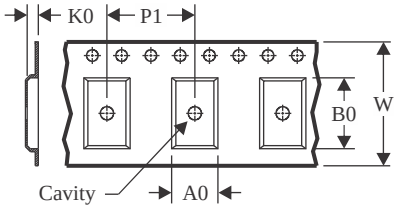
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

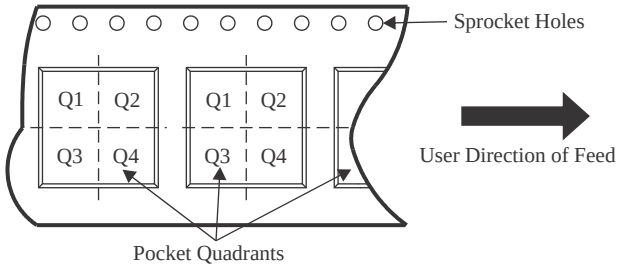


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

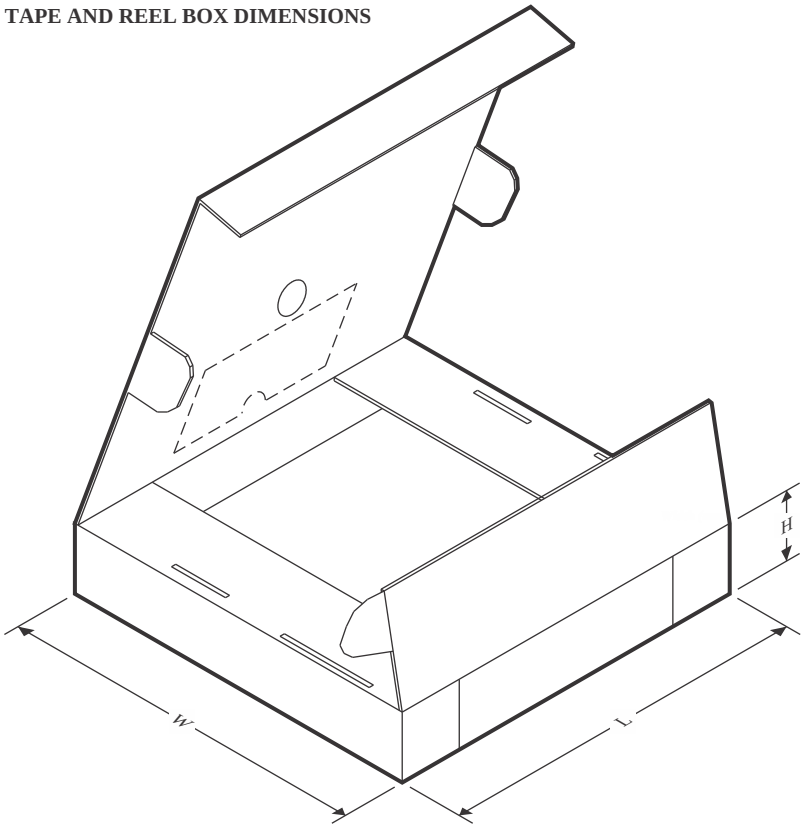
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LBC175ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN75LBC175ADR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

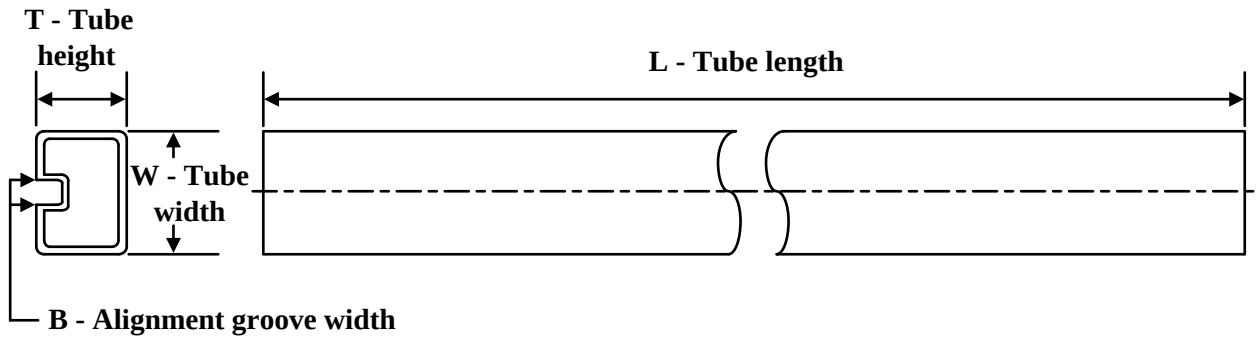
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LBC175ADR	SOIC	D	16	2500	353.0	353.0	32.0
SN75LBC175ADR	SOIC	D	16	2500	340.5	336.1	32.0

TUBE



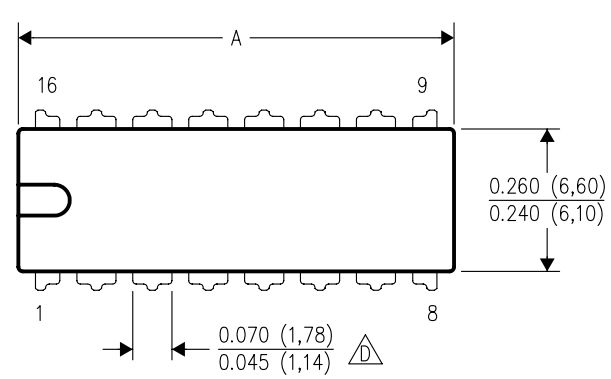
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN65LBC175AD	D	SOIC	16	40	507	8	3940	4.32
SN65LBC175ADG4	D	SOIC	16	40	507	8	3940	4.32
SN65LBC175AN	N	PDIP	16	25	506	13.97	11230	4.32
SN75LBC175AD	D	SOIC	16	40	507	8	3940	4.32
SN75LBC175AN	N	PDIP	16	25	506	13.97	11230	4.32

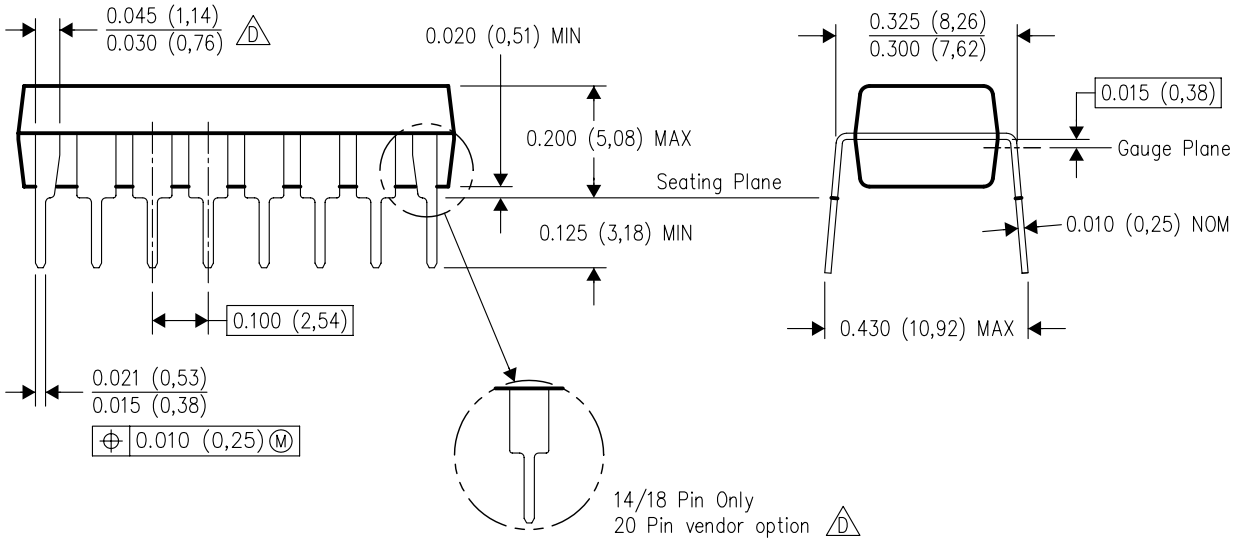
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



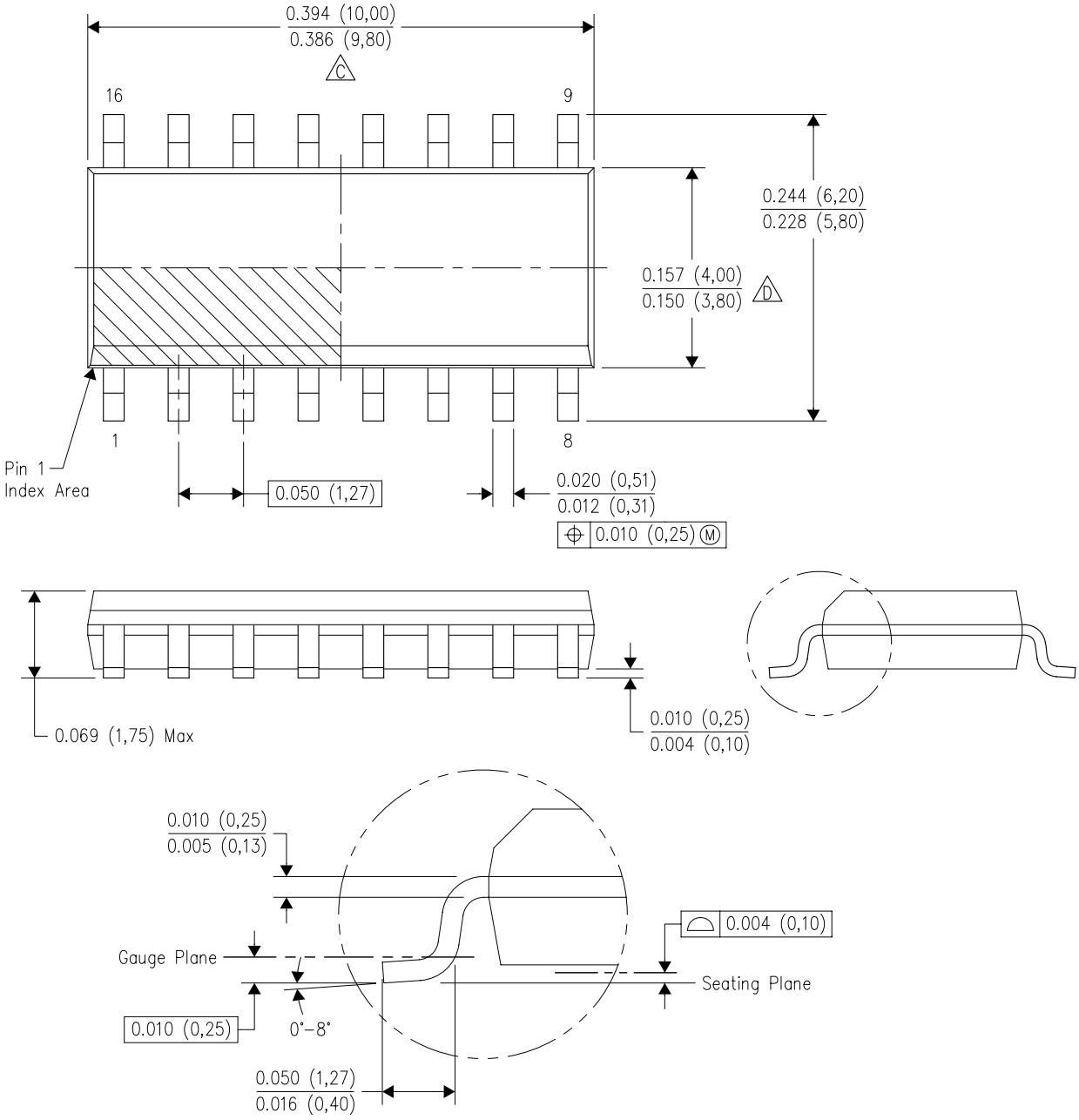
DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

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