

TAS2770 具有扬声器 I/V 感应 20W 数字输入单声道 D 类音频放大器

1 特性

- 高性能单声道 D 类放大器
 - 1% THD+N 时的功率为 20W (4 Ω, 16V)
 - 1% THD+N 时的功率为 15.4W (4 Ω, 12.6V)
- 1W 时的 THD+N 为 0.03% (4 Ω, VBAT = 12.6V)
- 8.4V Vbat 时的 A 加权空闲通道噪声为 32μVrms
- 20Hz 至 20kHz 内具有 90dB PSRR、200mV_{PP} 纹波
- 1W (4 Ω, VBAT = 12.6V) 下的效率为 82.5%
- < 1μA HW 关断 VBAT 电流
- 42mW / 63mW 空闲损耗 (8.4V / 12.6V)
- 扬声器电压和电流感测
- 使用 I/V 扬声器感测进行实时诊断
 - 过流
 - 短路 (电源短路、接地短路和终端至终端短路)
 - 过热
- VBAT 跟踪峰值电压限制器提供欠压保护
- 44.1kHz 至 192kHz 采样速率
- 灵活的用户界面
 - I²S/TDM : 8 通道 (32 位/96kHz)
 - I²C : 8 个可选择地址
- 无 MCLK 运行
- 低噗声和啁啾声
- 电源
 - VBAT : 4.5V 至 16V
 - AVDD : 1.8V
- 扩频频谱低 EMI 模式
- 热保护和过流保护

2 应用

- 笔记本电脑
- 蓝牙扬声器
- 家庭自动化
- 智能扬声器/物联网

3 说明

TAS2770 是一款经优化后可高效驱动小型扬声器的单声道数字输入 D 类音频放大器。凭借出色的输出功率、保护功能和封装, TAS2770 成为智能扬声器、蓝牙扬声器、家庭自动化设备、笔记本电脑和平板电脑的理想选择。

该 D 类放大器能够在 16V 电压下向 4 Ω 的负载提供 20W 的连续功率, 在 16V 电压下向 8 Ω 的负载提供 15W 的连续功率, 两种情况下的 THD 都为 1%。4.5V 至 16V 的宽输入电压范围和高输出功率使该放大器具有出色的通用性, 能够与电池电源或线路供电系统配合使用。

欠压保护器跟踪峰值电压, 并自动将增益限制为可用电压。该硬件实现的功能降低了放大器对系统电源的需求, 从而防止音频中断和系统关断。

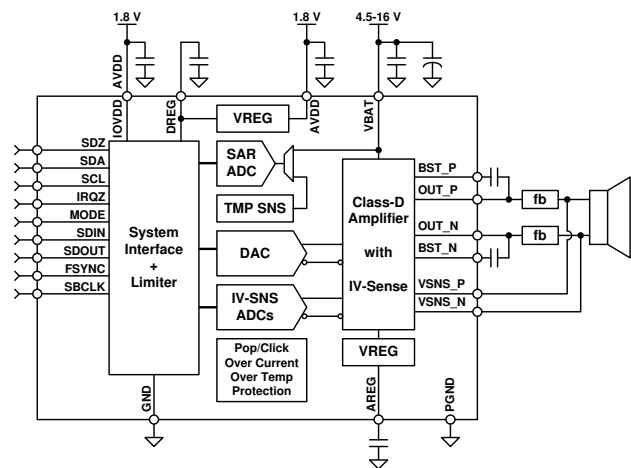
TAS2770 可用作常规放大器或与基于主机的扬声器保护算法配合使用。集成的扬声器电压和电流感应功能可通过 I²S 返回路径将扬声器状况实时反馈到保护算法。

最多有 8 个器件可以通过任意一个 I²S/TDM + I²C 共享一个公共总线。

TAS2770 器件采用 26 引脚、0.4mm 间距 QFN 封装, 实现紧凑的 PCB 空间。

器件信息

| 器件型号 | 封装 | 封装尺寸 (标称值) |
|------------|-------|--------------|
| TAS2770 | QFN | 4mm × 3.5mm |
| TAS2770 | DSBGA | 2mm × 2.52mm |
| SNP002770 | QFN | 4mm × 3.5mm |
| SNP002770 | DSBGA | 2mm × 2.52mm |
| TAS5770LC0 | DSBGA | 2mm × 2.52mm |



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功能方框图

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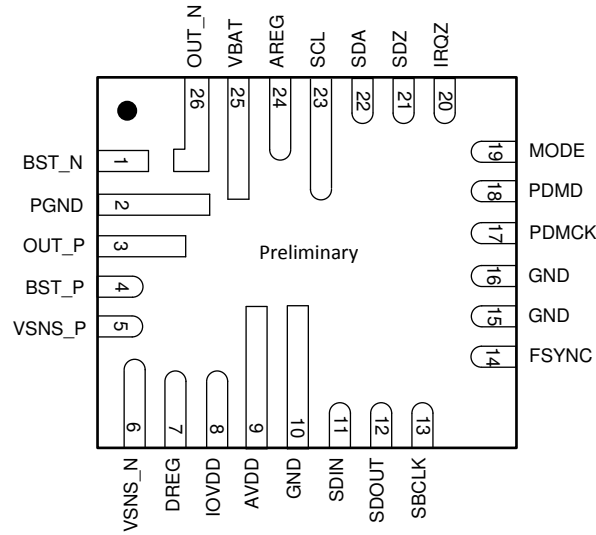
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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

| | |
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| Changes from Revision D (August 2022) to Revision E (April 2023) | Page |
| • Updated 表 8-70 | 45 |
| • Updated 图 8-64 | 74 |
| Changes from Revision C (October 2020) to Revision D (August 2022) | Page |
| • 向数据表添加了 TAS5770LC0 器件..... | 1 |
| Changes from Revision B (October 2018) to Revision C (October 2020) | Page |
| • 更改了首页中的信息..... | 1 |
| • Changed VBAT Max in 节 6.3 from 16 V to 18 V..... | 5 |
| • Changed REV_ID..... | 75 |
| Changes from Revision A (December 2017) to Revision B (October 2018) | Page |
| • Changed From: Efficiency (%) To: VDD PSRR (dB) in 图 6-15 | 14 |
| • Changed From: Efficiency (%) To: VBAT PSRR (dB) in 图 6-16 | 14 |
| Changes from Revision * (October 2017) to Revision A (December 2017) | Page |
| • 将 TAS2770 发布为“量产数据” | 1 |

5 Pin Configuration and Functions



Drawing is Preliminary.

图 5-1. QFN Package 26-Pin RJQ Top View

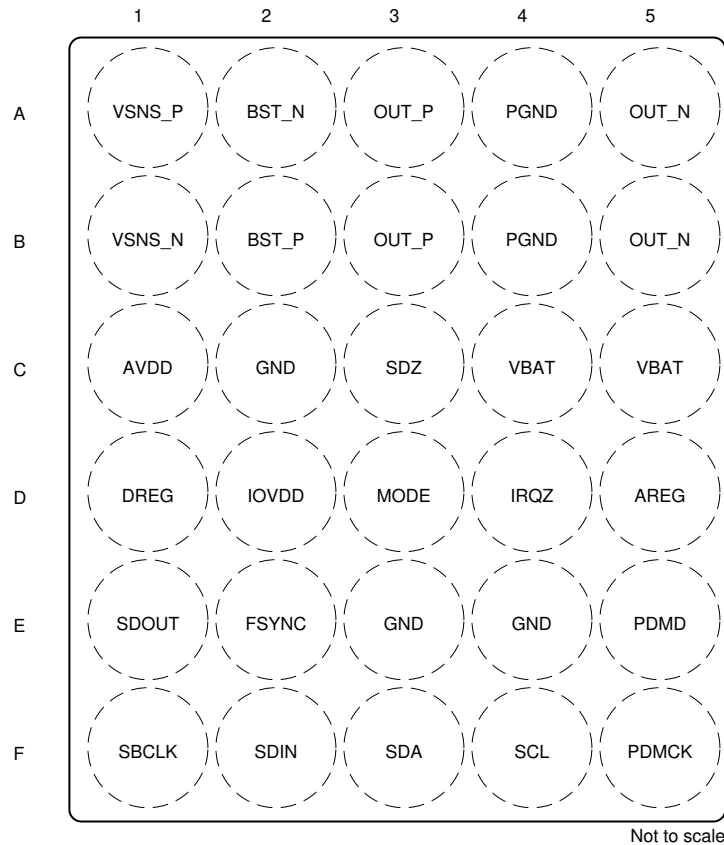


图 5-2. WCSP 30-Ball Top View

表 5-1. Pin Functions

| PIN | | | I/O | DESCRIPTION |
|------------|------------|--------|-----|---|
| DSBGA | QFN | NAME | | |
| D5 | 24 | AREG | O | Gate drive voltage regulator output. Decouple with cap to GND. Do not connect to external load. |
| C1 | 9 | AVDD | P | Analog power input. Connect to 1.8V supply and decouple to GND with cap. |
| A2 | 1 | BST_N | I | Class-D negative bootstrap. Connect a cap between BST_N and OUT_N. |
| B2 | 4 | BST_P | I | Class-D positive bootstrap. Connect a cap between BST_P and OUT_P. |
| D1 | 7 | DREG | O | Digital core voltage regulator output. Bypass to GND with a cap. Do not connect to external load. |
| E2 | 14 | FSYNC | I | TDM Frame Sync. |
| C2, E3, E4 | 10, 15, 16 | GND | P | Analog GND. Connect to PCB GND Plane. |
| D2 | 8 | IOVDD | P | Digital IO Supply. Connect to the same 1.8 V supply that powers AVDD and decouple with a cap to GND. |
| D4 | 20 | IRQZ | O | Open drain, active low interrupt pin. Pull up to IOVDD with resistor if optional internal pull up is not used. |
| D3 | 19 | MODE | I | Mode detect pin. This pin can detect a short to IOVDD or GND, a 470 Ω connection to IOVDD or GND, a 2.2 k Ω connection to IOVDD or GND, a 10 k Ω connection to IOVDD or GND and a 47 k Ω connection to IOVDD. Minimize capacitive loading on this pin and do not connect to any other load. |
| A5, B5 | 26 | OUT_N | O | Class-D negative output. |
| A3, B3 | 3 | OUT_P | O | Class-D positive output. |
| F5 | 17 | PDMCK | IO | PDM Clock. |
| E5 | 18 | PDMD | I | PDM Digital Input. |
| A4, B4 | 2 | PGND | P | Class-D GND. Connect to PCB GND Plane. |
| F1 | 13 | SBCLK | I | TDM Serial Bit Clock in TDM/I ² C Mode. |
| F4 | 23 | SCL | I | I ² C Clock Pin. Pull up to IOVDD with a resistor. |
| F3 | 22 | SDA | IO | I ² C Data Pin. Pull up to IOVDD with a resistor. |
| F2 | 11 | SDIN | I | TDM Serial Data Input. |
| E1 | 12 | SDOUT | IO | TDM Serial Data Output in TDM/I ² C Mode. |
| C3 | 21 | SDZ | I | Active low hardware shutdown. |
| C4, C5 | 25 | VBAT | P | Class-D power supply input. Connect to VBAT supply and decouple with a cap. |
| B1 | 6 | VSNS_N | I | Voltage Sense negative input. Connect to Class-D negative output after Ferrite bead filter. |
| A1 | 5 | VSNS_P | I | Voltage Sense positive input. Connect to Class-D positive output after Ferrite bead filter. |

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

| | | MIN | MAX | UNIT |
|---|--|-------|-----|------|
| Supply Voltage | AVDD | - 0.3 | 2 | V |
| | IOVDD | - 0.3 | 2 | V |
| | VBAT | - 0.3 | 18 | V |
| Input voltage ⁽²⁾ | Digital IOs referenced to IOVDD supply | - 0.3 | 2.3 | V |
| Operating free-air temperature, T _A ; Device is functional and reliable, some performance characteristics may be degraded. | | - 40 | 85 | °C |
| Performance free-air temperature, T _P ; All performance characteristics are met. | | - 20 | 70 | °C |
| Operating junction temperature, T _J | | - 40 | 150 | °C |
| Storage temperature, T _{stg} | | - 65 | 150 | °C |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* can cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Procedures*. Exposure to absolute-maximum-rated conditions for extended periods can affect device reliability.
- (2) All digital inputs and IOs are failsafe.

6.2 ESD Ratings

| | | VALUE | UNIT |
|--|--|-------|------|
| V _(ESD) Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | ±2500 | V |
| | Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾ | ±1500 | |

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|------------------|----------------------------------|------|-------|------|------|
| AVDD | Supply voltage | 1.65 | 1.8 | 1.95 | V |
| IOVDD | Supply voltage | 1.65 | 1.8 | 1.95 | V |
| VBAT | Supply voltage | 4.5 | | 16 | V |
| V _{IH} | High-level digital input voltage | | IOVDD | | V |
| V _{IL} | Low-level digital input voltage | | 0 | | V |
| R _{SPK} | Minimum speaker impedance | 3.2 | | | Ω |
| L _{SPK} | Minimum speaker inductance | 10 | | | μH |

6.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | TAS2770 | UNIT |
|-------------------------------|--|-----------|------|
| | | QFN (RJQ) | |
| | | 26 PINS | |
| R _{θJA} | Junction-to-ambient thermal resistance | 57.0 | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 0.3 | °C/W |
| R _{θJB} | Junction-to-board thermal resistance | 8.5 | °C/W |
| ψ _{JT} | Junction-to-top characterization parameter | 0.2 | °C/W |
| ψ _{JB} | Junction-to-board characterization parameter | 8.7 | °C/W |

| THERMAL METRIC ⁽¹⁾ | | TAS2770 | UNIT |
|-------------------------------|--|-----------|------|
| | | QFN (RJQ) | |
| | | 26 PINS | |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | NA | °C/W |

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

$T_A = 25\text{ }^\circ\text{C}$, $V_{BAT} = 12.6\text{ V}$, $AVDD = IOVDD = 1.8\text{ V}$, $R_L = 4\text{ }\Omega + 33\text{ }\mu\text{H}$, $f_{in} = 1\text{ kHz}$, SSM, $f_s = 48\text{ kHz}$, Gain = 21 dBV, SDZ = 1, Measured filter free using 节 7 (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|---|---|----------------|--------------|------|--------|
| DIGITAL INPUT and OUTPUT | | | | | | |
| V_{IH} | High-level digital input logic voltage threshold | All digital pins except SDA and SCL; IOVDD = 1.8 V. | 0.65 × IOVDD | | | V |
| V_{IL} | Low-level digital input logic voltage threshold | All digital pins except SDA and SCL; IOVDD = 1.8 V. | | 0.35 × IOVDD | | V |
| $V_{IH(I2C)}$ | High-level digital input logic voltage threshold | SDA and SCL; IOVDD = 1.8 V. | 0.7 × IOVDD | | | V |
| $V_{IL(I2C)}$ | Low-level digital input logic voltage threshold | SDA and SCL; IOVDD = 1.8 V. | | 0.3 × IOVDD | | V |
| V_{OH} | High-level digital output voltage | All digital pins except SDA, SCL and IRQZ; IOVDD = 1.8 V; $I_{OH} = 2\text{ mA}$. | IOVDD - 0.45 V | | | V |
| V_{OL} | Low-level digital output voltage | All digital pins except SDA, SCL and IRQZ; IOVDD = 1.8 V; $I_{OL} = -2\text{ mA}$. | | 0.45 | | V |
| $V_{OL(I2C)}$ | Low-level digital output voltage | SDA and SCL; IOVDD = 1.8 V; $I_{OL(I2C)} = -2\text{ mA}$. | | 0.2 × IOVDD | | V |
| $V_{OL(IRQZ)}$ | Low-level digital output voltage for IRQZ open drain Output | IRQZ; IOVDD = 1.8 V; $I_{OL(IRQZ)} = -2\text{ mA}$. | | 0.45 | | V |
| I_{IH} | Input logic-high leakage for digital inputs | All digital pins; Input = IOVDD. | - 5 | 0.1 | 5 | μA |
| I_{IL} | Input logic-low leakage for digital inputs | All digital pins; Input = GND. | - 5 | 0.1 | 5 | μA |
| C_{IN} | Input capacitance for digital inputs | All digital pins | | 5 | | pF |
| R_{PD} | Pull down resistance for digital input/IO pins when asserted on | SDOUT, SDIN, FSYNC, SBCLK, PDMD, PDMCK | | 18 | | kΩ |
| TDM SERIAL AUDIO PORT | | | | | | |
| PCM Sample Rates & FSYNC Input Frequency | Single Speed, I ² S/TDM Operation | | 48 | | kHz | |
| | Double Speed, I ² S/TDM Operation | | 96 | | | |
| | Quadruple Speed, I ² S/TDM Operation | | 192 | | | |
| SBCLK Input Frequency | I ² S/TDM Operation | | 2.54 | | 27.1 | MHz |
| SBCLK Maximum Input Jitter | RMS Jitter below 40 kHz that can be tolerated without performance degradation | | 1 | | ns | |
| | RMS Jitter above 40 kHz that can be tolerated without performance degradation | | 10 | | | |
| SBCLK Cycles per FSYNC in I ² S and TDM Modes | Values: 64, 96, 128, 192, 256, 384 and 512 | | 64 | | 512 | Cycles |
| PDM AUDIO PORT | | | | | | |
| PDM clock input frequency | Single Rate PDM | | 3.072 | | MHz | |
| | Double Rate PDM | | 6.144 | | | |

$T_A = 25\text{ }^\circ\text{C}$, $V_{BAT} = 12.6\text{ V}$, $AVDD = IOVDD = 1.8\text{ V}$, $R_L = 4\ \Omega + 33\ \mu\text{H}$, $f_{in} = 1\text{ kHz}$, $SSM, f_s = 48\text{ kHz}$, $\text{Gain} = 21\text{ dBV}$, $SDZ = 1$, Measured filter free using 节 7 (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|--|---|-----|--------|-----|------------------|
| PDM sensor clock rate to PCM sample rate oversampling ratios | | Single Speed PCM. Values: 64X and 128X. | 64 | | 128 | |
| | | Double Speed PCM. Values: 32X and 64X. | 32 | | 64 | |
| | | Quadruple Speed PCM. Values: 16X and 32X. | 16 | | 32 | |
| PROTECTION CIRCUITRY | | | | | | |
| Thermal shutdown temperature | | | | 140 | | $^\circ\text{C}$ |
| Thermal shutdown retry | | | | 1.5 | | s |
| VBAT undervoltage lockout threshold (UVLO) | | UVLO is asserted | | 4 | | V |
| VBAT overvoltage lockout threshold (OVLO) | | OVLO is asserted | | 18 | | V |
| AMPLIFIER PERFORMANCE | | | | | | |
| P_{OUT} | Maximum Continuous Output Power 0.1% THD+N | $R_L = 8\ \Omega + 33\ \mu\text{H}$, THD+N = 0.1 %, $f_{in} = 1\text{ kHz}$, $V_{BAT} = 8.4\text{ V}$ | | 3.7 | | W |
| | | $R_L = 4\ \Omega + 33\ \mu\text{H}$, THD+N = 0.1 %, $f_{in} = 1\text{ kHz}$, $V_{BAT} = 8.4\text{ V}$ | | 6.6 | | |
| | | $R_L = 8\ \Omega + 33\ \mu\text{H}$, THD+N = 0.1 %, $f_{in} = 1\text{ kHz}$, $V_{BAT} = 12.6\text{ V}$ | | 8.5 | | |
| | | $R_L = 4\ \Omega + 33\ \mu\text{H}$, THD+N = 0.1 %, $f_{in} = 1\text{ kHz}$, $V_{BAT} = 12.6\text{ V}$ | | 14.2 | | |
| | Maximum Continuous Output Power 1% THD+N | $R_L = 8\ \Omega + 33\ \mu\text{H}$, THD+N = 1 %, $f_{in} = 1\text{ kHz}$, $V_{BAT} = 8.4\text{ V}$ | | 4 | | |
| | | $R_L = 4\ \Omega + 33\ \mu\text{H}$, THD+N = 1 %, $f_{in} = 1\text{ kHz}$, $V_{BAT} = 8.4\text{ V}$ | | 7.1 | | |
| | | $R_L = 8\ \Omega + 33\ \mu\text{H}$, THD+N = 1 %, $f_{in} = 1\text{ kHz}$, $V_{BAT} = 12.6\text{ V}$ | | 9.1 | | |
| | | $R_L = 4\ \Omega + 33\ \mu\text{H}$, THD+N = 1 %, $f_{in} = 1\text{ kHz}$, $V_{BAT} = 12.6\text{ V}$ | | 15.4 | | |
| System efficiency at $P_{OUT} = 1\text{ W}$ | | $R_L = 8\ \Omega + 33\ \mu\text{H}$, $f_{in} = 1\text{ kHz}$, $V_{BAT} = 8.4\text{ V}$ | | 89 % | | |
| | | $R_L = 4\ \Omega + 33\ \mu\text{H}$, $f_{in} = 1\text{ kHz}$, $V_{BAT} = 8.4\text{ V}$ | | 84 % | | |
| | | $R_L = 8\ \Omega + 33\ \mu\text{H}$, $f_{in} = 1\text{ kHz}$, $V_{BAT} = 12.6\text{ V}$ | | 87.5 % | | |
| | | $R_L = 4\ \Omega + 33\ \mu\text{H}$, $f_{in} = 1\text{ kHz}$, $V_{BAT} = 12.6\text{ V}$ | | 82.7 % | | |
| System efficiency at 0.1% THD+N power level | | $R_L = 8\ \Omega + 33\ \mu\text{H}$, $P_{OUT} = 3.7\text{ W}$, $f_{in} = 1\text{ kHz}$, $V_{BAT} = 8.4\text{ V}$ | | 92 % | | |
| | | $R_L = 4\ \Omega + 33\ \mu\text{H}$, $P_{OUT} = 6.6\text{ W}$, $f_{in} = 1\text{ kHz}$, $V_{BAT} = 8.4\text{ V}$ | | 87 % | | |
| | | $R_L = 8\ \Omega + 33\ \mu\text{H}$, $P_{OUT} = 8.5\text{ W}$, $f_{in} = 1\text{ kHz}$, $V_{BAT} = 12.6\text{ V}$ | | 92 % | | |
| | | $R_L = 4\ \Omega + 33\ \mu\text{H}$, $P_{OUT} = 14.2\text{ W}$, $f_{in} = 1\text{ kHz}$, $V_{BAT} = 12.6\text{ V}$ | | 86 % | | |

$T_A = 25\text{ }^\circ\text{C}$, $V_{BAT} = 12.6\text{ V}$, $AVDD = IOVDD = 1.8\text{ V}$, $R_L = 4\text{ }\Omega + 33\text{ }\mu\text{H}$, $f_{in} = 1\text{ kHz}$, SSM, $f_s = 48\text{ kHz}$, Gain = 21 dBV, SDZ = 1, Measured filter free using 节 7 (unless otherwise noted).

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------|---|--|-------|-----------|-------|------------------|
| THD+N | Total harmonic distortion + noise | $P_{OUT} = 1\text{ W}$, $R_L = 8\text{ }\Omega + 33\text{ }\mu\text{H}$, $f_{in} = 20\text{ Hz} - 20\text{ kHz}$, $V_{BAT} = 8.4\text{ V}$ | | 0.01 % | | |
| | | $P_{OUT} = 1\text{ W}$, $R_L = 4\text{ }\Omega + 33\text{ }\mu\text{H}$, $f_{in} = 20\text{ Hz} - 20\text{ kHz}$, $V_{BAT} = 8.4\text{ V}$ | | 0.01 % | | |
| | | $P_{OUT} = 1\text{ W}$, $R_L = 8\text{ }\Omega + 33\text{ }\mu\text{H}$, $f_{in} = 20\text{ Hz} - 20\text{ kHz}$, $V_{BAT} = 12.6\text{ V}$ | | 0.01 % | | |
| | | $P_{OUT} = 1\text{ W}$, $R_L = 4\text{ }\Omega + 33\text{ }\mu\text{H}$, $f_{in} = 20\text{ Hz} - 20\text{ kHz}$, $V_{BAT} = 12.6\text{ V}$ | | 0.01 % | | |
| V_N | Idle channel noise | A-Weighted, 20 Hz - 20 kHz, DAC Modulator Running | | 31 | | μV |
| | | $V_{BAT} = 8.4\text{ V}$ | | 32 | | μV |
| | | $V_{BAT} = 12.6\text{ V}$ | | 36 | | μV |
| F_{PWM} | Class-D PWM switching frequency | Average frequency in Spread Spectrum Mode, CLASSD_SYNC=0 | | 384 | | kHz |
| | | Fixed Frequency Mode, CLASSD_SYNC=0 | 345.6 | 384 | 422.4 | |
| | | Fixed Frequency Mode, CLASSD_SYNC=1, $f_s = 44.1, 88.2, 174.6\text{ kHz}$ | | 44.1-8 | | |
| | | Fixed Frequency Mode, CLASSD_SYNC=1, $f_s = 48, 96, 192\text{ kHz}$ | | 48-8 | | |
| V_{OS} | Output offset voltage | | -1 | | 1 | mV |
| DNR | Dynamic range | A-Weighted, -60 dBFS Method | | 108 | | dB |
| SNR | Signal to noise ratio | A-Weighted, Referenced to 1 % THD+N Output Level | | 108 | | dB |
| K_{CP} | Click and pop performance | Into and out of Mute, Shutdown, Power Up, Power Down and audio clocks starting and stopping. A-weighted | | 5 | | mV |
| | | Programmable output level range | 12.5 | | 21 | dBV |
| | | Programmable output level step size | | 0.5 | | dB |
| AV_{ERROR} | Amplifier gain error | $P_{OUT}=1\text{ W}$ | | ± 0.1 | | dB |
| A_{RIPPLE} | Frequency response passband ripple | 20 Hz - 20 kHz | | ± 0.1 | | dB |
| | Mute attenuation | Device in Shutdown or Muted in Normal Operation | | 110 | | dB |
| | Output short circuit limit | $V_{BAT} = 12.6\text{ V}$, Output to Output, Output to GND or Output to V_{BAT} Short | | 6 | | A |
| $R_{DS(ON)FET}$ | Power stage on-resistance (high-side + low-side + sense resistor) | $T_A = 25\text{ }^\circ\text{C}$ | | 510 | | $\text{m}\Omega$ |
| | VBAT power-supply rejection ratio | $V_{BAT} = 12.6\text{ V} + 200\text{ mV}_{pp}$, $f_{ripple} = 217\text{ Hz}$ | | 105 | | dB |
| | | $V_{BAT} = 12.6\text{ V} + 200\text{ mV}_{pp}$, $f_{ripple} = 20\text{ kHz}$ | | 86 | | |
| | AVDD power-supply rejection ratio | $AVDD = 1.8\text{ V} + 200\text{ mV}_{pp}$, $f_{ripple} = 217\text{ Hz}$ | | 95 | | dB |
| | | $AVDD = 1.8\text{ V} + 200\text{ mV}_{pp}$, $f_{ripple} = 20\text{ kHz}$ | | 88 | | |
| | Turn on time from release of SW shutdown | No Volume Ramping | | 1.2 | | ms |
| | | Volume Ramping | | 5.3 | | |

$T_A = 25\text{ }^\circ\text{C}$, $V_{BAT} = 12.6\text{ V}$, $AVDD = IOVDD = 1.8\text{ V}$, $R_L = 4\text{ }\Omega + 33\text{ }\mu\text{H}$, $f_{in} = 1\text{ kHz}$, $SSM, f_s = 48\text{ kHz}$, $\text{Gain} = 21\text{ dBV}$, $SDZ = 1$, Measured filter free using 节 7 (unless otherwise noted).

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|--|--|------|--------------|---------------|
| Turn off time from assertion of SW shutdown to amp Hi-Z | No Volume Ramping | | 0.3 | | ms |
| | Volume Ramping | | 4.7 | | |
| PCM PLAYBACK CHARACTERISTICS | | | | | |
| Playback latency from latched input sample to speaker terminals | Single Speed, I ² S/TDM | | 3.5 | | samples |
| | Double Speed, I ² S/TDM | | 3.5 | | |
| | Quadruple Speed, I ² S/TDM | | 3.5 | | |
| Playback - 0.1 dB bandwidth | Single Speed, I ² S/TDM | | | 23.06 | kHz |
| | Double Speed, I ² S/TDM | | | 21.79 | |
| | Quadruple Speed, I ² S/TDM | | | 21.69 | |
| Playback - 3 dB bandwidth | Single Speed, I ² S/TDM | | | 24 | kHz |
| | Double Speed, I ² S/TDM | | | 23 | |
| | Quadruple Speed, I ² S/TDM | | | 27.26 | |
| PDM PLAYBACK CHARACTERISTICS | | | | | |
| Playback latency from latched data bit to speaker terminals | Single Rate PDM, PDMD input | | 7.07 | | μs |
| | Double Rate PDM, PDMD input | | 5.02 | | |
| Playback - 0.1 dB bandwidth | Single Rate PDM, PDMD input | | 41.5 | | kHz |
| | Double Rate PDM, PDMD input | | 88 | | |
| Playback - 3 dB bandwidth | Single Rate PDM, PDMD input | | 77.5 | | kHz |
| | Double Rate PDM, PDMD input | | 143 | | |
| SPEAKER CURRENT SENSE | | | | | |
| DNR | Dynamic range | Un-Weighted, Relative to 0 dBFS | | 69 | dB |
| THD+N | Total harmonic distortion + noise | $R_L = 8\text{ }\Omega + 33\text{ }\mu\text{H}$, $f_{in} = 1\text{ kHz}$, $P_{OUT} = 5\text{ W}$ | | - 60 | dB |
| | | $R_L = 4\text{ }\Omega + 33\text{ }\mu\text{H}$, $f_{in} = 1\text{ kHz}$, $P_{OUT} = 7.5\text{ W}$ | | - 60 | |
| | Full-scale input current | | | 3.75 | A |
| | Current-sense accuracy | $R_L = 8\text{ }\Omega + 33\text{ }\mu\text{H}$, $I_{OUT} = 354\text{ mA}_{RMS}$ ($P_{OUT} = 1\text{ W}$) | | $\pm 1\%$ | |
| | Current-sense gain error over temperature | - 20°C to 70°C, $P_{OUT} = 1\text{ W}$ | | $\pm 0.75\%$ | |
| | Current-sense gain error over output power | 50 mW to 0.1 % THD+N level, $f_{in} = 1\text{ kHz}$, $4\text{ }\Omega$, using a 40Hz-34dB pilot tone | | $\pm 0.75\%$ | |
| | Current-sense frequency response | Max deviation above and below passband gain | | ± 0.2 | dB |
| SPEAKER VOLTAGE SENSE | | | | | |
| DNR | Dynamic range | Un-Weighted, Relative 0 dBFS | | 69 | dB |
| THD+N | Total harmonic distortion + noise | $R_L = 8\text{ }\Omega + 33\text{ }\mu\text{H}$, $f_{in} = 1\text{ kHz}$, $P_{OUT} = 5\text{ W}$ | | - 60 | dB |
| | | $R_L = 4\text{ }\Omega + 33\text{ }\mu\text{H}$, $f_{in} = 1\text{ kHz}$, $P_{OUT} = 7.5\text{ W}$ | | - 60 | |
| | Full-scale input voltage | | | 14 | V_{PK} |
| | Voltage-sense accuracy | $R_L = 8\text{ }\Omega + 33\text{ }\mu\text{H}$, $I_{OUT} = 354\text{ mA}_{RMS}$ ($P_{OUT} = 1\text{ W}$) | | $\pm 1\%$ | |
| | Voltage-sense gain error over temperature | - 20°C to 70°C, $P_{OUT} = 1\text{ W}$ | | $\pm 0.75\%$ | |

$T_A = 25\text{ }^\circ\text{C}$, $V_{BAT} = 12.6\text{ V}$, $AVDD = IOVDD = 1.8\text{ V}$, $R_L = 4\text{ }\Omega + 33\text{ }\mu\text{H}$, $f_{in} = 1\text{ kHz}$, SSM , $f_s = 48\text{ kHz}$, $\text{Gain} = 21\text{ dBV}$, $SDZ = 1$, Measured filter free using 节 7 (unless otherwise noted).

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--|--|------|--------------|--------|---------------------------|
| Voltage-sense gain error over output power | 50 mW to 0.1 % THD+N level, $f_{in} = 1\text{ kHz}$, $4\text{ }\Omega$, using a 40Hz-34dB pilot tone | | $\pm 0.75\%$ | | |
| Voltage-sense frequency response | Max deviation above and below passband gain | | ± 0.2 | | dB |
| SPEAKER VOLTAGE/CURRENT SENSE RATIO | | | | | |
| Gain ratio error over output power | 50 mW to 0.1 % THD+N level, $f_{in} = 1\text{ kHz}$, $4\text{ }\Omega$, using a 40Hz-34dB pilot tone | | $\pm 0.75\%$ | | |
| Gain ratio error over temperature | $-20\text{ }^\circ\text{C}$ to $70\text{ }^\circ\text{C}$ | | $\pm 0.5\%$ | | |
| TYPICAL CURRENT CONSUMPTION | | | | | |
| Current consumption in hardware shutdown | SDZ = 0, VBAT | | 0.1 | | μA |
| | SDZ = 0, AVDD | | 1 | | |
| | SDZ = 0, IOVDD | | 0.1 | | |
| Current consumption in software shutdown | All Clocks Stopped, VBAT | | 10 | | μA |
| | All Clocks Stopped, AVDD | | 10 | | |
| | All Clocks Stopped, IOVDD | | 1 | | |
| Current consumption during active operation with IV sense disabled | $f_s = 48\text{ kHz}$, VBAT | | 3.1 | | mA |
| | $f_s = 48\text{ kHz}$, AVDD | | 10 | | |
| | $f_s = 48\text{ kHz}$, IOVDD | | 0.1 | | |
| Current consumption during active operation with IV sense enabled | $f_s = 48\text{ kHz}$, VBAT | | 3.1 | | mA |
| | $f_s = 48\text{ kHz}$, AVDD | | 12.5 | | |
| | $f_s = 48\text{ kHz}$, IOVDD | | 0.1 | | |
| PEAK VOLTAGE LIMITER | | | | | |
| Limiter maximum threshold | | 2 | | 14.7 | V |
| Limiter minimum threshold | | 2 | | 14.7 | V |
| Limiter inflection point | | 2 | | 14.7 | V |
| Limiter VBAT tracking slope | | 1 | | 4 | V/V |
| Limiter max attenuation | | 1 | | 16.5 | dB |
| Limiter latency | Time from VBAT dipping below threshold to initial gain reduction | | | 23 | μs |
| Limiter attack rate | | 5 | | 640 | $\mu\text{s}/\text{step}$ |
| Limiter attack step size | | 0.25 | | 2 | dB/step |
| Limiter hold time | | 0 | | 1000 | ms |
| Limiter release rate | | 10 | | 1500 | ms/step |
| Limiter release step size | | 0.25 | | 2 | dB/step |
| BROWN OUT PREVENTION LIMITER | | | | | |
| Brownout prevention threshold | | 4.5 | | 10.875 | V |
| Brownout prevention threshold step size | | | 25 | | mV |
| Brownout prevention threshold tolerance | Measured at VBAT of 5V and 10V | | ± 25 | | mV |
| Brownout prevention latency | Time from VBAT dipping below threshold to initial gain reduction | | | 20 | μs |
| Brownout prevention attack rate | | 5 | | 640 | $\mu\text{s}/\text{step}$ |
| Brownout prevention attack step size | | 0.5 | | 2 | dB/step |
| Brownout prevention hold time | | 0 | | 1000 | ms |

$T_A = 25\text{ }^\circ\text{C}$, $V_{BAT} = 12.6\text{ V}$, $AVDD = IOVDD = 1.8\text{ V}$, $R_L = 4\text{ }\Omega + 33\text{ }\mu\text{H}$, $f_{in} = 1\text{ kHz}$, $SSM, f_s = 48\text{ kHz}$, $\text{Gain} = 21\text{ dBV}$, $SDZ = 1$, Measured filter free using [节 7](#) (unless otherwise noted).

| PARAMETER | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------------------------|-----------------|------|-----|------|---------|
| Brownout prevention release rate | | 10 | | 1500 | ms/step |
| Brownout prevention release step size | | 0.25 | | 2 | dB/step |

6.6 I²C Timing Requirements

T_A = 25 °C, AVDD = IOVDD = 1.8 V (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|-----------------------|--|---------------------------|-----|------|------|
| Standard-Mode | | | | | |
| f _{SCL} | SCL clock frequency | 0 | | 100 | kHz |
| t _{HD,STA} | Hold time (repeated) START condition. After this period, the first clock pulse is generated. | 4 | | | μs |
| t _{LOW} | LOW period of the SCL clock | 4.7 | | | μs |
| t _{HIGH} | HIGH period of the SCL clock | 4 | | | μs |
| t _{SU,STA} | Setup time for a repeated START condition | 4.7 | | | μs |
| t _{HD,DAT} | Data hold time: For I ² C bus devices | 0 | | 3.45 | μs |
| t _{SU,DAT} | Data set-up time | 250 | | | ns |
| t _r | SDA and SCL rise time | | | 1000 | ns |
| t _f | SDA and SCL fall time | | | 300 | ns |
| t _{SU,STO} | Set-up time for STOP condition | 4 | | | μs |
| t _{BUF} | Bus free time between a STOP and START condition | 4.7 | | | μs |
| C _b | Capacitive load for each bus line | | | 400 | pF |
| Fast-Mode | | | | | |
| f _{SCL} | SCL clock frequency | 0 | | 400 | kHz |
| t _{HD,STA} | Hold time (repeated) START condition. After this period, the first clock pulse is generated. | 0.6 | | | μs |
| t _{LOW} | LOW period of the SCL clock | 1.3 | | | μs |
| t _{HIGH} | HIGH period of the SCL clock | 0.6 | | | μs |
| t _{SU,STA} | Setup time for a repeated START condition | 40.6 | | | μs |
| t _{HD,DAT} | Data hold time: For I ² C bus devices | 0 | | 0.9 | μs |
| t _{SU,DAT} | Data set-up time | 100 | | | ns |
| t _r | SDA and SCL rise time | 20 + 0.1 × C _b | | 300 | ns |
| t _f | SDA and SCL fall time | 20 + 0.1 × C _b | | 300 | ns |
| t _{SU,STO} | Set-up time for STOP condition | 0.26 | | | μs |
| t _{BUF} | Bus free time between a STOP and START condition | 1.3 | | | μs |
| C _b | Capacitive load for each bus line | | | 400 | pF |
| Fast-Mode Plus | | | | | |
| f _{SCL} | SCL clock frequency | 0 | | 1000 | kHz |
| t _{HD,STA} | Hold time (repeated) START condition. After this period, the first clock pulse is generated. | 0.26 | | | μs |
| t _{LOW} | LOW period of the SCL clock | 0.5 | | | μs |
| t _{HIGH} | HIGH period of the SCL clock | 0.26 | | | μs |
| t _{SU,STA} | Setup time for a repeated START condition | 0.26 | | | μs |
| t _{HD,DAT} | Data hold time: For I ² C bus devices | 0 | | | μs |
| t _{SU,DAT} | Data set-up time | 50 | | | ns |
| t _r | SDA and SCL Rise Time | | | 120 | ns |
| t _f | SDA and SCL Fall Time | | | 120 | ns |
| t _{SU,STO} | Set-up time for STOP condition | | | | μs |
| t _{BUF} | Bus free time between a STOP and START condition | 0.5 | | | μs |

$T_A = 25\text{ }^\circ\text{C}$, AVDD = IOVDD = 1.8 V (unless otherwise noted)

| | MIN | NOM | MAX | UNIT |
|--|-----|-----|-----|------|
| C _b Capacitive load for each bus line | | | 550 | pF |

6.7 TDM Port Timing Requirements

 $T_A = 25\text{ }^\circ\text{C}$, AVDD = IOVDD = 1.8 V, 20 pF load on all outputs (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|--|-------------------------------|-----|-----|-----|------|
| t _H (SBCLK) SBCLK high period | | 40 | | | ns |
| t _L (SBCLK) SBCLK low period | | 40 | | | ns |
| t _{SU} (FSYNC) FSYNC setup time | | 8 | | | ns |
| t _{HLD} (FSYNC) FSYNC hold time | | 8 | | | ns |
| t _{SU} (FSYNC) SDIN setup time | | 8 | | | ns |
| t _{HLD} (SDIN) SDIN hold time | | 8 | | | ns |
| t _d (DO-FSYNC) FSYNC to SDOOUT delay (tx_offset = 0 only) | 50% of FSYNC to 50% of SDOOUT | | | 35 | ns |
| t _d (DO-SBCLK) SBCLK to SDOOUT delay | 50% of FSYNC to 50% of SDOOUT | | | 35 | ns |
| t _r (SBCLK) SBCLK rise time | 10 % - 90 % Rise Time | | | 8 | ns |
| t _f (SBCLK) SBCLK fall time | 90 % - 10 % Fall Time | | | 8 | ns |

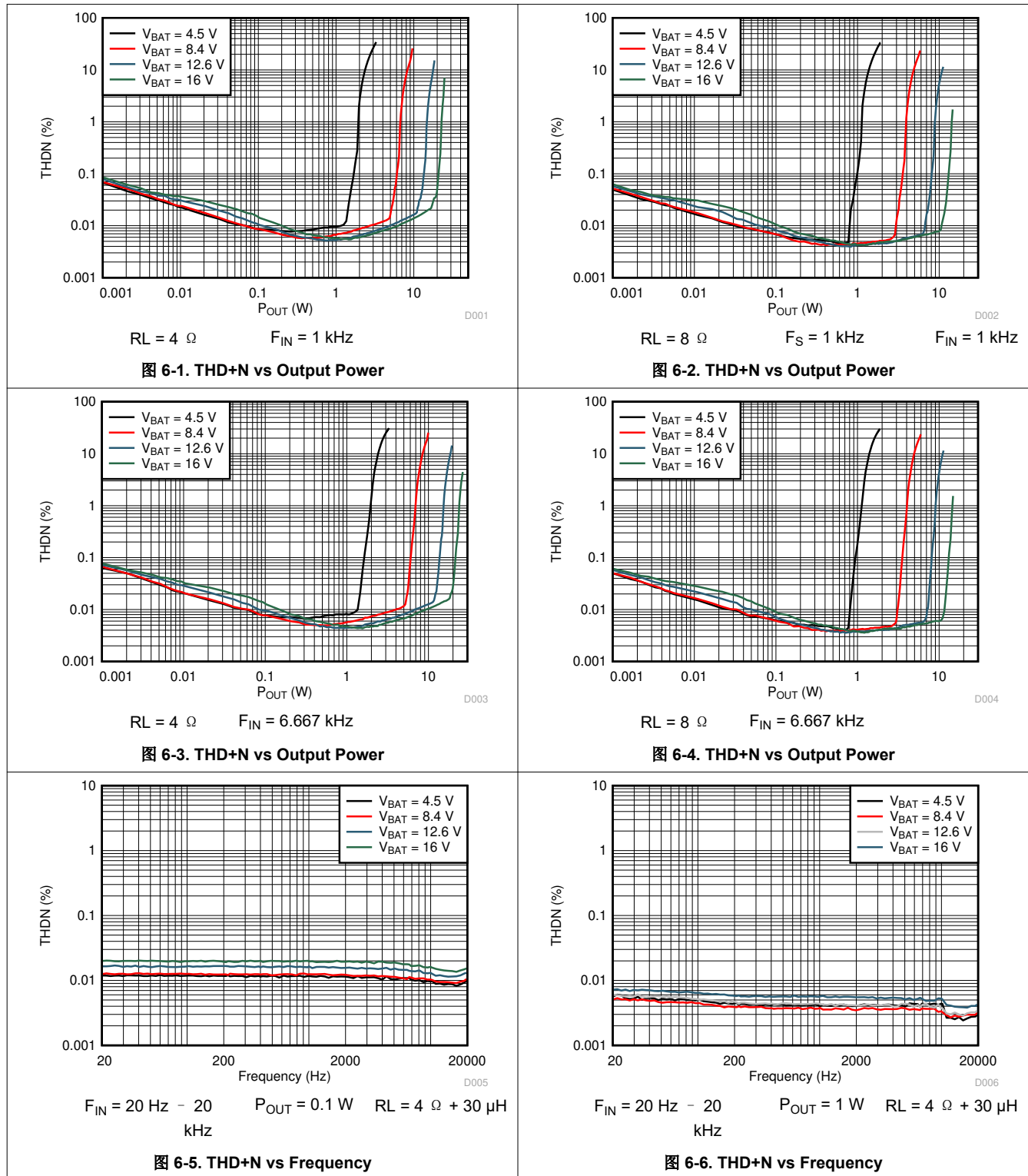
6.8 PDM Port Timing Requirements

 $T_A = 25\text{ }^\circ\text{C}$, AVDD = IOVDD = 1.8 V, 20 pF load on all outputs (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|-----------------------|-----|-----|-----|------|
| t _{SU} (PDM) PDM IN setup time | | 20 | | | ns |
| t _{HLD} (PDM) PDM IN hold time | | 3 | | | ns |
| t _r (PDM) PDM IN rise time | 10 % - 90 % Rise Time | | | 4 | ns |
| t _f (PDM) PDM IN fall time | 90 % - 10 % Fall Time | | | 4 | ns |

6.9 Typical Characteristics

At $T_A = 25^\circ\text{C}$, $f_{\text{SPK_AMP}} = 384 \text{ kHz}$, input signal is 1 kHz Sine, unless otherwise noted. Filter used for Load Resistance is 30 μH , unless otherwise noted.



6.9 Typical Characteristics (continued)

At $T_A = 25^\circ\text{C}$, $f_{\text{SPK_AMP}} = 384 \text{ kHz}$, input signal is 1 kHz Sine, unless otherwise noted. Filter used for Load Resistance is 30 μH , unless otherwise noted.

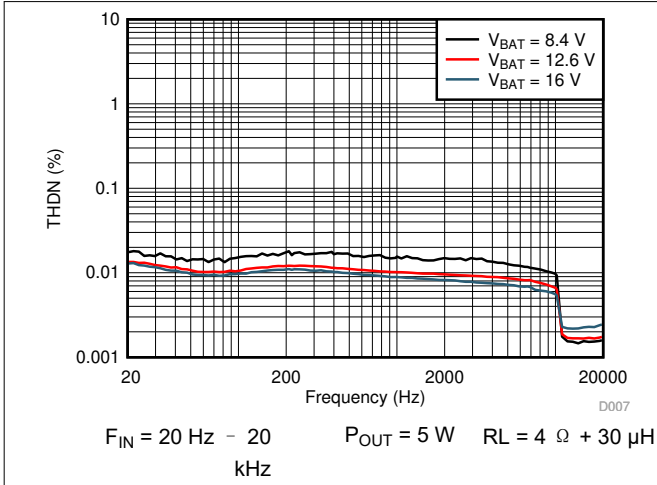


图 6-7. THD+N vs Frequency

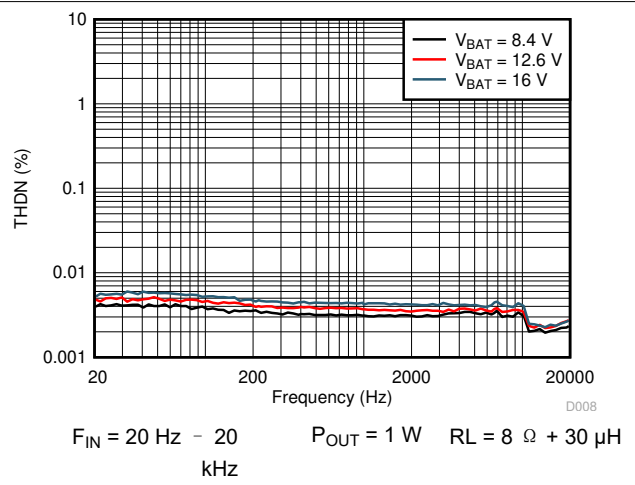


图 6-8. THD+N vs Frequency

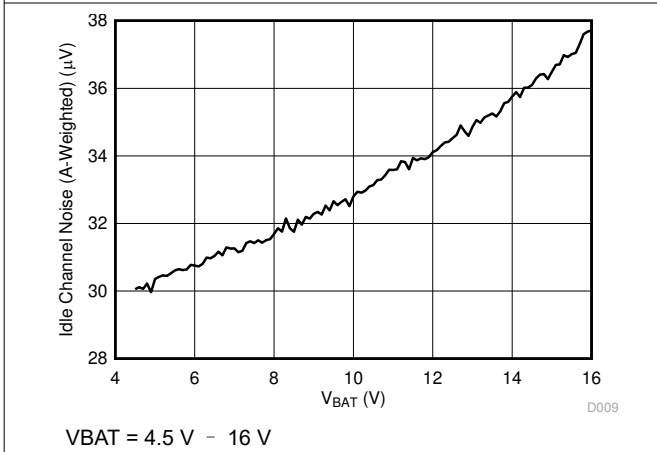


图 6-9. Idle Channel Noise (A-Weighted) vs V_{BAT}

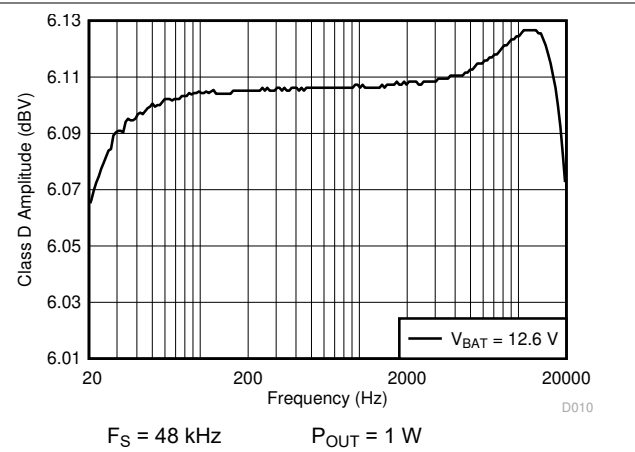


图 6-10. Amplitude vs Frequency

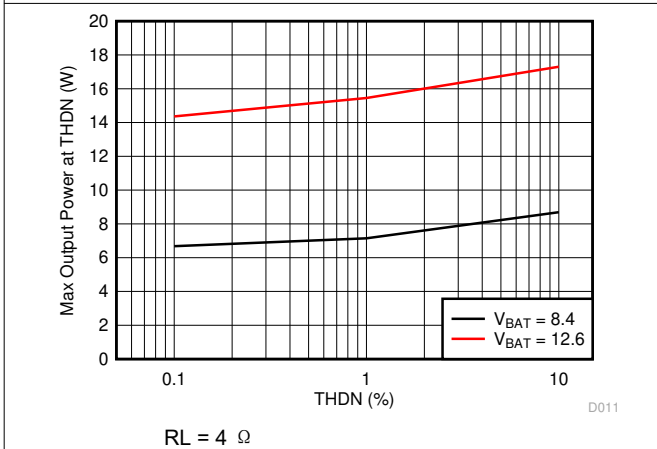


图 6-11. Max Output Power vs THD+N

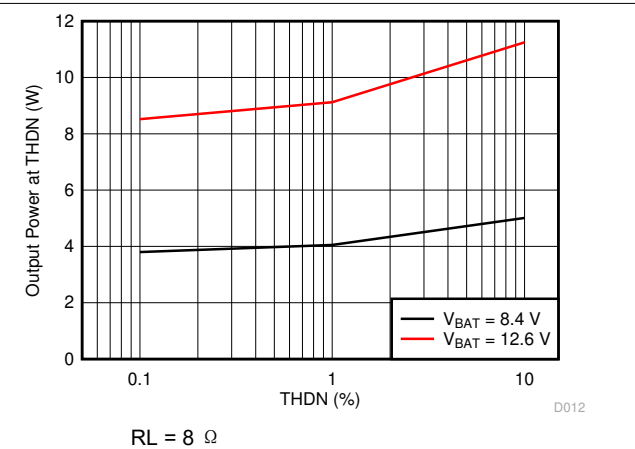
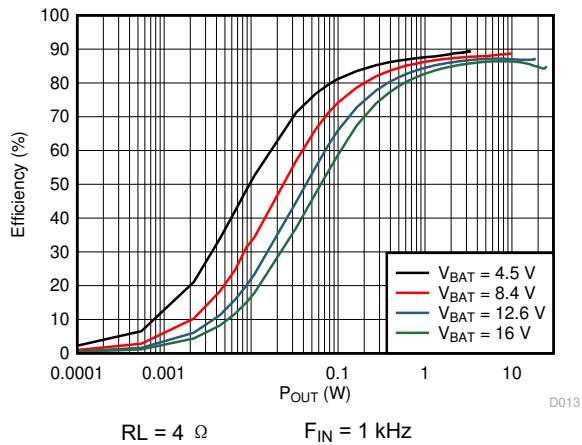


图 6-12. Max Output Power vs THD+N

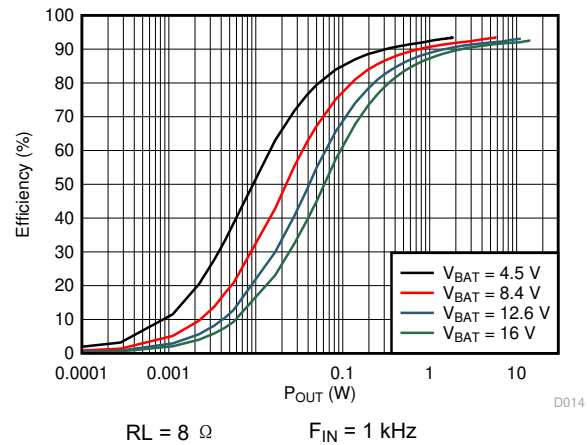
6.9 Typical Characteristics (continued)

At $T_A = 25^\circ\text{C}$, $f_{\text{SPK_AMP}} = 384 \text{ kHz}$, input signal is 1 kHz Sine, unless otherwise noted. Filter used for Load Resistance is 30 μH , unless otherwise noted.



RL = 4 Ω $F_{\text{IN}} = 1 \text{ kHz}$

图 6-13. Efficiency vs Output Power



RL = 8 Ω $F_{\text{IN}} = 1 \text{ kHz}$

图 6-14. Efficiency vs Output Power

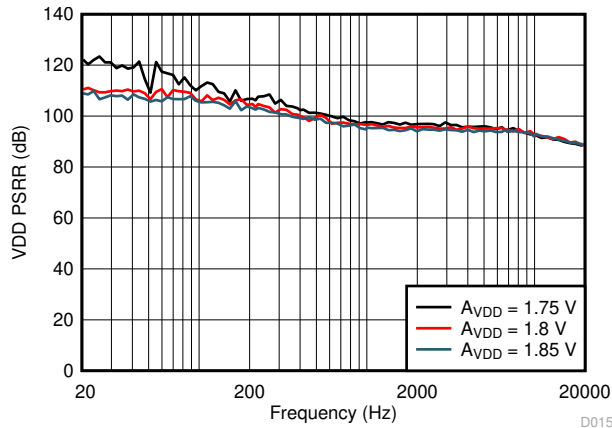


图 6-15. VDD PSRR vs Frequency

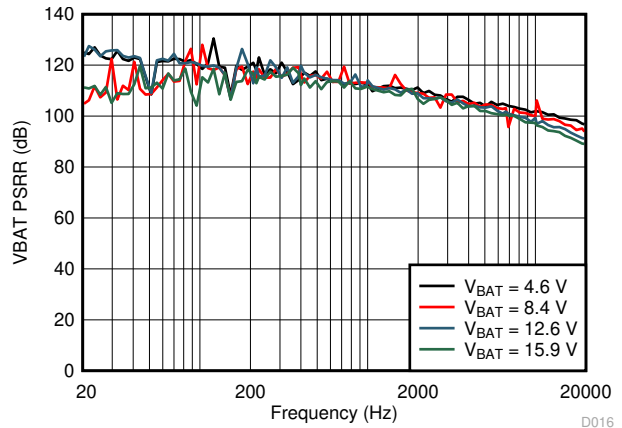
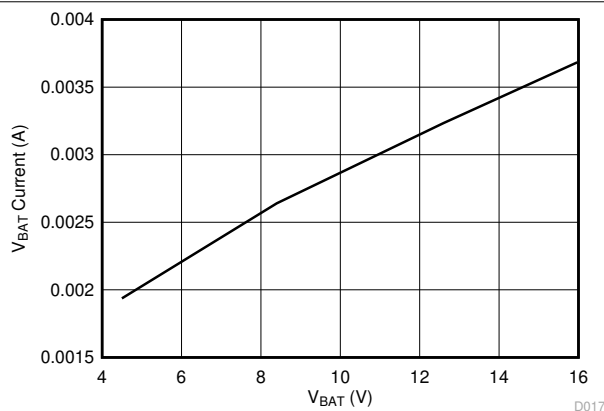
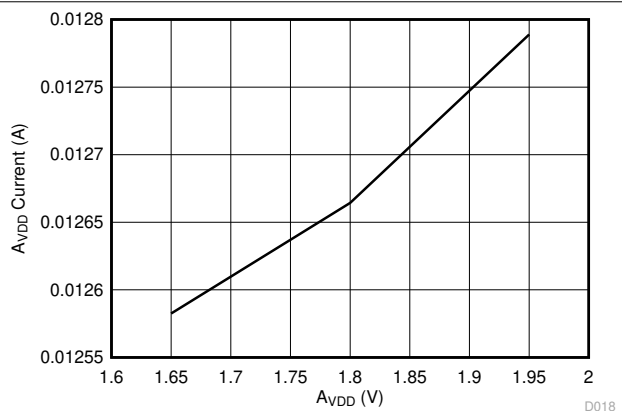


图 6-16. VBAT PSRR vs Frequency



$V_{\text{BAT}} = 4.5 \text{ V} - 16 \text{ V}$

图 6-17. V_{BAT} Idle Current vs V_{BAT}

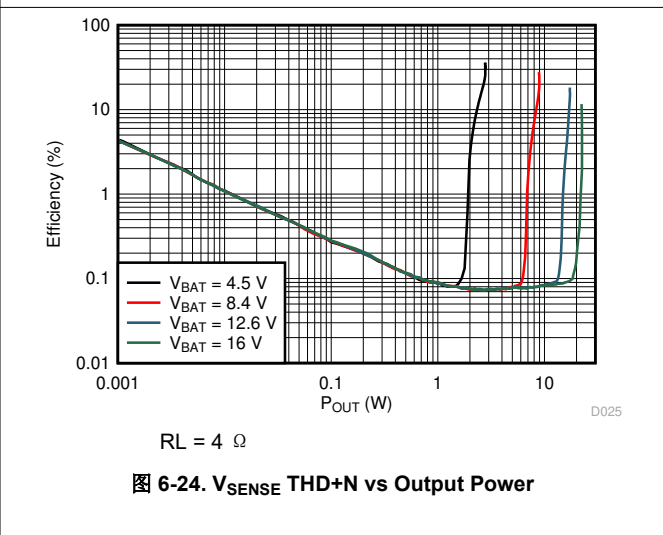
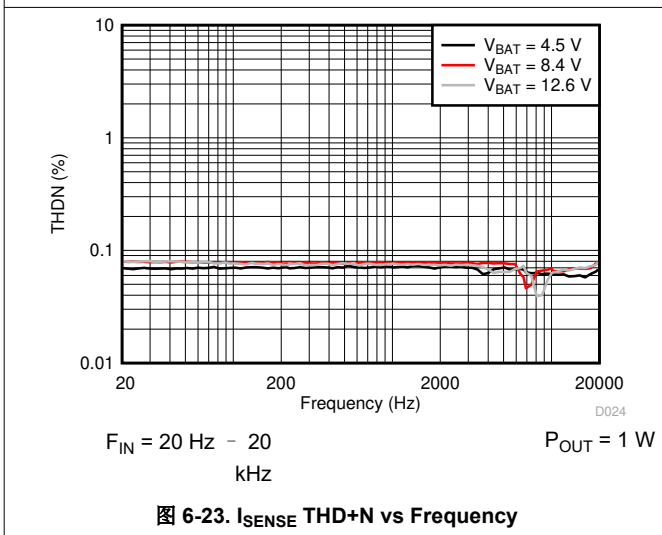
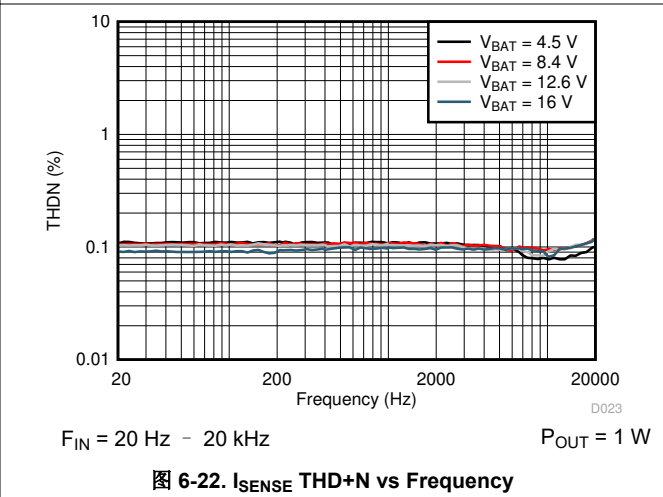
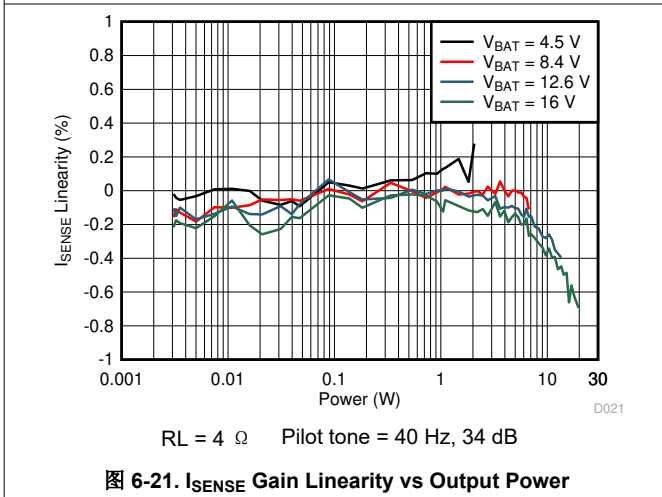
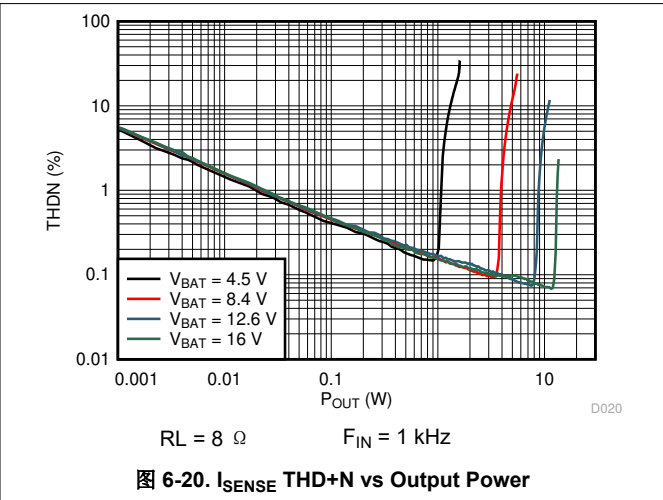
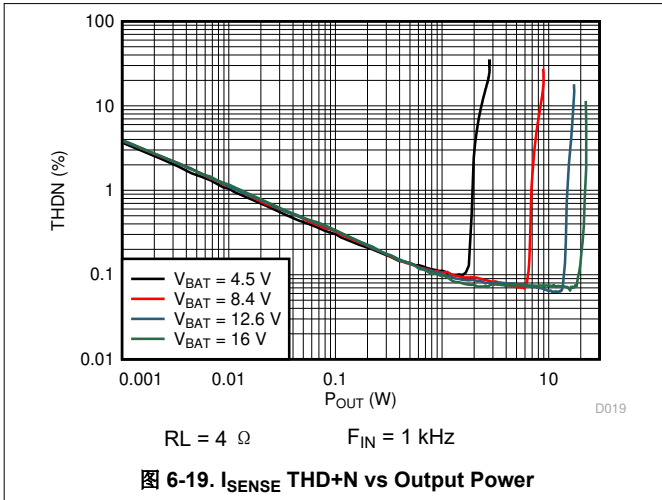


A. $A_{\text{VDD}} = 1.65 \text{ V} - 1.95 \text{ V}$ IV Sense Enabled

图 6-18. A_{VDD} Idle Current vs A_{VDD}

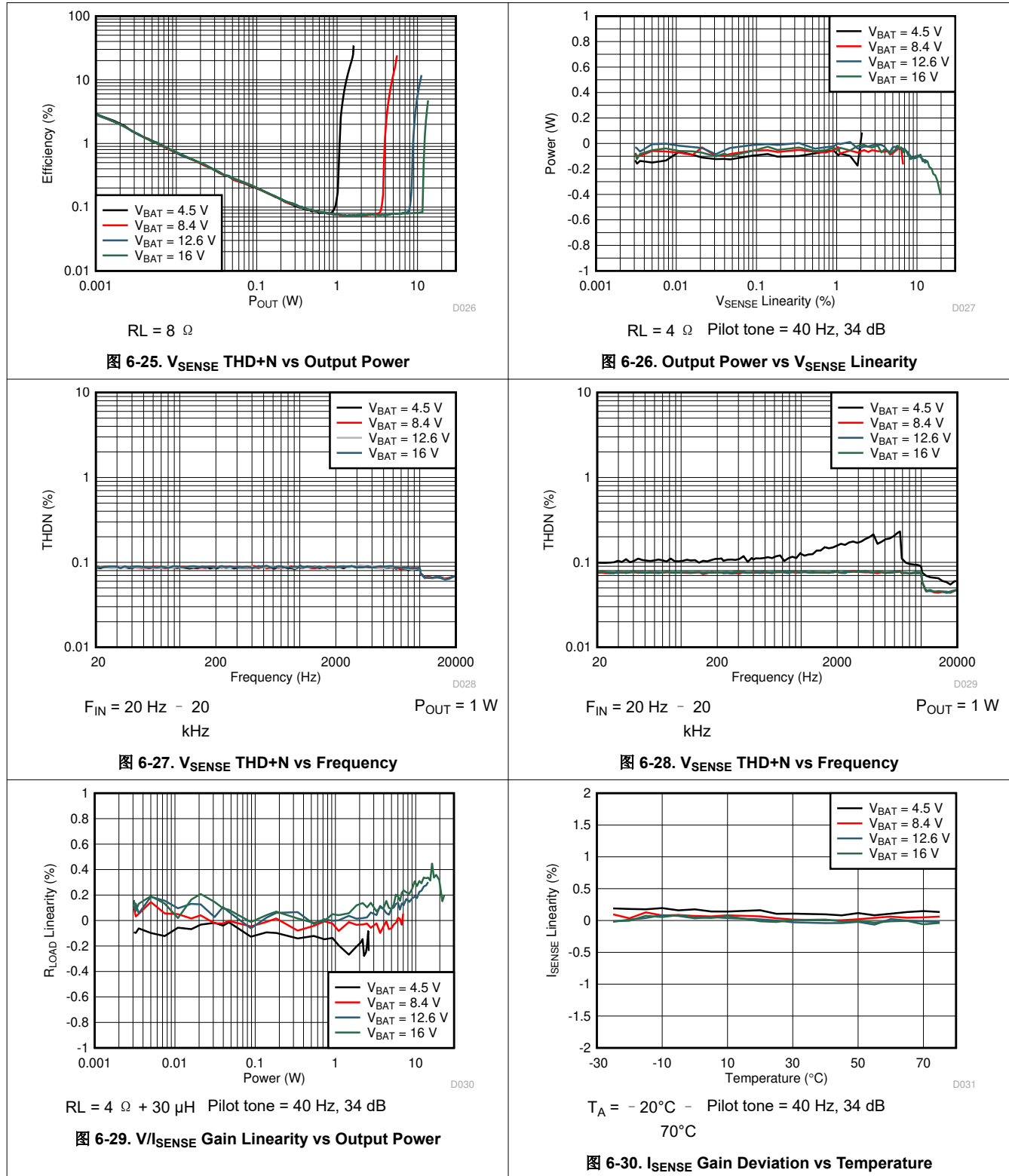
6.9 Typical Characteristics (continued)

At $T_A = 25^\circ\text{C}$, $f_{\text{SPK_AMP}} = 384 \text{ kHz}$, input signal is 1 kHz Sine, unless otherwise noted. Filter used for Load Resistance is 30 μH , unless otherwise noted.



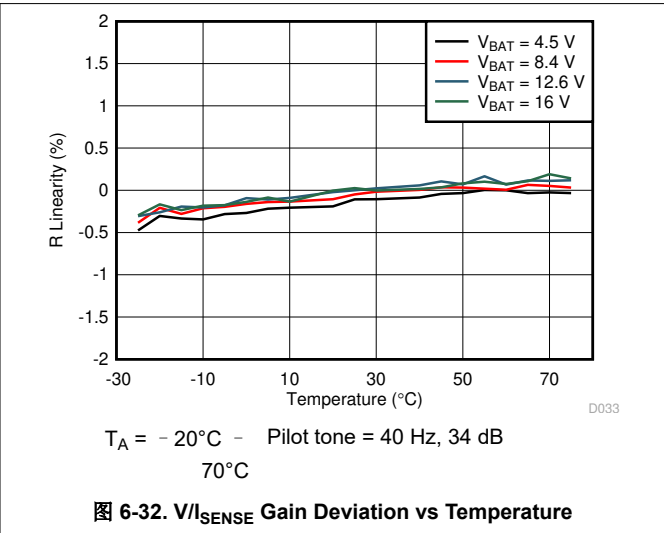
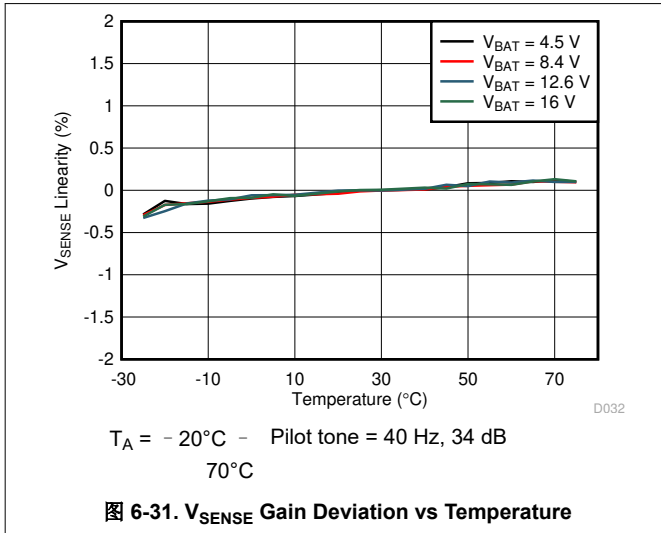
6.9 Typical Characteristics (continued)

At $T_A = 25^\circ\text{C}$, $f_{\text{SPK_AMP}} = 384\text{ kHz}$, input signal is 1 kHz Sine, unless otherwise noted. Filter used for Load Resistance is 30 μH , unless otherwise noted.



6.9 Typical Characteristics (continued)

At $T_A = 25^\circ\text{C}$, $f_{\text{SPK_AMP}} = 384 \text{ kHz}$, input signal is 1 kHz Sine, unless otherwise noted. Filter used for Load Resistance is 30 μH , unless otherwise noted.



7 Parameter Measurement Information

All typical characteristics for the devices are measured using the Bench EVM and an Audio Precision SYS-2722 Audio Analyzer. A PSIA interface is used to allow the I²S interface to be driven directly into the SYS-2722. Speaker output terminals are connected to the Audio-Precision analyzer analog inputs through a differential-to-single ended(D2S) filter as shown below. The D2S filter contains a 1st order Passive pole at 120 kHz. The D2S filter ensures the TAS2770 high performance class-D amplifier sees a fully differential matched loading at its outputs. This prevents measurement errors due to loading effects of AUX-0025 filter on the class-D outputs.

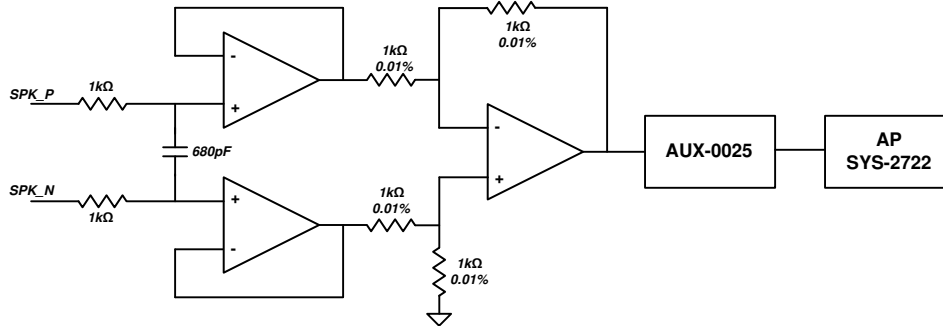


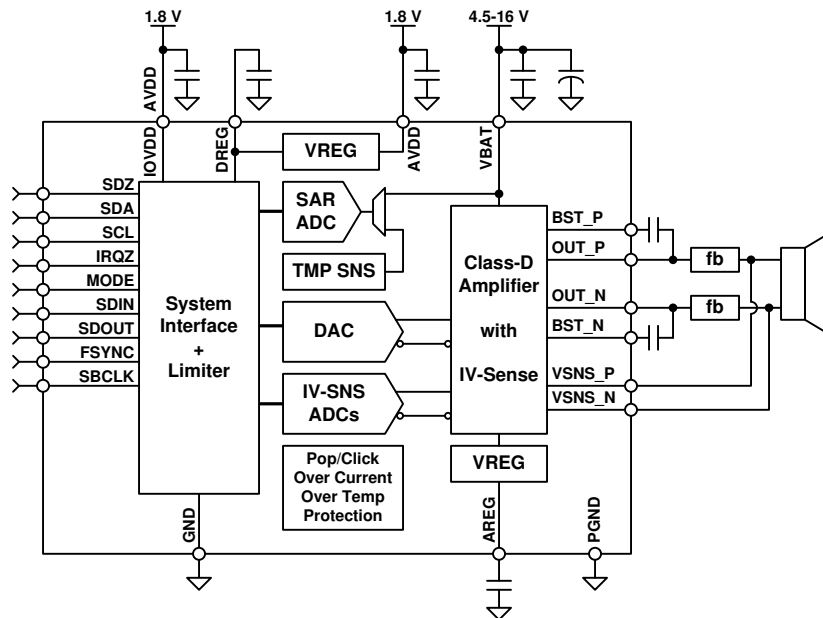
图 7-1. Differential To Single Ended (D2S) Filter

8 Detailed Description

8.1 Overview

The TAS2770 is a mono digital input Class-D amplifier optimized for mobile applications where efficient battery operation and small solution size are crucial. It integrates speaker voltage and current sensing and battery tracking limiting with brown out prevention. The device can operate in either TDM/I²C mode. Both modes support two PDM inputs that can be used for low latency playback or sensor aggregation.

8.2 Functional Block Diagram



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8.3 Feature Description

8.3.1 Device Mode and Address Selection

The TAS2770 can operate in two distinct operational modes, each with eight selectable device addresses. In TDM/I²C Mode, audio input and output are provided through the FSYNC, SBCLK, SDIN and SDOUT pins using formats including I²S, Left Justified and TDM. Configuration and status are provided through the SDA and SCL pins using the I²C protocol.

The PDM input can be used for a low latency playback path or as a sensor input.

表 8-1 below illustrates how to configure the device for TDM/I²C Mode. I²C slave addresses are shown left shifted by one bit with the R/W bit set to 0 (i.e. {ADDR[6:0], 1b0}). 5% or better tolerance resistors should be used for setting the mode configuration.

表 8-1. TDM/I²C Mode Address Selection

| MODE PIN | I2C SLAVE ADDRESS | |
|-----------------|-------------------|---------|
| | TAS5770LC0 | TAS2770 |
| Short to GND | 0x62 | 0x82 |
| 470 Ω to GND | 0x64 | 0x84 |
| 470 Ω to IOVDD | 0x66 | 0x86 |
| 2.2 KΩ to GND | 0x68 | 0x88 |
| 2.2 KΩ to IOVDD | 0x6A | 0x8A |
| 10 KΩ to GND | 0x6C | 0x8C |
| 10 KΩ to IOVDD | 0x6E | 0x8E |

表 8-1. TDM/I²C Mode Address Selection (continued)

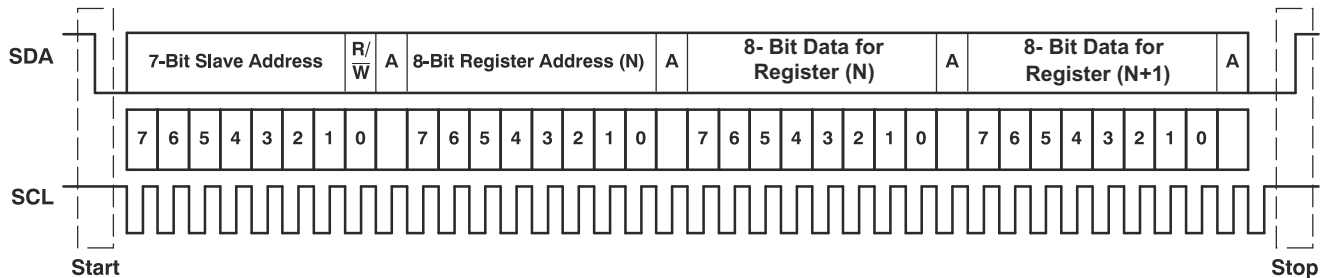
| MODE PIN | I ² C SLAVE ADDRESS | |
|------------------------|--------------------------------|---------|
| | TAS5770LC0 | TAS2770 |
| 47 K Ω to IOVDD | 0x70 | 0x90 |

8.3.2 General I²C Operation

The I²C bus employs two signals, SDA (data) and SCL (clock), to communicate between integrated circuits in a system using serial data transmission. The address and data 8-bit bytes are transferred most-significant bit (MSB) first. In addition, each byte transferred on the bus is acknowledged by the receiving device with an acknowledge bit. Each transfer operation begins with the master device driving a start condition on the bus and ends with the master device driving a stop condition on the bus. The bus uses transitions on the data terminal (SDA) while the clock is at logic high to indicate start and stop conditions. A high-to-low transition on SDA indicates a start, and a low-to-high transition indicates a stop. Normal data-bit transitions must occur within the low time of the clock period. shows a typical sequence.

The master generates the 7-bit slave address and the read/write (R/W) bit to open communication with another device and then waits for an acknowledge condition. The device holds SDA low during the acknowledge clock period to indicate acknowledgment. When this occurs, the master transmits the next byte of the sequence. Each device is addressed by a unique 7-bit slave address plus R/W bit (1 byte). All compatible devices share the same signals via a bi-directional bus using a wired-AND connection.

Use external pull-up resistors for the SDA and SCL signals to set the logic-high level for the bus. Use pull-up resistors between 2 k Ω and 4.7 k Ω . Do not allow the SDA and SCL voltages to exceed the device supply voltage, IOVDD.

图 8-1. Typical I²C Sequence

There is no limit on the number of bytes that can be transmitted between start and stop conditions. When the last word transfers, the master generates a stop condition to release the bus. 图 8-1 shows a generic data transfer sequence.

8.3.3 Single-Byte and Multiple-Byte Transfers

The serial control interface supports both single-byte and multiple-byte read/write operations for all registers. During multiple-byte read operations, the TAS2770 responds with data, a byte at a time, starting at the register assigned, as long as the master device continues to respond with acknowledges.

The TAS2770 supports sequential I²C addressing. For write transactions, if a register is issued followed by data for that register and all the remaining registers that follow, a sequential I²C write transaction has taken place. For I²C sequential write transactions, the register issued then serves as the starting point, and the amount of data subsequently transmitted, before a stop or start is transmitted, determines to how many registers are written.

8.3.4 Single-Byte Write

As shown in 图 8-2, a single-byte data-write transfer begins with the master device transmitting a start condition followed by the I²C device address and the read/write bit. The read/write bit determines the direction of the data transfer. For a write-data transfer, the read/write bit must be set to 0. After receiving the correct I²C device address and the read/write bit, the TAS2770 responds with an acknowledge bit. Next, the master transmits the

register byte corresponding to the device internal memory address being accessed. After receiving the register byte, the device again responds with an acknowledge bit. Finally, the master device transmits a stop condition to complete the single-byte data-write transfer.

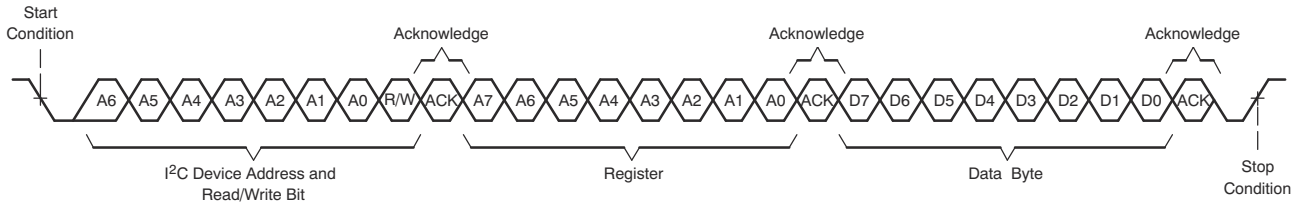


图 8-2. Single-Byte Write Transfer

8.3.5 Multiple-Byte Write and Incremental Multiple-Byte Write

A multiple-byte data write transfer is identical to a single-byte data write transfer except that multiple data bytes are transmitted by the master device to the TAS2770 as shown in 图 8-3. After receiving each data byte, the device responds with an acknowledge bit.

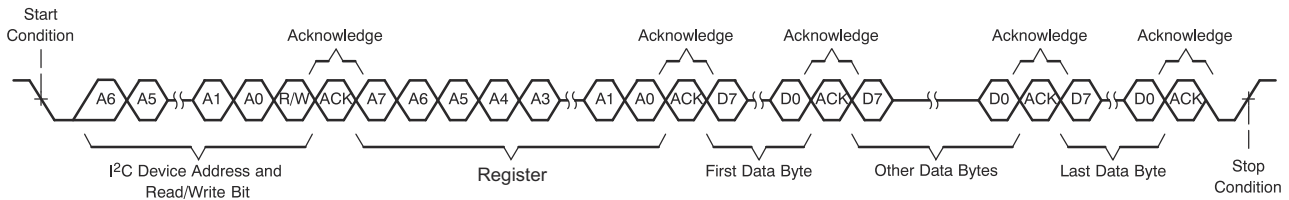


图 8-3. Multi-Byte Write Transfer

8.3.6 Single-Byte Read

As shown in 图 8-4, a single-byte data-read transfer begins with the master device transmitting a start condition followed by the I2C device address and the read/write bit. For the data-read transfer, both a write followed by a read are actually done. Initially, a write is done to transfer the address byte of the internal memory address to be read. As a result, the read/write bit is set to a 0.

After receiving the TAS2770 address and the read/write bit, the device responds with an acknowledge bit. The master then sends the internal memory address byte, after which the device issues an acknowledge bit. The master device transmits another start condition followed by the TAS2770 address and the read/write bit again. This time, the read/write bit is set to 1, indicating a read transfer. Next, the TAS2770 transmits the data byte from the memory address being read. After receiving the data byte, the master device transmits a not-acknowledge followed by a stop condition to complete the single-byte data read transfer.

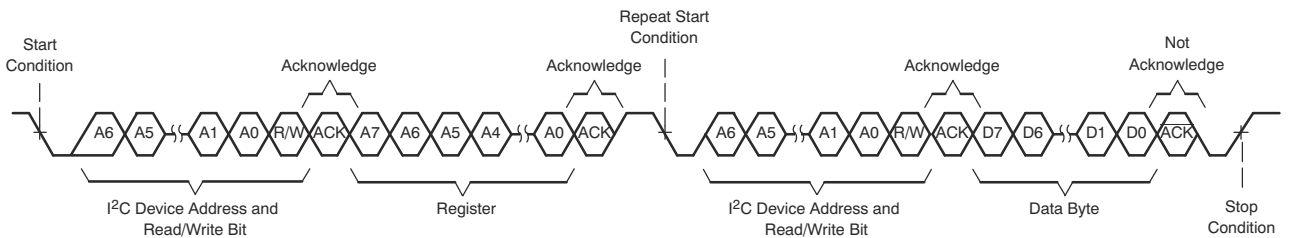


图 8-4. Single-Byte Read Transfer

8.3.7 Multiple-Byte Read

A multiple-byte data-read transfer is identical to a single-byte data-read transfer except that multiple data bytes are transmitted by the TAS2770 to the master device as shown in 图 8-5. With the exception of the last data byte, the master device responds with an acknowledge bit after receiving each data byte.

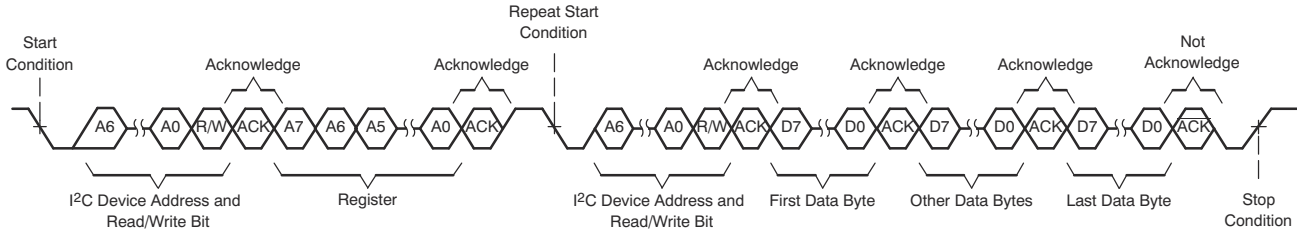


图 8-5. Multi-Byte Read Transfer

8.3.8 Register Organization

Device configuration and coefficients are stored using a page and book scheme. Each page contains 128 bytes and each book contains 256 pages. All device configuration registers are stored in book 0, page 0, which is the default setting at power up (and after a software reset). The book and page can be set by the *BOOK[7:0]* and *PAGE[7:0]* registers respectively.

8.4 Device Functional Modes

8.4.1 PDM Input

The TAS2770 provides one PDM input that can be used for low latency audio playback or sensor aggregation in TDM/I²C mode. 图 8-6 below illustrates the double data rate nature of the PDM inputs. Each input has two interleaved PDM channels, one sampled by the rising edge and the other by the falling edge of the clock.

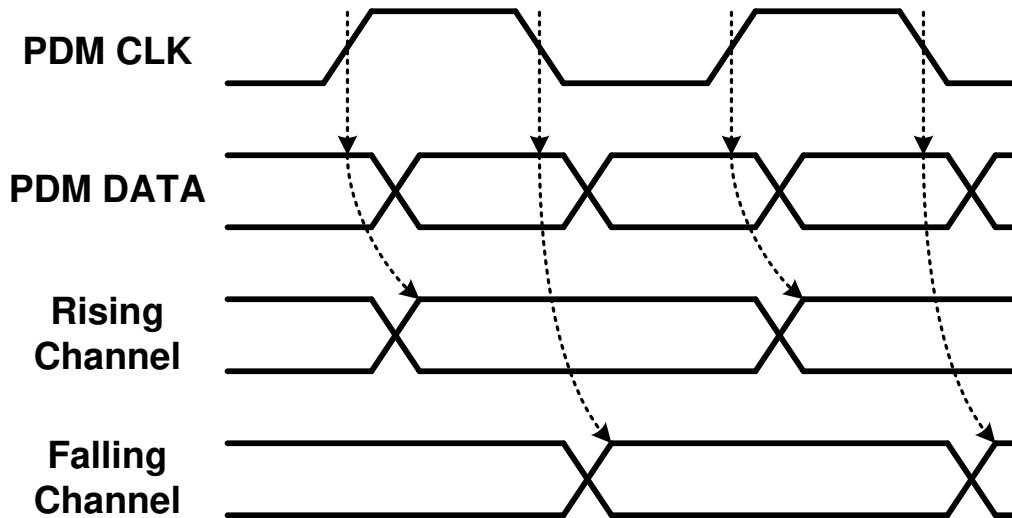


图 8-6. PDM Waveform

The PDM inputs are sampled by the PDMCK pin, which can be independently configured as either a PDM clock slave input or a PDM clock master output. The *PDM_EDGE[1:0]* and *PDM_SLV[1:0]* register bits select the sample clock edge and master/slave mode for each of the two PDM inputs. In master mode the PDMCK pin can disable the clocks (and drive a logic 0) by setting the *PDM_GATE[1:0]* register bits low. The *PDM_CLK[1:0]* register bits select which clock is used to sample each PDM input.

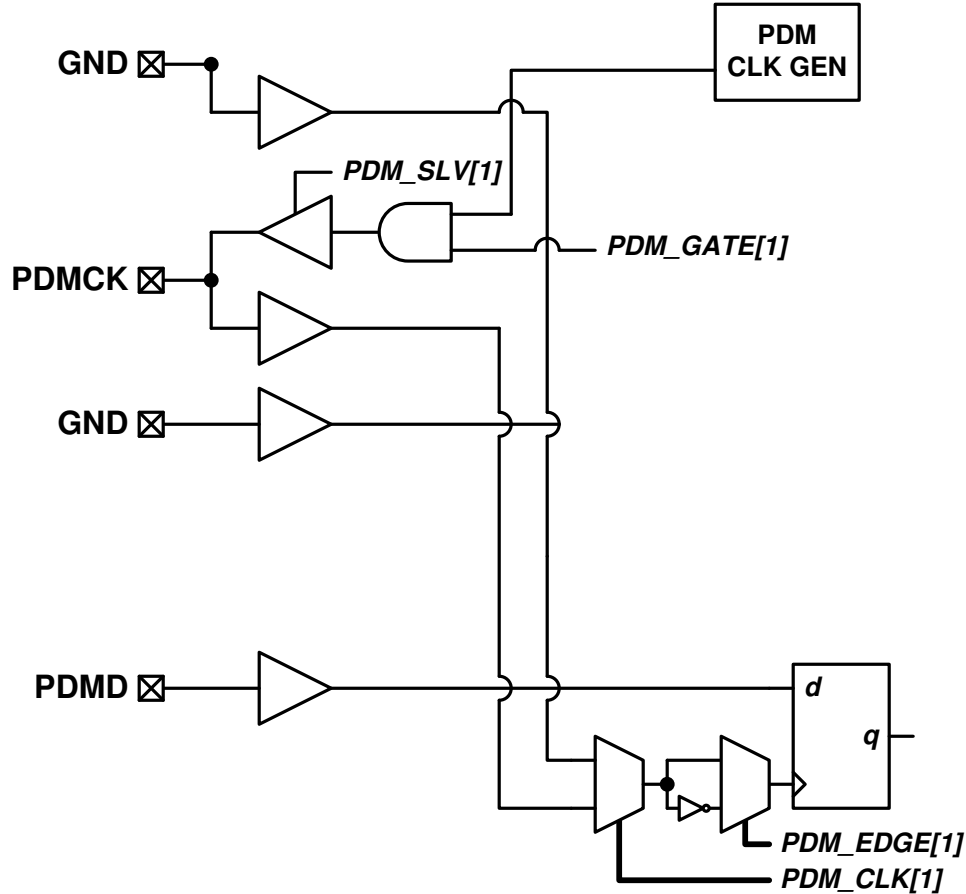


图 8-7. PDM Data and Clock Input Block Diagram

When configured as a clock slave, the PDM clock input does not require a specific phase relationship to the system clock (SBCLK in TDM/I²C Mode), but must have an exact frequency relationship to the audio sample rate. This is equivalent to 64/32/16 (~3 MHz) or 128/64/32 (~6 MHz) times a single/double/quadruple speed sample rate. The PDM rate is set by the *PDM_RATE1[1:0]* register bits.

When the PDMCK pin is configured as a clock master, the TAS2770 will output a 50% duty cycle clock of frequency that is set by the *PDM_RATE1[1:0]* register bits (64/32/16 or 128/64/32 times a single/double/quadruple speed sample rate).

The *PDM_MAP* register bit selects which PDM pin is used for audio playback input and which is used for PDM sensor input. The PDM sensor input can be decimated (time aligned with the IV sense) and transmitted on the SDOOUT pin when the device is in TDM/I²C mode.

表 8-2. PDM Input Capture Edge

| PDM Input Pin | Register Bit | Value | Capture Edge |
|---------------|--------------------|-------|------------------|
| PDMD | <i>PDM_EDGE[1]</i> | 0 | Rising (default) |
| | | 1 | Falling |

表 8-3. PDM Clock Slave

| PDM Input Pin | Register Bit | Value | Master/Slave |
|---------------|-------------------|-------|-----------------|
| PDMD | <i>PDM_SLV[1]</i> | 0 | Slave (default) |
| | | 1 | Master |

表 8-4. PDM Clock Select

| PDM Input Pin | Register Bit | Value | Clock Source |
|---------------|--------------|-------|-----------------|
| PDMD | PDM_CLK[1] | 0 | GND |
| | | 1 | PDMCK (default) |

表 8-5. PDM Master Mode Clock Gate

| PDM Clock Pin | Register Bit | Value | Gating |
|---------------|--------------|-------|---------------------|
| PDMCK | PDM_GATE[1] | 0 | Gated Off (default) |
| | | 1 | Active |

表 8-6. PDM Input Sample Rate

| PDM Input Pin | Register Bits | Value | Sample Rate |
|---------------|--------------------|-------|---------------------------|
| PDMD | PDM_RATE 1[1:0] | 00 | 2.54 - 3.38 MHz (default) |
| | | 01 | 5.08 - 6.76 MHz |
| | | 10 | Reserved |
| | | 11 | Reserved |

表 8-7. PDM Pin Mapping

| PDM_MAP | Mapping |
|---------|-------------------------------------|
| 0 | PDMD pin for sensor input (default) |
| 1 | PDMD pin for playback |

8.4.2 TDM Port

The TAS2770 provides a flexible TDM serial audio port for use in TDM/I²C Mode. The port can be configured to support a variety of formats including stereo I²S, Left Justified and TDM. Mono audio playback is available via the SDIN pin. The SDOUT pin is used to transmit sample streams including speaker voltage and current sense, VBAT voltage, die temperature and channel gain.

The TDM serial audio port supports up to 8 32-bit time slots at 44.1/48 kHz, 4 32-bit time slots at a 88.2/96 kHz sample rate and 2 32-bit time slots at a 176.4/192 kHz sample rate. The device supports 2 time slots at 32 bits in width and 4 or 8 time slots at 16, 24 or 32 bits in width. Valid SBCLK to FSYNC ratios are 64, 96, 128, 192, and 256.. Note that the device will automatically detect the number of time slots and this does not need to be programmed.

By default, the TAS2770 will automatically detect the PCM playback sample rate. This can be disabled by setting the *AUTO_RATE* register bit high.

The *SAMP_RATE[2:0]* register bits set the PCM audio sample rate when *AUTO_RATE* = 1. The TAS2770 employs a robust clock fault detection engine that will automatically volume ramp down the playback path if FSYNC does not match the configured sample rate (if *AUTO_RATE* = 1) or the ratio of SBCLK to FSYNC is not supported (minimizing any audible artifacts). Once the clocks are detected to be valid in both frequency and ratio, the device will automatically volume ramp the playback path back to the configured volume and resume playback.

表 8-8. PCM Auto Sample Rate Detection

| AUTO_RATE | Setting |
|-----------|-------------------|
| 0 | Enabled (default) |

表 8-8. PCM Auto Sample Rate Detection (continued)

| AUTO_RATE | Setting |
|-----------|----------|
| 1 | Disabled |

表 8-9. PCM Audio Sample Rates

| SAMP_RATE[1:0] | Sample Rate |
|----------------|-----------------------------|
| 000 | Reserved |
| 001 | Reserved |
| 010 | Reserved |
| 011 | 44.1 kHz / 48 kHz (default) |
| 100 | 88.2 kHz / 96 kHz |
| 101 | 176.4 kHz / 192 kHz |
| 110 | Reserved |
| 111 | Reserved |

图 8-8 和 图 8-9 下方说明了接收器帧参数，用于配置端口以进行播放。帧以 FSYNC 从高位到低位或从低位到高位（由 *FRAME_START* 寄存器位设置）的过渡开始。FSYNC 和 SDIN 由 SBCLK 的上升沿或下降沿（由 *RX_EDGE* 寄存器位设置）采样。RX_OFFSET[4:0] 寄存器位定义了从 FSYNC 的过渡到时间槽 0 的开始所需的 SBCLK 周期数。这通常设置为左对齐格式的值 0 和 I²S 格式的值 1。

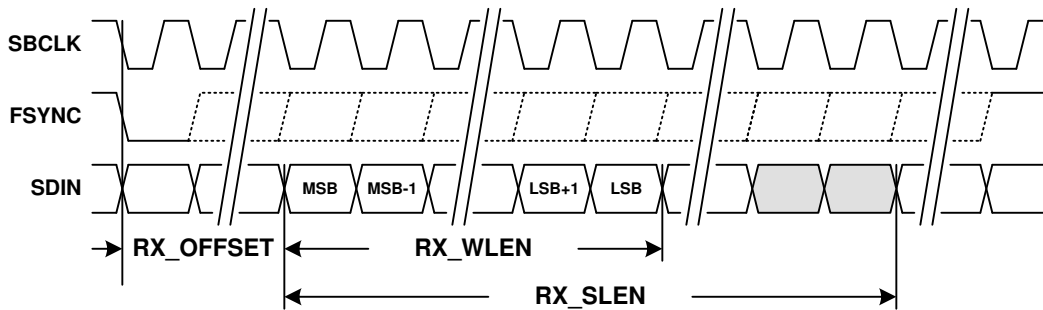


图 8-8. TDM RX Time Slot with Left Justification

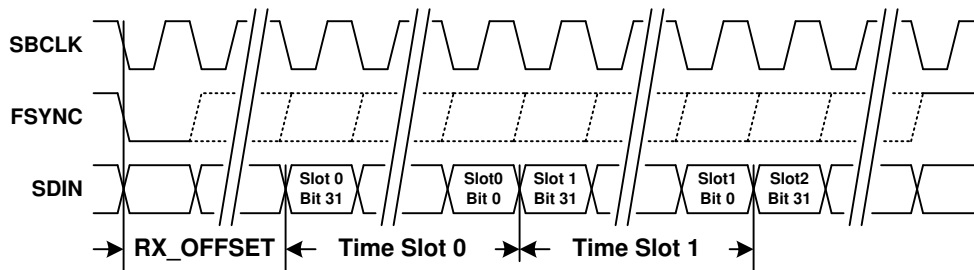


图 8-9. TDM RX Time Slots

表 8-10. TDM Start of Frame Polarity

| FRAME_START | Polarity |
|-------------|----------------------|
| 0 | Low to High on FSYNC |

表 8-10. TDM Start of Frame Polarity (continued)

| FRAME_START | Polarity |
|-------------|--------------------------------|
| 1 | High to Low on FSYNC (default) |

表 8-11. TDM RX Capture Polarity

| RX_EDGE | FSYNC and SDIN Capture Edge |
|---------|--------------------------------|
| 0 | Rising edge of SBCLK (default) |
| 1 | Falling edge of SBCLK |

表 8-12. TDM RX Start of Frame to Time Slot 0 Offset

| RX_OFFSET[4:0] | SBCLK Cycles |
|----------------|--------------|
| 0x00 | 0 |
| 0x01 | 1 (default) |
| 0x02 | 2 |
| ... | ... |
| 0x1E | 30 |
| 0x1F | 31 |

The *RX_SLEN[1:0]* register bits set the length of the RX time slot. The length of the audio sample word within the time slot is configured by the *RX_WLEN[1:0]* register bits. The RX port will left justify the audio sample within the time slot by default, but this can be changed to right justification via the *RX_JUSTIFY* register bit. The TAS2770 supports mono and stereo down mix playback ($[L+R]/2$) via the left time slot, right time slot and time slot configuration register bits (*RX_SLOT_L[3:0]*, *RX_SLOT_R[3:0]* and *RX_SCFG[1:0]* respectively). By default the device will playback mono from the time slot equal to the I²C base address offset (set by the MODE pin) for playback. The *RX_SCFG [1:0]* register bits can be used to override the playback source to the left time slot, right time slot or stereo down mix set by the *RX_SLOT_L[3:0]* and *RX_SLOT_R[3:0]* register bits.

If time slot selections places reception either partially or fully beyond the frame boundary, the receiver will return a null sample equivalent to a digitally muted sample.

表 8-13. TDM RX Time Slot Length

| RX_SLEN[1:0] | Time Slot Length |
|--------------|-------------------|
| 00 | 16-bits |
| 01 | 24-bits |
| 10 | 32-bits (default) |
| 11 | reserved |

表 8-14. TDM RX Sample Word Length

| RX_WLEN[1:0] | Length |
|--------------|-------------------|
| 00 | 16-bits |
| 01 | 20-bits |
| 10 | 24-bits (default) |
| 11 | 32-bits |

表 8-15. TDM RX Sample Justification

| <i>RX_JUSTIFY</i> | Justification |
|-------------------|----------------|
| 0 | Left (default) |
| 1 | Right |

表 8-16. TDM RX Time Slot Select Configuration

| <i>RX_SCFG[1:0]</i> | Config Origin |
|---------------------|--|
| 00 | Mono with Time Slot equal to I ² C Address Offset (default) |
| 01 | Mono Left Channel |
| 10 | Mono Right Channel |
| 11 | Stereo Down Mix [L+R]/2 |

表 8-17. TDM RX Left Channel Time Slot

| <i>RX_SLOT_L[3:0]</i> | Time Slot |
|-----------------------|-------------|
| 0x0 | 0 (default) |
| 0x1 | 1 |
| ... | ... |
| 0xE | 14 |
| 0xF | 15 |

表 8-18. TDM RX Right Channel Time Slot

| <i>RX_SLOT_R[3:0]</i> | Time Slot |
|-----------------------|-------------|
| 0x0 | 0 (default) |
| 0x1 | 1 |
| ... | ... |
| 0xE | 14 |
| 0xF | 15 |

The TDM port can transmit a number sample streams on the SDOOUT pin including speaker voltage sense, speaker current sense, decimated PDM input, VBAT voltage, die temperature and channel gain. 图 8-10 below illustrates the alignment of time slots to the beginning of a frame and how a given sample stream is mapped to time slots. Either the rising or falling edge of SBCLK can be used to transmit data on the SDOOUT pin, which can be configured by setting the *TX_EDGE* register bit. The *TX_OFFSET[2:0]* register bits define the number SBCLK cycles between the start of a frame and the beginning of time slot 0. This would typically be programmed to 0 for Left Justified format and 1 for I²S format. The TDM TX can either transmit logic 0 or Hi-Z depending on the setting of the *TX_FILL* register bit setting. An optional bus keeper will weakly hold the state of SDOOUT when all devices driving are Hi-Z. Since only one bus keeper is required on SDOOUT, this feature can be disabled via the *TX_KEEPER* register bit.

Each sample stream is composed of either one or two 8-bit time slots. Speaker voltage sense, speaker current sense and decimated PDM sample streams are 16-bit precision, so they will always utilize two TX time slots. The VBAT voltage stream is 12-bit precision, and can either be transmitted left justified in a 16-bit word (using two time slots) or can be truncated to 8-bits (the top 8 MSBs) and be transmitted in a single time slot. This is configured by setting *VBAT_SLEN* register bit. The Die temperature and gain are both 8-bit precision and are transmitted in a single time slot.

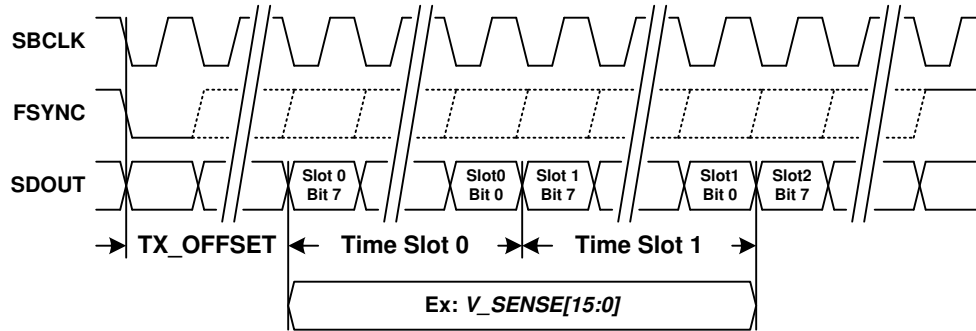


图 8-10. TDM Port TX Diagram

表 8-19. TDM TX Transmit Polarity

| TX_EDGE | SDOUT Transmit Edge |
|---------|---------------------------------|
| 0 | Rising edge of SBCLK |
| 1 | Falling edge of SBCLK (default) |

表 8-20. TDM TX Start of Frame to Time Slot 0 Offset

| TX_OFFSET[2:0] | SBCLK Cycles |
|----------------|--------------|
| 0x0 | 0 |
| 0x1 | 1 (default) |
| 0x2 | 2 |
| ... | ... |
| 0x6 | 6 |
| 0x7 | 7 |

表 8-21. TDM TX Unused Bit Field Fill

| TX_FILL | SDOUT Unused Bit Fields |
|---------|-------------------------|
| 0 | Transmit 0 |
| 1 | Transmit Hi-Z (default) |

表 8-22. TDM TX SDOUT Bus Keeper Enable

| TX_KEEPER | SDOUT Bus Keeper |
|-----------|-----------------------------|
| 0 | Disable bus keeper |
| 1 | Enable bus keeper (default) |

The time slot register for each sample stream defines where the MSB transmission begins. For instance, if $VSNS_SLOT[5:0]$ is set to 2, the upper 8 MSBs will be transmitted in time slot 2 and the lower 8 LSBs will be transmitted in time slot 3. Each sample stream can be individually enabled or disabled. This is useful to manage limited TDM bandwidth since it may not be necessary to transmit all streams for all devices on the bus.

It is important to ensure that time slot assignments for actively transmitted sample streams do not conflict. For instance, if $VSNS_SLOT[5:0]$ is set to 2 and $ISNS_SLOT[5:0]$ is set to 3, the lower 8 LSBs of voltage sense will conflict with the upper 8 MSBs of current sense. This will produce unpredictable transmission results in the conflicting bit slots (i.e. the priority is not defined).

If time slot selections place transmission beyond the frame boundary, the transmitter will truncate transmission at the frame boundary.

表 8-23. TDM Voltage Sense Time Slot

| <i>VSNS_SLOT[5:0]</i> | Slot |
|-----------------------|-------------|
| 0x00 | 0 (default) |
| 0x01 | 1 |
| 0x02 | 2 |
| ... | ... |
| 0x3E | 62 |
| 0x3F | 63 |

表 8-24. TDM Voltage Sense Transmit Enable

| <i>VSNS_TX</i> | State |
|----------------|--------------------|
| 0 | Disabled (default) |
| 1 | Enabled |

表 8-25. TDM Current Sense Time Slot

| <i>ISNS_SLOT[5:0]</i> | Slot |
|-----------------------|-------------|
| 0x00 | 0 |
| 0x01 | 1 |
| 0x02 | 2 (default) |
| ... | ... |
| 0x3E | 62 |
| 0x3F | 63 |

表 8-26. TDM Current Sense Transmit Enable

| <i>ISNS_TX</i> | State |
|----------------|--------------------|
| 0 | Disabled (default) |
| 1 | Enabled |

表 8-27. TDM Decimated PDM Input Time Slot

| <i>PDM_SLOT[5:0]</i> | Slot |
|----------------------|-------------|
| 0x00 | 0 |
| 0x01 | 1 |
| ... | ... |
| 0x04 | 4 (default) |
| ... | ... |
| 0x3E | 62 |
| 0x3F | 63 |

表 8-28. TDM Decimated PDM Input Transmit Enable

| <i>PDM_TX</i> | State |
|---------------|--------------------|
| 0 | Disabled (default) |
| 1 | Enabled |

表 8-29. TDM VBAT Time Slot

| VBAT_SLOT[5:0] | Slot |
|-----------------------|-------------|
| 0x00 | 0 |
| 0x01 | 1 |
| ... | ... |
| 0x06 | 6 (default) |
| ... | ... |
| 0x3E | 62 |
| 0x3F | 63 |

表 8-30. TDM VBAT Time Slot Length

| VBAT_SLEN | Slot Length |
|------------------|------------------------------|
| 0 | Truncate to 8-bits (default) |
| 1 | Left justify to 16-bits |

表 8-31. TDM VBAT Transmit Enable

| VBAT_TX | State |
|----------------|--------------------|
| 0 | Disabled (default) |
| 1 | Enabled |

表 8-32. TDM Temp Sensor Time Slot

| TEMP_SLOT[5:0] | Slot |
|-----------------------|-------------|
| 0x00 | 0 |
| 0x01 | 1 |
| ... | ... |
| 0x07 | 7 (default) |
| ... | ... |
| 0x3E | 62 |
| 0x3F | 63 |

表 8-33. TDM Temp Sensor Transmit Enable

| TEMP_TX | State |
|----------------|--------------------|
| 0 | Disabled (default) |
| 1 | Enabled |

表 8-34. TDM Limiter Gain Reduction Time Slot

| GAIN_SLOT[5:0] | Slot |
|-----------------------|-------------|
| 0x00 | 0 |
| 0x01 | 1 |
| ... | ... |
| 0x08 | 8 (default) |
| ... | ... |

表 8-34. TDM Limiter Gain Reduction Time Slot
(continued)

| GAIN_SLOT[5:0] | Slot |
|----------------|------|
| 0x3E | 62 |
| 0x3F | 63 |

表 8-35. TDM Limiter Gain Reduction Transmit
Enable

| GAIN_TX | State |
|---------|--------------------|
| 0 | Disabled (default) |
| 1 | Enabled |

8.4.3 Playback Signal Path

8.4.3.1 High Pass Filter

Excessive DC and low frequency content in audio playback signal can damage loudspeakers, so the TAS2770 employs a high-pass filter (HPF) to prevent this from occurring for the PCM playback path. No HPF is available in the PDM playback path. 表 8-36 below shows the -3 dB corner frequencies available for each sample rate set by register bits *HPF_FREQ[2:0]*. The filter can be bypassed by setting the *HPF_FREQ[2:0]* register to 3'b000. The HPF Bi-Quad filter coefficients can also be directly programmed via the TBD register bits.

表 8-36. HPF Filter Settings

| HPF_FREQ[2:0] | -3 dB FREQUENCY (Hz) | |
|---------------|----------------------|---------------|
| | 44.1/88.2/176.4 kHz | 48/96/192 kHz |
| 000 | bypass | bypass |
| 001 | 1.8 (default) | 2 (default) |
| 010 | 46 | 50 |
| 011 | 92 | 100 |
| 100 | 184 | 200 |
| 101 | 368 | 400 |
| 110 | 735 | 800 |
| 111 | Reserved | Reserved |

8.4.3.2 Digital Volume Control and Amplifier Output Level

The gain from audio input to speaker terminals is controlled by setting the amplifier's output level and digital volume control (DVC). A separate DVC is provided for PDM (available from the PDM input pins) and PCM (available from the TDM ports pins) playback paths.

Amplifier output level settings are presented in dBV (dB relative to 1 V_{rms}) with a full scale digital audio input (0 dBFS) and the digital volume control set to 0 dB. It should be noted that these levels may not be achievable because of analog clipping in the amplifier, so they should be used to convey gain only. 表 8-37 below shows analog gain settings that can be programmed via the *AMP_LEVEL[4:0]* register bits.

表 8-37. Amplifier Output Level Settings

| AMP_LEVEL[4:0] | FULL SCALE OUTPUT | |
|----------------|-------------------|-----------------------|
| | dBV | V _{PEAK} (V) |
| 0x00 | 11.0 | 5.02 |
| 0x01 | 11.5 | 5.32 |

表 8-37. Amplifier Output Level Settings (continued)

| AMP_LEVEL[4:0] | FULL SCALE OUTPUT | |
|----------------|-------------------|-----------------------|
| | dBV | V _{PEAK} (V) |
| 0x02 | 12.0 | 5.63 |
| 0x03 | 12.5 | 5.96 |
| 0x04 | 13.0 | 6.32 |
| 0x05 | 13.5 | 6.69 |
| 0x06 | 14.0 | 7.09 |
| 0x07 | 14.5 | 7.51 |
| 0x08 | 15.0 | 7.95 |
| 0x09 | 15.5 | 8.42 |
| 0x0A | 16.0 | 8.92 |
| 0x0B | 16.5 | 9.45 |
| 0x0C | 17.0 | 10.0 |
| 0x0D | 17.5 | 10.6 |
| 0x0E | 18.0 | 11.2 |
| 0x0F | 18.5 | 11.9 |
| 0x10 | 19.0 (default) | 12.6 (default) |
| 0x11 | 19.5 | 13.4 |
| 0x12 | 20.0 | 14.1 |
| 0x13 | 20.5 | 14.98 |
| 0x14 | 21.0 | 15.87 |
| 0x15 - 0x1F | Reserved | Reserved |

方程式 1 calculates the amplifiers output voltage.

$$V_{AMP} = \text{Input} + A_{dvc} + A_{AMP} \text{ dBV} \quad (1)$$

where

- V_{AMP} is the amplifier output voltage in dBV
- Input is the digital input amplitude in dB with respect to 0 dBFS
- A_{dvc} is the digital volume control setting, 0 dB to -100 dB in 0.5 dB steps
- A_{AMP} is the amplifier output level setting in dBV

The digital volume control (DVC) is independently configurable for PCM and PDM streams from 0 dB to -100 dB in 0.5 dB steps by setting the $DVC_PCM[7:0]$ and $PVC_PDM[7:0]$ register bits respectively. Settings greater than 0xC8 are interpreted as mute. When a change in digital volume control occurs, the device ramps the volume to the new setting based on the $DVC_RATE[1:0]$ register bits. If $DVC_RATE[1:0]$ is set to 2'b11, volume ramping is disabled. This can be used to speed up startup, shutdown and digital volume changes when volume ramping is handled by the system master.

表 8-38. PCM Digital Volume Control

| DVC_PCM[7:0] | Volume (dB) |
|--------------|-------------|
| 0x00 | 0 (default) |

表 8-38. PCM Digital Volume Control (continued)

| <i>DVC_PCM[7:0]</i> | Volume (dB) |
|---------------------|-------------|
| 0x01 | -0.5 |
| 0x02 | -1 |
| ... | ... |
| 0xC8 | -100 |
| 0xC9 - 0xFF | Mute |

表 8-39. PDM Digital Volume Control

| <i>DVC_PDM[7:0]</i> | Volume (dB) |
|---------------------|-------------|
| 0x00 | 0 (default) |
| 0x01 | -0.5 |
| 0x02 | -1 |
| ... | ... |
| 0xC8 | -100 |
| 0xC9 - 0xFF | Mute |

表 8-40. Digital Volume Ramp Rate

| <i>DVC_RAMP[1:0]</i> | Ramp Rate |
|----------------------|-------------------------------|
| 00 | 0.5 dB per 1 Sample (default) |
| 01 | 0.5 dB per 4 Samples |
| 10 | 0.5 dB per 8 Samples |
| 11 | Volume Ramping Disabled |

The Class-D amplifier uses a closed-loop architecture, so the gain does not depend on VBAT. The approximate threshold for the onset of analog clipping is calculated in [方程式 2](#).

$$V_{PK(max,preclip)} = V_{BAT} \times \left(\frac{R_L}{R_{FET(tot)} + R_{interconnect} + R_L} \right) V \quad (2)$$

where

- $V_{PK(max,preclip)}$ is the maximum peak unclipped output voltage in V
- V_{BAT} is the power supply voltage
- R_L is the speaker load in Ω
- $R_{interconnect}$ is the additional resistance in the PCB (such as cabling and filters) in Ω
- $R_{FET(on)}$ is the power stage total on resistance (HS FET+LS FET+Sense Resistor+bonding+packaging) in Ω

The effective on-resistance for this device (including HS+LS FET, Sense Resistor and bonding and packaging leads) is approximately 510 m Ω at room temperature. [表 8-41](#) shows approximate maximum unclipped peak output voltages at room temperature (excluding interconnect resistances).

表 8-41. Approximate Maximum Unclipped Peak Output Voltage at Room Temperature

| SUPPLY VOLTAGE VBAT (V) | MAXIMUM UNCLIPPED PEAK VOLTAGE V _{PK} (V) | |
|----------------------------|--|----------------------|
| | R _L = 4 Ω | R _L = 8 Ω |
| 8.4 | 7.45 | 7.90 |
| 12.6 | 11.18 | 11.84 |

8.4.3.3 Audio Playback Selection

Audio playback can be sourced from either PCM (through the TDM) or PDM (through the PDMD PDM Inputs) input sources through the *PB_SRC* register bit. The *PB_PDM_SRC* register bit determines the source of the PDM source.

表 8-42. Audio Playback Source

| <i>PB_SRC</i> | Source |
|---------------|---------------|
| 0 | PCM (default) |
| 1 | PDM |

表 8-43. PDM Playback Source

| <i>PB_PDM_SRC</i> | Source |
|-------------------|---|
| 0 | PDM input pin defined by PDM_MAP register bit (default) |
| 1 | Reserved |

8.4.3.4 Battery Tracking Limiter with Brown Out Prevention

The TAS2770 monitors battery voltage (VBAT) and the audio signal to automatically decrease gain when the audio signal peaks exceed a programmable threshold. This helps prevent clipping and extends playback time through end of charge battery conditions. The limiter threshold can be configured to track VBAT below a programmable inflection point with a programmable slope. A minimum threshold sets the limit of threshold reduction from VBAT tracking. Configurable attack rate, hold time and release rate are provided to shape the dynamic response of the limiter (through the *LIM_ATK_RT[2:0]*, *LIM_HLD_TM[2:0]* and *LIM_RLS_RT[2:0]* register bits).

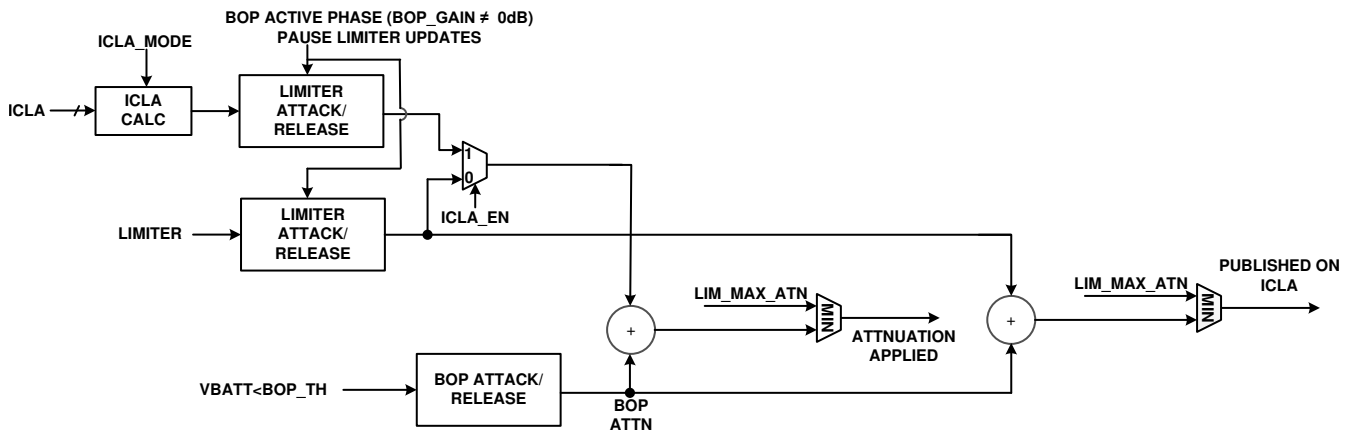


图 8-11. Limiter and Brown Out Prevention Interaction Diagram

A Brown Out Prevention (BOP) feature provides a priority input to the limiter to provide very fast response to transient dips in VBAT at end of charge conditions that can cause system level brown out. When VBAT dips below the BOP threshold, the limiter begins reducing gain with an attack latency of less than 10 μs and a

configurable attack rate. When VBAT rises above the BOP threshold, the limiter will begin to release after the programmed hold time.

The limiter is enabled by setting the *LIM_EN* bit register bit high.

表 8-44. Battery Tracking Limiter Enable

| <i>LIM_EN</i> | Value |
|---------------|--------------------|
| 0 | Disabled (default) |
| 1 | Enabled |

The limiter has configurable attack rate, hold time and release rate, which are available through the *LIM_ATK_RT[2:0]*, *LIM_HLD_TM[2:0]* and *LIM_RLS_RT[2:0]* register bits respectively. The limiter attack and release step size can be set by configuring the *LIM_ATK_ST[1:0]* and *LIM_RLS_ST[1:0]* register bits respectively.

表 8-45. Limiter Attack Rate

| <i>LIM_ATK_RT[2:0]</i> | Attack Rate (μ s) |
|------------------------|------------------------|
| 0x0 | 5 |
| 0x1 | 10 |
| 0x2 | 20 (default) |
| 0x3 | 40 |
| 0x4 | 80 |
| 0x5 | 160 |
| 0x6 | 320 |
| 0x7 | 640 |

表 8-46. Limiter Hold Time

| <i>LIM_HLD_TM[2:0]</i> | Hold Time (ms) |
|------------------------|----------------|
| 0x0 | 0 |
| 0x1 | 10 |
| 0x2 | 25 |
| 0x3 | 50 |
| 0x4 | 100 |
| 0x5 | 250 |
| 0x6 | 500 (default) |
| 0x7 | 1000 |

表 8-47. Limiter Release Rate

| <i>LIM_RLS_RT[2:0]</i> | Release Time (ms) |
|------------------------|-------------------|
| 0x0 | 10 |
| 0x1 | 50 |
| 0x2 | 100 |
| 0x3 | 250 |
| 0x4 | 500 |

表 8-47. Limiter Release Rate (continued)

| <i>LIM_RLS_RT[2:0]</i> | Release Time (ms) |
|------------------------|-------------------|
| 0x5 | 750 |
| 0x6 | 1000 (default) |
| 0x7 | 1500 |

表 8-48. Limiter Attack Step Size

| <i>LIM_ATK_ST[1:0]</i> | Step Size (dB) |
|------------------------|----------------|
| 00 | 0.25 |
| 01 | 0.5 (default) |
| 10 | 1 |
| 11 | 2 |

表 8-49. Limiter Release Step Size

| <i>LIM_RLS_ST[1:0]</i> | Step Size (dB) |
|------------------------|----------------|
| 00 | 0.25 |
| 01 | 0.5 (default) |
| 10 | 1 |
| 11 | 2 |

A maximum level of attenuation applied by the limiter and brown out prevention feature is configurable through the *LIM_MAX_ATN[4:0]* register bits. This attenuation limit is shared between the features. For instance, if the maximum attenuation is set to 6 dB and the limiter has reduced gain by 4 dB, the brown out prevention feature will only be able to reduce the gain further by another 2 dB. If the limiter or brown out prevention feature is attacking and it reaches the maximum attenuation, gain will not be reduced any further.

表 8-50. Limiter Max Attenuation

| <i>LIM_MAX_ATN[4:0]</i> | Attenuation (dB) |
|-------------------------|------------------|
| 0x00 | 1 |
| 0x01 | 1.5 |
| ... | ... |
| 0x10 | 9 (default) |
| ... | ... |
| 0x1E | 16 |
| 0x1F | 16.5 |

The limiter begins reducing gain when the output signal level is greater than the limiter threshold. The limiter can be configured to track VBAT below a programmable inflection point with a minimum threshold value. 图 8-12 below shows the limiter configured to limit to a constant level regardless of VBAT level. To achieve this behavior, set the limiter maximum threshold to the desired level through the *LIM_TH_MAX[6:0]* register bits. Set the limiter inflection point (through the *LIM_INF_PT[6:0]* register bits) below the minimum allowable VBAT setting. The limiter minimum threshold register bits (*LIM_TH_MIN[6:0]*) do not impact limiter behavior in this use case.

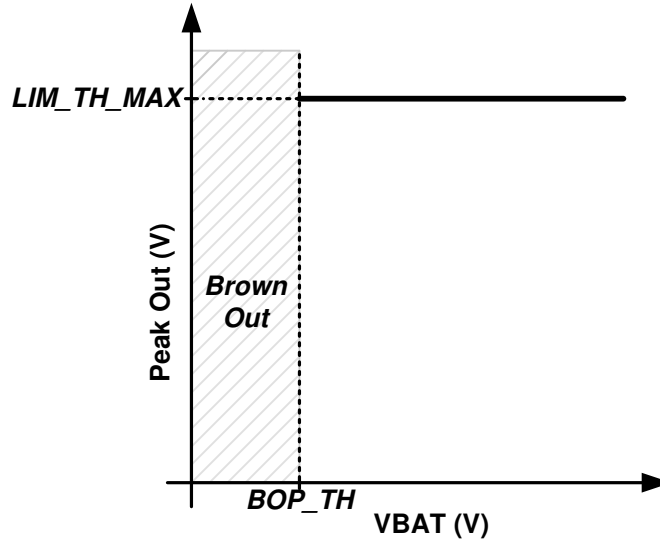


图 8-12. Limiter with Fixed Threshold

表 8-51. Limiter Maximum Threshold

| LIM_TH_MAX[6:0] | Threshold (V) |
|-----------------|---------------|
| 0x00 | 2 |
| 0x01 | 2.1 |
| ... | ... |
| 0x6E | 13 (default) |
| ... | ... |
| 0x7E | 14.6 |
| 0x7F | 14.7 |

表 8-52. Limiter Minimum Threshold

| LIM_TH_MIN[6:0] | Threshold (V) |
|-----------------|---------------|
| 0x00 | 2 |
| 0x01 | 2.1 |
| ... | ... |
| 0x1E | 5 (default) |
| ... | ... |
| 0x7E | 14.6 |
| 0x7F | 14.7 |

表 8-53. Limiter Inflection Point

| LIM_INF_PT[6:0] | Inflection Point (V) |
|-----------------|----------------------|
| 0x00 | 2 |
| 0x01 | 2.1 |
| ... | ... |
| 0x58 | 10.8 (default) |

表 8-53. Limiter Inflection Point (continued)

| LIM_INF_PT[6:0] | Inflection Point (V) |
|-----------------|----------------------|
| ... | ... |
| 0x7E | 14.6 |
| 0x7F | 14.7 |

图 8-13 shows how to configure the limiter to track VBAT below a threshold without a minimum threshold. Set the LIM_TH_MAX[6:0] register bits to the desired threshold and LIM_INF_PT[6:0] register bits to the desired inflection point where the limiter will begin reducing the threshold with VBAT. The LIM_SLOPE[1:0] register bits can be used to change the slope of the limiter tracking with VBAT. The default value of 1 V/V will reduce the threshold 1 V for every 1 V of drop in VBAT. More aggressive tracking slopes can be programmed if desired. Program the LIM_TH_MIN[6:0] below the minimum VBAT to prevent the limiter from having a minimum threshold reduction when tracking VBAT.

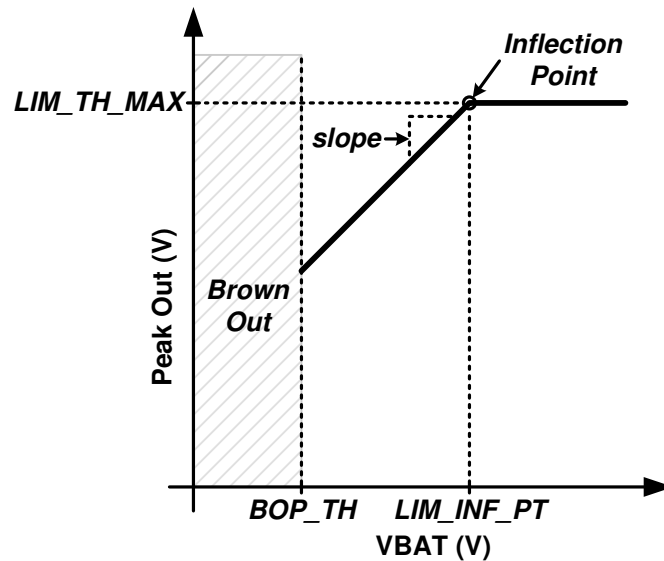


图 8-13. Limiter with Inflection Point

表 8-54. Limiter VBAT Tracking Slope

| LIM_SLOPE[1:0] | Slope (V/V) |
|----------------|-------------|
| 00 | 1 (default) |
| 01 | 1.5 |
| 10 | 2 |
| 11 | 4 |

To achieve a limiter that tracks VBAT below a threshold, configure the limiter as explained in the previous example, except program the LIM_TH_MIN[6:0] register bits to the desired minimum threshold. This is shown in 图 8-14 below.

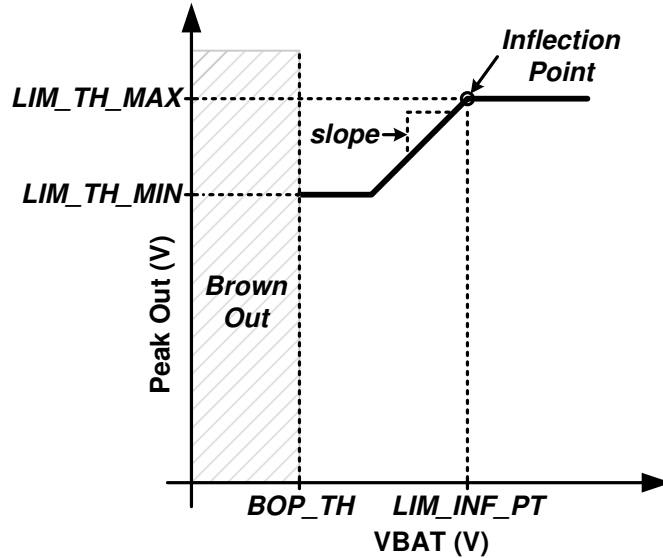


图 8-14. Limiter with Inflection Point and Minimum Threshold

The TAS2770 also employs a Brown Out Prevention (BOP) feature that serves as a low latency priority input to the limiter engine that begins attacking within 10 μ s of VBAT dipping below the programmed BOP threshold. This feature can be enabled by setting the *BOP_EN* register bit high. It should be noted that the BOP feature is independent of the limiter and will function if enabled even if the limiter is disabled. The BOP threshold is configured by setting the threshold with register bits *BOP_TH[7:0]*.

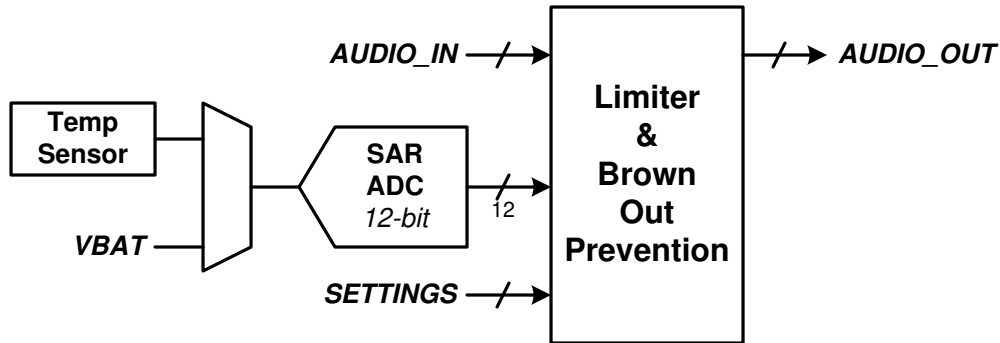


图 8-15. Limiter Block Diagram

表 8-55. Brown Out Prevention Enable

| <i>BOP_EN</i> | Value |
|---------------|-------------------|
| 0 | Disabled |
| 1 | Enabled (default) |

表 8-56. Brown Out Prevention Threshold

| <i>BOP_TH[7:0]</i> | Threshold (V) |
|--------------------|---------------|
| 0x00 | 4.5 |
| 0x01 | 4.525 |
| 0x02 | 4.55 |
| ... | ... |
| 0x14 | 5.0 (default) |

**表 8-56. Brown Out Prevention Threshold
(continued)**

| <i>BOP_TH[7:0]</i> | Threshold (V) |
|--------------------|---------------|
| ... | ... |
| 0xFE | 10.85 |
| 0xFF | 10.875 |

The BOP feature has a separate attack rate, attack step size and hold time from the battery tracking limiter (register bits *BOP_ATK_RT[2:0]*, *BOP_ATK_ST[1:0]* and *BOP_HLD_TM[2:0]* respectively). The BOP feature uses the *LIM_RLS_RT[2:0]* register setting to release after a brown out event.

表 8-57. Brown Out Prevention Attack Rate

| <i>BOP_ATK_RT[2:0]</i> | Attack Rate (μ s) |
|------------------------|------------------------|
| 0x0 | 5 |
| 0x1 | 10 |
| 0x2 | 20 (default) |
| 0x3 | 40 |
| 0x4 | 80 |
| 0x5 | 160 |
| 0x6 | 320 |
| 0x7 | 640 |

表 8-58. Brown Out Prevention Attack Step Size

| <i>BOP_ATK_ST[1:0]</i> | Step Size (dB) |
|------------------------|----------------|
| 00 | 0.5 |
| 01 | 1 (default) |
| 10 | 1.5 |
| 11 | 2 |

表 8-59. Brown Out Prevention Hold Time

| <i>BOP_HLD_TM[2:0]</i> | Hold Time (ms) |
|------------------------|----------------|
| 0x0 | 0 |
| 0x1 | 10 |
| 0x2 | 25 |
| 0x3 | 50 |
| 0x4 | 100 |
| 0x5 | 250 |
| 0x6 | 500 (default) |
| 0x7 | 1000 |

The TAS2770 can also shutdown the device when a brown out event occurs if the *BOP_SHUTDOWN* register bit is set high. For the device to continue playing audio again, the device must transition through a SW/HW shutdown state. Setting the *BOP_INF_HLD* high will cause the limiter to stay in the hold state (i.e. never release)

after a cleared brown out event until either the device transitions through a mute or SW/HW shutdown state or the register bit *BOP_HLD_CLR* is written to a high value (which will cause the device to exit the hold state and begin releasing). This bit is self clearing and will always readback low. 图 8-16 below illustrates the entering and exiting from a brown out event.

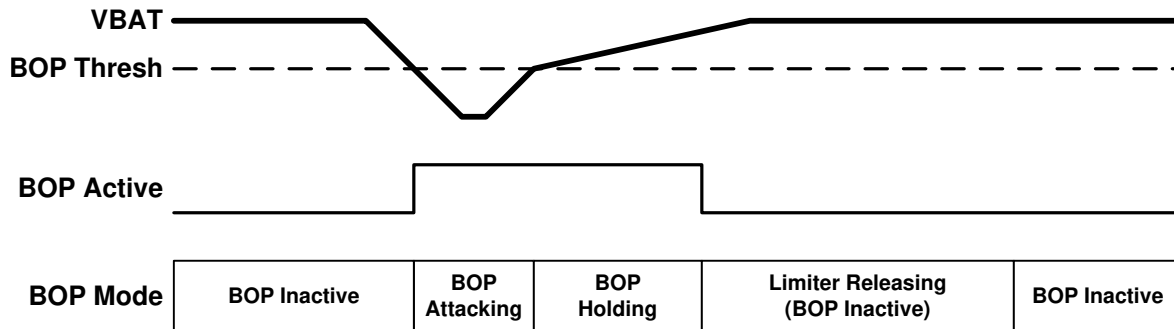


图 8-16. Brown Out Prevention Event

表 8-60. Shutdown on Brown Out Event

| <i>BOP_SHUTDOWN</i> | Value |
|---------------------|--------------------------|
| 0 | Don't Shutdown (default) |
| 1 | Shutdown |

表 8-61. Infinite Hold on Brown Out Event

| <i>BOP_INF_HLD</i> | Value |
|--------------------|--|
| 0 | Use <i>BOP_HLD_TM</i> after Brown Out event (default) |
| 1 | Do not release until <i>BOP_HLD_CLR</i> is asserted high |

表 8-62. BOP Infinite Hold Clear

| <i>BOP_HLD_CLR</i> | Value |
|--------------------|-----------------------------|
| 0 | Don't clear (default) |
| 1 | Clear event (self clearing) |

8.4.3.5 Inter Chip Limiter Alignment

8.4.3.5.1 TDM Mode

The TAS2770 supports alignment of limiter (including brown out prevention) dynamics across devices that share the same TDM bus. This ensures consistent gain between channels during limiting or brown out events since these dynamics are dependent on audio content, which can vary across channels. Each device can be configured to align to a specified number of other devices, which allows creation of groupings of devices that align only to each other.

Limiter activity is communicated through the limiter gain reduction parameter that can be optionally transmitted by each device on SDOOUT in an 8-bit time slot. Gain reduction should be transmitted in adjacent time slots for all devices that are to be aligned beginning with the first slot that is specified by the *ICLA_SLOT[5:0]* register bits. The order of the devices is not important as long as they are adjacent. The time slot for limiter gain reduction is configured by the *GAIN_SLOT[5:0]* register bits and enabled by the *GAIN_TX* register bit.

The *ICLA_SEN[7:0]* register bits specify which time slots should be listened to for gain alignment. This allows any number of devices between two and eight to be grouped together. At least two of these bits should be enabled for alignment to take place. The *ICLA_USE_MAX* register bit determines whether alignment is based on the maximum or minimum gain reduction value from the group of enabled devices.

To enable the inter chip limiter alignment feature, the *ICLA_EN* register bit should be asserted high and all devices should be configured with identical limiter and brown out prevention settings. Limiter gain reduction transmission should be enabled on all devices as described above.

表 8-63. Inter Chip Limiter Alignment

| <i>ICLA_EN</i> | Value |
|----------------|--------------------|
| 0 | Disabled (default) |
| 1 | Enabled |

表 8-64. ICLA Alignment Configuration

| <i>ICLA_MODE</i> | Value |
|------------------|--|
| 00 | Use the minimum gain reduction of the ICLA group including 0dB (default) |
| 01 | Use the maximum gain reduction of the ICLA group |
| 10 | Use the minimum gain reduction of the ICLA group that is non-0dB |
| 11 | Reserved |

表 8-65. Inter Chip Limiter Alignment Starting Time Slot

| <i>ICLA_SLOT[5:0]</i> | Starting Time Slot |
|-----------------------|-----------------------|
| 0x00 | Time Slot 0 (default) |
| 0x01 | Time Slot 1 |
| 0x02 | Time Slot 2 |
| ... | ... |
| 0x3F | Time Slot 63 |

表 8-66. Inter Chip Limiter Alignment Time Slot Enable

| Register Bit | Description | Bit Value | State |
|--------------------|--|-----------|--------------------|
| <i>ICLA_SEN[0]</i> | Time Slot = <i>ICLA_SLOT[5:0]</i> . When enabled, the limiter will include this time slot in the alignment group. | 0 | Disabled (default) |
| | | 1 | Enabled |
| <i>ICLA_SEN[1]</i> | Time Slot = <i>ICLA_SLOT[5:0]</i> + 1. When enabled, the limiter will include this time slot in the alignment group. | 0 | Disabled (default) |
| | | 1 | Enabled |
| <i>ICLA_SEN[2]</i> | Time Slot = <i>ICLA_SLOT[5:0]</i> + 2. When enabled, the limiter will include this time slot in the alignment group. | 0 | Disabled (default) |
| | | 1 | Enabled |
| <i>ICLA_SEN[3]</i> | Time Slot = <i>ICLA_SLOT[5:0]</i> + 3. When enabled, the limiter will include this time slot in the alignment group. | 0 | Disabled (default) |
| | | 1 | Enabled |
| <i>ICLA_SEN[4]</i> | Time Slot = <i>ICLA_SLOT[5:0]</i> + 4. When enabled, the limiter will include this time slot in the alignment group. | 0 | Disabled (default) |
| | | 1 | Enabled |
| <i>ICLA_SEN[5]</i> | Time Slot = <i>ICLA_SLOT[5:0]</i> + 5. When enabled, the limiter will include this time slot in the alignment group. | 0 | Disabled (default) |
| | | 1 | Enabled |
| <i>ICLA_SEN[6]</i> | Time Slot = <i>ICLA_SLOT[5:0]</i> + 6. When enabled, the limiter will include this time slot in the alignment group. | 0 | Disabled (default) |
| | | 1 | Enabled |

表 8-66. Inter Chip Limiter Alignment Time Slot Enable (continued)

| Register Bit | Description | Bit Value | State |
|--------------|---|-----------|--------------------|
| ICLA_SEN[7] | Time Slot = ICLA_SLOT[5:0] + 7. When enabled, the limiter will include this time slot in the alignment group. | 0 | Disabled (default) |
| | | 1 | Enabled |

8.4.3.6 Class-D Settings

The TAS2770 Class-D amplifier supports spread spectrum PWM modulation, which can be enabled by setting the AMP_SS register bit high. This can help reduce EMI in some systems.

表 8-67. Low EMI Spread Spectrum Mode

| AMP_SS | Spread Spectrum |
|--------|-------------------|
| 0 | Disabled |
| 1 | Enabled (default) |

By default the Class-D amplifier's switching frequency is based on the device's trimmed internal oscillator. To synchronize switching to the audio sample rate, set the CLASSD_SYNC register bit high. When the Class-D is synchronized to the audio sample rate, the RATE_RAMP register bit must be set based whether the audio sample rate is based on a 44.1 kHz or 48 kHz frequency. For 44.1, 88.2 and 176.4 kHz, set this bit high. for 48, 96 and 192 kHz, set this bit low. This ensures that the internal ramp generator has the appropriate slope.

表 8-68. Class-D Synchronization Mode

| CLASSD_SYNC | Synchronization Mode |
|-------------|--|
| 0 | Not synchronized to audio clocks (default) |
| 1 | Synchronized to audio clocks |

表 8-69. Sample Rate for Class-D Synchronized Mode

| RAMP_RATE | Playback Sample Rate |
|-----------|------------------------------|
| 0 | 48, 96 and 192 kHz (default) |
| 1 | 44.1, 88.2 and 174.6 kHz |

8.4.4 SAR ADC

A 12-bit SAR ADC monitors VBAT voltage and die temperature. The results of these conversions are available through the register readback (VBAT_CNV[11:0] and TMP_CNV[7:0] registers respectively). VBAT voltage conversions are also used by the limiter and brown out prevention features.

The ADC runs at a fixed 667 kHz sample rate (1.5 μs per conversion) interleaved between VBAT voltage and die temperature measurements. This gives an effective sample rate of 333 kHz (3 μs per conversion) with a latency of 1 sample (1.5 μs). This gives a worst case measurement latency of 4.5 μs. Actual VBAT voltage is calculated by dividing the VBAT_CNV[11:0] register by 256. Actual die temperature is calculated by dividing the TMP_CNV[11:0] register by 16 and then subtracting 93.

表 8-70. ADC VBAT Voltage Conversion

| VBAT_CNV[11:0] | VBAT Voltage (V) |
|----------------|------------------|
| 0x000 | 0 V |
| 0x001 | 0.0039 V |
| ... | ... |
| 0xC9A | 12.6016 V |

表 8-70. ADC VBAT Voltage Conversion (continued)

| VBAT_CNVR[11:0] | VBAT Voltage (V) |
|-----------------|------------------|
| ... | ... |
| 0xE00 | 14.0000 V |

表 8-71. ADC Die Temperature Conversion

| TMP_CNVR[11:0] | Die Temperature (°C) |
|----------------|----------------------|
| 0x000 | -93 °C |
| 0x001 | -92.9375 °C |
| ... | ... |
| 0x760 | 25 °C |
| ... | ... |
| 0xFFE | 162.8750 °C |
| 0xFFF | 162.9375 °C |

8.4.5 IV Sense

The TAS2770 provides speaker voltage and current sense for real time monitoring of loudspeaker behavior. The VSNS_P and VSNS_N pins should be connected after any ferrite bead filter (or directly to the OUT_P and OUT_N connections if no EMI filter is used). The V-Sense connections eliminate IR drop error due to packaging, PCB interconnect or ferrite bead filter resistance. It should be noted that any interconnect resistance after the V-Sense terminals will not be corrected for, so it is advised to connect the sense connections as close to the load as possible.

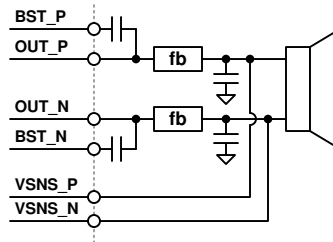


图 8-17. V-Sense Connections

I-Sense and V-Sense can be powered down by asserting the *ISNS_PD* and *VSNS_PD* register bits respectively. When powered down, the device will return null samples for the powered down block.

表 8-72. I-Sense Power Down

| ISNS_PD | Setting |
|---------|-----------------------------|
| 0 | I-Sense is active (default) |
| 1 | I-Sense is powered down |

表 8-73. V-Sense Power Down

| VSNS_PD | Setting |
|---------|-----------------------------|
| 0 | V-Sense is active (default) |
| 1 | V-Sense is powered down |

8.4.6 Clocks and PLL

In TMD/I²C Mode, the device operates from SBCLK. 表 8-74 和 表 8-75 below shows the valid SBCLK frequencies for each sample rate and SBCLK to FSYNC ratio (for 44.1 kHz and 48 kHz family frequencies respectively).

If the sample rate is properly configured through the *SAMP_RATE[1:0]* bits, no additional configuration is required as long as the SBCLK to FSYNC ratio is valid. The device will detect improper SBCLK frequencies and SBCLK to FSYNC ratios and volume ramp down the playback path to minimize audible artifacts.

表 8-74. Supported SBCLK Frequencies (48 kHz based sample rates)

| Sample Rate (kHz) | SBCLK to FSYNC Ratio | | | | | | |
|-------------------|----------------------|------------|------------|------------|------------|------------|------------|
| | 64 | 96 | 128 | 192 | 256 | 384 | 512 |
| 48 kHz | 3.072 MHz | 4.608 MHz | 6.144 MHz | 9.216 MHz | 12.288 MHz | 18.432 MHz | 24.576 MHz |
| 96 kHz | 6.144 MHz | 9.216 MHz | 12.288 MHz | 18.432 MHz | 24.576 MHz | - | - |
| 192 kHz | 12.288 MHz | 18.432 MHz | 24.576 MHz | - | - | - | - |

表 8-75. Supported SBCLK Frequencies (44.1 kHz based sample rates)

| Sample Rate (kHz) | SBCLK to FSYNC Ratio | | | | | | |
|-------------------|----------------------|-------------|-------------|-------------|-------------|-------------|-------------|
| | 64 | 96 | 128 | 192 | 256 | 384 | 512 |
| 44.1 kHz | 2.8224 MHz | 4.2336 MHz | 5.6448 MHz | 8.4672 MHz | 11.2896 MHz | 16.9344 MHz | 22.5792 MHz |
| 88.2 kHz | 5.6448 MHz | 8.4672 MHz | 11.2896 MHz | 16.9344 MHz | 22.5792 MHz | - | - |
| 176.4 kHz | 11.2896 MHz | 16.9344 MHz | 22.5792 MHz | - | - | - | - |

8.4.7 Operational Modes

8.4.7.1 Hardware Shutdown

The device enters Hardware Shutdown mode if the SDZ pin is asserted low. In Hardware Shutdown mode, the device consumes the minimum quiescent current from AVDD and VBAT supplies. All registers loose state in this mode and communication is disabled (through the I²C).

If SDZ is asserted low while audio is playing, the device will ramp down volume on the audio, stop the Class-D switching, power down analog and digital blocks and finally put the device into Hardware Shutdown mode.

When SDZ is released, the device will sample the MODE pin and enter the selected operational mode (i.e. either TDM/I²C).

8.4.7.2 Software Shutdown

Software Shutdown mode powers down all analog blocks required to playback audio, but does not cause the device to loose register state. Software Shutdown is enabled by asserting the *MODE[1:0]* register bits to 2'b10. If audio is playing when Software Shutdown is asserted, the Class-D will volume ramp down before shutting down. When deasserted, the Class-D will begin switching and volume ramp back to the programmed digital volume setting.

8.4.7.3 Mute

The TAS2770 will volume ramp down the Class-D amplifier to a mute state by setting the *MODE[1:0]* register bits to 2'b01. During mute the Class-D still switches, but transmits no audio content. If mute is deasserted, the device will volume ramp back to the programmed digital volume setting.

8.4.7.4 Active

In Active Mode the Class-D switches and plays back audio. Speaker voltage and current sensing are operational if enabled. PDM inputs are also active if enabled. Set the *MODE[1:0]* register bits to 2'b00 to enter active mode.

8.4.7.5 Mode Control and Software Reset

The TAS2770 mode can be configured by writing the *MODE[1:0]* bits.

表 8-76. Mode Control

| <i>MODE[1:0]</i> | Setting |
|------------------|-----------------------------|
| 00 | Active |
| 01 | Mute |
| 10 | Software Shutdown (default) |
| 11 | Reserved |

A software reset can be accomplished by asserting the *SW_RESET* bit, which is self clearing. This will restore all registers to their default values.

表 8-77. Software Reset

| <i>SW_RESET</i> | Setting |
|-----------------|-----------------------|
| 0 | Don't reset (default) |
| 1 | Reset |

8.4.8 Faults and Status

During the power-up sequence, the power-on-reset circuit (POR) monitoring the AVDD pin will hold the device in reset (including all configuration registers) until the supply is valid. The device will not exit hardware shutdown until AVDD is valid and the SDZ pin is released. Once SDZ is released, the digital core voltage regulator will power up, enabling detection of the operational mode. If AVDD dips below the POR threshold, the device will immediately be forced into a reset state.

The device also monitors the VBAT supply and holds the analog core in power down if the supply is below the UVLO threshold or above the OVLO threshold. If the TAS2770 is in active operation and a UVLO or OVLO fault occurs, the analog supplies will immediately power down to protect the device. These faults are latching and require a transition through HW/SW shutdown to clear the fault. The live and latched registers will report UVLO/OVLO faults.

The device transitions into software shutdown mode if it detects any faults with the TDM clocks such as:

- Invalid SBCLK to FSYNC ratio
- Invalid FSYNC frequency
- Halting of SBCLK or FSYNC clocks

Upon detection of a TDM clock error, the device transitions into software shutdown mode as quickly as possible to limit the possibility of audio artifacts. Once all TDM clock errors are resolved, the device volume ramps back to its previous playback state. During a TDM clock error, the IRQZ pin will assert low if the clock error interrupt mask register bit is set low (*INT_MASK[2]*). The clock fault is also available for readback in the live or latched fault status registers (*INT_LIVE[2]* and *INT_LTCH[2]*). Reading the latched fault status register (*INT_LTCH[7:0]*) clears the register.

The TAS2770 also monitors die temperature and Class-D load current and will enter software shutdown mode if either of these exceed safe values. As with the TDM clock error, the IRQZ pin will assert low for these faults if the appropriate fault interrupt mask register bit is set low (*INT_MASK[0]* for over temp and *INT_MASK[1]* for over current). The fault status can also be monitored in the live and latched fault registers as with the TDM clock error.

Die over temp and Class-D over current errors can either be latching (i.e. the device will enter software shutdown until a HW/SW shutdown sequence is applied) or they can be configured to automatically retry after a prescribed time. This behavior can be configured in the *OTE_RETRY* and *OCE_RETRY* register bits (for over temp and over current respectively). Even in latched mode, the Class-D will not attempt to retry after an over temp or over current error until the retry time period (1.5s) has elapsed. This prevents applying repeated stress to the device in a rapid fashion that could lead to device damage. If the device has been cycled through SW/HW shutdown, the device will only begin to operate after the retry time period.

The status registers (and IRQZ pin if enabled through the status mask register) also indicates limiter behavior including when the limiter is activity, when VBAT is below the inflection point, when maximum attenuation has been applied, when the limiter is in infinite hold and when the limiter has muted the audio.

The IRQZ pin is an open drain output that asserts low during unmasked fault conditions and therefore must be pulled up with a resistor to IOVDD. An internal pull up resistor is provided in the TAS2770 and can be accessed by setting the *IRQZ_PU* register bit high. 图 8-18 below highlights the IRQZ pin circuit.

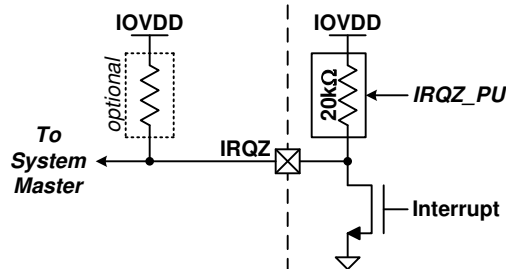


图 8-18. IRQZ Pin

表 8-78. Fault Interrupt Mask

| INT_MASK[10:0] Bit | Interrupt | Default (1 = Mask) |
|--------------------|--------------------|--------------------|
| 0 | Over Temp Error | 0 |
| 1 | Over Current Error | 0 |
| 2 | TDM Clock Error | 1 |
| 3 | Limiter Active | 1 |
| 4 | VBAT < Inf Point | 1 |
| 5 | Limiter Max Atten | 1 |
| 6 | Limiter Inf Hold | 1 |
| 7 | Limiter Mute | 1 |
| 8 | PDM Clock Error | 1 |
| 9 | VBAT Brown Out | 1 |
| 10 | VBAT UVLO | 1 |
| 11 | VBAT OVLO | 1 |

表 8-79. IRQZ Internal Pull Up Enable

| IRQZ_PU | State |
|---------|--------------------|
| 0 | Disabled (default) |
| 1 | Enabled |

表 8-80. IRQZ Interrupt Configuration

| IRQZ_PIN_CFG[1:0] | Value |
|-------------------|---|
| 00 | IRQZ will assert on any unmasked live interrupts |
| 01 | IRQZ will assert on any unmasked latched interrupts (default) |
| 10 | Reserved |

表 8-80. IRQZ Interrupt Configuration (continued)

| IRQZ_PIN_CFG[1:0] | Value |
|-------------------|----------|
| 11 | Reserved |

8.4.9 Power Sequencing Requirements

AVDD and IOVDD pins should be connected to the same 1.8 V supply domain. There are no other power sequencing requirements for order of rate of ramping up or down.

8.4.10 Digital Input Pull Downs

Each digital input and IO has an optional weak pull down to prevent the pin from floating. Pull downs are not enabled during HW shutdown.

表 8-81. Digital Input Pull Down Enables

| Register Bit | Description | Bit Value | State |
|--------------|---------------------------|-----------|-------------------|
| DIN_PD[0] | Weak pull down for PDMCK. | 0 | Disabled |
| | | 1 | Enabled (default) |
| DIN_PD[2] | Weak pull down for PDMD. | 0 | Disabled |
| | | 1 | Enabled (default) |
| DIN_PD[5] | Weak pull down for FSYNC. | 0 | Disabled |
| | | 1 | Enabled (default) |
| DIN_PD[6] | Weak pull down for SDIN. | 0 | Disabled |
| | | 1 | Enabled (default) |
| DIN_PD[7] | Weak pull down for SDOUT. | 0 | Disabled |
| | | 1 | Enabled (default) |

8.5 Register Maps

8.5.1 Register Summary Table Book=0x00 Page=0x00

| Addr | Register | Description | Section |
|------|----------|--------------------------|----------------------------|
| 0x00 | PAGE | Device Page | 节 8.5.2.1 |
| 0x01 | SW_RESET | Software Reset | 节 8.5.2.2 |
| 0x02 | PWR_CTL | Power Control | 节 8.5.2.3 |
| 0x03 | PB_CFG0 | Playback Configuration 0 | 节 8.5.2.4 |
| 0x04 | PB_CFG1 | Playback Configuration 1 | 节 8.5.2.5 |
| 0x05 | PB_CFG2 | Playback Configuration 2 | 节 8.5.2.6 |
| 0x06 | PB_CFG3 | Playback Configuration 3 | 节 8.5.2.7 |
| 0x07 | MISC_CFG | Misc Configuration | 节 8.5.2.8 |
| 0x08 | PDM_CFG0 | PDM Input Register 0 | 节 8.5.2.9 |
| 0x09 | PDM_CFG1 | PDM Configuration 1 | 节 8.5.2.10 |
| 0x0A | TDM_CFG0 | TDM Configuration 0 | 节 8.5.2.11 |
| 0x0B | TDM_CFG1 | TDM Configuration 1 | 节 8.5.2.12 |
| 0x0C | TDM_CFG2 | TDM Configuration 2 | 节 8.5.2.13 |
| 0x0D | TDM_CFG3 | TDM Configuration 3 | 节 8.5.2.14 |
| 0x0E | TDM_CFG4 | TDM Configuration 4 | 节 8.5.2.15 |
| 0x0F | TDM_CFG5 | TDM Configuration 5 | 节 8.5.2.16 |
| 0x10 | TDM_CFG6 | TDM Configuration 6 | 节 8.5.2.17 |
| 0x11 | TDM_CFG7 | TDM Configuration 7 | 节 8.5.2.18 |

| | | | |
|------|-----------|--------------------------------|----------------------------|
| 0x12 | TDM_CFG8 | TDM Configuration 8 | 节 8.5.2.19 |
| 0x13 | TDM_CFG9 | TDM Configuration 9 | 节 8.5.2.20 |
| 0x14 | TDM_CFG10 | TDM Configuration 10 | 节 8.5.2.21 |
| 0x15 | LIM_CFG0 | Limiter Configuration 0 | 节 8.5.2.22 |
| 0x16 | LIM_CFG1 | Limiter Configuration 1 | 节 8.5.2.23 |
| 0x17 | LIM_CFG2 | Limiter Configuration 2 | 节 8.5.2.24 |
| 0x18 | LIM_CFG3 | Limiter Configuration 3 | 节 8.5.2.25 |
| 0x19 | LIM_CFG4 | Limiter Configuration 4 | 节 8.5.2.26 |
| 0x1A | LIM_CFG5 | Limiter Configuration 5 | 节 8.5.2.27 |
| 0x1B | BOP_CFG0 | Brown Out Prevention 0 | 节 8.5.2.28 |
| 0x1C | BOP_CFG1 | Brown Out Prevention 1 | 节 8.5.2.29 |
| 0x1D | BOP_CFG2 | Brown Out Prevention 2 | 节 8.5.2.30 |
| 0x1E | ICLA_CFG0 | Inter Chip Limiter Alignment 0 | 节 8.5.2.31 |
| 0x1F | ICLA_CFG1 | Inter Chip Limiter Alignment 1 | 节 8.5.2.32 |
| 0x20 | INT_MASK0 | Interrupt Mask 0 | 节 8.5.2.33 |
| 0x21 | INT_MASK1 | Interrupt Mask 1 | 节 8.5.2.34 |
| 0x22 | INT_LIVE0 | Live Interrupt Readback 0 | 节 8.5.2.35 |
| 0x23 | INT_LIVE1 | Live Interrupt Readback 1 | 节 8.5.2.36 |
| 0x24 | INT_LTCH0 | Latched Interrupt Readback 0 | 节 8.5.2.37 |
| 0x25 | INT_LTCH1 | Latched Interrupt Readback 1 | 节 8.5.2.38 |
| 0x27 | VBAT_MSB | SAR ADC Conversion 0 | 节 8.5.2.40 |
| 0x28 | VBAT_LSB | SAR ADC Conversion 1 | 节 8.5.2.41 |
| 0x29 | TEMP_MSB | SAR ADC Conversion 2 | 节 8.5.2.42 |
| 0x2A | TEMP_LSB | SAR ADC Conversion 2 | 节 8.5.2.43 |
| 0x30 | INT_CFG | Interrupt Configuration | 节 8.5.2.44 |
| 0x31 | DIN_PD | Digital Input Pin Pull Down | 节 8.5.2.45 |
| 0x32 | MISC_IRQ | Misc Configuration | 节 8.5.2.46 |
| 0x3C | CLOCK_CFG | Clock Configuration | 节 8.5.2.47 |
| 0x77 | TDM_DET | TDM Clock detection monitor | 节 8.5.2.48 |
| 0x7D | REV_ID | Revision and PG ID | 节 8.5.2.49 |
| 0x7E | I2C_CKSUM | I2C Checksum | 节 8.5.2.50 |
| 0x7F | BOOK | Device Book | 节 8.5.2.51 |

8.5.2 Register Maps

8.5.2.1 PAGE (book=0x00 page=0x00 address=0x00) [reset=0h]

The device's memory map is divided into pages and books. This register sets the page.

图 8-19. PAGE Register Address: 0x00

| | | | | | | | |
|-----------|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PAGE[7:0] | | | | | | | |
| RW-0h | | | | | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 8-82. Device Page Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------|------|-------|--|
| 7-0 | PAGE[7:0] | RW | 0h | Sets the device page. 00h = Page 0 01h = Page 1 ... FFh = Page 255 |

8.5.2.2 SW_RESET (book=0x00 page=0x00 address=0x01) [reset=0h]

Asserting Software Reset will place all register values in their default POR (Power on Reset) state.

图 8-20. SW_RESET Register Address: 0x01

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|---|---|---|---|---|---|----------|
| Reserved | | | | | | | SW_RESET |
| RW-0h | | | | | | | RW-0h |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 8-83. Software Reset Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------|------|-------|---|
| 7-1 | Reserved | RW | 0h | Reserved |
| 0 | SW_RESET | RW | 0h | Software reset. Bit is self clearing. 0b = Don't reset 1b = Reset |

8.5.2.3 PWR_CTL (book=0x00 page=0x00 address=0x02) [reset=Eh]

Sets device's mode of operation and power down of IV sense blocks.

图 8-21. PWR_CTL Register Address: 0x02

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|---|----------|----------|---------|---------|-----------|---|
| Reserved | | Reserved | Reserved | ISNS_PD | VSNS_PD | MODE[1:0] | |
| RW-0h | | RW-0h | RW-0h | RW-1h | RW-1h | RW-2h | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 8-84. Power Control Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------|------|-------|---|
| 7-6 | Reserved | RW | 0h | Reserved |
| 5 | Reserved | RW | 0h | Reserved |
| 4 | Reserved | RW | 0h | Reserved |
| 3 | ISNS_PD | RW | 1h | Current sense power down. 0b = Current sense active 1b = Current sense is powered down |
| 2 | VSNS_PD | RW | 1h | Voltage sense power down. 0b = voltage sense is active 1b = Voltage sense is powered down |
| 1-0 | MODE[1:0] | RW | 2h | Device operational mode. 00b = Active 01b = Mute 10b = Software Shutdown 11b = Reserved |

8.5.2.4 PB_CFG0 (book=0x00 page=0x00 address=0x03) [reset=10h]

Sets playback source, including PDM input and amplifier output level setting.

图 8-22. PB_CFG0 Register Address: 0x03

| | | | | | | | |
|---------|------------|--------|----------------|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PDM_MAP | PB_PDM_SRC | PB_SRC | AMP_LEVEL[4:0] | | | | |
| RW-0h | RW-0h | RW-0h | RW-10h | | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 8-85. Playback Configuration 0 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------------|------|-------|---|
| 7 | PDM_MAP | RW | 0h | PDM Pin Mapping 0b = PDMD1 for sensor input. 1b = PDMD1 for playback. |
| 6 | PB_PDM_SRC | RW | 0h | PDM playback source. 0b = PDM input pin defined by PDM_MAP. 1b = Reserved. |
| 5 | PB_SRC | RW | 0h | Playback source. 0b = PCM 1b = PDM |
| 4-0 | AMP_LEVEL[4:0] | RW | 10h | Amplifier output level setting. 00h = 11.0 dBV (5.02 Vpk) 01h = 11.5 dBV (5.32 Vpk) 02h = 12.0 dBV (5.63 Vpk) 03h = 12.5 dBV (5.96 Vpk) 04h = 13.0 dBV (6.32 Vpk) 05h = 13.5 dBV (6.69 Vpk) 06h = 14.0 dBV (7.09 Vpk) 07h = 14.5 dBV (7.51 Vpk) 08h = 15.0 dBV (7.95 Vpk) 09h = 15.5 dBV (8.42 Vpk) 0Ah = 16.0 dBV (8.92 Vpk) 0Bh = 16.5 dBV (9.45 Vpk) 0Ch = 17.0 dBV (10.01 Vpk) 0Dh = 17.5 dBV (10.61 Vpk) 0Eh = 18.0 dBV (11.23 Vpk) 0Fh = 18.5 dBV (11.90 Vpk) 10h = 19.0 dBV (12.60 Vpk) 11h = 19.5 dBV (13.35 Vpk) 12h = 20.0 dBV (14.14 Vpk) 13h = 20.5 dBV (14.98 Vpk) 14h = 21.0 dBV (15.87 Vpk) 15h - 1Fh = Reserved |

8.5.2.5 PB_CFG1 (book=0x00 page=0x00 address=0x04) [reset=1h]

Sets playback high pass filter corner (PCM playback only).

图 8-23. PB_CFG1 Register Address: 0x04

| | | | | | | | |
|----------|----------|----------|----------|----------|---------------|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | Reserved | Reserved | Reserved | Reserved | HPF_FREQ[2:0] | | |
| RW-0h | RW-0h | RW-0h | RW-0h | RW-0h | RW-1h | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 8-86. Playback Configuration 1 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------|------|-------|-------------|
| 7 | Reserved | RW | 0h | Reserved |
| 6 | Reserved | RW | 0h | Reserved |
| 5 | Reserved | RW | 0h | Reserved |
| 4 | Reserved | RW | 0h | Reserved |

表 8-86. Playback Configuration 1 Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|---------------|------|-------|---|
| 3 | Reserved | RW | 0h | Reserved |
| 2-0 | HPF_FREQ[2:0] | RW | 1h | High Pass Filter Corner Frequency. 000b = Bypass 001b = 2 Hz 010b = 50 Hz 011b = 100 Hz 100b = 200 Hz 101b = 400 Hz 110b = 800 Hz 111b = Reserved |

8.5.2.6 PB_CFG2 (book=0x00 page=0x00 address=0x05) [reset=0h]

Sets playback volume for PCM playback path.

图 8-24. PB_CFG2 Register Address: 0x05

| | | | | | | | |
|--------------|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DVC_PCM[7:0] | | | | | | | |
| RW-0h | | | | | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 8-87. Playback Configuration 2 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------|------|-------|---|
| 7-0 | DVC_PCM[7:0] | RW | 0h | PCM digital volume control. 00h = 0 dB 01h = -0.5 dB 02h = -1 dB C7h = -99.5 dB C8h = -100dB C9h - FFh = Mute |

8.5.2.7 PB_CFG3 (book=0x00 page=0x00 address=0x06) [reset=0h]

Sets playback volume for PDM playback path.

图 8-25. PB_CFG3 Register Address: 0x06

| | | | | | | | |
|--------------|---|---|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DVC_PDM[7:0] | | | | | | | |
| RW-0h | | | | | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 8-88. Playback Configuration 3 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------|------|-------|---|
| 7-0 | DVC_PDM[7:0] | RW | 0h | PDM digital volume control. 00h = 0 dB 01h = -0.5 dB 02h = -1 dB C7h = -99.5 dB C8h = -100dB C9h - FFh = Mute |

8.5.2.8 MISC_CFG (book=0x00 page=0x00 address=0x07) [reset=6h]

Sets DVC Ramp Rate, IRQZ pull up, amp spread spectrum and I-Sense current range.

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------------|---|----------|---|---------|--------|----------|---|
| DVC_RAMP_RATE[1:0] | | Reserved | | IRQZ_PU | AMP_SS | Reserved | |
| RW-0h | | RW-0h | | RW-0h | RW-1h | RW-2h | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 8-89. Misc Configuration Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------------|------|-------|---|
| 7-6 | DVC_RAMP_RATE[1:0] | RW | 0h | Digital volume control ramp rate. 00b = 0.5 dB per 1 sample 01b = 0.5 dB per 4 samples 10b = 0.5 dB per 8 samples 11b = Volume ramping disabled |
| 5-4 | Reserved | RW | 0h | Reserved |
| 3 | IRQZ_PU | RW | 0h | IRQZ internal pull up enable. 0b = Disabled 1b = Enabled |
| 2 | AMP_SS | RW | 1h | Low EMI spread spectrum enable. 0b = Disabled 1b = Enabled |
| 1-0 | Reserved | RW | 2h | Reserved |

8.5.2.9 PDM_CFG0 (book=0x00 page=0x00 address=0x08) [reset=0h]

Sets Class-D sync mode and PDM sample rates.

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

图 8-26. PDM_CFG0 Register Address: 0x08

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|-------------|----------|---|----------------|---|----------|---|
| Reserved | CLASSD_SYNC | Reserved | | PDM_RATE1[1:0] | | Reserved | |
| RW-0h | RW-0h | RW-0h | | RW-0h | | RW-0h | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 8-90. PDM Input Register 0 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------------|------|-------|--|
| 7 | Reserved | RW | 0h | Reserved |
| 6 | CLASSD_SYNC | RW | 0h | Class-D synchronization mode. 0b = Not synchronized to audio clocks 1b = Synchronized to audio clocks |
| 5-4 | Reserved | RW | 0h | Reserved |
| 3-2 | PDM_RATE1[1:0] | RW | 0h | PDMD1 input sample rate. 00b = 2.54 - 3.38 MHz 01b = 5.08 - 6.76 MHz 10b = Reserved 11b = Reserved |
| 1-0 | Reserved | RW | 0h | Reserved |

8.5.2.10 PDM_CFG1 (book=0x00 page=0x00 address=0x09) [reset=8h]

Sets PDM capture edge, master/slave, clock source and gating.

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

图 8-27. PDM_CFG1 Register Address: 0x09

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------|----------|----------|----------|----------|----------|-----------|----------|
| PDM_EDGE1 | Reserved | PDM_SLV1 | Reserved | PDM_CLK1 | Reserved | PDM_GATE1 | Reserved |
| RW-0h | RW-0h | RW-0h | RW-0h | RW-1h | RW-0h | RW-0h | RW-0h |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 8-91. PDM Configuration 1 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------|------|-------|---|
| 7 | PDM_EDGE1 | RW | 0h | PDMD1 input capture edge. 0b = Rising 1b = Falling |
| 6 | Reserved | RW | 0h | Reserved |
| 5 | PDM_SLV1 | RW | 0h | PDMD1 input master or slave. 0b = Slave 1b = Master |
| 4 | Reserved | RW | 0h | Reserved |
| 3 | PDM_CLK1 | RW | 1h | PDMD1 clock select. 0b = GND 1b = PDMCK1 |
| 2 | Reserved | RW | 0h | Reserved |
| 1 | PDM_GATE1 | RW | 0h | PDMD1 clock gate. 0b = Gated Off 1b = Active |
| 0 | Reserved | RW | 0h | Reserved |

8.5.2.11 TDM_CFG0 (book=0x00 page=0x00 address=0x0A) [reset=7h]

Sets the TDM frame start, TDM sample rate, TDM auto rate detection and whether rate is based on 44.1 kHz or 48 kHz frequency.

图 8-28. TDM_CFG0 Register Address: 0x0A

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|---|-----------|-----------|----------------|---|---|-------------|
| Reserved | | RATE_RAMP | AUTO_RATE | SAMP_RATE[2:0] | | | FRAME_START |
| RW-0h | | RW-0h | RW-0h | RW-3h | | | RW-1h |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 8-92. TDM Configuration 0 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------------|------|-------|--|
| 7-6 | Reserved | RW | 0h | Reserved |
| 5 | RATE_RAMP | RW | 0h | Sample rate based on 44.1kHz or 48kHz when CLASSD_SYNC=1. 0b = 48kHz 1b = 44.1kHz |
| 4 | AUTO_RATE | RW | 0h | Auto detection of TDM sample rate. 0b = Enabled 1b = Disabled |
| 3-1 | SAMP_RATE[2:0] | RW | 3h | Sample rate of the TDM bus. 000b = Reserved 001b = Reserved 010b = Reserved 011b = 44.1/48 kHz 100b = 88.2/96 kHz 101b = 176.4/192 kHz 110b = Reserved 111b = Reserved |

表 8-92. TDM Configuration 0 Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------------|------|-------|---|
| 0 | FRAME_START | RW | 1h | TDM frame start polarity. 0b = Low to High on FSYNC 1b = High to Low on FSYNC |

8.5.2.12 TDM_CFG1 (book=0x00 page=0x00 address=0x0B) [reset=2h]

Sets TDM RX justification, offset and capture edge.

图 8-29. TDM_CFG1 Register Address: 0x0B

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|------------|----------------|---|---|---|---|---------|
| Reserved | RX_JUSTIFY | RX_OFFSET[4:0] | | | | | RX_EDGE |
| RW-0h | RW-0h | RW-1h | | | | | RW-0h |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 8-93. TDM Configuration 1 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------------|------|-------|---|
| 7 | Reserved | RW | 0h | Reserved |
| 6 | RX_JUSTIFY | RW | 0h | TDM RX sample justification within the time slot. 0b = Left 1b = Right |
| 5-1 | RX_OFFSET[4:0] | RW | 1h | TDM RX start of frame to time slot 0 offset (SBCLK cycles). |
| 0 | RX_EDGE | RW | 0h | TDM RX capture clock polarity. 0b = Rising edge of SBCLK 1b = Falling edge of SBCLK |

8.5.2.13 TDM_CFG2 (book=0x00 page=0x00 address=0x0C) [reset=Ah]

Sets TDM RX time slot select, word length and time slot length.

图 8-30. TDM_CFG2 Register Address: 0x0C

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|---|--------------|---|--------------|---|--------------|---|
| Reserved | | RX_SCFG[1:0] | | RX_WLEN[1:0] | | RX_SLEN[1:0] | |
| RW-0h | | RW-0h | | RW-2h | | RW-2h | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 8-94. TDM Configuration 2 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------|------|-------|---|
| 7-6 | Reserved | RW | 0h | Reserved |
| 5-4 | RX_SCFG[1:0] | RW | 0h | TDM RX time slot select config. 00b = Mono with time slot equal to I2C address offset 01b = Mono left channel 10b = Mono right channel 11b = Stereo downmix (L+R)/2 |
| 3-2 | RX_WLEN[1:0] | RW | 2h | TDM RX word length. 00b = 16-bits 01b = 20-bits 10b = 24-bits 11b = 32-bits |
| 1-0 | RX_SLEN[1:0] | RW | 2h | TDM RX time slot length. 00b = 16-bits 01b = 24-bits 10b = 32-bits 11b = Reserved |

8.5.2.14 TDM_CFG3 (book=0x00 page=0x00 address=0x0D) [reset=10h]

Sets TDM RX left and right time slots.

图 8-31. TDM_CFG3 Register Address: 0x0D

| | | | | | | | |
|----------------|---|---|---|----------------|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RX_SLOT_R[3:0] | | | | RX_SLOT_L[3:0] | | | |
| RW-1h | | | | RW-0h | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 8-95. TDM Configuration 3 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------------|------|-------|---------------------------------|
| 7-4 | RX_SLOT_R[3:0] | RW | 1h | TDM RX Right Channel Time Slot. |
| 3-0 | RX_SLOT_L[3:0] | RW | 0h | TDM RX Left Channel Time Slot. |

8.5.2.15 TDM_CFG4 (book=0x00 page=0x00 address=0x0E) [reset=13h]

Sets TDM TX bus keeper, fill, offset and transmit edge.

图 8-32. TDM_CFG4 Register Address: 0x0E

| | | | | | | | |
|------------|---------------|-----------|---------|----------------|---|---------|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| TX_LSB_CFG | TX_KEEPER_CFG | TX_KEEPER | TX_FILL | TX_OFFSET[2:0] | | TX_EDGE | |
| RW-0h | RW-0h | RW-0h | RW-1h | RW-1h | | RW-1h | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 8-96. TDM Configuration 4 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------------|------|-------|--|
| 7 | TX_LSB_CFG | RW | 0h | TDM TX SDOUT LSB data option 0b = TX SDOUT LSB is driven for full-cycle (provided TX_KEEPER is '0') 1b = TX SDOUT LSB is driven for half-cycle |
| 6 | TX_KEEPER_CFG | RW | 0h | TDM TX SDOUT bus keeper configuration. 0b = Bus keeper is enabled only for 1 LSB bit cycle & SDOUT LSB driven for half cycle (provided TX_KEEPER is '1') 1b = Bus keeper is always enabled & SDOUT LSB driven for half cycle (provided TX_KEEPER is '1') |
| 5 | TX_KEEPER | RW | 0h | TDM TX SDOUT bus keeper enable. 0b = Disable bus keeper 1b = Enable bus keeper |
| 4 | TX_FILL | RW | 1h | TDM TX SDOUT unused bitfield fill. 0b = Transmit 0 1b = Transmit Hi-Z |
| 3-1 | TX_OFFSET[2:0] | RW | 1h | TDM TX start of frame to time slot 0 offset. |
| 0 | TX_EDGE | RW | 1h | TDM TX launch clock polarity. 0b = Rising edge of SBCLK 1b = Falling edge of SBCLK |

8.5.2.16 TDM_CFG5 (book=0x00 page=0x00 address=0x0F) [reset=2h]

Sets TDM TX V-Sense time slot and enable.

图 8-33. TDM_CFG5 Register Address: 0x0F

| | | | | | | | |
|----------|---------|----------------|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | VSNS_TX | VSNS_SLOT[5:0] | | | | | |

图 8-33. TDM_CFG5 Register Address: 0x0F (continued)

| | | |
|-------|-------|-------|
| RW-0h | RW-0h | RW-2h |
|-------|-------|-------|

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 8-97. TDM Configuration 5 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------------|------|-------|--|
| 7 | Reserved | RW | 0h | Reserved |
| 6 | VSNS_TX | RW | 0h | TDM TX voltage sense transmit enable. 0b = Disabled 1b = Enabled |
| 5-0 | VSNS_SLOT[5:0] | RW | 2h | TDM TX voltage sense time slot. It is recommended to maintain the following order: ISNS_SLOT<VSNS_SLOT<PDM_SLOT<VBAT_SLOT<TEMP_SLOT<GAIN_SLOT |

8.5.2.17 TDM_CFG6 (book=0x00 page=0x00 address=0x10) [reset=0h]

Sets TDM TX I-Sense time slot and enable.

图 8-34. TDM_CFG6 Register Address: 0x10

| | | | | | | | |
|----------|---------|----------------|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | ISNS_TX | ISNS_SLOT[5:0] | | | | | |
| RW-0h | RW-0h | RW-0h | | | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 8-98. TDM Configuration 6 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------------|------|-------|--|
| 7 | Reserved | RW | 0h | Reserved |
| 6 | ISNS_TX | RW | 0h | TDM TX current sense transmit enable. 0b = Disabled 1b = Enabled |
| 5-0 | ISNS_SLOT[5:0] | RW | 0h | TDM TX current sense time slot. It is recommended to maintain the following order: ISNS_SLOT<VSNS_SLOT<PDM_SLOT<VBAT_SLOT<TEMP_SLOT<GAIN_SLOT |

8.5.2.18 TDM_CFG7 (book=0x00 page=0x00 address=0x11) [reset=4h]

Sets TDM TX time slot and transmit enable for decimated PDM.

图 8-35. TDM_CFG7 Register Address: 0x11

| | | | | | | | |
|----------|--------|---------------|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | PDM_TX | PDM_SLOT[5:0] | | | | | |
| RW-0h | RW-0h | RW-4h | | | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 8-99. TDM Configuration 7 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|---------------|------|-------|--|
| 7 | Reserved | RW | 0h | Reserved |
| 6 | PDM_TX | RW | 0h | TDM TX decimated PDM transmit enable. 0b = Disabled 1b = Enabled |
| 5-0 | PDM_SLOT[5:0] | RW | 4h | TDM TX decimated PDM time slot. |

8.5.2.19 TDM_CFG8 (book=0x00 page=0x00 address=0x12) [reset=6h]

Sets TDM TX VBAT time slot and enable.

图 8-36. TDM_CFG8 Register Address: 0x12

| | | | | | | | |
|-----------|---------|----------------|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| VBAT_SLEN | VBAT_TX | VBAT_SLOT[5:0] | | | | | |
| RW-0h | RW-0h | RW-6h | | | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 8-100. TDM Configuration 8 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------------|------|-------|--|
| 7 | VBAT_SLEN | RW | 0h | TDM TX VBAT time slot length. 0b = Truncate to 8-bits 1b = Left justify to 16-bits |
| 6 | VBAT_TX | RW | 0h | TDM TX VBAT transmit enable. 0b = Disabled 1b = Enabled |
| 5-0 | VBAT_SLOT[5:0] | RW | 6h | TDM TX VBAT time slot. |

8.5.2.20 TDM_CFG9 (book=0x00 page=0x00 address=0x13) [reset=7h]

Sets TDM TX temp time slot and enable.

图 8-37. TDM_CFG9 Register Address: 0x13

| | | | | | | | |
|----------|---------|----------------|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | TEMP_TX | TEMP_SLOT[5:0] | | | | | |
| RW-0h | RW-0h | RW-7h | | | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 8-101. TDM Configuration 9 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------------|------|-------|--|
| 7 | Reserved | RW | 0h | Reserved |
| 6 | TEMP_TX | RW | 0h | TDM TX temp sensor transmit enable. 0b = Disabled 1b = Enabled |
| 5-0 | TEMP_SLOT[5:0] | RW | 7h | TDM TX temp sensor time slot. |

8.5.2.21 TDM_CFG10 (book=0x00 page=0x00 address=0x14) [reset=8h]

Sets TDM TX limiter gain reduction time slot and enable.

图 8-38. TDM_CFG10 Register Address: 0x14

| | | | | | | | |
|----------|---------|----------------|---|---|---|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | GAIN_TX | GAIN_SLOT[5:0] | | | | | |
| RW-0h | RW-0h | RW-8h | | | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 8-102. TDM Configuration 10 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------|------|-------|-------------|
| 7 | Reserved | RW | 0h | Reserved |

表 8-102. TDM Configuration 10 Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|----------------|------|-------|---|
| 6 | GAIN_TX | RW | 0h | TDM TX limiter gain reduction transmit enable. 0b = Disabled 1b = Enabled |
| 5-0 | GAIN_SLOT[5:0] | RW | 8h | TDM TX limiter gain reduction time slot. |

8.5.2.22 LIM_CFG0 (book=0x00 page=0x00 address=0x15) [reset=14h]

Sets Limiter attack step size, attack rate and enable.

图 8-39. LIM_CFG0 Register Address: 0x15

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|---|-----------------|---|-----------------|---|---|--------|
| Reserved | | LIM_ATK_ST[1:0] | | LIM_ATK_RT[2:0] | | | LIM_EN |
| RW-0h | | RW-1h | | RW-2h | | | RW-0h |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 8-103. Limiter Configuration 0 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------------|------|-------|---|
| 7-6 | Reserved | RW | 0h | Reserved |
| 5-4 | LIM_ATK_ST[1:0] | RW | 1h | Limiter/ICLA attack step size. 00b = 0.25 dB 01b = 0.5 dB 10b = 1 dB 11b = 2 dB |
| 3-1 | LIM_ATK_RT[2:0] | RW | 2h | Limiter/ICLA attack rate. 000b = 5 us/step 001b = 10 us/step 010b = 20 us/step 011b = 40 us/step 100b = 80 us/step 101b = 160 us/step 110b = 320 us/step 111b = 640 us/step |
| 0 | LIM_EN | RW | 0h | Limiter enable. 0b = Disabled 1b = Enabled |

8.5.2.23 LIM_CFG1 (book=0x00 page=0x00 address=0x16) [reset=76h]

Sets limiter release step size, release rate and hold time.

图 8-40. LIM_CFG1 Register Address: 0x16

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------------|---|-----------------|---|---|-----------------|---|---|
| LIM_RLS_ST[1:0] | | LIM_RLS_RT[2:0] | | | LIM_HLD_TM[2:0] | | |
| RW-1h | | RW-6h | | | RW-6h | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 8-104. Limiter Configuration 1 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------------|------|-------|--|
| 7-6 | LIM_RLS_ST[1:0] | RW | 1h | Limiter/BOP/ICLA release step size. 00b = 0.25 dB 01b = 0.5 dB 10b = 1 dB 11b = 2 dB |

表 8-104. Limiter Configuration 1 Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-----------------|------|-------|--|
| 5-3 | LIM_RLS_RT[2:0] | RW | 6h | Limiter/BOP/ICLA release rate. 000b = 10 ms/step 001b = 50 ms/step 010b = 100 ms/step 011b = 250 ms/step 100b = 500 ms/step 101b = 750 ms/step 110b = 1000 ms/step 111b = 1500 ms/step |
| 2-0 | LIM_HLD_TM[2:0] | RW | 6h | Limiter hold time. 000b = 0 ms 001b = 10 ms 010b = 25 ms 011b = 50 ms 100b = 100 ms 101b = 250 ms 110b = 500 ms 111b = 1000 ms |

8.5.2.24 LIM_CFG2 (book=0x00 page=0x00 address=0x17) [reset=10h]

Sets limiter VBAT tracking slope and max attenuatio.

图 8-41. LIM_CFG2 Register Address: 0x17

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|---|---|------------------|---|---|---|---|
| Reserved | | | LIM_MAX_ATN[4:0] | | | | |
| RW-0h | | | RW-10h | | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 8-105. Limiter Configuration 2 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|------------------|------|-------|--|
| 7-5 | Reserved | RW | 0h | Reserved |
| 4-0 | LIM_MAX_ATN[4:0] | RW | 10h | Limiter max attenuation. 00h = 1 dB 01h = 1.5 dB ... 10h = 9 dB ... 1Eh = 16 dB 1Fh = 16.5 dB |

8.5.2.25 LIM_CFG3 (book=0x00 page=0x00 address=0x18) [reset=6Eh]

Sets Limiter max threshold.

图 8-42. LIM_CFG3 Register Address: 0x18

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|-----------------|---|---|---|---|---|---|
| Reserved | LIM_TH_MAX[6:0] | | | | | | |
| RW-0h | RW-6Eh | | | | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 8-106. Limiter Configuration 3 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------|------|-------|-------------|
| 7 | Reserved | RW | 0h | Reserved |

表 8-106. Limiter Configuration 3 Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-----------------|------|-------|--|
| 6-0 | LIM_TH_MAX[6:0] | RW | 6Eh | Limiter max threshold. 00h = 2 V 01h = 2.1 V ... 6Eh = 13 V ... 7Eh = 14.6 V 7Fh = 14.7 V |

8.5.2.26 LIM_CFG4 (book=0x00 page=0x00 address=0x19) [reset=1Eh]

Sets limiter min threshold.

图 8-43. LIM_CFG4 Register Address: 0x19

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|-----------------|---|---|---|---|---|---|
| Reserved | LIM_TH_MIN[6:0] | | | | | | |
| RW-0h | RW-1Eh | | | | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 8-107. Limiter Configuration 4 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------------|------|-------|---|
| 7 | Reserved | RW | 0h | Reserved |
| 6-0 | LIM_TH_MIN[6:0] | RW | 1Eh | Limiter min threshold. 00h = 2 V 01h = 2.1 V ... 1Eh = 5 V ... 7Eh = 14.6 V 7Fh = 14.7 V |

8.5.2.27 LIM_CFG5 (book=0x00 page=0x00 address=0x1A) [reset=58h]

Sets limiter inflection point.

图 8-44. LIM_CFG5 Register Address: 0x1A

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|-----------------|---|---|---|---|---|---|
| Reserved | LIM_INF_PT[6:0] | | | | | | |
| RW-0h | RW-58h | | | | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 8-108. Limiter Configuration 5 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------------|------|-------|---|
| 7 | Reserved | RW | 0h | Reserved |
| 6-0 | LIM_INF_PT[6:0] | RW | 58h | Limiter inflection point. 00h = 2 V 01h = 2.1 V ... 58h = 10.8 V ... 7Eh = 14.6 V 7Fh = 14.7 V |

8.5.2.28 BOP_CFG0 (book=0x00 page=0x00 address=0x1B) [reset=1h]

Sets BOP infinite hold clear, infinite hold enable, mute on brown out and enable.

图 8-45. BOP_CFG0 Register Address: 0x1B

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|--------------------------|----------------|---|-------------|-------------|----------|--------|
| Reserved | EN_BO_RECOVERY_HYSTERSIS | LIM_SLOPE[1:0] | | BOP_HLD_CLR | BOP_INF_HLD | BOP_MUTE | BOP_EN |
| RW-0h | RW-0h | RW-0h | | RW-0h | RW-0h | RW-0h | RW-1h |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 8-109. Brown Out Prevention 0 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------------------|------|-------|---|
| 7 | Reserved | RW | 0h | Reserved |
| 6 | EN_BO_RECOVERY_HYSTERSIS | RW | 0h | |
| 5-4 | LIM_SLOPE[1:0] | RW | 0h | Limiter VBAT tracking slope. 00b = 1 V/V 01b = 1.5 V/V 10b = 2 V/V 11b = 4 V/V |
| 3 | BOP_HLD_CLR | RW | 0h | BOP infinite hold clear (self clearing). 0b = Don't clear 1b = Clear |
| 2 | BOP_INF_HLD | RW | 0h | Infinite hold on brown out event. 0b = Use BOP_HLD_TM after brown out event 1b = Don't release until BOP_HLD_CLR is asserted high |
| 1 | BOP_MUTE | RW | 0h | Mute on brown out event. 0b = Don't mute 1b = Mute followed by device shutdown |
| 0 | BOP_EN | RW | 1h | Brown out prevention enable. 0b = Disabled 1b = Enabled |

8.5.2.29 BOP_CFG1 (book=0x00 page=0x00 address=0x1C) [reset=14h]

BOP threshold.

图 8-46. BOP_CFG1 Register Address: 0x1C

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|---|---|---|---|---|---|---|
| BOP_TH[7:0] | | | | | | | |
| RW-14h | | | | | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 8-110. Brown Out Prevention 1 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------|------|-------|---|
| 7-0 | BOP_TH[7:0] | RW | 14h | Brown out prevention threshold. 00h = 4.5 V 01h = 4.525 V ... 14h = 5.0 V ... FEh = 10.85 V FFh = 10.875 V |

8.5.2.30 BOP_CFG2 (book=0x00 page=0x00 address=0x1D) [reset=4Eh]

BOP attack rate, attack step size and hold time.

图 8-47. BOP_CFG2 Register Address: 0x1D

| | | | | | | | |
|-----------------|---|---|-----------------|---|-----------------|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BOP_ATK_RT[2:0] | | | BOP_ATK_ST[1:0] | | BOP_HLD_TM[2:0] | | |
| RW-2h | | | RW-1h | | RW-6h | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 8-111. Brown Out Prevention 2 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------------|------|-------|---|
| 7-5 | BOP_ATK_RT[2:0] | RW | 2h | Brown out prevention attack rate. 000b = 5 us/step 001b = 10 us/step 010b = 20 us/step 011b = 40 us/step 100b = 80 us/step 101b = 160 us/step 110b = 320 us/step 111b = 640 us/step |
| 4-3 | BOP_ATK_ST[1:0] | RW | 1h | Brown out prevention attack step size. 00b = 0.5 dB 01b = 1 dB 10b = 1.5 dB 11b = 2 dB |
| 2-0 | BOP_HLD_TM[2:0] | RW | 6h | Brown out prevention hold time. 000b = 0 ms 001b = 10 ms 010b = 25 ms 011b = 50 ms 100b = 100 ms 101b = 250 ms 110b = 500 ms 111b = 1000 ms |

8.5.2.31 ICLA_CFG0 (book=0x00 page=0x00 address=0x1E) [reset=0h]

ICLA starting time slot and enable.

图 8-48. ICLA_CFG0 Register Address: 0x1E

| | | | | | | | |
|--------------|---|----------------|---|---|---|---|---------|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| ICLA_USE_MAX | | ICLA_SLOT[5:0] | | | | | ICLA_EN |
| RW-0h | | RW-0h | | | | | RW-0h |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 8-112. Inter Chip Limiter Alignment 0 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------------|------|-------|---|
| 7 | ICLA_USE_MAX | RW | 0h | Inter chip limiter alignment min/max config 0b = Use the maximum of the ICLA group gain reduction 1b = Use the minimum of the ICLA group gain reduction |
| 6-1 | ICLA_SLOT[5:0] | RW | 0h | Inter chip limiter alignment starting time slot. |
| 0 | ICLA_EN | RW | 0h | Inter chip limiter alignment enable. 0b = Disabled 1b = Enabled |

8.5.2.32 ICLA_CFG1 (book=0x00 page=0x00 address=0x1F) [reset=0h]

ICLA time slot enables.

图 8-49. ICLA_CFG1 Register Address: 0x1F

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| ICLA_SEN[7] | ICLA_SEN[6] | ICLA_SEN[5] | ICLA_SEN[4] | ICLA_SEN[3] | ICLA_SEN[2] | ICLA_SEN[1] | ICLA_SEN[0] |
| RW-0h | RW-0h | RW-0h | RW-0h | RW-0h | RW-0h | RW-0h | RW-0h |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 8-113. Inter Chip Limiter Alignment 1 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------|------|-------|---|
| 7 | ICLA_SEN[7] | RW | 0h | Time slot equals ICLA_SLOT[5:0]+7. When enabled, the limiter will include this time slot in the alignment group. 0b = Disabled 1b = Enabled |
| 6 | ICLA_SEN[6] | RW | 0h | Time slot equals ICLA_SLOT[5:0]+6. When enabled, the limiter will include this time slot in the alignment group. 0b = Disabled 1b = Enabled |
| 5 | ICLA_SEN[5] | RW | 0h | Time slot equals ICLA_SLOT[5:0]+5. When enabled, the limiter will include this time slot in the alignment group. 0b = Disabled 1b = Enabled |
| 4 | ICLA_SEN[4] | RW | 0h | Time slot equals ICLA_SLOT[5:0]+4. When enabled, the limiter will include this time slot in the alignment group. 0b = Disabled 1b = Enabled |
| 3 | ICLA_SEN[3] | RW | 0h | Time slot equals ICLA_SLOT[5:0]+3. When enabled, the limiter will include this time slot in the alignment group. 0b = Disabled 1b = Enabled |
| 2 | ICLA_SEN[2] | RW | 0h | Time slot equals ICLA_SLOT[5:0]+2. When enabled, the limiter will include this time slot in the alignment group. 0b = Disabled 1b = Enabled |
| 1 | ICLA_SEN[1] | RW | 0h | Time slot equals ICLA_SLOT[5:0]+1. When enabled, the limiter will include this time slot in the alignment group. 0b = Disabled 1b = Enabled |
| 0 | ICLA_SEN[0] | RW | 0h | Time slot equals ICLA_SLOT[5:0]. When enabled, the limiter will include this time slot in the alignment group. 0b = Disabled 1b = Enabled |

8.5.2.33 INT_MASK0 (book=0x00 page=0x00 address=0x20) [reset=FCh]

Interrupt masks.

图 8-50. INT_MASK0 Register Address: 0x20

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| INT_MASK[7] | INT_MASK[6] | INT_MASK[5] | INT_MASK[4] | INT_MASK[3] | INT_MASK[2] | INT_MASK[1] | INT_MASK[0] |
| RW-1h | RW-1h | RW-1h | RW-1h | RW-1h | RW-1h | RW-0h | RW-0h |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 8-114. Interrupt Mask 0 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------|------|-------|---|
| 7 | INT_MASK[7] | RW | 1h | Limiter mute mask. 0b = Don't Mask 1b = Mask |
| 6 | INT_MASK[6] | RW | 1h | Limiter infinite hold mask. 0b = Don't Mask 1b = Mask |
| 5 | INT_MASK[5] | RW | 1h | Limiter max attenuation mask. 0b = Don't Mask 1b = Mask |
| 4 | INT_MASK[4] | RW | 1h | VBAT <N521 Inflection Point mask. 0b = Don't Mask 1b = Mask |
| 3 | INT_MASK[3] | RW | 1h | Limiter active mask. 0b = Don't Mask 1b = Mask |
| 2 | INT_MASK[2] | RW | 1h | TDM clock error mask. 0b = Don't Mask 1b = Mask |
| 1 | INT_MASK[1] | RW | 0h | Over current error mask. 0b = Don't Mask 1b = Mask |
| 0 | INT_MASK[0] | RW | 0h | Over temp error mask. 0b = Don't Mask 1b = Mask |

8.5.2.34 INT_MASK1 (book=0x00 page=0x00 address=0x21) [reset=B1h]

Interrupt masks.

图 8-51. INT_MASK1 Register Address: 0x21

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|----------|----------|----------|--------------|--------------|-------------|-------------|
| INT_MASK[14] | Reserved | Reserved | Reserved | INT_MASK[11] | INT_MASK[10] | INT_MASK[9] | INT_MASK[8] |
| RW-1h | RW-0h | RW-1h | RW-1h | RW-0h | RW-0h | RW-0h | RW-1h |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 8-115. Interrupt Mask 1 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------|------|-------|--|
| 7 | INT_MASK[14] | RW | 1h | PDM audio data invalid mask. 0b = Don't Mask 1b = Mask |
| 6 | Reserved | RW | 0h | Reserved |
| 5 | Reserved | RW | 1h | Reserved |
| 4 | Reserved | RW | 1h | Reserved |
| 3 | INT_MASK[11] | RW | 0h | VBAT OVLO mask. 0b = Don't Mask 1b = Mask |
| 2 | INT_MASK[10] | RW | 0h | VBAT UVLO mask. 0b = Don't Mask 1b = Mask |
| 1 | INT_MASK[9] | RW | 0h | VBAT Brown out mask 0b = Don't Mask 1b = Mask |

表 8-115. Interrupt Mask 1 Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------------|------|-------|---|
| 0 | INT_MASK[8] | RW | 1h | PDM clock error mask. 0b = Don't Mask 1b = Mask |

8.5.2.35 INT_LIVE0 (book=0x00 page=0x00 address=0x22) [reset=0h]

Live interrupt readback.

图 8-52. INT_LIVE0 Register Address: 0x22

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| INT_LIVE[7] | INT_LIVE[6] | INT_LIVE[5] | INT_LIVE[4] | INT_LIVE[3] | INT_LIVE[2] | INT_LIVE[1] | INT_LIVE[0] |
| R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 8-116. Live Interrupt Readback 0 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------|------|-------|--|
| 7 | INT_LIVE[7] | R | 0h | Interrupt due to limiter mute. 0b = No interrupt 1b = Interrupt |
| 6 | INT_LIVE[6] | R | 0h | Interrupt due to limiter infinite hold. 0b = No interrupt 1b = Interrupt |
| 5 | INT_LIVE[5] | R | 0h | Interrupt due to limiter max attenuation. 0b = No interrupt 1b = Interrupt |
| 4 | INT_LIVE[4] | R | 0h | Interrupt due to VBAT below limiter inflection point. 0b = No interrupt 1b = Interrupt |
| 3 | INT_LIVE[3] | R | 0h | Interrupt due to limiter active. 0b = No interrupt 1b = Interrupt |
| 2 | INT_LIVE[2] | R | 0h | Interrupt due to TDM clock error. 0b = No interrupt 1b = Interrupt |
| 1 | INT_LIVE[1] | R | 0h | Interrupt due to over current error. 0b = No interrupt 1b = Interrupt |
| 0 | INT_LIVE[0] | R | 0h | Interrupt due to over temp error. 0b = No interrupt 1b = Interrupt |

8.5.2.36 INT_LIVE1 (book=0x00 page=0x00 address=0x23) [reset=0h]

Live interrupt readback.

图 8-53. INT_LIVE1 Register Address: 0x23

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|----------|----------|----------|--------------|--------------|-------------|-------------|
| INT_LIVE[15] | Reserved | Reserved | Reserved | INT_LIVE[11] | INT_LIVE[10] | INT_LIVE[9] | INT_LIVE[8] |
| R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 8-117. Live Interrupt Readback 1 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------|------|-------|--|
| 7 | INT_LIVE[15] | R | 0h | Interrupt due to PDM audio data invalid 0b = No interrupt 1b = Interrupt |
| 6 | Reserved | R | 0h | Reserved |
| 5 | Reserved | R | 0h | Reserved |
| 4 | Reserved | R | 0h | Reserved |
| 3 | INT_LIVE[11] | R | 0h | Interrupt due to VBAT OVLO flag. 0b = No interrupt 1b = Interrupt |
| 2 | INT_LIVE[10] | R | 0h | Interrupt due to VBAT UVLO flag. 0b = No interrupt 1b = Interrupt |
| 1 | INT_LIVE[9] | R | 0h | Interrupt due to VBAT brown out flag. 0b = No interrupt 1b = Interrupt |
| 0 | INT_LIVE[8] | R | 0h | Interrupt due to PDM clock error. 0b = No interrupt 1b = Interrupt |

8.5.2.37 INT_LTCH0 (book=0x00 page=0x00 address=0x24) [reset=0h]

Latched interrupt readback.

图 8-54. INT_LTCH0 Register Address: 0x24

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-------------|-------------|-------------|-------------|-------------|-------------|-------------|-------------|
| INT_LTCH[7] | INT_LTCH[6] | INT_LTCH[5] | INT_LTCH[4] | INT_LTCH[3] | INT_LTCH[2] | INT_LTCH[1] | INT_LTCH[0] |
| R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 8-118. Latched Interrupt Readback 0 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------|------|-------|--|
| 7 | INT_LTCH[7] | R | 0h | Interrupt due to limiter mute (read to clear). 0b = No interrupt 1b = Interrupt |
| 6 | INT_LTCH[6] | R | 0h | Interrupt due to limiter infinite hold (read to clear). 0b = No interrupt 1b = Interrupt |
| 5 | INT_LTCH[5] | R | 0h | Interrupt due to limiter max attenuation (read to clear). 0b = No interrupt 1b = Interrupt |
| 4 | INT_LTCH[4] | R | 0h | Interrupt due to VBAT < limiter inflection point (read to clear). 0b = No interrupt 1b = Interrupt |
| 3 | INT_LTCH[3] | R | 0h | Interrupt due to limiter active (read to clear). 0b = No interrupt 1b = Interrupt |
| 2 | INT_LTCH[2] | R | 0h | Interrupt due to TDM clock error (read to clear). 0b = No interrupt 1b = Interrupt |
| 1 | INT_LTCH[1] | R | 0h | Interrupt due to over current error (read to clear). 0b = No interrupt 1b = Interrupt |

表 8-118. Latched Interrupt Readback 0 Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|-------------|------|-------|--|
| 0 | INT_LTCH[0] | R | 0h | Interrupt due to over temp error (read to clear). 0b = No interrupt 1b = Interrupt |

8.5.2.38 INT_LTCH1 (book=0x00 page=0x00 address=0x25) [reset=0h]

Latched interrupt readback.

图 8-55. INT_LTCH1 Register Address: 0x25

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|----------|----------|----------|--------------|--------------|-------------|-------------|
| INT_LTCH[15] | Reserved | Reserved | Reserved | INT_LTCH[11] | INT_LTCH[10] | INT_LTCH[9] | INT_LTCH[8] |
| R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 8-119. Latched Interrupt Readback 1 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------|------|-------|--|
| 7 | INT_LTCH[15] | R | 0h | Interrupt due to PDM audio data invalid. (read to clear). 0b = No interrupt 1b = Interrupt |
| 6 | Reserved | R | 0h | Reserved |
| 5 | Reserved | R | 0h | Reserved |
| 4 | Reserved | R | 0h | Reserved |
| 3 | INT_LTCH[11] | R | 0h | Interrupt due to VBAT OVLO flag (read to clear). 0b = No interrupt 1b = Interrupt |
| 2 | INT_LTCH[10] | R | 0h | Interrupt due to VBAT UVLO flag (read to clear). 0b = No interrupt 1b = Interrupt |
| 1 | INT_LTCH[9] | R | 0h | Interrupt due to VBAT brown out flag (read to clear). 0b = No interrupt 1b = Interrupt |
| 0 | INT_LTCH[8] | R | 0h | Interrupt due to PDM clock error (read to clear). 0b = No interrupt 1b = Interrupt |

8.5.2.39 INT_LTCH2 (book=0x00 page=0x00 address=0x26) [reset=0h]

表 8-120. INT_LTCH2 Register Address: 0x26

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|--------------|--------------|--------------|--------------|--------------|--------------|--------------|
| INT_LTCH[23] | INT_LTCH[22] | INT_LTCH[21] | INT_LTCH[20] | INT_LTCH[19] | INT_LTCH[18] | INT_LTCH[17] | INT_LTCH[16] |
| R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h | R-0h |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 8-121. INT_LTCH2 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------|------|-------|--|
| 7 | INT_LTCH[23] | R | 0h | Interrupt due to clock halt flag (read to clear) 0b = No interrupt 1b = Interrupt |
| 6 | INT_LTCH[22] | R | 0h | Interrupt due to DMA Request to DSP lost flag (read to clear) 0b = No interrupt 1b = Interrupt |

表 8-121. INT_LTCH2 Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|--------------|------|-------|--|
| 5 | INT_LTCH[21] | R | 0h | Interrupt due to Auto Trim converged status (read to clear) 0b = No interrupt 1b = Interrupt |
| 4 | INT_LTCH[20] | R | 0h | Interrupt due to Class D Clamp status flag (read to clear) 0b = No interrupt 1b = Interrupt |
| 3 | INT_LTCH[19] | R | 0h | Interrupt due to HIGH SIDE OC flag (read to clear). 0b = No interrupt 1b = Interrupt |
| 2 | INT_LTCH[18] | R | 0h | Interrupt due to LOW SIDE OC flag (read to clear). 0b = No interrupt 1b = Interrupt |
| 1 | INT_LTCH[17] | R | 1h | Interrupt due to LDO 5 V PG flag (read to clear). 0b = No interrupt 1b = Interrupt |
| 0 | INT_LTCH[16] | R | 0h | Interrupt due to LDO 5 V OL (read to clear). 0b = No interrupt 1b = Interrupt |

8.5.2.40 VBAT_MSB (book=0x00 page=0x00 address=0x27) [reset=0h]

MSBs of SAR ADC VBAT conversion.

图 8-56. VBAT_MSB Register Address: 0x27

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------------|---|---|---|---|---|---|---|
| VBAT_CNV[11:4] | | | | | | | |
| R-0h | | | | | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 8-122. SAR ADC Conversion 0 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------------|------|-------|---------------------------------------|
| 7-4 | VBAT_CNV[11:0] | R | 0h | Returns SAR ADC VBAT conversion MSBs. |

8.5.2.41 VBAT_LSB (book=0x00 page=0x00 address=0x28) [reset=0h]

LSBs of SAR ADC VBAT conversion.

图 8-57. VBAT_LSB Register Address: 0x28

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------------|---|---|---|----------|---|---|---|
| VBAT_CNV[3:0] | | | | Reserved | | | |
| R-0h | | | | R-0h | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 8-123. SAR ADC Conversion 1 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|---------------|------|-------|---------------------------------------|
| 7-4 | VBAT_CNV[3:0] | R | 0h | Returns SAR ADC VBAT conversion LSBs. |
| 3-0 | Reserved | R | 0h | Reserved |

8.5.2.42 TEMP_MSB (book=0x00 page=0x00 address=0x29) [reset=0h]

SARD ADC Temp conversion.

图 8-58. TEMP_MSB Register Address: 0x29

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------------|---|---|---|---|---|---|---|
| TMP_CNV[11:4] | | | | | | | |
| R-0h | | | | | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 8-124. SAR ADC Conversion 2 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|---------------|------|-------|---|
| 7-4 | TMP_CNV[11:0] | R | 0h | Returns SAR ADC temp sensor conversion. |

8.5.2.43 TEMP_LSB (book=0x00 page=0x00 address=0x2A) [reset=0h]

SARD ADC Temp conversion.

图 8-59. TEMP_LSB Register Address: 0x2A

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--------------|---|---|---|----------|---|---|---|
| TMP_CNV[3:0] | | | | Reserved | | | |
| -0h | | | | R-0h | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 8-125. SAR ADC Conversion 2 Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|--------------|------|-------|---|
| 7-4 | TMP_CNV[3:0] | | 0h | Returns SAR ADC temp sensor conversion. |
| 3-0 | Reserved | R | 0h | Reserved |

8.5.2.44 INT_CFG (book=0x00 page=0x00 address=0x30) [reset=5h]

Sets whether latched or live interrupts will trigger IRQZ pin.

图 8-60. INT_CFG Register Address: 0x30

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|---|---|---|---|---|-------------------|---|
| Reserved | | | | | | IRQZ_PIN_CFG[1:0] | |
| RW-0h | | | | | | RW-1h | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 8-126. Interrupt Configuration Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------------|------|-------|---|
| 7-2 | Reserved | RW | 0h | Reserved |
| 1-0 | IRQZ_PIN_CFG[1:0] | RW | 1h | IRQZ interrupt configuration. 00b = IRQZ will assert on any unmasked live interrupts 01b = IRQZ will assert on any unmasked latched interrupts 10b = IRQZ will assert for 2ms one time on any unmasked live interrupt event 11b = IRQZ will assert for 2ms every 4ms on any unmasked latched interrupts |

8.5.2.45 DIN_PD (book=0x00 page=0x00 address=0x31) [reset=0h]

Sets enables of input pin weak pull down.

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

图 8-61. DIN_PD Register Address: 0x31

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------|-----------|-----------|-----------|----------|-----------|----------|-----------|
| DIN_PD[7] | DIN_PD[6] | DIN_PD[5] | DIN_PD[4] | Reserved | DIN_PD[2] | Reserved | DIN_PD[0] |
| RW-0h | RW-0h | RW-0h | RW-0h | RW-0h | RW-0h | RW-0h | RW-0h |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 8-127. Digital Input Pin Pull Down Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------|------|-------|---|
| 7 | DIN_PD[7] | RW | 0h | Weak pull down for SDOOUT 0b = Disabled 1b = Enabled |
| 6 | DIN_PD[6] | RW | 0h | Weak pull down for SDIN. 0b = Disabled 1b = Enabled |
| 5 | DIN_PD[5] | RW | 0h | Weak pull down for FSYNC. 0b = Disabled 1b = Enabled |
| 4 | DIN_PD[4] | RW | 0h | Weak pull down for SBCLK. 0b = Disabled 1b = Enabled |
| 3 | Reserved | RW | 0h | Reserved |
| 2 | DIN_PD[2] | RW | 0h | Weak pull down for PDMD1. 0b = Disabled 1b = Enabled |
| 0 | Reserved | RW | 0h | Reserved |
| 0 | DIN_PD[0] | RW | 0h | Weak pull down for PDMCK1. 0b = Disabled 1b = Enabled |

8.5.2.46 MISC_IRQ (book=0x00 page=0x00 address=0x32) [reset=81h]

Set IRQZ pin active state

图 8-62. MISC_IRQ Register Address: 0x32

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------|----------|---|---|----------|----------|----------|----------|
| IRQZ_POL | Reserved | | | Reserved | Reserved | Reserved | IRQZ_VAL |
| RW-1h | RW-0h | | | RW-0h | RW-0h | RW-0h | R-1h |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 8-128. Misc Configuration Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------|------|-------|--|
| 7 | IRQZ_POL | RW | 1h | IRQZ pin polarity for interrupt. 0b = Active high (IRQ) 1b = Active low (IRQZ) |
| 6-4 | Reserved | RW | 0h | Reserved |
| 3 | Reserved | RW | 0h | Reserved |
| 2 | Reserved | RW | 0h | Reserved |
| 1 | Reserved | RW | 0h | Reserved |
| 0 | IRQZ_VAL | R | 1h | IRQZ bit bang in read value. Default is 1b'1 if there are no interrupts/errors 0b = IRQZ Input Buffer Value=0 1b = IRQZ Input Buffer Value=1 |

8.5.2.47 CLOCK_CFG (book=0x00 page=0x00 address=0x3C) [reset=Dh]

Can override audio configure and set the clocking ratio

图 8-63. CLOCK_CFG Register Address: 0x3C

| | | | | | | | |
|----------|----------|---------------------|---|---|---|---------------|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | Reserved | SBCLK_FS_RATIO[3:0] | | | | AUTO_CLK[1:0] | |
| RW-0h | RW-0h | RW-3h | | | | RW-1h | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 8-129. Clock Configuration Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|---------------------|------|-------|---|
| 7 | Reserved | RW | 0h | Reserved |
| 6 | Reserved | RW | 0h | Reserved |
| 5-2 | SBCLK_FS_RATIO[3:0] | RW | 3h | Program manually SBCLK to FS ratio when auto clock detection is disabled 00h = 16 01h = 24 02h = 32 03h = 48 04h = 64 05h = 96 06h = 128 07h = 192 08h = 256 09h = 384 0Ah = 512 |
| 1-0 | AUTO_CLK[1:0] | RW | 1h | Clocking automatic configuraiton 00b = Auto configure clock dividers based on SBCLK to FSYNC ratio 01b = Manually configure clock dividers by programming SBCLK_FS_RATIO |

8.5.2.48 TDM_DET (book=0x00 page=0x00 address=0x77) [reset=7Fh]

Readback of internal auto-rate detection.

图 8-64. TDM_DET Register Address: 0x77

| | | | | | | | |
|----------|---------------|---|---|---|----------------|---|---|
| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | FS_RATIO[3:0] | | | | FS_RATE_V[2:0] | | |
| R-0h | R-Fh | | | | R-7h | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 8-130. TDM Clock detection monitor Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------|------|-------|-------------|
| 7 | Reserved | R | 0h | Reserved |

表 8-130. TDM Clock detection monitor Field Descriptions (continued)

| Bit | Field | Type | Reset | Description |
|-----|----------------|------|-------|---|
| 6-3 | FS_RATIO[3:0] | R | Fh | Detected SBCLK to FSYNC ratio. 00h = 16 01h = 24 02h = 32 03h = 48 04h = 64 05h = 96 06h = 128 07h = 192 08h = 256 09h = 384 0Ah = 512 0Bh-0Eh = Reserved 0F = Invalid ratio |
| 2-0 | FS_RATE_V[2:0] | R | 7h | Detected sample rate of TDM bus. 000b = Reserved 001b = Reserved 010b = Reserved 011b = 44.1/48 KHz 100b = 88.2/96 kHz 101b = 176.4/192 kHz 110b = Reserved 111b = Error condition |

8.5.2.49 REV_ID (book=0x00 page=0x00 address=0x7D) [reset=20h]

Returns REV and PG ID.

图 8-65. REV_ID Register Address: 0x7D

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|--|---|---|---|------------|---|---|---|
| REV_ID[3:0] | | | | PG_ID[3:0] | | | |
| R-1h (TAS2770 QFN Rev A) R-2h (TAS2770 QFN Rev B) R- 4h (TAS2770 WCSP Rev B) R- 5h (TAS2770 WCSP Rev C) | | | | R-0h | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 8-131. Revision and PG ID Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-------------|------|-------------------|--------------------------|
| 7-4 | REV_ID[3:0] | R | (see above table) | Returns the revision ID. |
| 3-0 | PG_ID[3:0] | R | 0h | Returns the PG ID. |

8.5.2.50 I2C_CKSUM (book=0x00 page=0x00 address=0x7E) [reset=0h]

Returns I2C checksum.

图 8-66. I2C_CKSUM Register Address: 0x7E

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|----------------|---|---|---|---|---|---|---|
| I2C_CKSUM[7:0] | | | | | | | |
| RW-0h | | | | | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 8-132. I2C Checksum Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|----------------|------|-------|--|
| 7-0 | I2C_CKSUM[7:0] | RW | 0h | Returns I2C checksum. Writing to this register will reset the checksum to the written value. This register is updated on writes to other registers on all books and pages. |

8.5.2.51 BOOK (book=0x00 page=0x00 address=0x7F) [reset=0h]

Device's memory map is divided into pages and books. This register sets the book.

图 8-67. BOOK Register Address: 0x7F

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|-----------|---|---|---|---|---|---|---|
| BOOK[7:0] | | | | | | | |
| RW-0h | | | | | | | |

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

表 8-133. Device Book Field Descriptions

| Bit | Field | Type | Reset | Description |
|-----|-----------|------|-------|--|
| 7-0 | BOOK[7:0] | RW | 0h | Sets the device book. 00h = Book 0 01h = Book 1 ... FFh = Book 255 |

9 Application and Implementation

备注

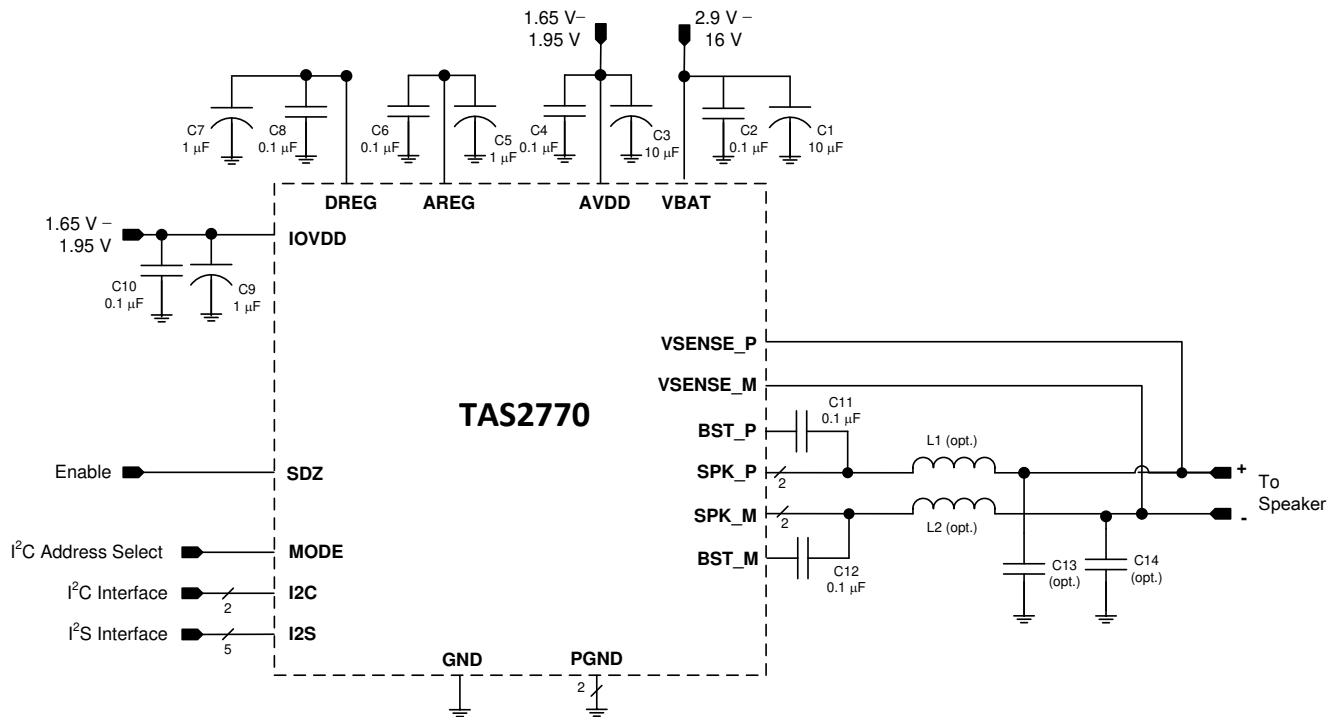
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TAS2770 is a digital input Class-D audio power amplifier with integrated I/V sense. I2S audio data is supplied by host processor. It also accepts I/V data in I2S format. I²C bus is used for configuration and control.

9.2 Typical Application

图 9-1 below shows a typical configuration of the TAS2770.



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图 9-1. TAS2770 Typical Application

表 9-1. Recommended External Components

| COMPONENT | DESCRIPTION | SPECIFICATIO N | MIN | TYP | MAX | UNIT | NOTES |
|-----------|---------------------------------|-------------------|-----|-----|-----|------|-------|
| C1 | VBAT Decoupling Capacitor | Capacitance | 10 | 22 | | μF | |
| | | Rated Voltage | 25 | | | V | |
| C2 | VBAT Decoupling Capacitor | Capacitance | 0.1 | | | μF | |
| | | Rated Voltage | 25 | | | V | |

表 9-1. Recommended External Components (continued)

| COMPONENT | DESCRIPTION | SPECIFICATION | MIN | TYP | MAX | UNIT | NOTES |
|-----------|---|---------------|------|-----|------|------|--------------------|
| C3 | AVDD Decoupling Capacitor | Capacitance | 1 | 10 | | μF | |
| | | Rated Voltage | 10 | | | V | |
| C4 | AVDD Decoupling Capacitor | Capacitance | 0.1 | | | μF | |
| | | Rated Voltage | 10 | | | V | |
| C5 | AREG Decoupling Capacitor | Capacitance | 0.68 | 1 | 1.5 | μF | |
| | | Rated Voltage | 10 | | | V | |
| C6 | AREG Decoupling Capacitor | Capacitance | | 0.1 | | μF | C5 + C6 < 1.5μF |
| | | Rated Voltage | 10 | | | V | |
| C7 | DREG Decoupling Capacitor | Capacitance | 0.68 | 1 | 1.5 | μF | |
| | | Rated Voltage | 10 | | | V | |
| C8 | DREG Decoupling Capacitor | Capacitance | | 0.1 | | μF | C7 + C8 < 1.5μF |
| | | Rated Voltage | 10 | | | V | |
| C9 | IOVDD Decoupling Capacitor | Capacitance | 1 | | | μF | |
| | | Rated Voltage | 10 | | | V | |
| C10 | IOVDD Decoupling Capacitor | Capacitance | 0.1 | | | μF | |
| | | Rated Voltage | 10 | | | V | |
| C11 | Class-D Positive Bootstrap Capacitor | Capacitance | | 0.1 | 0.12 | μF | |
| | | Rated Voltage | 25 | | | V | |
| C12 | Class-D Negative Bootstrap Capacitor | Capacitance | | 0.1 | 0.12 | μF | |
| | | Rated Voltage | 25 | | | V | |
| C13, C14 | EMI Filter Capacitors (optional). Optional inductors L1 and L2 must be connected when the EMI Filter capacitors are placed | Capacitance | | 1 | | nF | |
| | | Rated Voltage | 25 | | | V | |

表 9-1. Recommended External Components (continued)

| COMPONENT | DESCRIPTION | SPECIFICATIO N | MIN | TYP | MAX | UNIT | NOTES |
|-----------|---|---------------------|-----|------|-------|----------|-------|
| L1, L2 | EMI Filter Inductors (optional). SPK_P pin must be directly connected to VSENSE_P when the inductors are used. Optional capacitors C13 and C14 must be connected when the EMI filter inductors are placed | Impedance at 100MHz | | 120 | | Ω | |
| | | DC Resistance | | | 0.095 | Ω | |
| | | DC Current | | 4 | 6 | A | |
| | | Size | | 0402 | | EIA | |

9.2.1 Design Requirements

表 9-2 shows the design parameters.

表 9-2. Recommended Component Selection

| PARAMETER | EXAMPLE VALUE |
|-------------------------------|------------------|
| Amplifier power supply (VBAT) | 4.5 V to 16 V |
| EVM power supply | 4.5 V to 16 V |
| IO power supply (IOVDD) | 1.65 V to 1.95 V |
| Output Power | 18.3 W |
| USB, USB class-audio | Micro-USB B |

9.2.2 Detailed Design Procedure

9.2.2.1 Overview

The TAS2770 is a flexible and easy-to-use Class D amplifier. Therefore, the design process is straightforward.

Before beginning the design, gather the following information regarding the audio system:

- VBAT rail planned for the design
- Speaker or load impedance
- Audio sample rate
- Maximum output power requirement

9.2.2.2 Select Input Capacitance

Select the bulk capacitors at the VBAT inputs for proper voltage margin and adequate capacitance to support the power requirements. The TAS2770 has very good PSRR, so the capacitor is more about limiting the ripple and droop for the rest of system than preserving good audio performance. The amount of bulk decoupling can be reduced as long as the droop and ripple is acceptable. One capacitor should be placed near the VBAT pin. VBATY capacitors should be a low ESR type because they are being used in a high-speed switching application.

9.2.2.3 Select Decoupling Capacitors

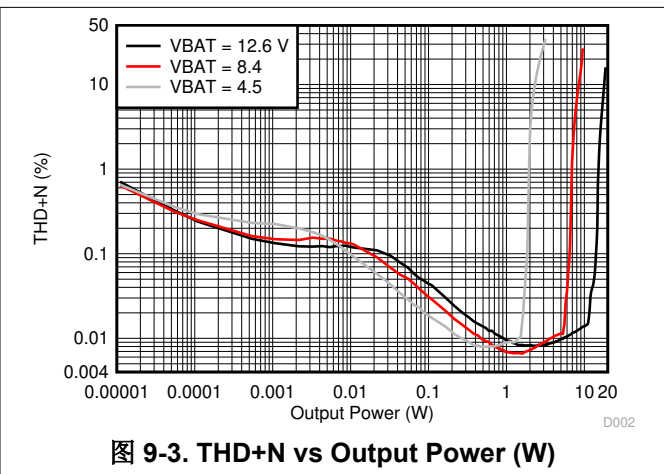
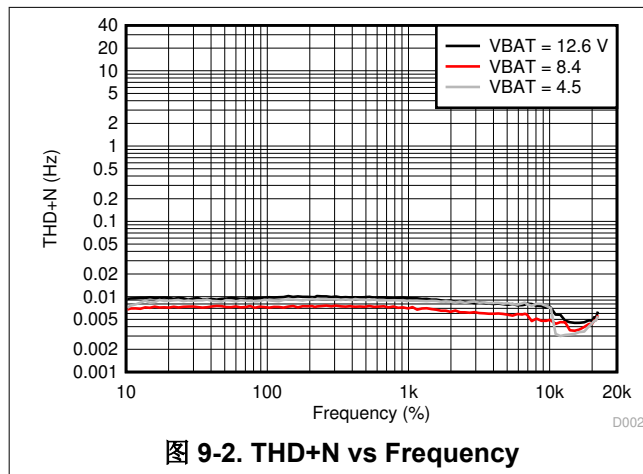
Good quality decoupling capacitors should be added at each of the VBAT input to provide good reliability, good audio performance, and to meet regulatory requirements. X5R or better ratings should be used in this application. Consider temperature, ripple current, and voltage overshoots when selecting decoupling capacitors.

Also, the decoupling capacitors should be located near the VBAT and GND connections to the device to minimize series inductances.

9.2.2.4 Select Bootstrap Capacitors

Each of the outputs require bootstrap capacitors to provide gate drive for the high-side output FETs. For this design, use 0.1- μ F, 25-V capacitors of X5R quality or better.

9.2.3 Application Curves



9.3 Initialization Set Up

9.3.1 Initial Device Configuration - Auto Rate

The following I2C sequence is an example of initializing four TAS5770LC0 devices. The devices will be configured to use the TDM auto-rate detection feature. This sequence contains a 1 ms delay required after a software or hardware reset as illustrated in [节 10](#).

备注

For TAS2770 the device I2C address needs to be changed. See [表 8-1](#).

```
w 62 00 00 # Page-0
w 62 7f 00 # Book-0
w 62 01 01 # Software Reset
w 64 00 00 # Page-0
w 64 7f 00 # Book-0
w 64 01 01 # Software Reset
w 66 00 00 # Page-0
w 66 7f 00 # Book-0
w 66 01 01 # Software Reset
w 68 00 00 # Page-0
w 68 7f 00 # Book-0
w 68 01 01 # Software Reset
d 1 # 1ms Delay
##### Configure Channel 1
w 62 3c 11 # sbclk to fs ratio = 64
w 62 0e 33 # TX bus keeper, Hi-Z, offset 1, TX on Falling edge
w 62 0f 42 # TDM TX voltage sense transmit enable with slot 2,
w 62 10 40 # TDM TX current sense transmit enable with slot 0
w 62 03 14 # 21 dB gain
w 62 02 00 # power up audio playback with I,V enabled
##### Configure Channel 2
w 64 3c 11 # sbclk to fs ratio = 64
w 64 0e 13 # TX bus keeper, Hi-Z, offset 1, TX on Falling edge
w 64 0f 46 # TDM TX voltage sense transmit enable with slot 6,
w 64 10 44 # TDM TX current sense transmit enable with slot 4
w 64 03 14 # 21 dB gain
w 64 02 00 # power up audio playback with I,V enabled
##### Configure Channel 3
w 66 3c 11 # sbclk to fs ratio = 64
w 66 0e 13 # TX bus keeper, Hi-Z, offset 1, TX on Falling edge
w 66 0f 4a # TDM TX voltage sense transmit enable with slot 10,
w 66 10 48 # TDM TX current sense transmit enable with slot 8
w 66 03 14 # 21 dB gain
w 66 02 00 # power up audio playback with I,V enabled
##### Configure Channel 4
w 68 3c 11 # sbclk to fs ratio = 64
w 68 0e 13 # TX bus keeper, Hi-Z, offset 1, TX on Falling edge
w 68 0f 4e # TDM TX voltage sense transmit enable with slot 14,
w 68 10 4c # TDM TX current sense transmit enable with slot 12
w 68 03 14 # 21 dB gain
w 68 02 00 # power up audio playback with I,V enabled
```

9.3.2 Initial Device Configuration - 48 kHz

The following I2C sequence is an example of initializing a TAS5770LC0 device into 48 kHz sampling rate. This sequence contains a 1 ms delay required after a software or hardware reset as illustrated in [节 10](#).

备注

For TAS2770 the device I2C address needs to be changed. See [表 8-1](#).

```
w 62 00 00 # Page-0
w 62 7f 00 # Book-0
w 62 01 01 # Software Reset
d 1 # 1ms Delay
##### Configure Channel 1
w 62 3c 21 # sbclk to fs ratio = 256 / 8 TDM slots
```

```
w 62 0a 17 # 48KHz, Auto TDM off, Frame start High to Low
w 62 0b 03 # Offset = 1, Sync on BCLK falling edge
w 62 0c 0a # TDM slot by address, Word = 24 bit, Frame = 32 bit
w 62 0d 20 # Right Ch = TDM slot 2, Left Ch = TDM slot 0
w 62 0e 33 # TX bus keeper, Hi-Z, offset 1, TX on Falling edge
w 62 0f 42 # TDM TX voltage sense transmit enable with slot 2,
w 62 10 40 # TDM TX current sense transmit enable with slot 0
w 62 03 14 # 21 dB gain
w 62 02 00 # power up audio playback with I,V enabled
```

9.3.3 Initial Device Configuration - 44.1 kHz

The following I2C sequence is an example of initializing a TAS5770LC0 device into 48 kHz sampling rate. This sequence contains a 1 ms delay required after a software or hardware reset as illustrated in [节 10](#).

备注

For TAS2770 the device I2C address needs to be changed. See [表 8-1](#).

```
w 62 00 00 # Page-0
w 62 7f 00 # Book-0
w 62 01 01 # Software Reset
d 1 # 1mS Delay
##### Configure Channel 1
w 62 3c 21 # sbclk to fs ratio = 256 / 8 TDM Slots
w 62 0a 37 # 44.1KHz, Auto TDM off, Frame start High to Low
w 62 0b 03 # Offset = 1, Sync on BCLK falling edge
w 62 0c 0a # TDM slot by address, Word = 24 bit, Frame = 32 bit
w 62 0d 20 # Right Ch = TDM slot 2, Left Ch = TDM slot 0
w 62 0e 33 # TX bus keeper, Hi-Z, offset 1, TX on Falling edge
w 62 0f 42 # TDM TX voltage sense transmit enable with slot 2,
w 62 10 40 # TDM TX current sense transmit enable with slot 0
w 62 03 14 # 21 dB gain
w 62 02 00 # power up audio playback with I,V enabled
```

9.3.4 Sample Rate Change - 48 kHz to 44.1kHz

The following I2C sequence is an example of changing the sampling rate from 48 kHz to 44.1 kHz .

```
w 62 07 80 #Set DVC Ramp Rate to 0.5 dB / 8 samples
w 62 02 01 #Mute
d 1
w 62 02 02 #Software shutdown
w 62 0a 37 #44.1KHz, Auto TDM off, Frame start High to Low
### change source sample rate now
w 62 02 01 #Take device out of low-power shutdown
d 1
w 62 02 00 #Un-mute
```

9.3.5 Sample Rate Change - 44.1 kHz to 48 kHz

The following I2C sequence is an example of changing the sampling rate from 44.1 kHz to 48 kHz .

```
w 62 07 80 #Set DVC Ramp Rate to 0.5 dB / 8 samples
w 62 02 01 #Mute
d 1
w 62 02 02 #Software shutdown
w 62 0a 17 #44.1KHz, Auto TDM off, Frame start High to Low
### change source sample rate now
w 62 02 01 #Take device out of low-power shutdown
d 1
w 62 02 00 #Un-mute
```

9.3.6 Device Mute

The following I2C sequence will mute one device at address 62 using a digital volume ramp rate of 0.5 dB per 8 samples.

备注

For TAS2770 the device I2C address is 82

```
w 62 07 80 #Set DVC Ramp Rate to 0.5 dB / 8 samples
w 62 02 01 #Mute
```

9.3.7 Device Un-Mute

The following I2C sequence will un-mute one device at address 62 using a digital volume ramp rate of 0.5 dB per 8 samples.

备注

For TAS2770 the device I2C address is 82

```
w 62 07 80 #Set DVC Ramp Rate to 0.5 dB / 8 samples
w 62 02 00 #Un-Mute
```

9.3.8 Device Sleep

The following I2C sequence will mute the device and put it into low power mode for one device at address 62 using a digital volume ramp rate of 0.5 dB per 8 samples.

备注

For TAS2770 the device I2C address is 82

```
w 62 07 80 #Set DVC Ramp Rate to 0.5 dB / 8 samples
w 62 02 01 #Mute
d 1 # 1mS Delay
w 62 02 02 #Software shutdown
```

9.3.9 Device Wake

The following I2C sequence will wake the device from low power mode (sleep) and un-mute one device at address 62 using a digital volume ramp rate of 0.5 dB per 8 samples.

备注

For TAS2770 the device I2C address is 82

```
w 62 07 80 #Set DVC Ramp Rate to 0.5 dB / 8 samples
w 62 02 01 #Take device out of low-power shutdown
d 1 # 1mS Delay
w 62 02 00 #Un-mute TAS2770
```

10 Power Supply Recommendations

The power sequence between the supply rails can be applied in any order as long as SDZ pin is held low. Generally VBAT would be applied before IOVDD and AVDD in most system applications. Once all supplies are stable the SDZ pin can be set high to initialize the part. After a hardware or software reset additional commands to the device should be delayed for 1 mS to allow the OTP to load.

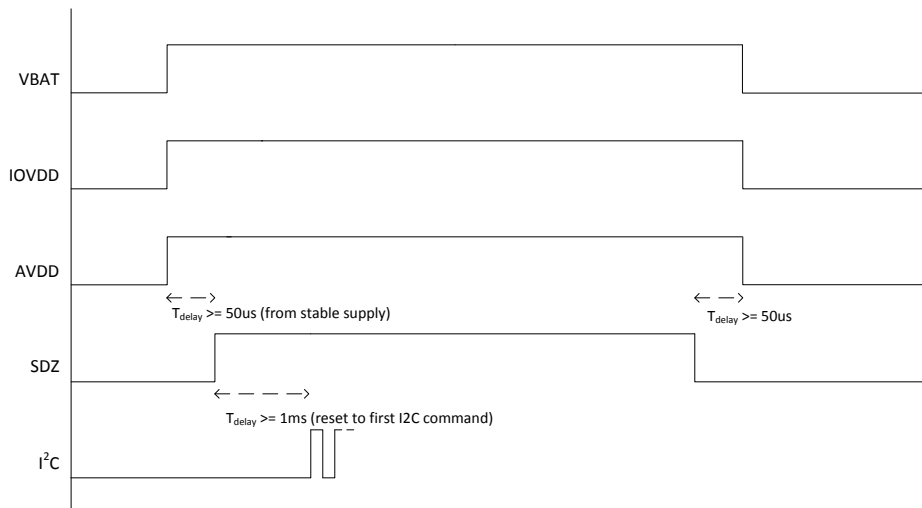


图 10-1. Power Supply Sequence for Power-Up and Power-Down

11 Layout

11.1 Layout Guidelines

Pay special attention to the power stage power supply layout.

- Use 4.7 μf for decoupling of VBAT supply.
- Keep the current circulating loops containing the supply decoupling capacitors, the H-bridges in the device and the connections to the speakers as tight as possible to reduce emissions.
- Use ground planes to provide the lowest impedance for power and signal current between the device and the decoupling capacitors. The area directly under the device should be treated as a central ground area for the device, and all device grounds must be connected directly to that area.
- Use a via pattern to connect the area directly under the device to the ground planes in copper layers below the surface. This connection helps to dissipate heat from the device.
- Avoid interrupting the ground plane with circular traces around the device. Interruption disconnects the copper and interrupt flow of heat and current. Radial copper traces are better to use if necessary.

11.2 Layout Example

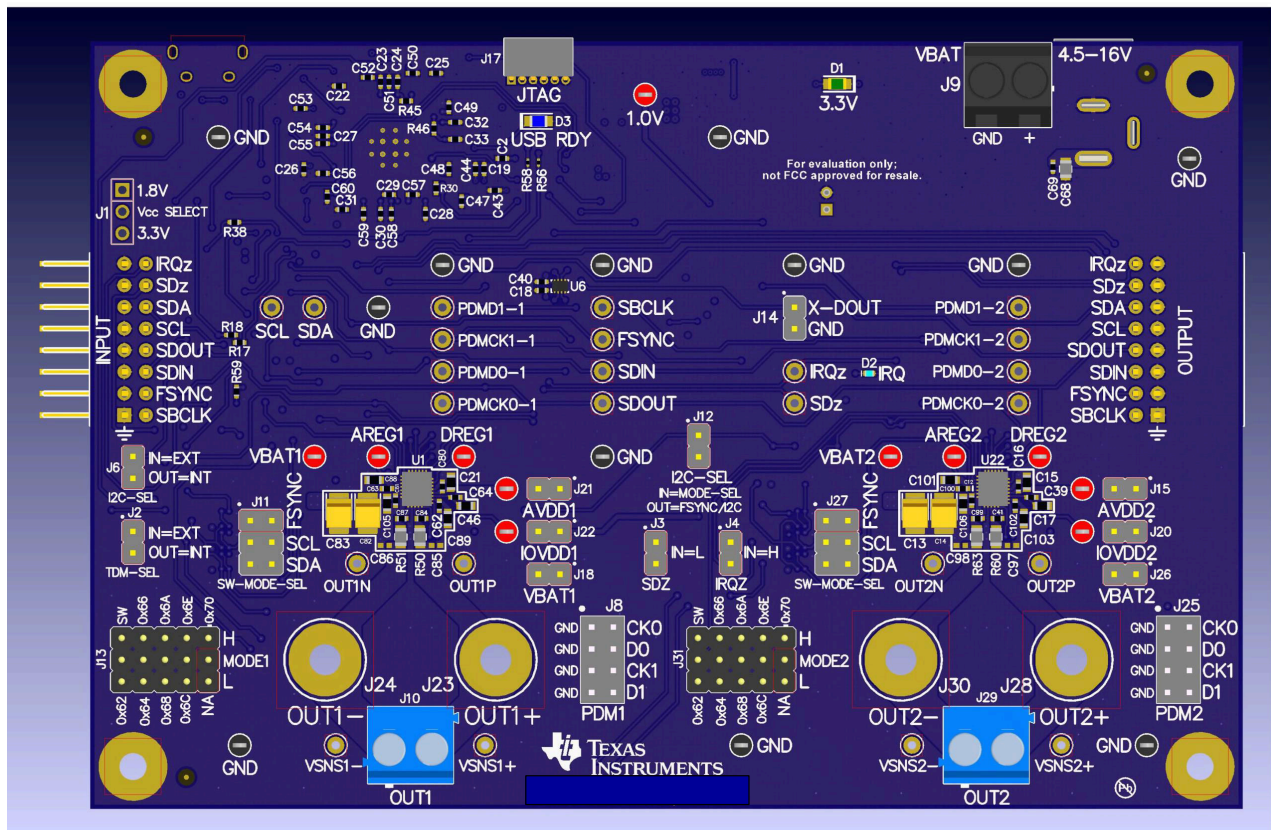


图 11-1. Stereo EVM Layout Diagram

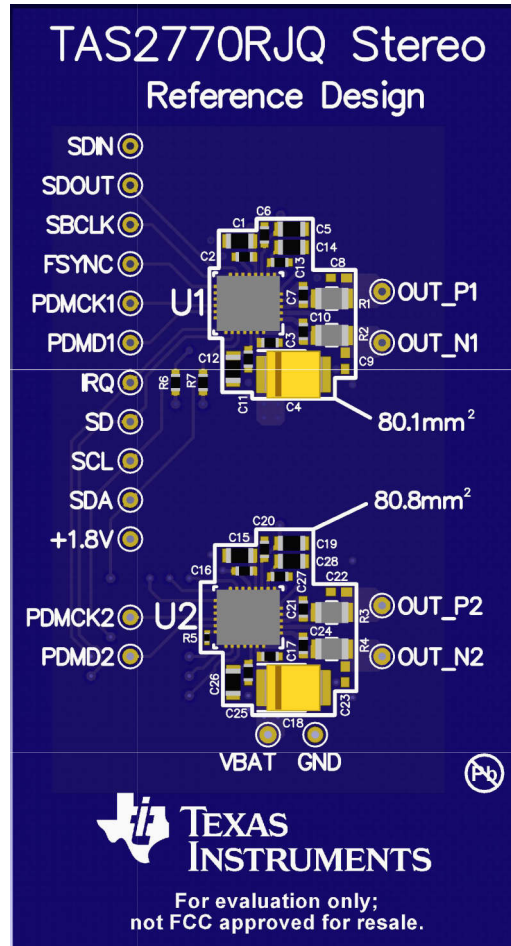


图 11-2. Stereo EVM Layout Reference Design - 01

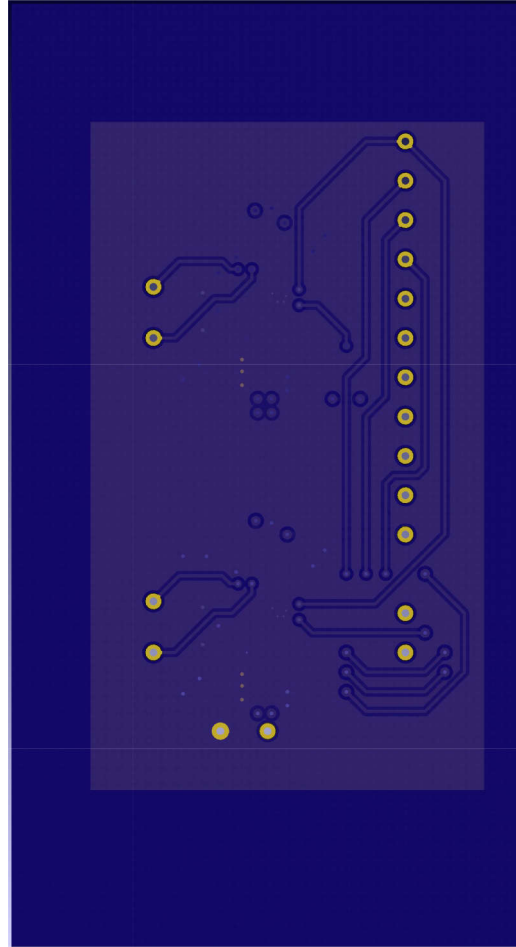


图 11-3. Stereo EVM Layout Reference Design - 02

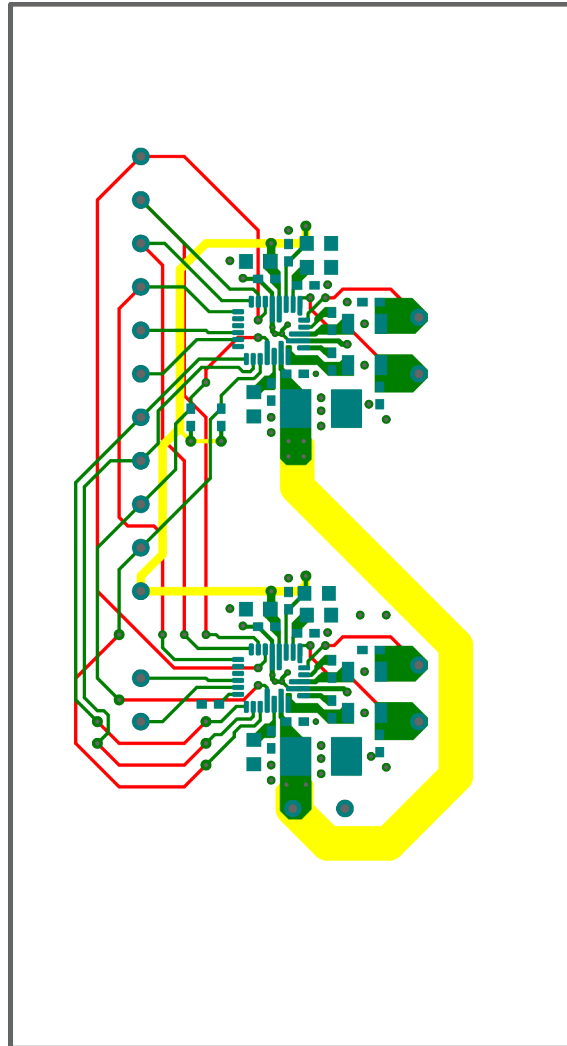


图 11-4. Layout Reference - TAS2770RJQ

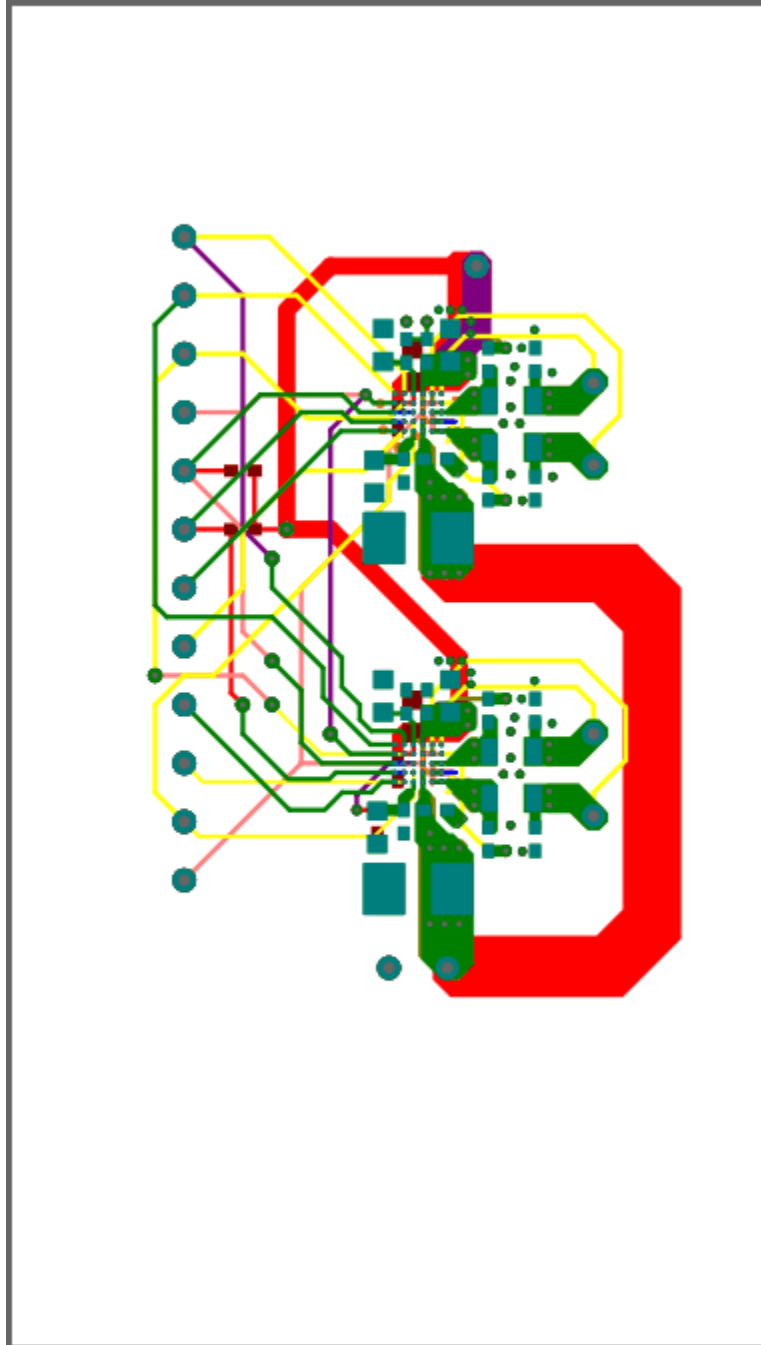


图 11-5. Layout Reference - TAS2770YFF

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Community Resources

12.3 Trademarks

所有商标均为其各自所有者的财产。

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| TAS2770RJQR | ACTIVE | VQFN-HR | RJQ | 26 | 3000 | RoHS & Green | Call TI NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | 2770 | Samples |
| TAS2770RJQT | ACTIVE | VQFN-HR | RJQ | 26 | 250 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | 2770 | Samples |
| TAS2770YFFR | ACTIVE | DSBGA | YFF | 30 | 3000 | RoHS & Green | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | 2770 | Samples |
| TAS2770YFFT | ACTIVE | DSBGA | YFF | 30 | 250 | RoHS & Green | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | 2770 | Samples |
| TAS5770LC0YFFR | ACTIVE | DSBGA | YFF | 30 | 3000 | RoHS & Green | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | TAS5770LC0 | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TAS2770RJQR | VQFN-HR | RJQ | 26 | 3000 | 330.0 | 12.4 | 3.8 | 4.3 | 1.5 | 8.0 | 12.0 | Q2 |
| TAS2770RJQT | VQFN-HR | RJQ | 26 | 250 | 180.0 | 12.4 | 3.8 | 4.3 | 1.5 | 8.0 | 12.0 | Q2 |
| TAS2770YFFR | DSBGA | YFF | 30 | 3000 | 180.0 | 8.4 | 2.13 | 2.66 | 0.69 | 4.0 | 8.0 | Q1 |
| TAS2770YFFT | DSBGA | YFF | 30 | 250 | 180.0 | 8.4 | 2.13 | 2.66 | 0.69 | 4.0 | 8.0 | Q1 |
| TAS5770LC0YFFR | DSBGA | YFF | 30 | 3000 | 180.0 | 8.4 | 2.13 | 2.66 | 0.69 | 4.0 | 8.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



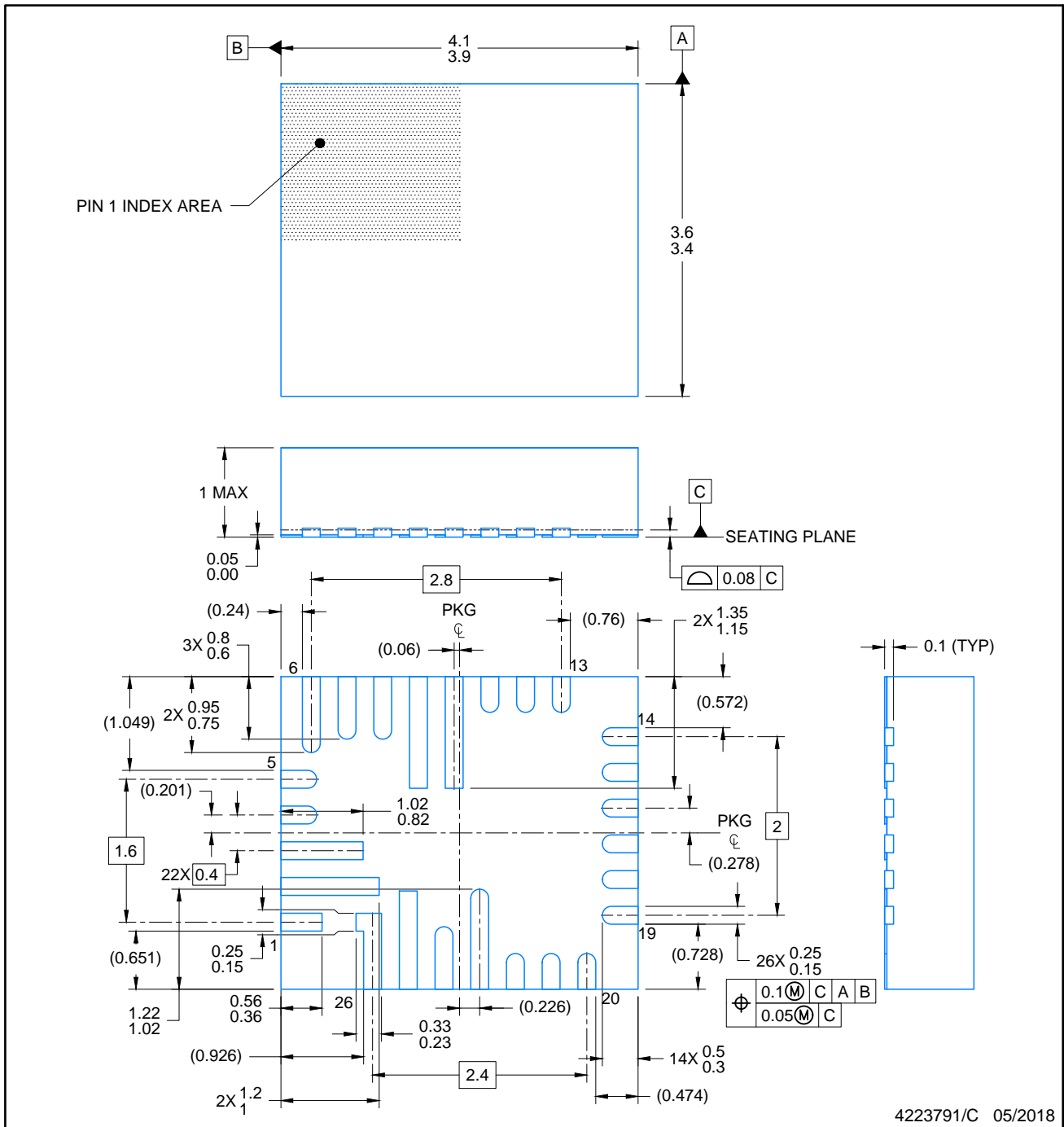
*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TAS2770RJQR | VQFN-HR | RJQ | 26 | 3000 | 346.0 | 346.0 | 33.0 |
| TAS2770RJQT | VQFN-HR | RJQ | 26 | 250 | 210.0 | 185.0 | 35.0 |
| TAS2770YFFR | DSBGA | YFF | 30 | 3000 | 182.0 | 182.0 | 20.0 |
| TAS2770YFFT | DSBGA | YFF | 30 | 250 | 182.0 | 182.0 | 20.0 |
| TAS5770LC0YFFR | DSBGA | YFF | 30 | 3000 | 182.0 | 182.0 | 20.0 |

RJQ0026A

PACKAGE OUTLINE VQFN-HR - 1 mm max height

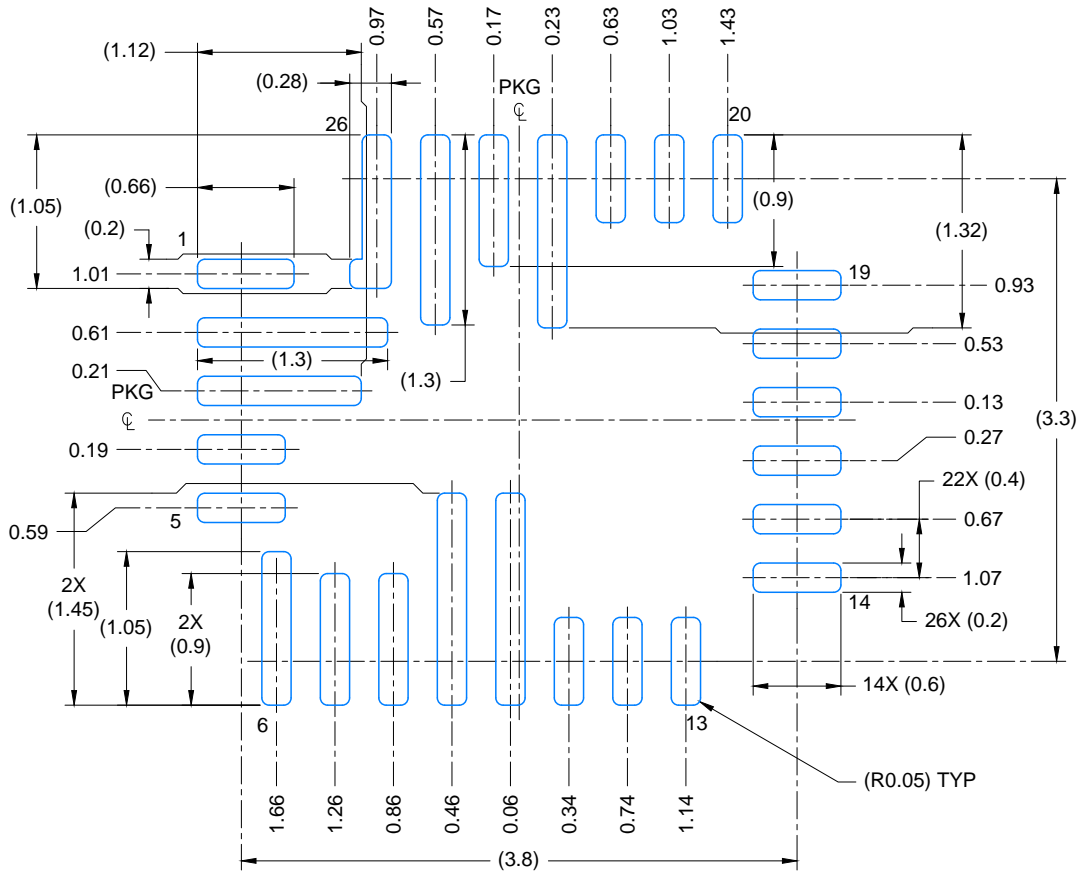
PLASTIC QUAD FLATPACK- NO LEAD



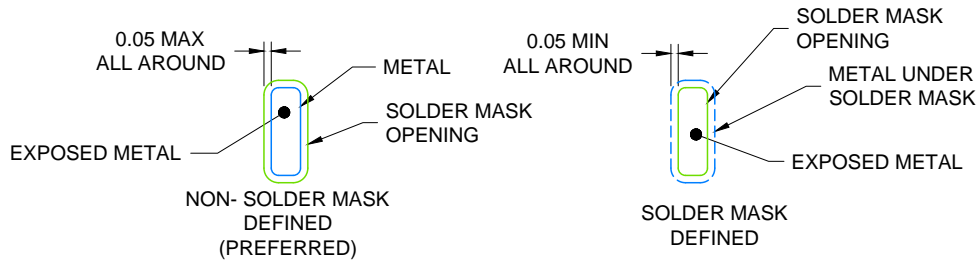
4223791/C 05/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

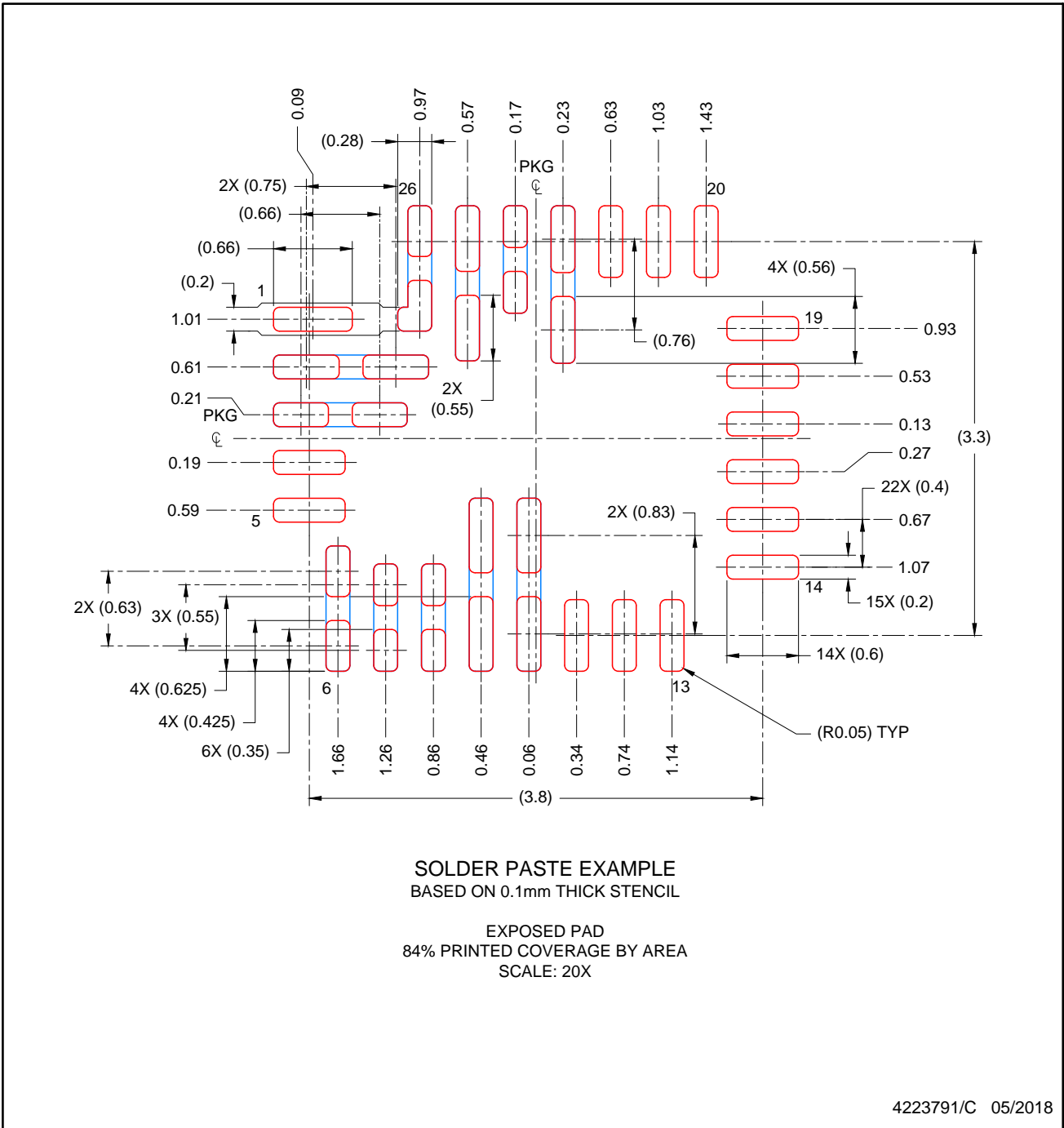


SOLDER MASK DETAILS

4223791/C 05/2018

NOTES: (continued)

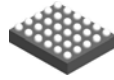
3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271) .
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

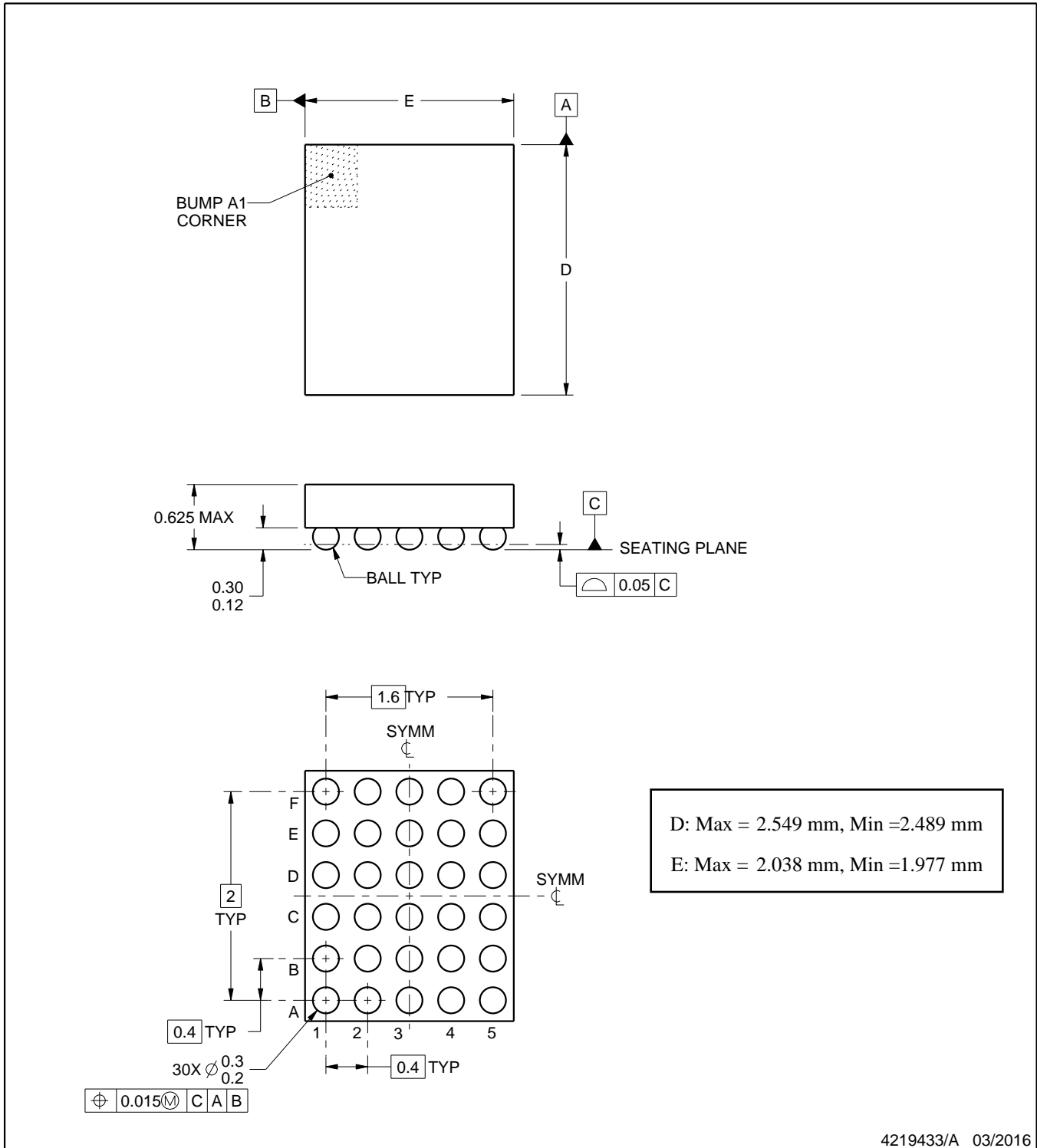
YFF0030



PACKAGE OUTLINE

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

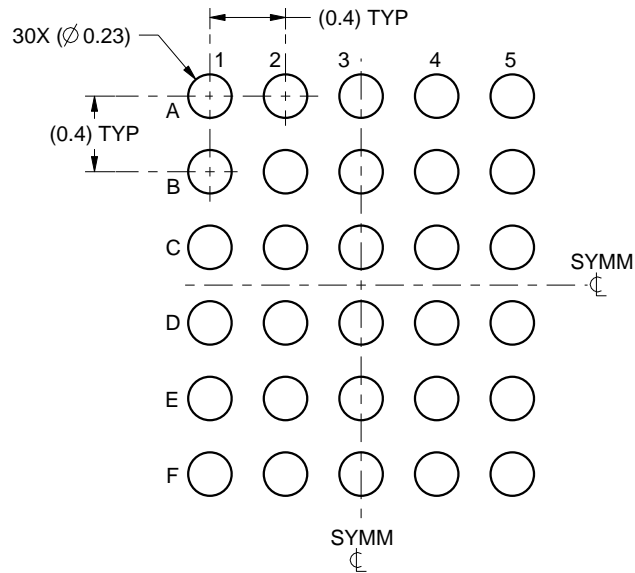
- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.

EXAMPLE BOARD LAYOUT

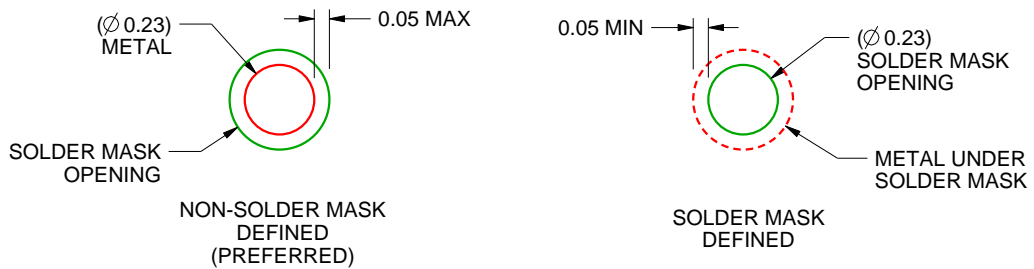
YFF0030

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:25X



SOLDER MASK DETAILS
NOT TO SCALE

4219433/A 03/2016

NOTES: (continued)

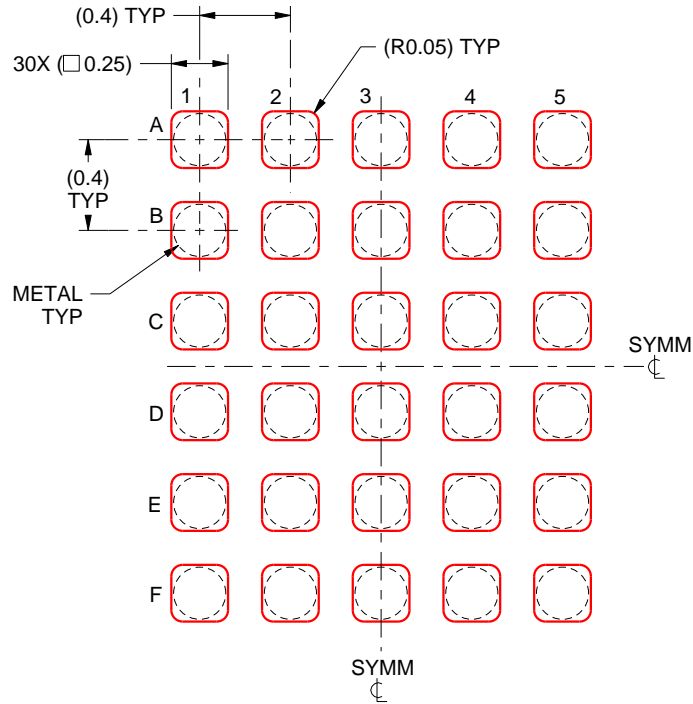
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

YFF0030

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4219433/A 03/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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