四通道汽车数字 放大器

查询样品: TAS5514B-Q1

特性

- 单端输入
- 四通道数字功率 放大器
- **4** 个模拟输入，**4** 个平衡桥路功放电路 **(BTL)** 功率输出
- 在 **10%** 总谐波失真 **(THD) + N** 上的典型输出功率
  - **14.4V** 上，每通道 **28W** 进入 **4 Ω** 负载
  - **14.4V** 上，每通道 **50W** 进入 **2Ω** 负载
  - **24V** 上，每通道 **79W** 进入 **4Ω** 负载
  - **24V**上，每通道 **150W** 进入 **2Ω** 负载 **(PBTL)**
- 针对高电流 应用，通道可被并行 **(PBTL)**
- **THD+N<0.02%**，**1kHz**，**1W** 进入 **4Ω** 负载
- 已获专利的弹出和点击衰减技术
  - 具有增益斜波控制的软静音
  - 共模 斜波修整
- 已获专利的 **AM** 干扰避免
- 已获专利的逐周期电流限制
- **75dB** 电源抑制比 **(PSRR)**
- 同步时钟的主器件/从器件性能
- 负载 诊断功能：
  - 输出打开和短接 负载
  - 输出到电源和输出到接地短接
- 保护和监控 功能：
  - 短路保护功能
  - 负载突降保护 达 **50V**
  - 偶然开放式接地和电源容错
  - 已获专利的在音乐 播放的同时进行输出 **DC** 电平侦测
  - 过热保护
  - 过压和欠压 条件
  - 芯片检测器
- 带有散热 块的 **36** 引脚塑料小型封装 **(PSOP)3 (DKD)** 功率小外形 **(SOP)** 封装
- 设计用于汽车电磁兼容性 **(EMC)** 要求
- 符合 **AEC-Q100** 标准
- 经 **ISO9000：2002 TS16949** 认证
- **-40°C** 至 **105°C** 环境温度范围

应用范围

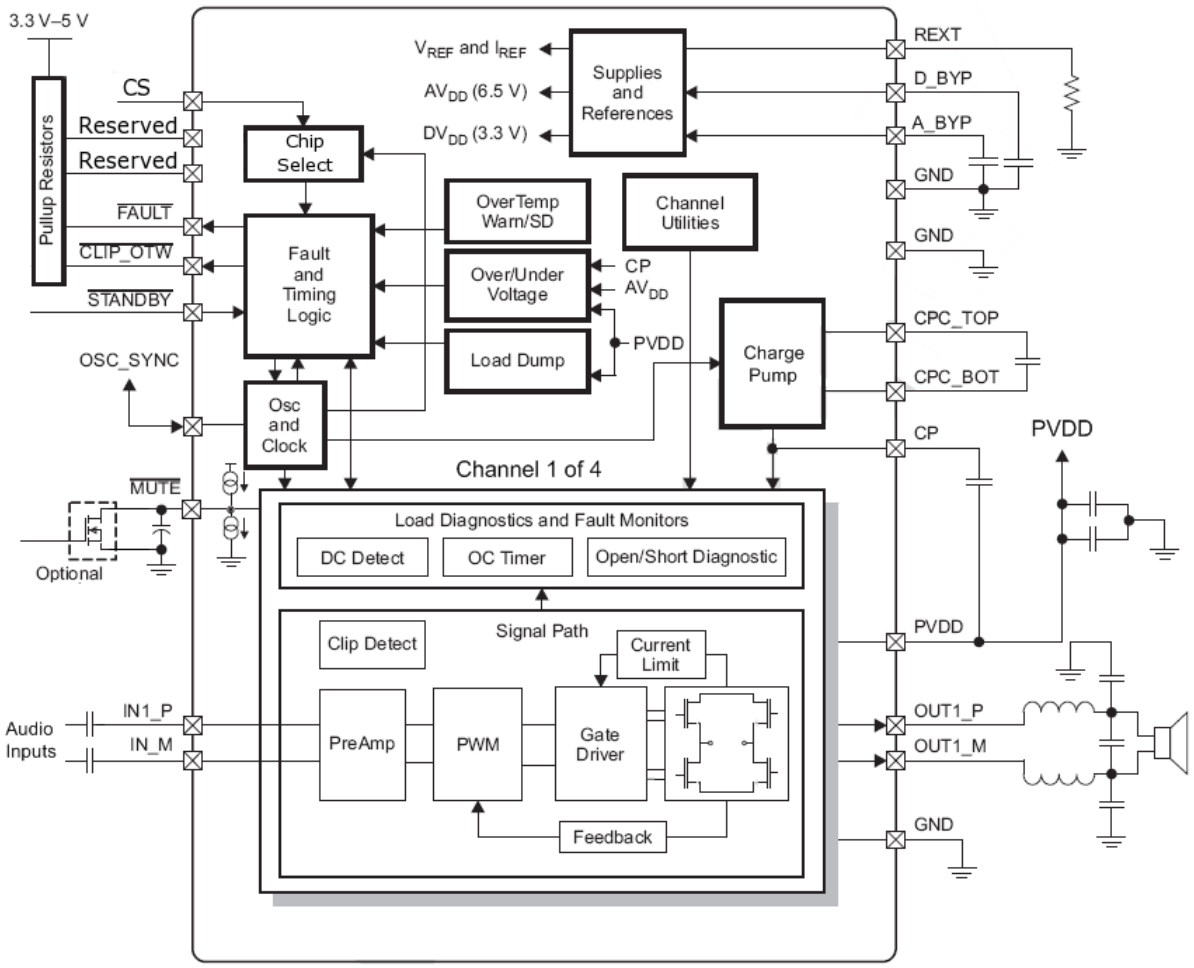
原设备生产商 **(OEM) /** 零售音响本体和放大器模块，在这些器件中特性密度和系统 配置要求减少来自音频功率放大器的热量

说明

TAS5514B-Q1 是设计用于汽车 音响本体和外部放大器模块的 4 声道数字音频放大器。 在由 14.4V 电源供电时，它在少于 1% THD+N 下在 4 个通道上持续提供进入 4Ω 负载的 23W 功率。 每个通道还能够为 1% THD+N 上 2Ω 负载传送 38W 的功率。 此器件的数字脉宽调制 (PWM) 拓扑大大提升了 传统线性放大器解决方案的效率。 这将典型音乐回放条件下放大器的功率耗散减少了 因数 10。 此器件包含要求严格的 OEM 应用领域中运转所需的所有 功能性。 TAS5514B-Q1 有 内置的负载诊断功能用来侦测和诊断错误连接的输出以帮助 减少制造过程中的测试时间。

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

FUNCTIONAL BLOCK DIAGRAM



PIN ASSIGNMENTS AND FUNCTIONS

The pin assignments are shown as follows.

TAS5514B
DKD Package
(Top View)

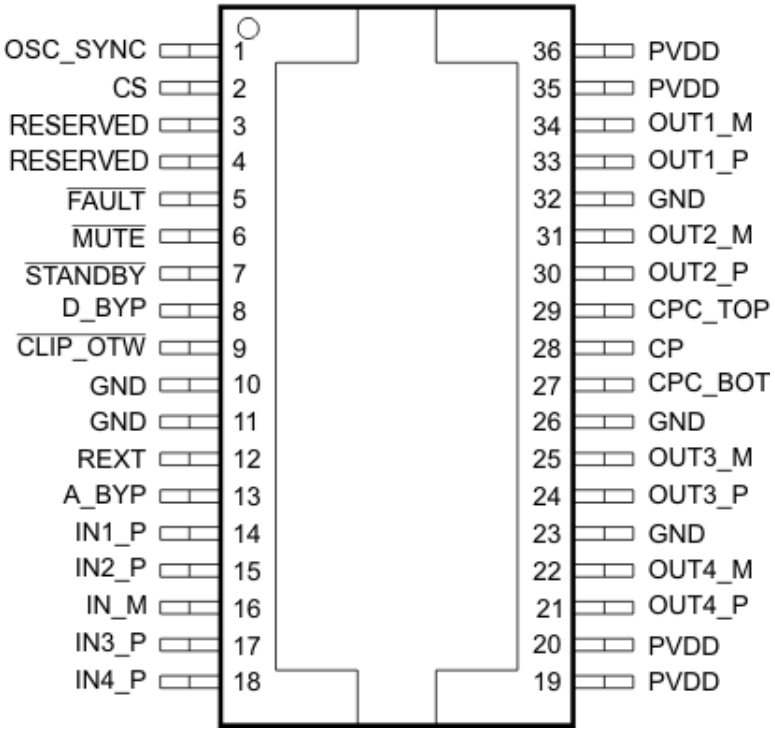


Table 1. PIN FUNCTIONS

PIN		TYPE	DESCRIPTION
NAME	DKD PACKAGE TAS5514B-Q1 NO.		
A_BYP	13	PBY	Bypass pin for the AVDD analog regulator
$\overline{\text{CLIP\_OTW}}$	9	DO	Reports CLIP, OTW, or both. It also reports tweeter detection during tweeter mode. Open-drain
CP	28	CP	Top of main storage capacitor for charge pump (bottom goes to PVDD)
CPC_BOT	27	CP	Bottom of flying capacitor for charge pump
CPC_TOP	29	CP	Top of flying capacitor for charge pump
D_BYP	8	PBY	Bypass pin for DVDD regulator output
$\overline{\text{FAULT}}$	5	DO	Global fault output (open-drain): UV, OV, OTSD, OCSD, DC
GND	10, 11, 23, 26, 32	GND	Ground
CS	2	AI	Chip select
IN1_P	14	AI	Non-inverting analog input for channel 1
IN2_P	15	AI	Non-inverting analog input for channel 2
IN3_P	17	AI	Non-inverting analog input for channel 3
IN4_P	18	AI	Non-inverting analog input for channel 4
IN_M	16	ARTN	Signal return for the four analog channel inputs
$\overline{\text{MUTE}}$	6	AI	Gain ramp control: mute (low), play (high)
OSC_SYNC	1	DI/DO	Oscillator input from master or output to slave amplifiers
OUT1_M	34	PO	– polarity output for bridge 1
OUT1_P	33	PO	+ polarity output for bridge 1
OUT2_M	31	PO	– polarity output for bridge 2
OUT2_P	30	PO	+ polarity output for bridge 2
OUT3_M	25	PO	– polarity output for bridge 3
OUT3_P	24	PO	+ polarity output for bridge 3
OUT4_M	22	PO	– polarity output for bridge 4
OUT4_P	21	PO	+ polarity output for bridge 4
PVDD	19, 20, 35, 36	PWR	PVDD supply
REXT	12	AI	Precision resistor pin to set analog reference
RESERVED	3, 4		
$\overline{\text{STANDBY}}$	7	DI	Active-low STANDBY pin. Standby (low), power up (high)

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

			VALUE	UNIT
PVDD	DC supply-voltage range	Relative to GND	–0.3 to 30	V
$PVDD_{MAX}$	Pulsed supply-voltage range	t ≤ 100 ms exposure	–1 to 50	V
$PVDD_{RAMP}$	Supply-voltage ramp rate		15	V/ms
I_{PVDD}	Externally imposed dc supply current per PVDD or GND pin		±12	A
I_{PVDD_MAX}	Pulsed supply current per PVDD pin (one shot)	t < 100 ms	17	A
I_O	Maximum allowed dc current per output pin		±13.5	A
I_{O_MAX} (1)	Pulsed output current per output pin (single pulse)	t < 100 ms	±17	A
I_{IN_MAX}	Maximum current, all digital and analog input pins(2)	DC or pulsed	±1	mA
I_{MUTE_MAX}	Maximum current on $\overline{\text{MUTE}}$ pin	DC or pulsed	±20	mA
I_{IN_ODMAX}	Maximum sink current for open-drain pins		7	mA
V_{LOGIC}	Input voltage range for pin relative to GND (SCL, SDA, CS pins)	Supply voltage range: 6V < PVDD < 24 V	–0.3 to 6	V
V_{MUTE}	Voltage range for $\overline{\text{MUTE}}$ pin relative to GND	Supply voltage range: 6 V < PVDD < 24 V	–0.3 to 7.5	V
$V_{STANDBY}$	Input voltage range for $\overline{\text{STANDBY}}$ pin	Supply voltage range: 6 V < PVDD < 24 V	–0.3 to 5.5	V
V_{OSC_SYNC}	Input voltage range for OSC_SYNC pin relative to GND	Supply voltage range: 6 V < PVDD < 24 V	–0.3 to 3.6	V
V_{GND}	Maximum voltage between GND pins		±0.3	V
$V_{AIN\_AC\_MAX\_5514}$	Maximum ac-coupled input voltage for TAS5514B-Q1(2), analog input pins	Supply voltage range: 6 V < PVDD < 24 V	1.9	Vrms
T_J	Maximum operating junction temperature range		–55 to 150	°C
T_{stg}	Storage temperature range		–55 to 150	°C

(1) Pulsed current ratings are maximum survivable currents externally applied to the device. High currents may be encountered during reverse battery, fortuitous open-ground, and fortuitous open-supply fault conditions.
(2) See *Application Information* section for information on analog input voltage and ac coupling.

THERMAL CHARACTERISTICS

PARAMETER		VALUE (Typical)	UNIT
$R_{\theta JC}$	Junction-to-case (heat slug) thermal resistance, DKD package	1	°C/W
$R_{\theta JC}$	Junction-to-case (heat slug) thermal resistance, PHD package	1.2	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	This device is not intended to be used without a heatsink. Therefore, $R_{\theta JA}$ is not specified. See the *Thermal Information* section.	
	Exposed pad dimensions, DKD package	13.8 × 5.8	mm

ELECTROSTATIC DISCHARGE (ESD)

PARAMETER	Package	Pins	VALUE (Typical)	UNIT
Human-body model (HBM) AEC-Q100-002	All	All	3000	V
Charged-device model (CDM) AEC-Q100-011	DKD/DKE	Corner pins excluding OSC_SYNC	1000	
		All other pins (including OSC_SYNC) except CP pin	500	
		CP pin (non-corner Pin)	400	
	PHD	Corner pins excluding SCL	750	
		All pins (including SCL) except CP and CP_TOP	600	
		CP and CP_TOP pins	400	
Machine model (MM) AEC-Q100-003	DKD/DKE		150	
	PHD		100	

RECOMMENDED OPERATING CONDITIONS(1)

			MIN	TYP	MAX	UNIT
$PVDD_{OP}$	DC supply-voltage range relative to GND		6	14.4	24	V
V_{AIN_5514} (2)	Analog audio input signal level (TAS5514B-Q1)	AC-coupled input voltage	0		0.25–1(3)	Vrms
T_A	Ambient temperature		–40		105	°C
T_J	Junction temperature	An adequate heat sink is required to keep T_J within the specified range.	–40		115	°C
R_L	Nominal speaker load impedance		2	4		Ω
V_{PU}	Pullup voltage supply (for open-drain logic outputs)		3	3.3 or 5	5.5	V
R_{PU_I2C}	I^2C pullup resistance on SDA and SCL pins		1	4.7	10	kΩ
R_{CS}	Total resistance of voltage divider for I^2C address slave 1 or slave 2, connected between D_BYP and GND pins		10		50	kΩ
R_{REXT}	External resistance on REXT pin	1% tolerance required	19.8	20	20.2	kΩ
C_{D_BYP} , C_{A_BYP}	External capacitance on D_BYP and A_BYP pins		10		120	nF
C_{OUT}	External capacitance to GND on OUT_X pins			150	680	nF
C_{IN}	External capacitance to analog input pin in series with input signal			0.47		µF
C_{FLY}	Flying capacitor on charge pump		0.47	1	1.5	µF
C_P	Charge pump capacitor	50 V needed for load dump	0.47	1	1.5	µF
C_{MUTE}	$\overline{MUTE}$ pin capacitor		100	220	1000	nF
$C_{OSCSYNC\_MAX}$	Allowed loading capacitance on OSC_SYNC pin			75		pF

(1) The *Recommended Operating Conditions* table specifies only that the device is functional in the given range. See the *Electrical Characteristics* table for specified performance limits.
(2) Signal input for full unclipped output with gains of 32 dB, 26 dB, 20 dB, and 12 dB
(3) Maximum recommended input voltage is determined by the gain setting.

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise noted): T_{Case} = 25°C, PVDD = 14.4 V, R_L = 4 Ω, f_S = 417 kHz, P_{out} = 1 W/ch, Rext = 20 kΩ, AES17 Filter, default I^2C settings, master mode operation (see application diagram)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OPERATING CURRENT						
I_{PVDD_IDLE}	PVDD idle current	All four channels in MUTE mode		170	220	mA
I_{PVDD_Hi-Z}		All four channels in Hi-Z mode		93		
I_{PVDD_STBY}	PVDD standby current	STANDBY mode, $T_J \le 85°C$		2	10	µA
OUTPUT POWER						
P_{OUT}	Output power per channel	4 Ω, PVDD = 14.4 V, THD+N ≤ 1%, 1 kHz, T_c = 75°C		23		W
		4 Ω, PVDD = 14.4 V, THD+N = 10%, 1 kHz, T_c = 75°C	25	28		
		4 Ω, PVDD = 24 V, THD+N = 10%, 1 kHz, T_c = 75°C	63	79		
		2 Ω, PVDD = 14.4 V, THD+N = 1%, 1 kHz, T_c = 75°C		38		
		2 Ω, PVDD = 14.4 V, THD+N = 10%, 1 kHz, T_c = 75°C	40	50		
		PBTL 2-Ω operation, PVDD = 24 V, THD+N = 10%, 1 kHz, T_c = 75°C		150		
		PBTL 1-Ω operation, PVDD = 14.4 V, THD+N = 10%, 1 kHz, T_c = 75°C		90		
EFF_P	Power efficiency	4 channels operating, 23-W output power/ch, L = 10 µH, $T_J \le 85°C$		90%		
AUDIO PERFORMANCE						
V_{NOISE}	Noise voltage at output	Zero input, and A-weighting		60	100	µV
Crosstalk	Channel crosstalk	P = 1W, f = 1 kHz, enhanced crosstalk enabled via I^2C (reg 0x10)	70	85		dB
PSRR	Power-supply rejection ratio	PVDD = 14.4 Vdc + 1 Vrms, f = 1 kHz	60	75		dB
THD+N	Total harmonic distortion + noise	P = 1W, f = 1 kHz		0.02%	0.1%	
f_S	Switching frequency	Switching frequency selectable for AM interference avoidance	336	357	378	kHz
			392	417	442	
			470	500	530	
R_{AIN}	Analog input resistance	Internal shunt resistance on each input pin	63	85	106	kΩ
V_{IN_CM}	Common-mode input voltage	AC-coupled common-mode input voltage (zero differential input)		1.3		Vrms
V_{CM_INT}	Internal common-mode input bias voltage	Internal bias applied to IN_M pin		3.3		V
G	Voltage gain (V_O/V_{IN})	Source impedance = 0 Ω, gain measurement taken at 1 W of power per channel	11	12	13	dB
			19	20	21	
			25	26	27	
			31	32	33	
G_{CH}	Channel-to-channel variation	Any gain commanded	–1	0	1	dB
PWM OUTPUT STAGE						
R_{DSon}	FET drain-to-source resistance	Not including bond wire resistance, T_J = 25°C		65	90	mΩ
V_{O_OFFSET}	Output offset voltage	Zero input signal, G = 26 dB		±10	±50	mV
PVDD OVERVOLTAGE (OV) PROTECTION						
V_{OV_SET}	PVDD overvoltage shutdown set		24.6	26.4	28.2	V
V_{OV_CLEAR}	PVDD overvoltage shutdown clear		24.4	25.9	27.4	
PVDD UNDERVOLTAGE (UV) PROTECTION						
V_{UV_SET}	PVDD undervoltage shutdown set		4.9	5.3	5.6	V
V_{UV_CLEAR}	PVDD undervoltage shutdown clear		6.2	6.6	7.0	V
AVDD						
V_{A_BYP}	A_BYP pin voltage			6.5		V
$V_{A\_BYP\_UV\_SET}$	A_BYP UV voltage			4.8		V
$V_{A\_BYP\_UV\_CLEAR}$	Recovery voltage A_BYP UV			5.3		V
DVDD						
V_{D_BYP}	D_BYP pin voltage			3.3		V

ELECTRICAL CHARACTERISTICS (continued)

Test conditions (unless otherwise noted): T_{Case} = 25°C, PVDD = 14.4 V, R_L = 4 Ω, f_S = 417 kHz, P_{out} = 1 W/ch, Rext = 20 kΩ, AES17 Filter, default I^2C settings, master mode operation (see application diagram)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER-ON RESET (POR)						
V_{POR}	PVDD voltage for POR	State machine active above this voltage			3.5	V
V_{POR_HY}	PVDD recovery hysteresis voltage for POR			0.1		V
REXT						
V_{REXT}	Rext pin voltage			1.27		V
CHARGE PUMP (CP)						
V_{CPUV_SET}	CP undervoltage			4.8		V
V_{CPUV_CLEAR}	Recovery voltage for CP UV			4.9		V
OVERTEMPERATURE (OT) PROTECTION						
T_{OTW_CLEAR}	Junction temperature for overtemperature warning		96	112	128	°C
T_{OTW_SET}			106	122	138	°C
T_{OTSD_CLEAR}	Junction temperature for overtemperature shutdown		126	142	158	°C
T_{OTSD}			136	152	168	°C
T_{FB}	Junction temperature for overtemperature foldback	Per channel	130	150	170	°C
CURRENT LIMITING PROTECTION						
I_{LIM}	Current limit (load current)	Level 1	5.5	7.3	9	A
		Level 2 (default)	10.6	12.7	15	
OVERCURRENT (OC) SHUTDOWN PROTECTION						
I_{MAX}	Maximum current (peak output current)	Level 2 (default), Any short to supply, ground, or other channels	11.9	14.8	17.7	A
STANDBY MODE						
V_{IH_STBY}	$\overline{\text{STANDBY}}$ input voltage for logic-level high		2			V
V_{IL_STBY}	$\overline{\text{STANDBY}}$ input voltage for logic-level low				0.7	V
I_{STBY_PIN}	$\overline{\text{STANDBY}}$ pin current			0.1	0.2	µA
MUTE MODE						
G_{MUTE}	Output attenuation	$\overline{\text{MUTE}}$ pin ≤ 0.5 V + 200mS		100		dB
DC DETECT						
$V_{TH\_DC\_TOL}$	DC detect threshold tolerance			25		%
t_{DCD}	DC detect step response time for four channels				5.3	s
CLIP_OTW REPORT						
$V_{OH\_CLIPOTW}$	$\overline{\text{CLIP\_OTW}}$ pin output voltage for logic level high (open-drain logic output)	External 47-kΩ pullup resistor to 3 V–5.5 V	2.4			V
$V_{OL\_CLIPOTW}$	$\overline{\text{CLIP\_OTW}}$ pin output voltage for logic level low (open-drain logic output)				0.5	V
$t_{DELAY\_CLIPDET}$	$\overline{\text{CLIP\_OTW}}$ signal delay when output clipping detected				20	µs
FAULT REPORT						
V_{OH_FAULT}	$\overline{\text{FAULT}}$ pin output voltage for logic-level high (open-drain logic output)	External 47-kΩ pullup resistor to 3 V–5.5 V	2.4			V
V_{OL_FAULT}	$\overline{\text{FAULT}}$ pin output voltage for logic-level low (open-drain logic output)				0.5	
OPEN/SHORT DIAGNOSTICS						
R_{S2P}, R_{S2G}	Maximum resistance to detect a short from OUT pin(s) to PVDD or ground				200	Ω
R_{OPEN_LOAD}	Minimum load resistance to detect open circuit	Including speaker wires	300	740	1300	Ω
$R_{SHORTED\_LOAD}$	Maximum load resistance to detect short circuit	Including speaker wires	0.5	1	1.5	Ω

ELECTRICAL CHARACTERISTICS (continued)

Test conditions (unless otherwise noted): T_{Case} = 25°C, PVDD = 14.4 V, R_L = 4 Ω, f_S = 417 kHz, P_{out} = 1 W/ch, Rext = 20 kΩ, AES17 Filter, default I^2C settings, master mode operation (see application diagram)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Chip Select DECODER						
t_{LATCH_CS}	Time delay to latch CS after POR			300		µs
V_{CS}	Voltage on CS pin for address 0	Connect to GND	0%	0%	15%	V_{D_BYP}
	Voltage on CS pin for address 1	External resistors in series between D_BYP and GND as a voltage divider	25%	35%	45%	
	Voltage on CS pin for address 2		55%	65%	75%	
	Voltage on CS pin for address 3	Connect to D_BYP	85%	100%	100%	
OSCILLATOR						
$V_{OH\_OSCSYNC}$	OSC_SYNC pin output voltage for logic-level high	CS pin set to MASTER mode	2.4			V
$V_{OL\_OSCSYNC}$	OSC_SYNC pin output voltage for logic-level low				0.5	V
$V_{IH\_OSCSYNC}$	OSC_SYNC pin input voltage for logic-level high	CS pin set to SLAVE mode	2			V
$V_{IL\_OSCSYNC}$	OSC_SYNC pin input voltage for logic-level low				0.8	V
f_{OSC_SYNC}	OSC_SYNC pin clock frequency	CS pin set to MASTER mode, f_S = 417 kHz	3.13	3.33	3.63	MHz

TYPICAL CHARACTERISTICS

THD+N
vs
BTL OUTPUT POWER at 1kHz

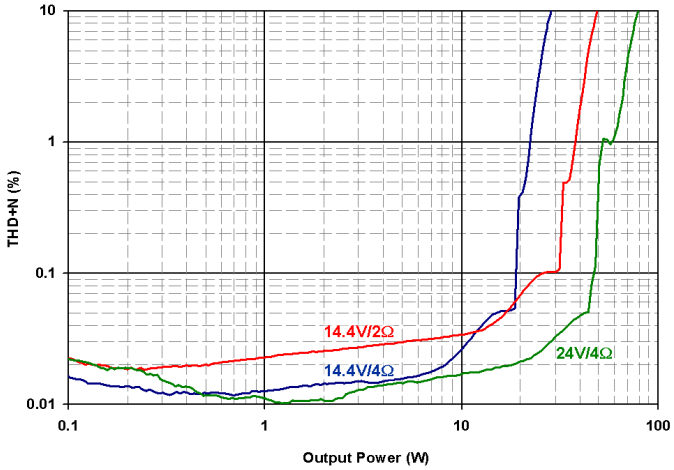


Figure 1.

THD+N
vs
PBTL OUTPUT POWER at 1kHz

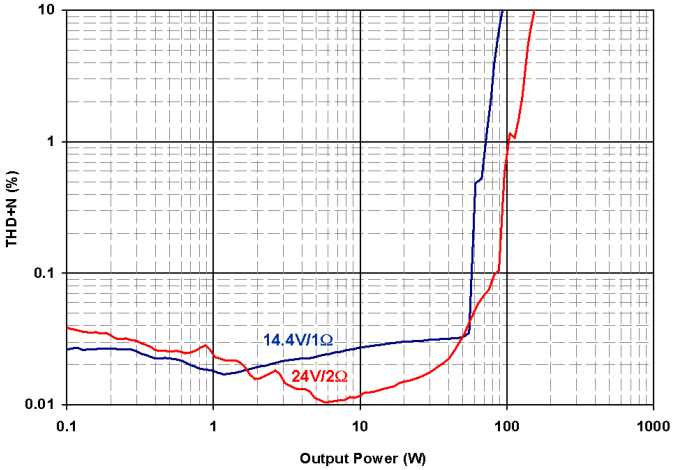


Figure 2.

THD+N
vs
FREQUENCY at 1 Watt

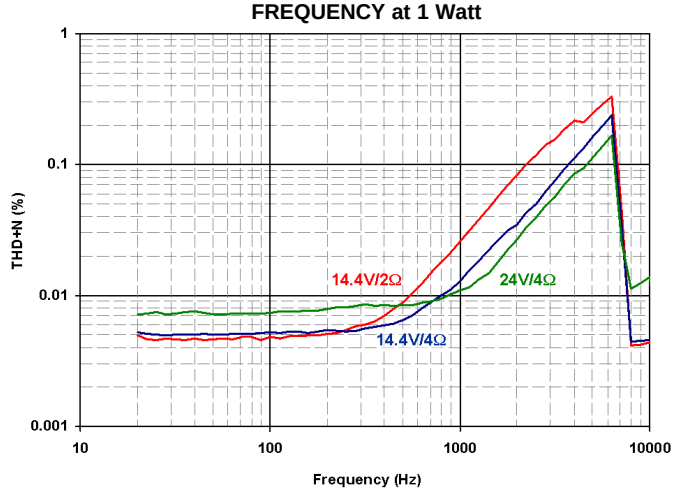


Figure 3.

TAS5524B-Q1
COMMON-MODE REJECTION RATIO
vs
FREQUENCY

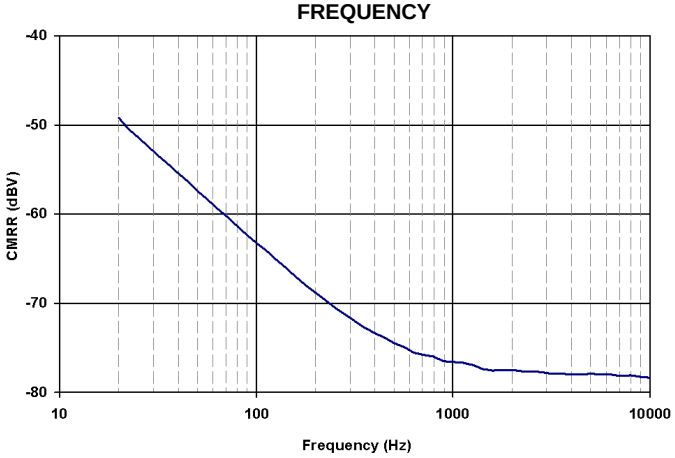


Figure 4.

TYPICAL CHARACTERISTICS (continued)

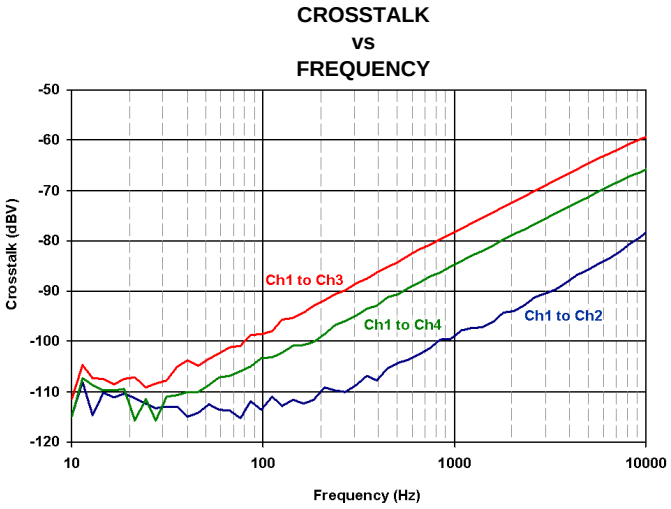


Figure 5.

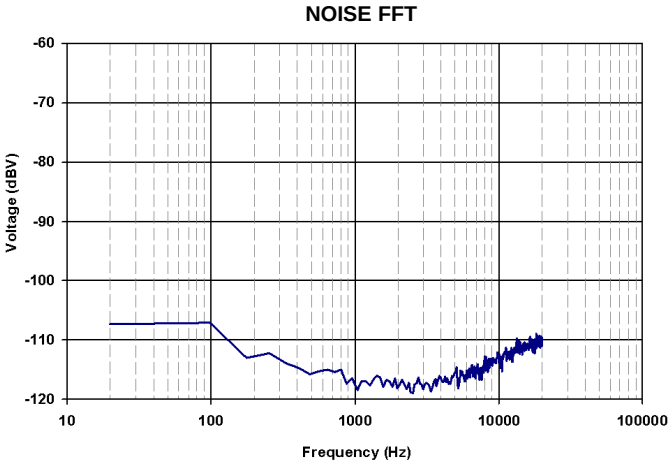


Figure 6.

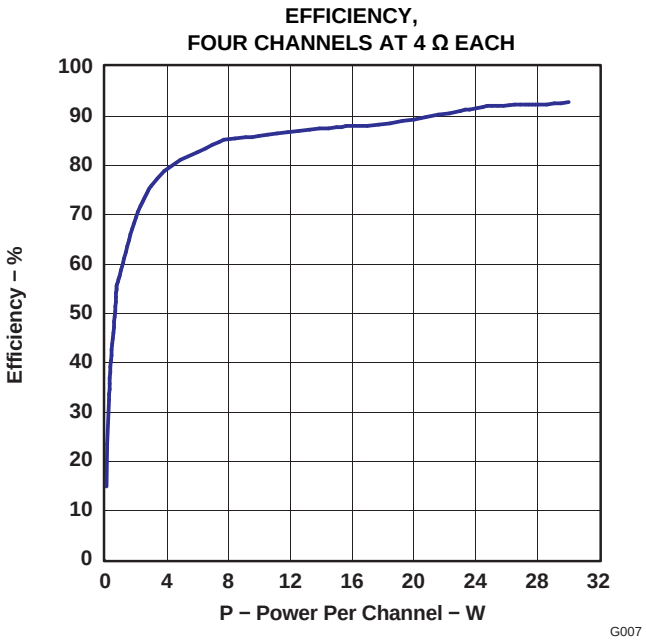


Figure 7.

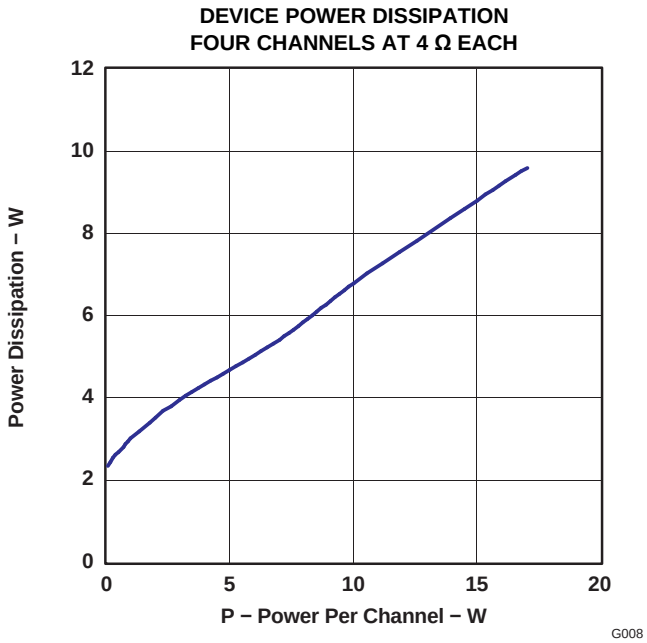


Figure 8.

DESCRIPTION OF OPERATION

OVERVIEW

The TAS5514B-Q1 is a single-chip, four-channel, analog-input audio amplifier for use in the automotive environment. The design uses an ultra-efficient class-D technology developed by Texas Instruments, but with changes needed by the automotive industry. This technology allows for reduced power consumption, reduced heat, and reduced peak currents in the electrical system. The device realizes an audio sound system design with smaller size and lower weight than traditional class-AB solutions.

There are eight core design blocks:

- Preamplifier
- PWM
- Gate drive
- Power FETs
- Diagnostics
- Protection
- Power supply
- State machine

Preamplifier

The preamplifier is a high-input-impedance, low-noise, low-offset-voltage input stage with adjustable gain. The high input impedance allows the use of low-cost input capacitors while still achieving extended low-frequency response. The preamplifier is powered by a dedicated, internally regulated supply, which gives it excellent noise immunity and channel separation. Also included in the preamplifier is **Mute Pop-and-Click Control**—The device ramps the gain gradually when a mute or play command is received. Another form of click and pop can be caused by the start or stopping of switching in a class-D amplifier. The TAS5514B-Q1 incorporates a patented method to reduce the pop energy during the switching startup and shutdown sequences. Fault conditions require rapid protection response by the TAS5514B-Q1, which do not have time to ramp the gain down in a pop-free manner. The device transitions into Hi-Z mode when an OV, UV, OC, OT, or dc fault is encountered.

Pulse-Width Modulator (PWM)

The PWM converts the analog signal from the preamplifier into a switched signal of varying duty cycle. This is the critical stage that defines the class-D architecture. In the TAS5514B-Q1, the modulator is an advanced design with high bandwidth, low noise, low distortion, excellent stability, and full 0–100% modulation capability. The patented PWM uses clipping recovery circuitry to eliminate the deep saturation characteristic of PWMs when the input signal exceeds the modulator waveform.

Gate Drive

The gate driver accepts the low-voltage PWM signal and level-shifts it to drive a high-current, full-bridge, power FET stage. The device uses proprietary techniques to optimize EMI and audio performance.

Power FETs

The BTL output for each channel comprises four rugged N-channel 30-V 65-mΩ FETs for high efficiency and maximum power transfer to the load. These FETs are designed to handle large voltage transients during load dump.

Load Diagnostics

The device incorporates load diagnostic circuitry designed to help pinpoint the nature of output misconnections or faulty loads. The TAS5514B-Q1 includes functions for detecting and determining the status of output connections. The following diagnostics are performed when the device transitions from standby to play mode.

- Short to GND
- Short to PVDD
- Short across load

- Open load

The presence of any of the short or open conditions does not allow the channel with the fault to transition to play mode. Only an open load is allowed to transition to play mode.

Output Short and Open Diagnostics—The device contains circuitry designed to detect shorts and open conditions on the outputs. There are four phases of test during load diagnostics and two levels of test. All four phases are tested on each channel, all four channels at the same time. The diagnostics are performed as shown in Figure 9. Figure 10 shows the impedance ranges for the open-load and shorted-load diagnostics. With the default value of the $\overline{\text{MUTE}}$ capacitor the S2G and S2P phase take approximately 20 ms each, the OL phase takes approximately 100 ms, and the SL phase takes approximately 230 ms.

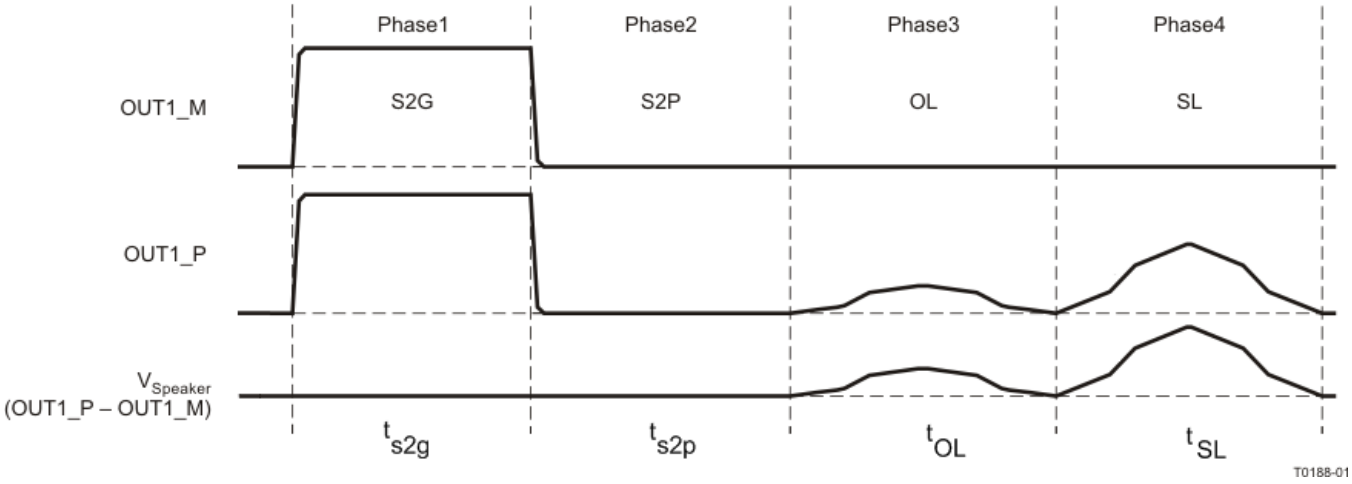


Figure 9. Load Diagnostics Sequence of Events

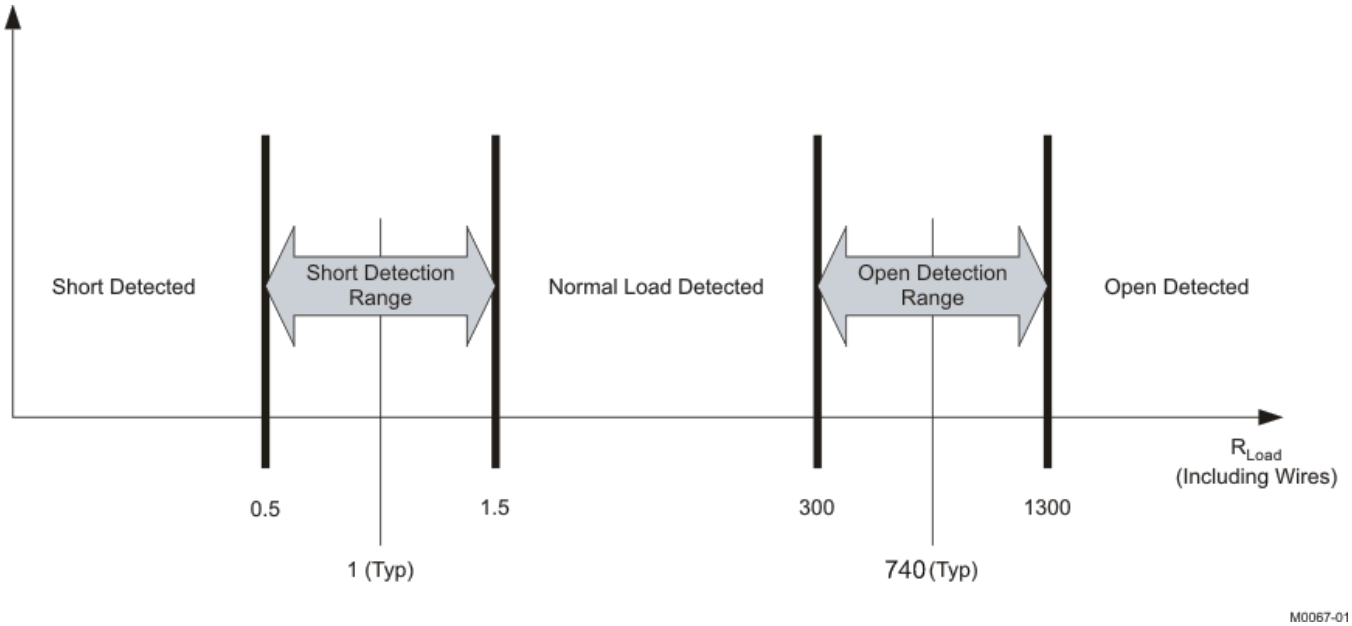


Figure 10. Open- and Shorted-Load Detection

Protection and Monitoring

- **Cycle-By-Cycle Current Limit (CBC)**—The CBC current-limiting circuit terminates each PWM pulse to limit the output current flow when the average current limit (I_{LIM}) threshold is exceeded. The overall effect on the audio in the case of a current overload is quite similar to a voltage-clipping event, where power is temporarily limited at the peaks of the musical signal and normal operation continues without disruption when the overload is removed. The TAS5514B-Q1 does not prematurely shut down in this condition. All four channels continue in play mode and pass signal.
- **Overcurrent Shutdown (OCSD)**—Under severe short-circuit events, such as a short to PVDD or ground, a peak-current detector is used, and the affected channel shuts down in 200 µs to 390 µs if the conditions are severe enough. The shutdown speed depends on a number of factors, such as the impedance of the short circuit, supply voltage, and switching frequency. Only the shorted channels are shut down in such a scenario. An OCSD event activates the fault pin, and the affected channel(s) are placed in Hi-Z mode. Normal operation is restored 1 second after the short is removed. If the supply or ground short is strong enough to exceed the peak current threshold but not severe enough to trigger the OCSD, the peak current limiter prevents excess current from damaging the output FETs, and operation returns to normal after the short is removed.
- **DC Detect**—This circuit detects a dc offset continuously during normal operation at the output of the amplifier. If the dc offset reaches the trip level for 1 second, the circuit triggers and latches off the output. The $\overline{\text{FAULT}}$ pin is asserted. The only method to recover is to cycle the device into standby mode and back to play mode. If the dc offset is still present, it latches off again after 1 second.
- **Clip Detect**—The clip detect circuit alerts the user to the presence of a 100% duty-cycle PWM due to a clipped waveform. When this occurs, a signal is passed to the $\overline{\text{CLIP\_OTW}}$ pin, and this pin is asserted until the 100% duty-cycle PWM signal is no longer present. All four channels are connected to the same $\overline{\text{CLIP\_OTW}}$ pin.
- **Overtemperature Warning (OTW), Overtemperature Shutdown (OTSD), and Thermal Foldback**—By default, the $\overline{\text{CLIP\_OTW}}$ pin is set to indicate an OTW. The $\overline{\text{CLIP\_OTW}}$ pin is asserted when the die temperature reaches the warning level as shown in the electrical characteristics. The device still functions until the temperature reaches the OTSD threshold, at which time the outputs are placed into Hi-Z mode and the $\overline{\text{FAULT}}$ pin is asserted. After the OTSD recovers at the OTSD clear value, the device automatically returns to play mode. The OTW is still indicated until the temperature drops below warning level value. The thermal foldback decreases the channel gain.
- **Undervoltage (UV) and Power-On-Reset (POR)**—The undervoltage (UV) protection detects low voltages on PVDD, AVDD, and CP. In the event of an undervoltage, the $\overline{\text{FAULT}}$ pin is asserted. Power-on-reset (POR) occurs when PVDD drops low enough. Recovery from a POR event is the same as a transition from standby to play mode.
- **Overvoltage (OV) and Load Dump**—The OV protection detects high voltages on PVDD. If PVDD reaches the overvoltage threshold, the $\overline{\text{FAULT}}$ pin is asserted. The device can withstand 50-V load-dump voltage spikes. Also depicted in this graph are the voltage thresholds for normal operation region, overvoltage operation region, and load-dump protection region. Figure 9 shows the regions of operating voltage and the profile of the load dump event.

Power Supply

The power for the device is most commonly provided by a car battery that can have a large voltage range. PVDD is a filtered battery voltage, and it is the supply for the output FETS and the low-side FET gate driver. The high-side FET gate driver is supplied by a charge pump (CP) supply. The charge pump supplies the gate-drive voltage for all four channels. The analog circuitry is powered by AVDD, which is provided by an internal linear regulator. A 0.1-µF/10V external bypass capacitor is needed at the A_BYP pin for this supply. It is recommended that no external components except the bypass capacitor be attached to this pin. The digital circuitry is powered by DVDD, which is provided by an internal linear regulator. A 0.1-µF/10V external bypass capacitor is needed at the D_BYP pin. It is recommended that no external components except the bypass capacitor and CS encoding resistors be attached to this pin.

The TAS5514B-Q1 can withstand fortuitous open-ground and power conditions. Fortuitous open ground usually occurs when a speaker wire is shorted to ground, allowing for a second ground path through the body diode in the output FETs. The diagnostic capability allows the speakers and speaker wires to be debugged, eliminating the need to remove the amplifier to diagnose the problem.

Oscillator Master/Slave Operation

The TAS5514B includes a single pin that allows for multiple devices to work together in a system with no additional hardware required for synchronization. The CS pin sets the device in master or slave mode. Connect the CS pin to GND for master mode, but no clock is on available on the OSC_SYNC pin. Connect the CS pin to 1.2 Vdc for a master mode with a clock on the OSC_SYNC pin, and to D_BYP for slave mode. In slave mode, the OSC_SYNC pin accepts a clock signal from a master device or external clock. The outputs cease to switch if an oscillator is not present on the OSC_SYNC pin while in slave mode.

Table 2. Table 7. CS Pin Connection

DESCRIPTION	CS PIN CONNECTION
TAS5514B-Q1 (master without clock)	To SGND pin
TAS5514B-Q1 (master with clock)	35% DVDD (resistive voltage divider between D_BYP pin and SGND pin)(1)
TAS5514B-Q1 (slave)	To D_BYP pin

(1) R_{CS} with 5% or better tolerance is recommended.

Hardware Control Pins

There are four discrete hardware pins for real-time control and indication of device status.

$\overline{\text{FAULT}}$ pin: This active-low open-drain output pin indicates the presence of a fault condition that requires the device to go into the Hi-Z mode or standby mode. When this pin is asserted, the device has protected itself and the system from potential damage. However, the fault is still indicated due to the fact that the $\overline{\text{FAULT}}$ pin is asserted. When the fault is removed, the device transitions from standby mode to play mode.

$\overline{\text{CLIP\_OTW}}$ pin: This active-low open-drain pin is configured to indicate both overtemperature warning and the detection of clipping.

$\overline{\text{MUTE}}$ pin: This active-low pin is used for hardware control of the mute/unmute function for all four channels. Capacitor C_{MUTE} is used to control the time constant for the gain ramp needed to produce a pop- and click-free mute function. The use of a hard mute with an external transistor does not ensure pop- and click-free operation, and is not recommended unless an *emergency hard mute* function is required. The C_{MUTE} capacitor may not be shared between multiple devices.

$\overline{\text{STANDBY}}$ pin: When this active-low pin is asserted, the device goes into a complete shutdown, and current draw is limited to 2 μA, typical. It can be used to shut down the device rapidly. If all channels are in Hi-Z, the device enters standby in approximately 1 ms, and if not, a quick rampdown occurs that takes approximately 20 ms. The outputs are ramped down quickly if not already in Hi-Z, so externally biasing the $\overline{\text{MUTE}}$ pin prevents the device from entering standby.

EMI Considerations

Automotive-level EMI performance depends on both careful integrated circuit design and good system-level design. Controlling sources of electromagnetic interference (EMI) was a major consideration in all aspects of the design.

The design has minimal parasitic inductances due to the short leads on the package. This dramatically reduces the EMI that results from current passing from the die to the system PCB. Each channel also operates at a different phase to reduce EMI caused by high-current switching. The design also incorporates circuitry that optimizes output transitions that cause EMI.

Operating Modes and Faults

The operating modes and faults are depicted in the following tables.

Table 3. Operating Modes

STATE NAME	OUTPUT FETS	CHARGE PUMP	OSCILLATOR	AVDD and DVDD
STANDBY	Hi-Z, floating	Stopped	Stopped	OFF
Hi-Z	Hi-Z, weak pulldown	Active	Active	ON
Mute	Switching at 50%	Active	Active	ON
Normal operation	Switching with audio	Active	Active	ON

Table 4. Global Faults and Actions

FAULT/ EVENT	FAULT/EVENT CATEGORY	MONITORING MODES	REPORTING METHOD	ACTION TYPE	ACTION RESULT	LATCHED/ SELF-CLEARING
POR	Voltage fault	All	$\overline{\text{FAULT}}$ pin	Hard mute (no ramp)	Standby	Self-clearing
UV		Hi-Z, mute, normal	$\overline{\text{FAULT}}$ pin		Hi-Z	
CP UV						
OV						
Load dump		All	$\overline{\text{FAULT}}$ pin		Standby	
OTW	Thermal warning	Hi-Z, mute, normal	$\overline{\text{CLIP\_OTW}}$ pin	None	None	
OTSD	Thermal fault	Hi-Z, mute, normal	$\overline{\text{FAULT}}$ pin	Hard mute (no ramp)	Standby	

Table 5. Channel Faults and Actions

FAULT/ EVENT	FAULT/EVENT CATEGORY	MONITORING MODES	REPORTING METHOD	ACTION TYPE	ACTION RESULT	LATCHED/ SELF-CLEARING
Open/short diagnostic	Diagnostic at turnon	Hi-Z	Channel does not play	None	None	Self-clearing
Clipping	Warning	Play	$\overline{\text{CLIP\_OTW}}$ pin	None	None	
CBC load current limit	Online protection			Current Limit	Start OC timer	
OC fault	Output channel fault		$\overline{\text{FAULT}}$ pin	Hard mute	Hi-Z	
DC detect				Hard mute	Hi-Z	Latched
OT Foldback	Warning		$\overline{\text{CLIP\_OTW}}$ pin	Reduce Gain	None	Self-clearing

Audio Shutdown and Restart Sequence

The gain ramp of the filtered output signal corresponds to the MUTE pin voltage during the ramping process. The length of time that the MUTE pin takes to complete its ramp is dictated by the value of the external capacitor on the MUTE pin. With the default 220-nF capacitor, the turnon common-mode ramp takes approximately 26ms and the gain ramp takes approximately 76 ms.

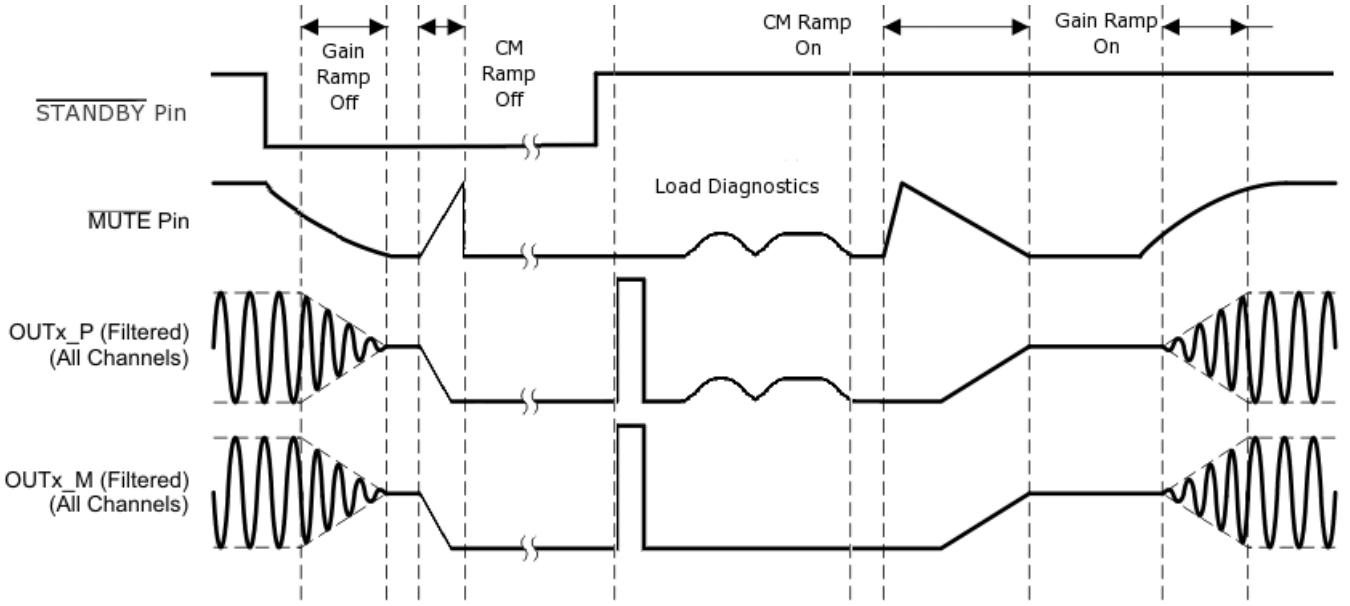


Figure 11. Click- and Pop-Free Shutdown and Restart Sequence Timing Diagram

Fault Shutdown and Restart Sequence Control

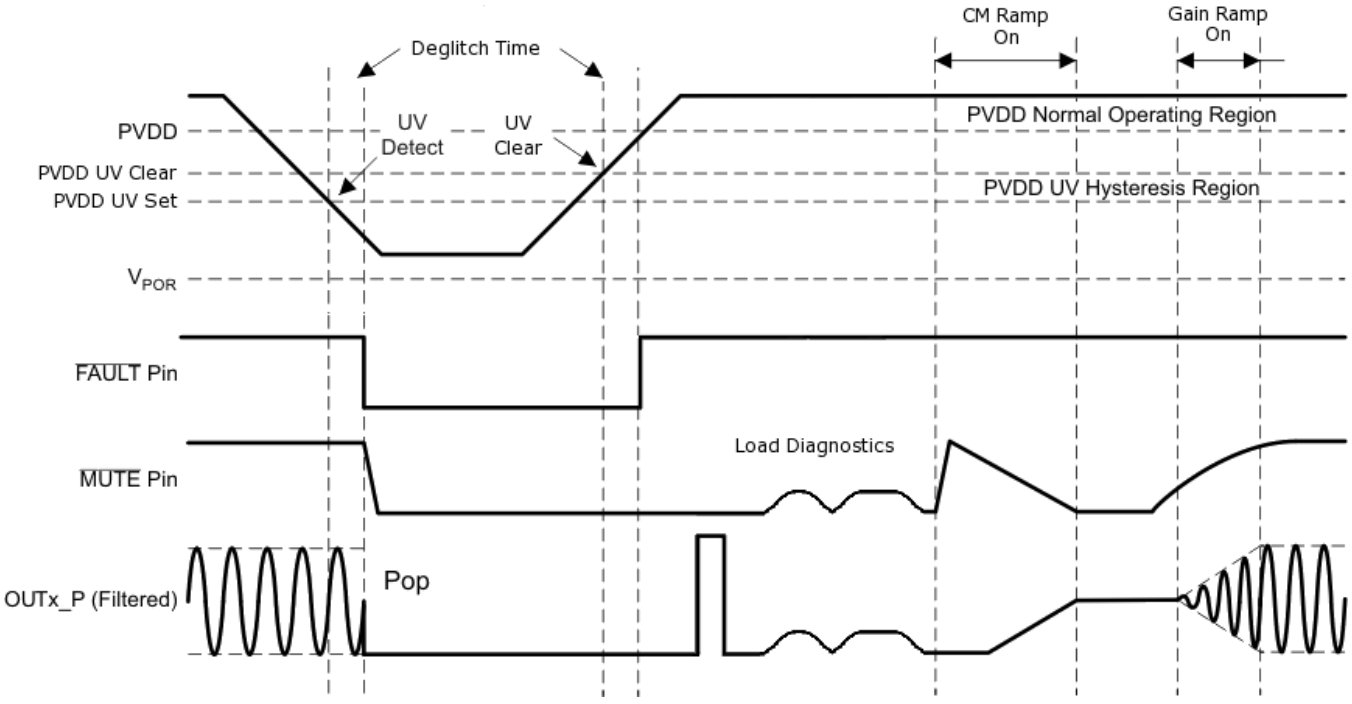


Figure 12. Global Fault Shutdown and Restart Diagram (UV Shutdown and Auto-Recovery)

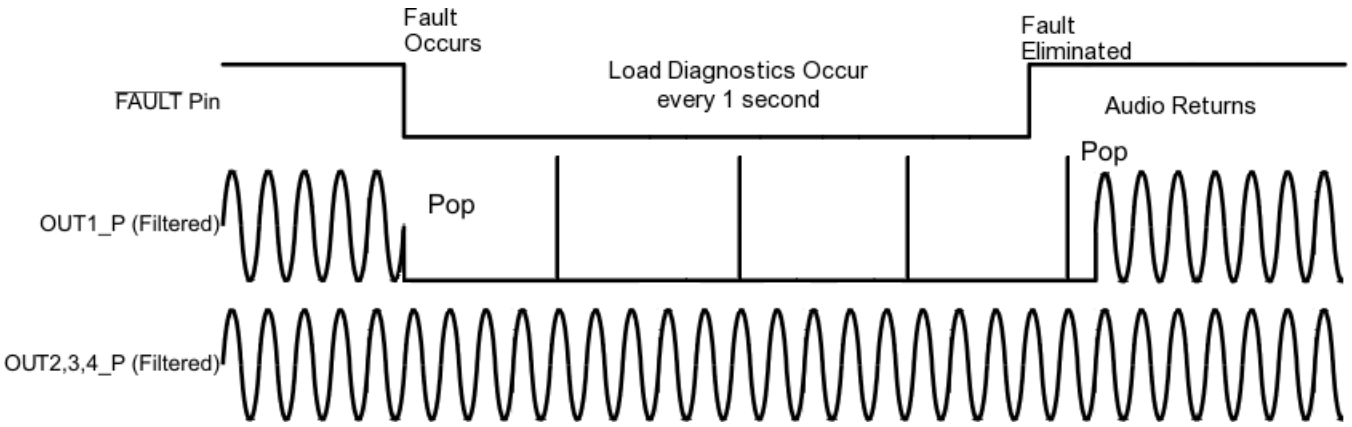


Figure 13. Channel-Fault Shutdown and Individual Channel Restart Diagram

APPLICATION INFORMATION

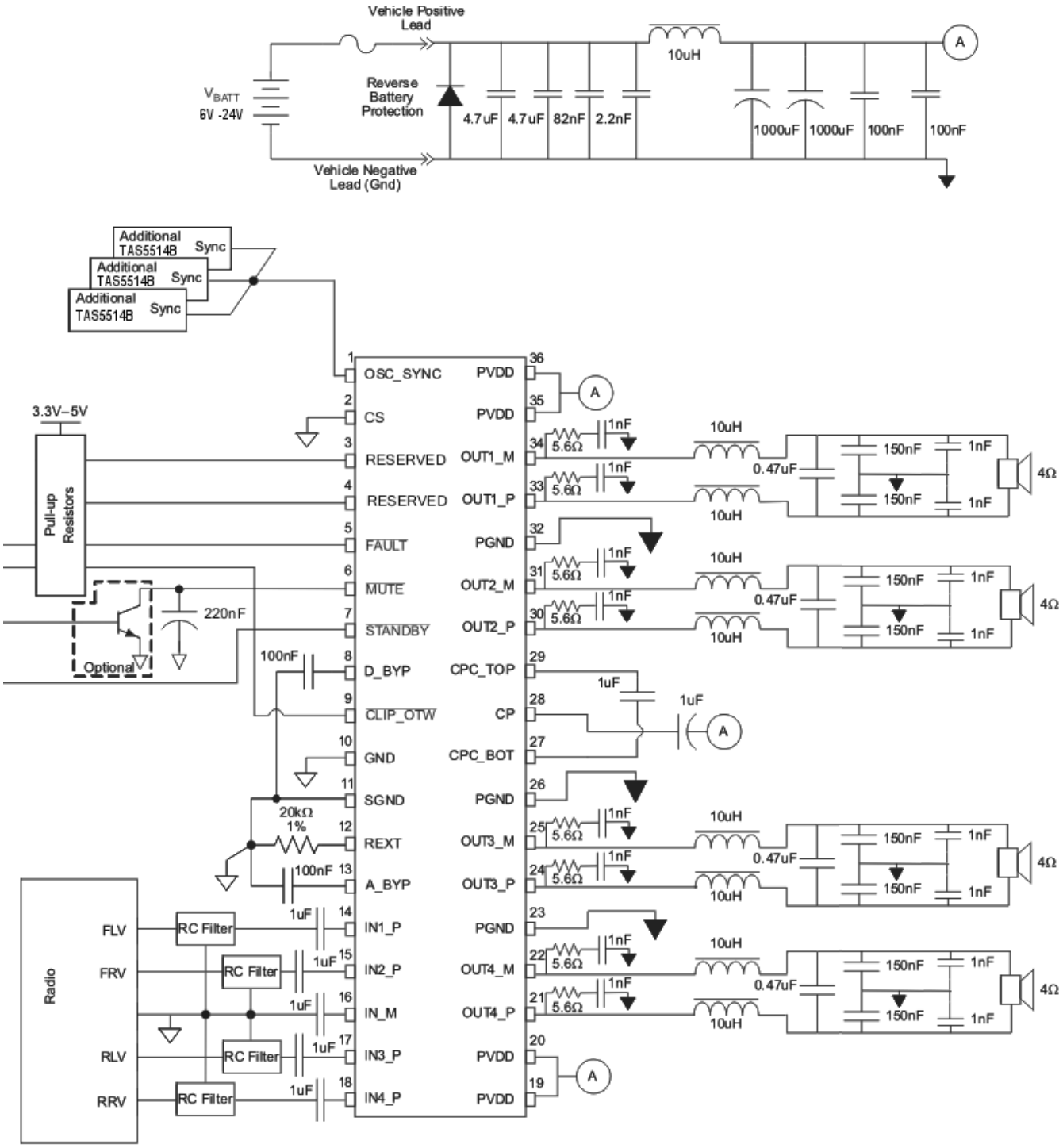


Figure 14. TAS5514B-Q1 Typical Application Schematic

Parallel Operation (PBTL)

The device can drive more current paralleling BTL channels on the load side of the LC output filter. For parallel operation, identical I^2C settings are required for any two paralleled channels in order to have reliable system performance and even power dissipation on multiple channels. For smooth power up, power down, and mute operation, the same control commands (such as mute, play, Hi-Z, etc.) should be sent to the paralleled channels at the same time. Load diagnostic is also supported for parallel connection. Paralleling on the device side of the LC output filter is not supported, and can result in device failure. When paralleling channels, it is important to monitor channels for thermal foldback and lower the system gain for paralleled channels.

Input Filter Design

The input filter for the TAS5514B-Q1 IN_M pin should have an impedance to GND that is equivalent to the parallel combination of the input impedances of all IN_P channels combined, including any source impedance from the previous stage in the system design. For example, if each of the four IN_P channels has a 1-µF dc blocking capacitor, 1 kΩ of series resistance due to an input RC filter, and 1 kΩ of source resistance from the DAC supplying the audio signal, then the IN_M channel should have a 4-µF capacitor in series with a 500-Ω resistor to GND (4 × 1 µF in parallel = 4 µF; 4 × 2 kΩ in parallel = 500 Ω).

Demodulation Filter Design

The amplifier outputs are driven by high-current LDMOS transistors in an H-bridge configuration. These transistors are either fully off or on. The result is a square-wave output signal with a duty cycle that is proportional to the amplitude of the audio signal. It is recommended that a second-order LC filter be used to recover the audio signal. The main purpose of the demodulation filter is to attenuate the high-frequency components of the output signals that are out of the audio band. Design of the demodulation filter significantly affects the audio performance of the power amplifier. Therefore, to meet the system THD+N needs, the selection of the inductors used in the output filter should be carefully considered. The rule is that the inductance should stay above 10% of the inductance value within the range of peak current seen at maximum output power in the system design.

Line Driver Applications

In many automotive audio applications, the end user would like to use the same head unit to drive either a speaker (with several ohms of impedance) or an external amplifier (with several kilohms of impedance). The design is capable of supporting both applications; however, the output filter and system must be designed to handle the expected output load conditions.

Thermal Information

The thermally augmented package is designed to interface directly to heat sinks using a thermal interface compound (for example, Arctic Silver or Ceramique thermal compound). The heat sink then absorbs heat from the ICs and couples it to the local air. If proper thermal management is applied, a proper operating temperature can be maintained the heat can be continually removed from the ICs. Because of the device efficiency, heat sinks can be smaller than those required for linear amplifiers of equivalent performance.

$R_{\theta JA}$ is a system thermal resistance from junction to ambient air. As such, it is a system parameter with the following components:

- $R_{\theta JC}$ (the thermal resistance from junction to case, or in this case the heat slug)
- Thermal grease thermal resistance
- Heat sink thermal resistance

The thermal grease thermal resistance can be calculated from the exposed heat slug area and the thermal grease manufacturer's area thermal resistance (expressed in °C-in^2/W or °C-mm^2/W). The area thermal resistance of the example thermal grease with a 0.001-inch (0.0254-mm) thick layer is about 0.007°C-in^2/W (4.52°C-mm^2/W). The approximate exposed heat slug size is as follows:

36-pin PSOP3	0.124 in^2 (80 mm^2)

Dividing the example thermal grease area resistance by the area of the heat slug gives the actual resistance through the thermal grease for both parts:

36-pin PSOP3 0.06°C/W

The thermal resistance of thermal pads is generally considerably higher than that of a thin thermal grease layer. Thermal tape has an even higher thermal resistance and should not be used at all. Heat sink thermal resistance generally is predicted by the heat sink vendor, modeled using a continuous flow dynamics (CFD) model, or measured.

Thus, for a single monaural channel in the IC, the system $R_{\theta JA} = R_{\theta JC}$ + thermal grease resistance + heat sink resistance.

The following table indicates modeled parameters for one device on a heat sink. The junction temperature is set at 115°C while delivering 20 Wrms per channel into 4-Ω loads with no clipping. It is assumed that the thermal grease is about 0.001 inches (0.0254 mm) thick.

Device	36-Pin PSOP3
Ambient temperature	25°C
Power to load	20 W × 4
Power dissipation	1.90 W × 4
ΔT inside package	7.6°C
ΔT through thermal grease	0.46°C
Required heatsink thermal resistance	10.78°C/W
Junction temperature	115°C
System $R_{\theta JA}$	11.85°C/W
$R_{\theta JA}$ × power dissipation	90°C

Electrical Connection of Heat Slug and Heat Sink

The heat sink connected to the heat slug of the device should be connected to GND or left floating. The heat slug should not be connected to any other electrical node.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TAS5514BTDKDRQ1	OBSOLETE	HSSOP	DKD	36		TBD	Call TI	Call TI	-40 to 105	TAS5514BQ1	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

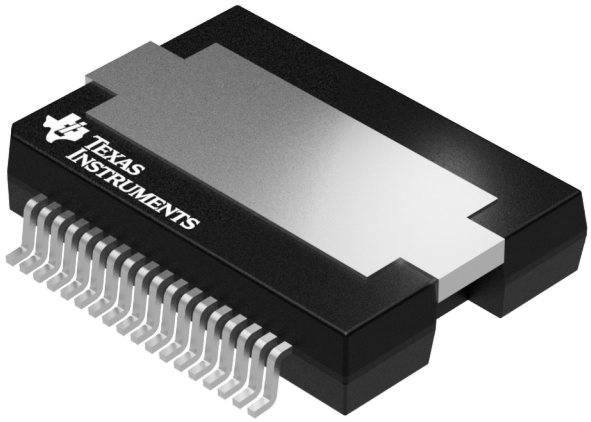
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

GENERIC PACKAGE VIEW

DKD 36 PowerPAD™ SSOP - 3.6 mm max height

PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4204421-2/N

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