

## TLV4011-Q1 具有精密基准的低功耗比较器

### 1 特性

- 符合汽车应用要求
- 具有符合 AEC-Q100 标准的下列特性：
  - 器件温度等级 1：-40°C 至 125°C 的环境工作温度范围
  - 器件 HBM ESD 分级等级 H1C
  - 器件 CDM ESD 分类等级 C6
- 低至 1.226V 的可调节阈值
- ±1.5% 阈值电压精度
- 电源电流：3  $\mu$ A
- 开漏输出
- 温度范围：-40°C 至 125°C
- 5 引脚 SC-70 封装

### 2 应用

- 紧急呼叫 (eCall)
- 远程信息处理控制单元
- 车载充电器 (OBC) 和无线充电器
- 直流/直流转换器
- 电池管理系统 (BMS)

### 3 说明

TLV4011-Q1 是一款具有精密集成基准的低功耗、高精度比较器。可通过将两个外部电阻器连接到输入端，实现低至 1.226V 的可调电压阈值。

经过工厂校准的开关阈值和精密迟滞相结合，使得 TLV4011-Q1 非常适合在必须将慢速输入信号转换为纯净数字输出的严苛、嘈杂环境中进行电压和电流监测。同样地，输入端的短时毛刺脉冲也得以抑制，因此可确保稳定的输出运行，不会引起误触发。

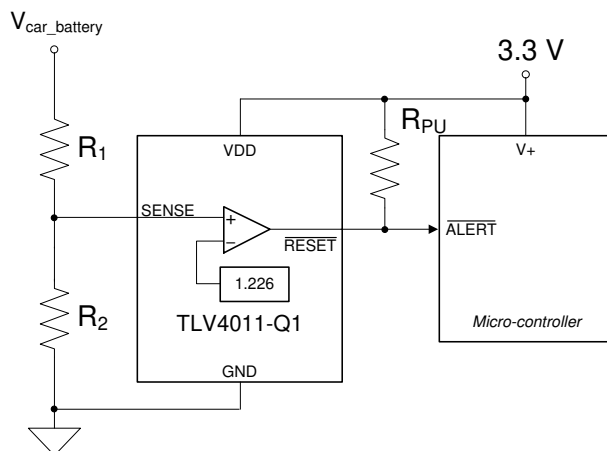
上电期间，当电源电压  $V_{DD}$  大于 0.8V 时， $\overline{RESET}$  有效运行（低电平）。因此，TLV4011-Q1 会监测输入并使  $\overline{RESET}$  运行（低电平），同时输入仍保持在阈值电压  $V_{IT}$  以下。一旦输入电压升至阈值电压  $V_{IT}$  以上， $\overline{RESET}$  则不再运行（高电平）。该产品系列专为 1.8V、3.3V、5V 和可调电源电压而设计。

TLV4011-Q1 采用 5 引脚 SC-70 封装，工作温度范围为 -40°C 至 125°C。

#### 器件信息<sup>(1)</sup>

器件型号	封装	封装尺寸 (标称值)
TLV4011-Q1	SC-70 (5)	2.00mm × 1.25mm

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。



典型应用原理图



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## 4 Revision History

DATE	REVISION	NOTES
September 2020	*	Initial release

## 5 Pin Configuration and Functions

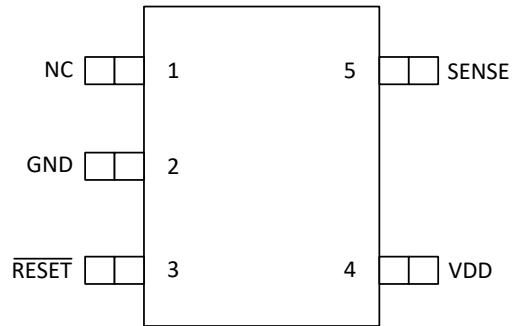


图 5-1. DCK Package, 5-Pin SC-70, Top View

## Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
GND	2	I	Ground
RESET	3	O	Active-low reset output (open-drain)
SENSE	5	I	Input
NC	1	—	No internal connection
V <sub>DD</sub>	4	I	Input supply voltage

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>DD</sub>	Supply voltage <sup>(2)</sup>	- 0.3	7	V
	Voltage applied to all other pins <sup>(2)</sup>	- 0.3	7	V
I <sub>OL</sub>	Maximum low-level output current		5	mA
I <sub>OH</sub>	Maximum high-level output current		- 5	mA
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0 or V <sub>I</sub> > V <sub>DD</sub>	±10	mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0 or V <sub>O</sub> > V <sub>DD</sub>	±10	mA
P <sub>D</sub>	Continuous total power dissipation	See <a href="#"># 6.8</a>		
T <sub>A</sub>	Operating free-air temperature	- 40	125	°C
T <sub>solder</sub>	Soldering temperature		260	°C
T <sub>stg</sub>	Storage temperature	- 65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to GND. For reliable operation, the device should not be continuously operated at 7 V for more than t = 1000 h.

### 6.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 <sup>(1)</sup>	±2000
		Charged-device model (CDM), per AEC Q100-011	±1000

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 6.3 Recommended Operating Conditions

		MIN	MAX	UNIT
V <sub>DD</sub>	Supply voltage	1.3	6	V
V <sub>I</sub>	Input voltage	0	V <sub>DD</sub> + 0.3	V
T <sub>A</sub>	Operating free-air temperature	- 40	125	°C

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TLV4011-Q1	UNIT
		DCK (SC-70)	
		5 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	246.6	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	68.2	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	78.4	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	0.9	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	77.7	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>OL</sub>	Low-level output voltage	V <sub>DD</sub> = 1.5 V, I <sub>OL</sub> = 1 mA				V
		V <sub>DD</sub> = 3.3 V, I <sub>OL</sub> = 2 mA			0.3	
		V <sub>DD</sub> = 6 V, I <sub>OL</sub> = 3 mA				
V <sub>POR</sub>	Power-up reset voltage <sup>(1)</sup>	V <sub>OL(max)</sub> = 0.2 V, I <sub>OL</sub> = 50 μA, T <sub>A</sub> = 25°C	0.8			V
V <sub>IT</sub>	Negative-going input threshold voltage <sup>(2)</sup>	SENSE	1.2	1.226	1.244	V
V <sub>hys</sub>	Hysteresis	T <sub>A</sub> = 25°C		15		mV
I <sub>I</sub>	Input current	SENSE	-25		25	nA
I <sub>OH</sub>	High-level output current at RESET	RESET	SENSE = V <sub>IT</sub> + 0.2 V, V <sub>OH</sub> = V <sub>DD</sub>		300	nA
I <sub>DD</sub>	Supply current	V <sub>DD</sub> = 3.3 V, Output unconnected		2	4	μA
		V <sub>DD</sub> = 6 V, Output unconnected		2	4	
C <sub>I</sub>	Input capacitance	V <sub>I</sub> = 0 V to V <sub>DD</sub>		1		pF

(1) The lowest supply voltage at which  $\overline{\text{RESET}}$  (V<sub>OL(max)</sub> = 0.2 V, I<sub>OL</sub> = 50 μA) becomes active. t<sub>r</sub>(V<sub>DD</sub>) ≥ 15 μs/V.

(2) To ensure the best stability of the threshold voltage, place a bypass capacitor (ceramic, 0.1-μF) near the supply terminals.

## 6.6 Timing Requirements

R<sub>L</sub> = 1 MΩ, C<sub>L</sub> = 50 pF, T<sub>A</sub> = -40°C to 125°C (unless otherwise noted)

			MIN	MAX	UNIT	
t <sub>w</sub>	Pulse duration	SENSE	V <sub>IH</sub> = 1.05 × V <sub>IT</sub> , V <sub>IL</sub> = 0.95 × V <sub>IT</sub>		5.5	μs

## 6.7 Switching Characteristics

R<sub>L</sub> = 1 MΩ, C<sub>L</sub> = 50 pF, T<sub>A</sub> = -40°C to 125°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t <sub>PHL</sub>	Propagation (delay) time, high-to-low-level output	SENSE to $\overline{\text{RESET}}$ delay		5	100	μs
t <sub>PLH</sub>	Propagation (delay) time, low-to-high-level output	SENSE to $\overline{\text{RESET}}$ delay		5	100	μs

## 6.8 Dissipation Ratings

PACKAGE	POWER RATING T <sub>A</sub> < 25°C	DERATING FACTOR ABOVE T <sub>A</sub> = 25°C	POWER RATING T <sub>A</sub> = 70°C	POWER RATING T <sub>A</sub> = 85°C
DCK	321 mW	2.6 mW/°C	206 mW	167 mW

## 6.9 Timing Diagrams

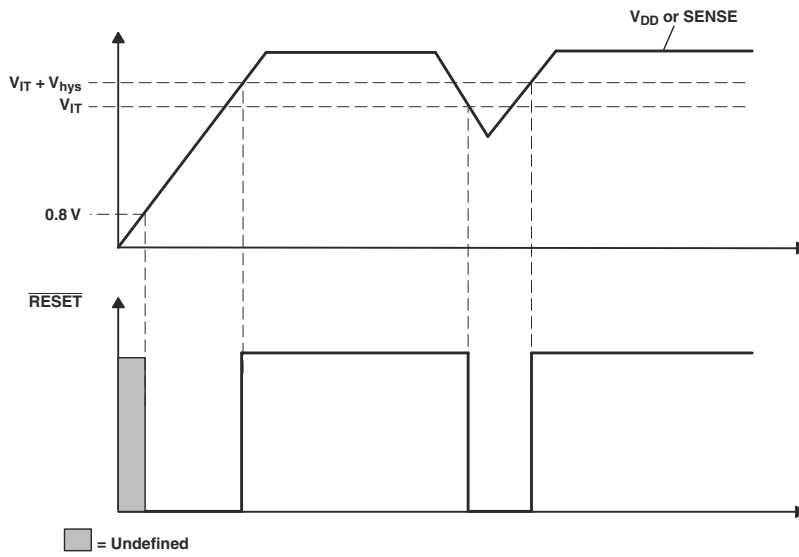


图 6-1. Timing Requirements

## 6.10 Typical Characteristics

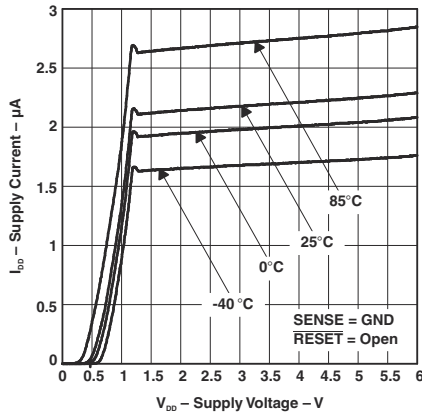


图 6-2. Supply Current vs Supply Voltage

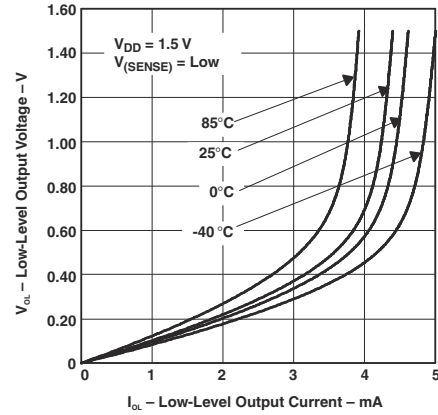


图 6-3. Low-Level Output Voltage vs Low-Level Output Current

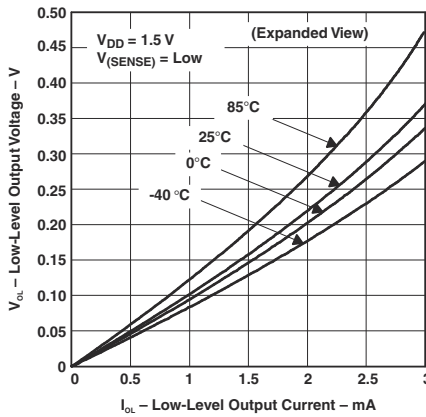


图 6-4. Low-Level Output Voltage vs Low-Level Output Current

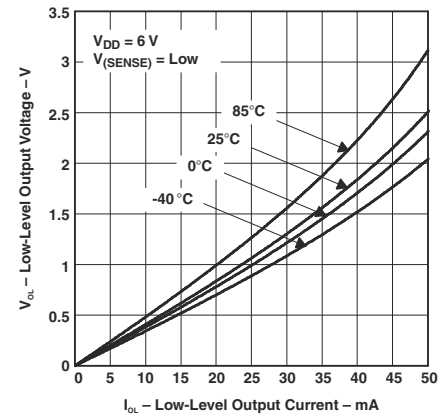


图 6-5. Low-Level Output Voltage vs Low-Level Output Current

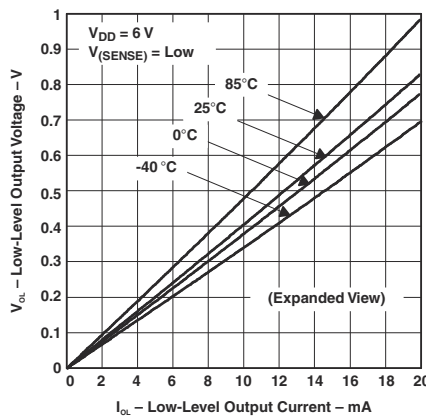


图 6-6. Low-Level Output Voltage vs Low-Level Output Current

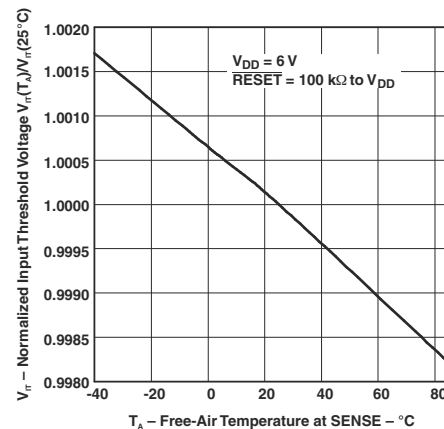


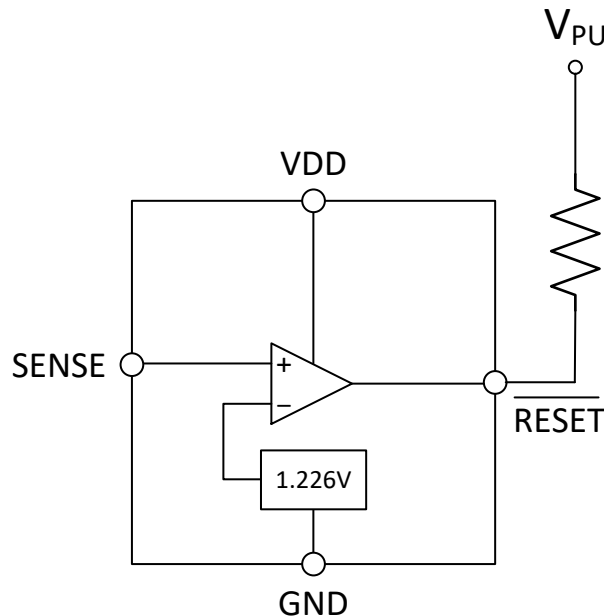
图 6-7. Normalized Input Threshold Voltage vs Free-Air Temperature At Sense

## 7 Detailed Description

### 7.1 Overview

The TLV4011-Q1 is a low-current comparator used to monitor system voltages above 1.226 V. The comparators assert an active low  $\overline{\text{RESET}}$  signal when the SENSE voltages drop below  $V_{IT}$ . The  $\overline{\text{RESET}}$  output remains low until the SENSE voltage returns above  $V_{IT}$  plus the integrated hysteresis level. The TLV4011-Q1 is also designed to be immune to short negative transients on the SENSE pin.

### 7.2 Functional Block Diagram



### 7.3 Feature Description

#### 7.3.1 SENSE Monitoring

The SENSE input is where a system voltage can be monitored. If the voltage on this pin drops below  $V_{IT}$ ,  $\overline{\text{RESET}}$  is asserted low. The comparator has a built-in hysteresis to ensure smooth  $\overline{\text{RESET}}$  assertions and de-assertions. By connecting a resistor divider network to the SENSE input as shown in the circuit below,  $V_{IN}$  is divided down so  $\overline{\text{RESET}}$  will assert when the divided down value of  $V_{IN}$  reaches  $V_{IT}$  (1.226 V). The TLV4011-Q1 is capable of monitoring any input voltage down to 1.226 V.

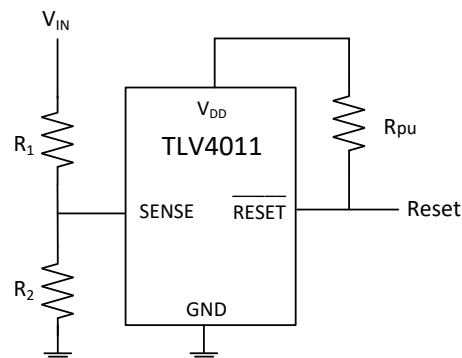


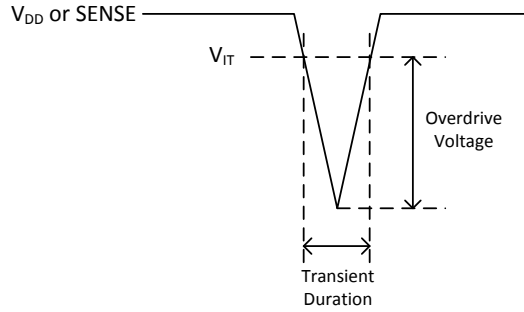
图 7-1. Voltage Monitor

#### 7.3.2 Transient Immunity

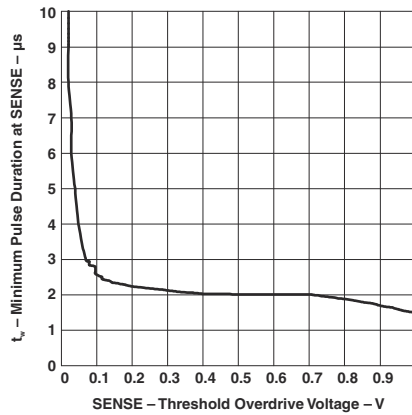
The TLV4011-Q1 is immune to short negative transients on the SENSE pin. Sensitivity to transients is dependent on threshold overdrive as shown in 图 7-2 and 图 7-3. These graphs show the duration that the transient is below



$V_{IT}$  compared to the magnitude of the voltage drop below  $V_{IT}$ , called the threshold overdrive voltage. Any combination of transient duration and overdrive voltage which lies above the curves will result in  $\overline{\text{RESET}}$  being asserted low. Any transient which lies below the curves will be ignored by the device.



**图 7-2. SENSE Overdrive Voltage**



**图 7-3. Minimum Pulse Duration at Sense vs Sense Threshold Overdrive Voltage**

### 7.4 Device Functional Modes

The SENSE input is used to monitor one supply. When that supply is above the  $V_{IT}$  threshold,  $\overline{\text{RESET}}$  will be high. Otherwise,  $\overline{\text{RESET}}$  will be low.

**表 7-1. Function and Truth Table**

TLV4011-Q1	
SENSE > $V_{IT}$	RESET
0 (False)	L
1 (True)	H

## 8 Application and Implementation

### 备注

以下应用部分的信息不属于 TI 组件规范，TI 不担保其准确性和完整性。客户应负责确定 TI 组件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

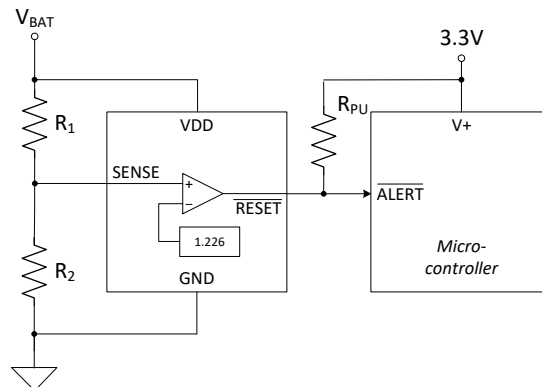
### 8.1 Application Information

The TLV4011-Q1 comparator is designed to assert an active-low  $\overline{\text{RESET}}$  signal when the SENSE input drops below the voltage threshold  $V_{IT}$ . The  $\overline{\text{RESET}}$  signal remains low until the voltages return above their respective threshold plus the hysteresis. If additional hysteresis is required, positive feedback can be implemented similar to how it is done on a discrete comparator. See [Application Note](#) for details on how to implement external hysteresis in a non-inverting configuration.

### 8.2 Typical Application

#### 8.2.1 Undervoltage Detection

Undervoltage detection is frequently required in battery-powered, portable electronics to alert the system that a battery voltage has dropped below the usable voltage level. [图 8-1](#) shows a simple undervoltage detection circuit using the TLV4011-Q1 which is a non-inverting comparator with an integrated 1.226 V reference and an open-drain output stage. A non-inverting is well suited for this application since the micro-controller requires an active low signal when an undervoltage level occurs.



**图 8-1. Undervoltage Detection**

##### 8.2.1.1 Design Requirements

For this design, follow these design requirements:

- TLV4011-Q1 operates from the  $V_{BAT}$  directly
- Output is level-shifted to the 3.3 V power supply that powers the microcontroller.
- Undervoltage alert is active low.
- Logic low output when  $V_{BAT}$  decreases below 2.0V.

##### 8.2.1.2 Detailed Design Procedure

Configure the circuit as shown in [图 8-1](#). Note that VDD of the comparator is connected directly to  $V_{BAT}$  (the battery being monitored) and the output of the comparator is level shifted with its open-drain output to 3.3 V which powers the micro-controller. Resistors  $R_1$  and  $R_2$  divide down  $V_{BAT}$  so that the resistor divided output equals 1.226 V when  $V_{BAT}$  reaches an undervoltage alert level of 2.0 V.

When the battery voltage sags down to 2.0 V, the resistor divider voltage crosses the ( $V_{IT} = 1.226$  V) threshold of the TLV4011-Q1. This causes the comparator output to transition from a logic high to a logic low. An open-drain comparator is selected so the comparator output is compatible with the input logic level of the microcontroller. In addition, selecting a comparator with an integrated reference value of 1.226 V is favorable because it is the

closest internal reference option that is less than the critical undervoltage level of 2.0 V. Choosing the internal reference option that is closest to the critical undervoltage level minimizes the resistor divider ratio which optimizes the accuracy of the circuit. Error at the falling edge threshold of ( $V_{IT}$ ) is amplified by the inverse of the resistor divider ratio. So minimizing the resistor divider ratio is a way of optimizing voltage monitoring accuracy.

方程式 1 is derived from the analysis of 图 8-1.

$$V_{IT} = \frac{R_2}{R_1 + R_2} \times V_{BAT} \quad (1)$$

where

- $R_1$  and  $R_2$  are the resistor values for the resistor divider connected to SENSE
- $V_{BAT}$  is the voltage source that is being monitored for an undervoltage condition.
- $V_{IT}$  is the falling edge threshold where the comparator output changes state from high to low

Rearranging 方程式 1 and solving for  $R_1$  yields 方程式 2.

$$R_1 = \frac{(V_{BAT} - V_{IT})}{V_{IT}} \times R_2 \quad (2)$$

For the specific undervoltage detection of 2.0 V using the TLV4011-Q1, the following results are calculated.

$$R_1 = \frac{(2.0 - 1.226)}{1.226} \times 1M = 631 \text{ k}\Omega \quad (3)$$

where

- $R_2$  is set to 1 M $\Omega$
- $V_{BAT}$  is set to 2.0 V
- $V_{IT}$  is set to 1.226 V

Choose  $R_{TOTAL}$  ( $R_1 + R_2$ ) such that the current through the divider is at approximately 100 times higher than the input bias current ( $I_{BIAS}$ ). The resistors can have high values to minimize current consumption in the circuit without adding significant error to the resistive divider.

### 8.2.1.3 Application Curve

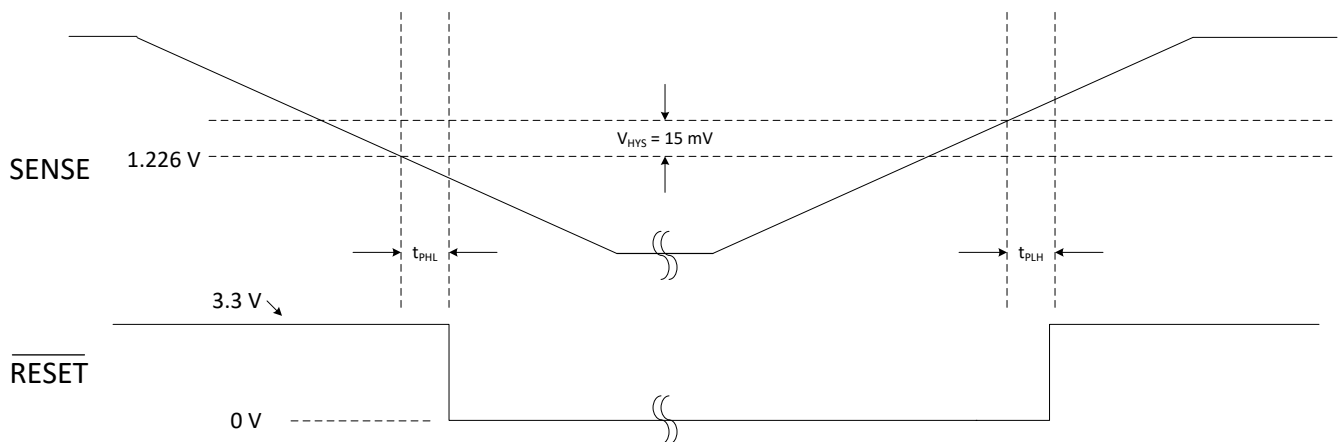


图 8-2. Undervoltage Detection

## 8.2.2 Additional Application Information

### 8.2.2.1 Pull-up Resistor Selection

Since the TLV4011-Q1 has an open drain output, care should be taken in selecting the pull-up resistor ( $R_{PU}$ ) value to ensure proper output voltage levels. First, consider the required output high logic level requirement of the logic device that is being driven by the comparator when calculating the maximum  $R_{PU}$  value. When in a logic high output state, the output impedance of the comparator is very high but there is a finite amount of leakage current that needs to be accounted for. Use  $I_{OH}$  from the EC Table and the  $V_{IH}$  minimum from the logic device being driven to determine  $R_{PU}$  maximum using [方程式 4](#).

$$R_{PU(max)} = \frac{(V_{PU} - V_{IH(min)})}{I_{OH}} \quad (4)$$

Next, determine the minimum value for  $R_{PU}$  by using the  $V_{IL}$  maximum from the logic device being driven. In order for the comparator output to be recognized as a logic low,  $V_{IL}$  maximum is used to determine the upper boundary of the comparator's  $V_{OL}$ .  $V_{OL}$  maximum for the comparator is available in the EC Table for specific sink current levels and can also be found from the  $V_{OUT}$  versus  $I_{SINK}$  curve in the Typical Application curves. A good design practice is to choose a value for  $V_{OL}$  maximum that is 1/2 the value of  $V_{IL}$  maximum for the input logic device. The corresponding sink current and  $V_{OL}$  maximum value will be needed to calculate the minimum  $R_{PU}$ . This method will ensure enough noise margin for the logic low level. With  $V_{OL}$  maximum determined and the corresponding  $I_{SINK}$  obtained, the minimum  $R_{PU}$  value is calculated with [方程式 5](#).

$$R_{PU(min)} = \frac{(V_{PU} - V_{OL(max)})}{I_{SINK}} \quad (5)$$

Since the range of possible  $R_{PU}$  values is large, a value between 5 k $\Omega$  and 100 k $\Omega$  is generally recommended. A smaller  $R_{PU}$  value provides faster output transition time and better noise immunity, while a larger  $R_{PU}$  value consumes less power when in a logic low output state.

### 8.2.2.2 Input Supply Capacitor

Although an input capacitor is not required for stability, for good analog design practice, connect a 100 nF low equivalent series resistance (ESR) capacitor from (VDD) to (GND).

### 8.2.2.3 Sense Capacitor

Although not required in most cases, for extremely noisy applications, place a 1 nF to 100 nF bypass capacitor from the comparator input (SENSE) to the (GND) for good analog design practice. This capacitor placement reduces device sensitivity to transients.

## 9 Power Supply Recommendations

The TLV4011-Q1 comparator is designed to operate from an input supply from 1.3 V to 6 V. It is recommended to place a 0.1- $\mu$ F capacitor from the VDD pin to GND.

## 10 Layout

### 10.1 Layout Guidelines

TI recommends to place the 0.1- $\mu$ F decoupling capacitor close to the VDD pin. The VDD trace should be able to carry 6  $\mu$ A without a significant drop in voltage. Avoid a long trace from the SENSE pin to the resistor divider.

### 10.2 Layout Examples

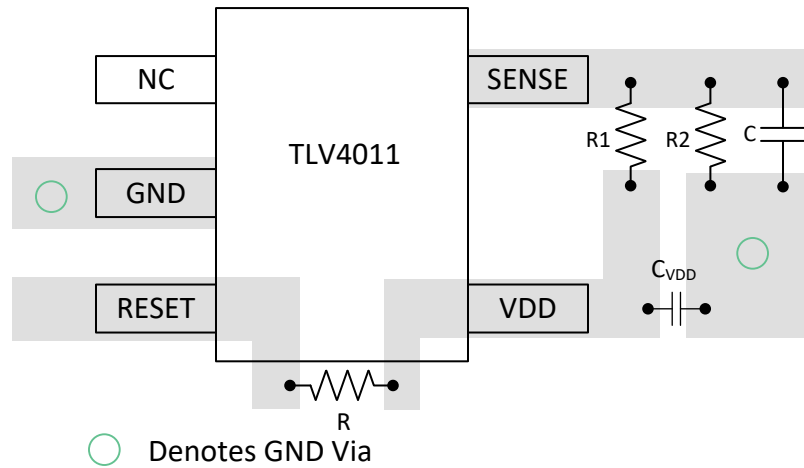


图 10-1. Layout Example

## 11 Device and Documentation Support

### 11.1 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](http://ti.com) 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

### 11.2 支持资源

**TI E2E™ 支持论坛** 是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《[使用条款](#)》。

### 11.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

### 11.4 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 11.5 术语表

**TI 术语表** 本术语表列出并解释了术语、首字母缩略词和定义。

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV4011QDCKRQ1	ACTIVE	SC70	DKK	5	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	119	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF TLV4011-Q1 :**



- Catalog : [TLV4011](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV4011QDCKRQ1	SC70	DCK	5	3000	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV4011QDCKRQ1	SC70	DCK	5	3000	183.0	183.0	20.0

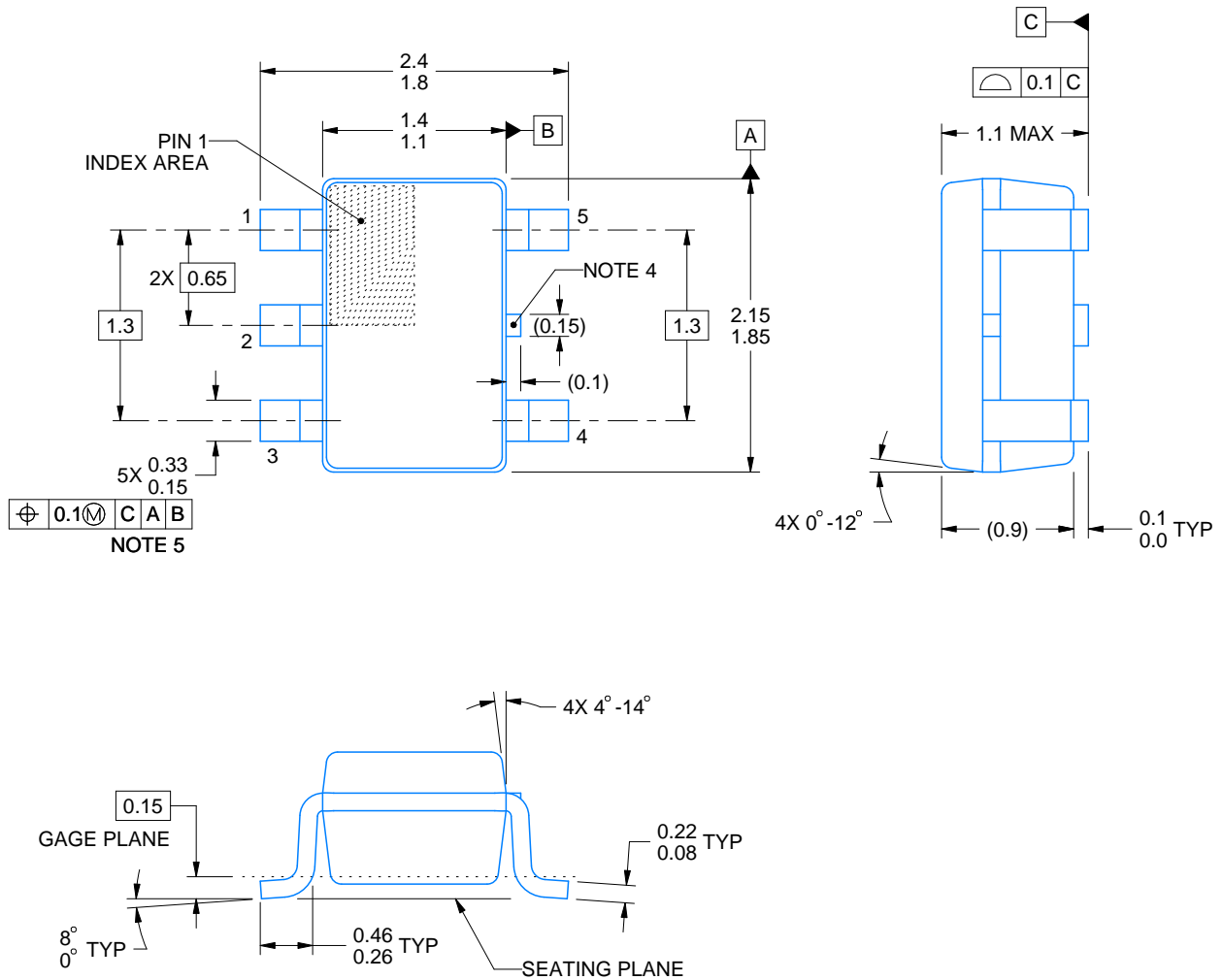


# DCK0005A

# PACKAGE OUTLINE

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



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### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side

# EXAMPLE BOARD LAYOUT

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:18X



SOLDER MASK DETAILS

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NOTES: (continued)

- 7. Publication IPC-7351 may have alternate designs.
- 8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DCK0005A

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 THICK STENCIL  
SCALE: 18X

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NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

## 重要声明和免责声明

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