

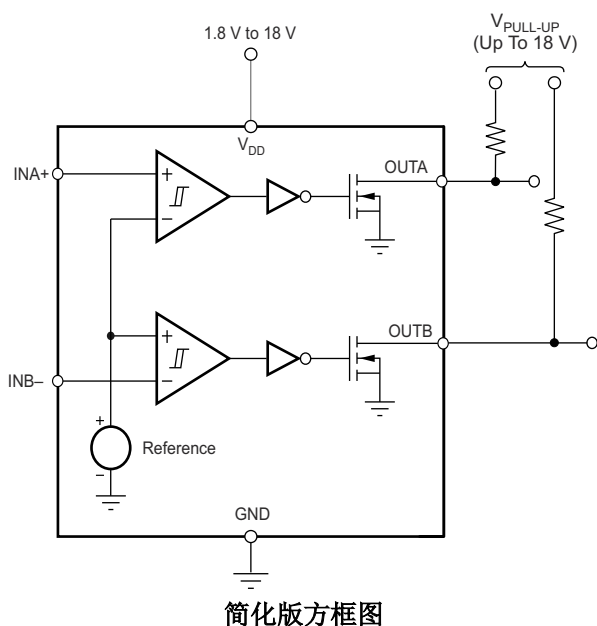
## 具有 400mV 基准电压的 TLV6700-Q1 低功耗、18V 窗口比较器

### 1 特性

- 符合汽车应用要求
- 具有符合 AEC-Q100 标准的下列特性：
  - 器件温度等级 1：-40°C 至 125°C 环境温度范围
  - 器件 HBM ESD 分类等级 H2
  - 器件 CDM ESD 分类等级 C6
- 宽电源电压范围：1.8 V 至 18V
- 可调节阈值：低至 400mV
- 高阈值精度：
  - 25°C 时最高为 0.5%
  - 在工作温度范围内最大值为 1.0%
- 低静态电流：5.5μA (典型值)
- 开漏输出
- 内部迟滞：5.5mV (典型值)
- 温度范围：-40°C 至 125°C
- 封装：
  - 薄型 SOT-23-6
  - 无引线 WSON-6

### 2 应用

- 紧急呼叫 (eCall)
- 汽车音响主机
- 仪表组
- 车载充电器 (OBC) 和无线充电器



### 3 说明

TLV6700-Q1 是一款高电压窗口比较器，工作电压范围为 1.8V 至 18V。该器件拥有两个内部基准电压为 400mV 的高精度比较器和两个额定电压为 18V 的开漏输出。TLV6700-Q1 可以作为窗口比较器使用，也可以作为两个独立的比较器使用；可以使用外部电阻设定监控的电压。

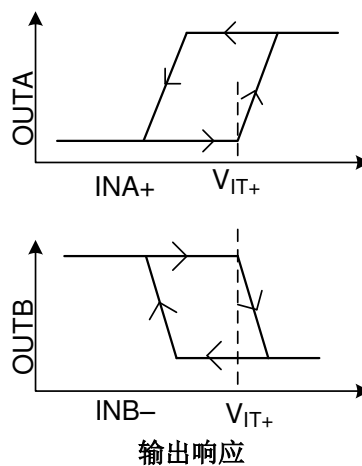
当 INA+ 上的电压下降至低于  $(V_{ITP} - V_{HYS})$  时，OUTA 被驱动至低电平，当电压返回到相应阈值  $(V_{ITP})$  之上时，OUTA 变为高电平。当 INB- 上的电压上升至高于  $V_{ITP}$  时，OUTB 被驱动至低电平，当电压下降至低于相应阈值  $(V_{ITP} - V_{HYS})$  时，OUTB 变为高电平。TLV6700-Q1 中的两个比较器都具有内置迟滞来抑制短时毛刺脉冲，确保稳定的输出运行，不会引起误触发。

TLV6700-Q1 采用薄型 SOT-23-6 和无引线 WSON-6 封装；这些比较器的额定结温范围为 -40°C 至 125°C。

#### 器件信息(1)

器件型号	封装	封装尺寸 (标称值)
TLV6700-Q1	SOT-23 (6)	2.90mm × 1.60mm
	WSON (6)	1.50mm × 1.50mm

- (1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



## Table of Contents

<b>1 特性</b> .....	1	8.3 Feature Description.....	10
<b>2 应用</b> .....	1	8.4 Device Functional Modes.....	12
<b>3 说明</b> .....	1	<b>9 Application and Implementation</b> .....	13
<b>4 Revision History</b> .....	2	9.1 Application Information.....	13
<b>5 Device Comparison Table</b> .....	3	9.2 Typical Application.....	16
<b>6 Pin Configuration and Functions</b> .....	4	9.3 Do's and Don'ts.....	18
<b>7 Specifications</b> .....	5	<b>10 Power Supply Recommendations</b> .....	19
7.1 Absolute Maximum Ratings.....	5	<b>11 Layout</b> .....	20
7.2 ESD Ratings.....	5	11.1 Layout Guidelines.....	20
7.3 Recommended Operating Conditions.....	5	11.2 Layout Example.....	20
7.4 Thermal Information.....	5	<b>12 Device and Documentation Support</b> .....	21
7.5 Electrical Characteristics.....	6	12.1 Device Support.....	21
7.6 Timing Requirements.....	7	12.2 Receiving Notification of Documentation Updates..	21
7.7 Switching Characteristics.....	7	12.3 支持资源.....	21
7.8 Timing Diagrams .....	7	12.4 Trademarks.....	21
7.9 Typical Characteristics.....	8	12.5 静电放电警告.....	21
<b>8 Detailed Description</b> .....	10	12.6 术语表.....	21
8.1 Overview.....	10	<b>13 Mechanical, Packaging, and Orderable Information</b> .....	21
8.2 Functional Block Diagram.....	10		

## 4 Revision History

注：以前版本的页码可能与当前版本的页码不同

DATE	REVISION	NOTES
November 2020	*	Initial Release

## 5 Device Comparison Table

**表 5-1. Industrial TLV67xx Comparator Family**

PART NUMBER	CONFIGURATION	OPERATING VOLTAGE RANGE	THRESHOLD ACCURACY OVER TEMPERATURE
<a href="#">TLV6700</a>	Window	1.8 V to 18 V	1%
<a href="#">TLV6703</a>	Non-Inverting Single Channel	1.8 V to 18 V	1%
<a href="#">TLV6710</a>	Window	1.8 V to 36 V	0.75%
<a href="#">TLV6713</a>	Non-Inverting Single Channel	1.8 V to 36 V	0.75%

## 6 Pin Configuration and Functions

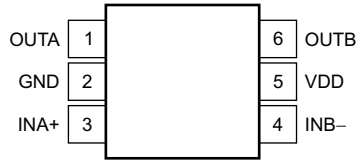


图 6-1. DDC Package, SOT-23-6, Top View

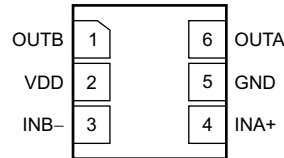


图 6-2. DSE Package, WSON-6, Top View

表 6-1. Pin Functions

NAME	PIN		I/O	DESCRIPTION
	DDC	DSE		
GND	2	5	—	Ground
INA+	3	4	I	This pin is connected to the voltage to be monitored with the use of an external resistor divider. When the voltage at this terminal drops below the threshold voltage ( $V_{ITP} - V_{HYS}$ ), OUTA is driven low.
INB -	4	3	I	This pin is connected to the voltage to be monitored with the use of an external resistor divider. When the voltage at this terminal exceeds the threshold voltage ( $V_{ITP}$ ), OUTB is driven low.
OUTA	1	6	O	INA+ comparator open-drain output. OUTA is driven low when the voltage at this comparator is below ( $V_{ITP} - V_{HYS}$ ). The output goes high when the sense voltage returns above the respective threshold ( $V_{ITP}$ ).
OUTB	6	1	O	INB - comparator open-drain output. OUTB is driven low when the voltage at this comparator exceeds $V_{ITP}$ . The output goes high when the sense voltage returns below the respective threshold ( $V_{ITP} - V_{HYS}$ ).
VDD	5	2	I	Supply voltage input. Connect a 1.8-V to 18-V supply to VDD to power the device. Good analog design practice is to place a 0.1- $\mu$ F ceramic capacitor close to this pin.

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Voltage <sup>(2)</sup>	V <sub>DD</sub>	- 0.3	20	V
	OUTA, OUTB	- 0.3	20	V
	INA+, INB -	- 0.3	7	V
Current	Output terminal current		40	mA
Operating junction temperature, T <sub>J</sub>		- 40	125	°C
Storage temperature, T <sub>stg</sub>		- 65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to network ground terminal.

### 7.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub> Electrostatic discharge	Human body model (HBM), per AEC Q100-002 <sup>(1)</sup>	±2500	V
	Charged-device model (CDM), per AEC Q100-011	±1000	

- (1) JEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 7.3 Recommended Operating Conditions

over operating temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V <sub>DD</sub>	Supply voltage	1.8		18	V
V <sub>I</sub>	Input voltage	0		6.5	V
V <sub>O</sub>	Output voltage	0		18	V

### 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		DDC (SOT)	DSE (WSON)	UNIT
		6 PINS	6 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	204.6	194.9	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	50.5	128.9	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	54.3	153.8	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	0.8	11.9	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	52.8	157.4	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

## 7.5 Electrical Characteristics

Over the operating temperature range of  $T_J = -40^\circ\text{C}$  to  $125^\circ\text{C}$ , and  $1.8\text{ V} < V_{DD} < 18\text{ V}$ , unless otherwise noted.

Typical values are at  $T_J = 25^\circ\text{C}$  and  $V_{DD} = 5\text{ V}$ .

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(POR)}$	Power-on reset voltage <sup>(1)</sup>	$V_{OLmax} = 0.2\text{ V}$ , $I_{(OUTA/B)} = 15\ \mu\text{A}$			0.8	V
$V_{IT+}$	Positive-going input threshold voltage	$V_{DD} = 1.8\text{V}$ and $18\text{ V}$ , $T_J = 25^\circ\text{C}$	398	400	402.5	mV
		$V_{DD} = 1.8\text{V}$ and $18\text{ V}$ , $T_J = -40^\circ\text{C}$ to $125^\circ\text{C}$	396		404	
$V_{IT-}$	Negative-going input threshold voltage	$V_{DD} = 1.8\text{V}$ and $18\text{ V}$ , $T_J = 25^\circ\text{C}$	391.6	394.5	397.5	mV
		$V_{DD} = 1.8\text{V}$ and $18\text{ V}$ , $T_J = -40^\circ\text{C}$ to $125^\circ\text{C}$	387		400	
$V_{hys}$	Hysteresis voltage ( $hys = V_{IT+} - V_{IT-}$ )			5.5	12	mV
$I_{(INA+)}$	Input current (at the INA+ terminal)	$V_{DD} = 1.8\text{ V}$ and $18\text{ V}$ , $V_I = 6.5\text{ V}$	- 25	1	25	nA
$I_{(INB-)}$	Input current (at the INB - terminal)	$V_{DD} = 1.8\text{ V}$ and $18\text{ V}$ , $V_I = 0.1\text{ V}$	- 15	1	15	nA
$V_{OL}$	Low-level output voltage	$V_{DD} = 1.8\text{ V}$ , $I_O = 3\text{ mA}$			250	mV
		$V_{DD} = 5\text{ V}$ , $I_O = 5\text{ mA}$			250	
$I_{(kg(OD))}$	Open-drain output leakage-current	$V_{DD} = 1.8\text{ V}$ and $18\text{ V}$ , $V_O = V_{DD}$			300	nA
		$V_{DD} = 1.8\text{ V}$ , $V_O = 18\text{ V}$			300	
$I_{DD}$	Supply current	$V_{DD} = 1.8\text{ V}$ , no load		5.5	11	$\mu\text{A}$
		$V_{DD} = 5\text{ V}$		6	13	
		$V_{DD} = 12\text{ V}$		6	13	
		$V_{DD} = 18\text{ V}$		7	13	
	Start-up delay <sup>(2)</sup>			150	450	$\mu\text{s}$
UVLO	Undervoltage lockout <sup>(3)</sup>	$V_{DD}$ falling	1.3		1.7	V

(1) The lowest supply voltage ( $V_{DD}$ ) at which output is active;  $t_{r(VDD)} > 15\ \mu\text{s/V}$ . Below  $V_{(POR)}$ , the output cannot be determined.

(2) During power on,  $V_{DD}$  must exceed  $1.8\text{ V}$  for  $450\ \mu\text{s}$  (max) before the output is in a correct state.

(3) When  $V_{DD}$  falls below UVLO, OUTA is driven low and OUTB goes to high impedance. The outputs cannot be determined below  $V_{(POR)}$ .

## 7.6 Timing Requirements

over operating temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$t_{PHL}$	High-to-low propagation delay <sup>(1)</sup>		18		$\mu\text{s}$
$t_{PLH}$	Low-to-high propagation delay <sup>(1)</sup>		29		$\mu\text{s}$

$V_{DD} = 5\text{ V}$ , 10-mV input overdrive,  $R_P = 10\text{ k}\Omega$ ,  $V_{OH} = 0.9 \times V_{DD}$ ,  $V_{OL} = 400\text{ mV}$ , see 图 7-1

$V_{DD} = 5\text{ V}$ , 10-mV input overdrive,  $R_P = 10\text{ k}\Omega$ ,  $V_{OH} = 0.9 \times V_{DD}$ ,  $V_{OL} = 400\text{ mV}$ , see 图 7-1

(1) High-to-low and low-to-high refers to the transition at the input terminals (INA+ and INB-).

## 7.7 Switching Characteristics

Over operating temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_r$	Output rise time		2.2		$\mu\text{s}$
$t_f$	Output fall time		0.22		$\mu\text{s}$

$V_{DD} = 5\text{ V}$ , 10-mV input overdrive,  $R_P = 10\text{ k}\Omega$ ,  $V_O = (0.1\text{ to }0.9) \times V_{DD}$

$V_{DD} = 5\text{ V}$ , 10-mV input overdrive,  $R_P = 10\text{ k}\Omega$ ,  $V_O = (0.1\text{ to }0.9) \times V_{DD}$

## 7.8 Timing Diagrams

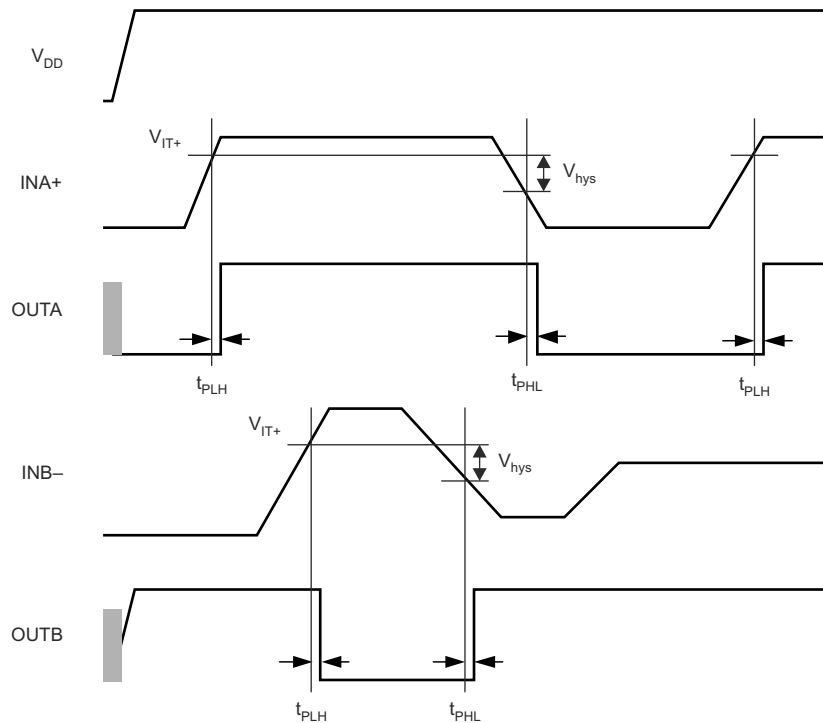


图 7-1. Timing Diagram

### 7.9 Typical Characteristics

at  $T_J = 25^\circ\text{C}$  and  $V_{DD} = 5\text{ V}$  (unless otherwise noted)

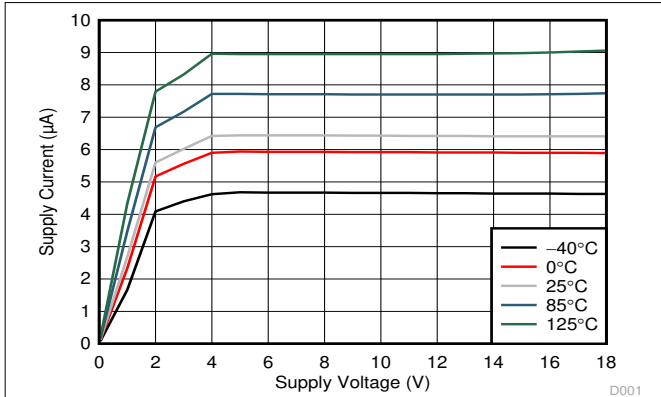


图 7-2. Supply Current ( $I_{DD}$ ) vs Supply Voltage ( $V_{DD}$ )

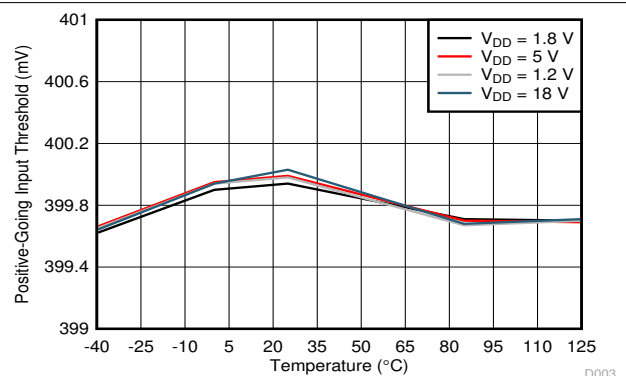


图 7-3. Rising Input Threshold Voltage ( $V_{IT+}$ ) vs Temperature

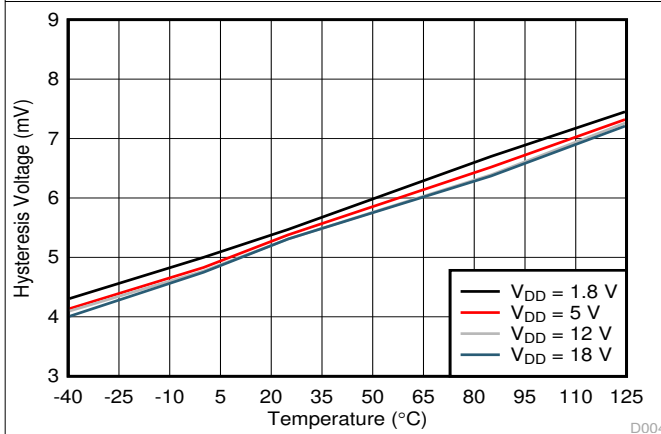


图 7-4. Hysteresis ( $V_{hys}$ ) vs Temperature

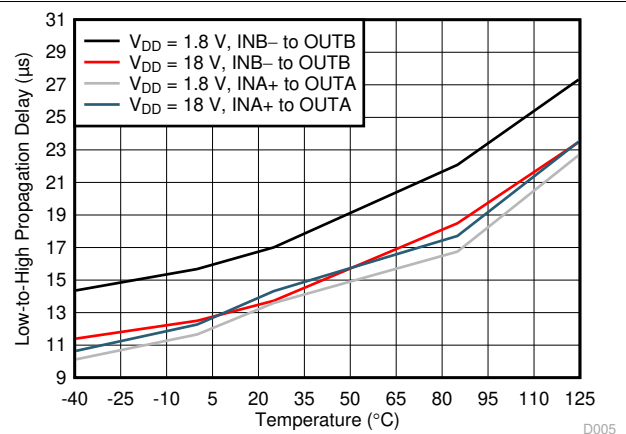


图 7-5. Propagation Delay vs Temperature (High-to-Low Transition at the Inputs)

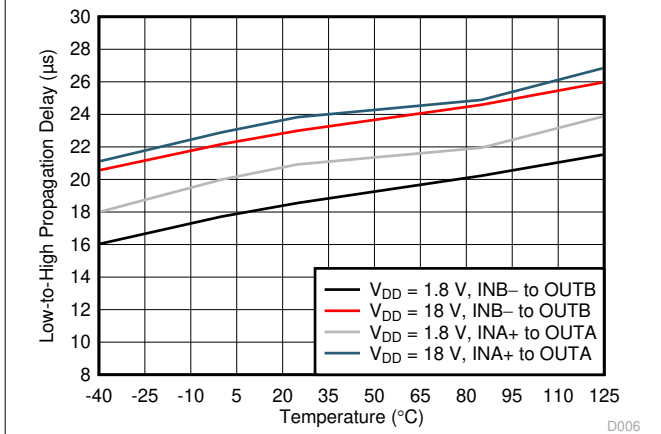


图 7-6. Propagation Delay vs Temperature (Low-to-High Transition at the Inputs)

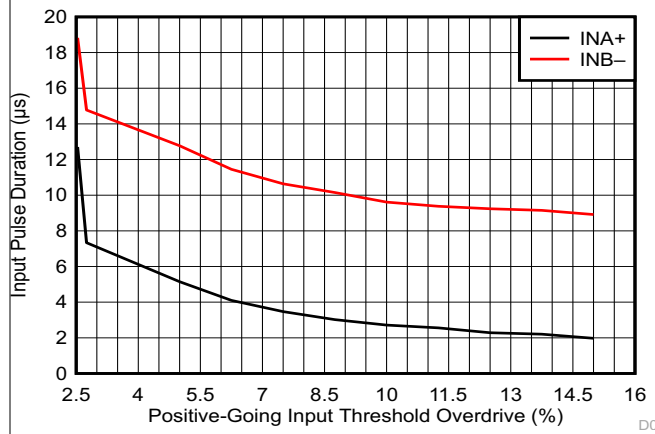


图 7-7. Minimum Pulse Duration vs Threshold Overdrive Voltage

INA+ = negative spike below  $V_{IT-}$   
INB- = positive spike above  $V_{IT+}$



## 7.9 Typical Characteristics (continued)

at  $T_J = 25^\circ\text{C}$  and  $V_{DD} = 5\text{ V}$  (unless otherwise noted)

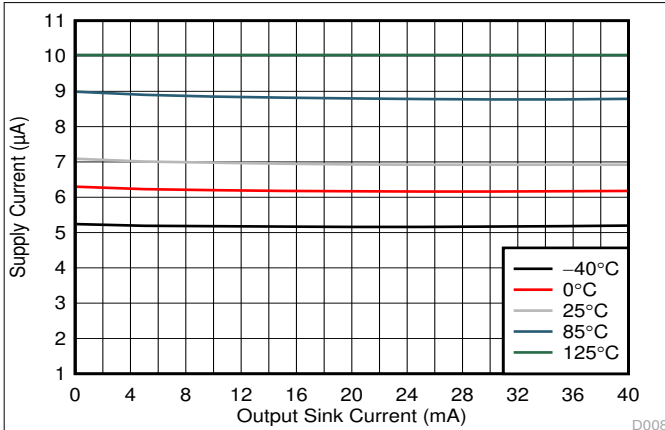


图 7-8. Supply Current ( $I_{DD}$ ) vs Output Sink Current

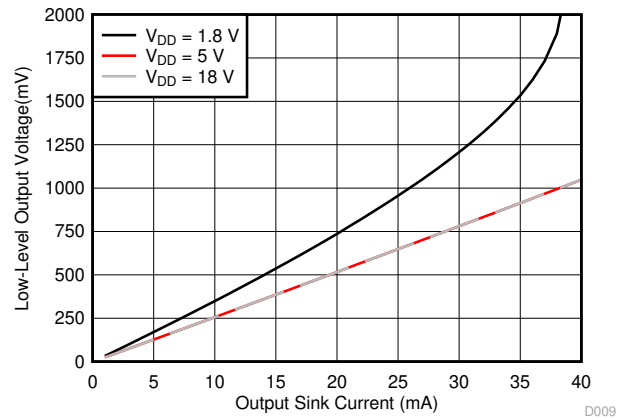


图 7-9. Output Voltage Low ( $V_{OL}$ ) vs Output Sink Current ( $-40^\circ\text{C}$ )

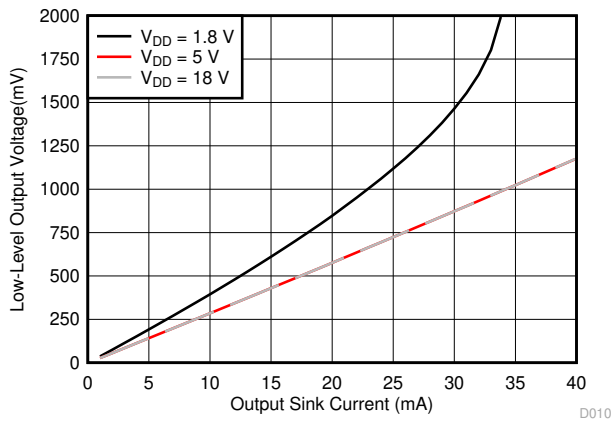


图 7-10. Output Voltage Low ( $V_{OL}$ ) vs Output Sink Current ( $0^\circ\text{C}$ )

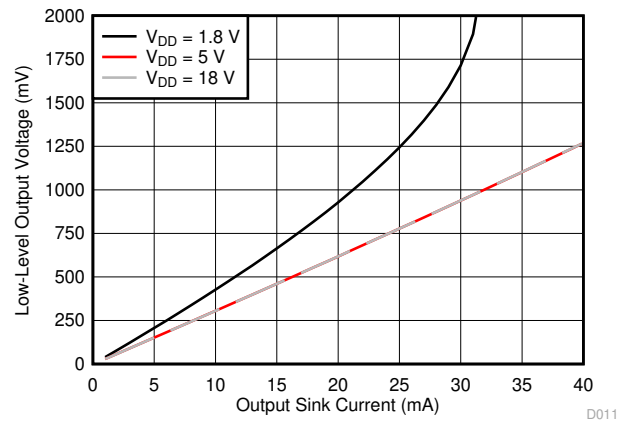


图 7-11. Output Voltage Low ( $V_{OL}$ ) vs Output Sink Current ( $25^\circ\text{C}$ )

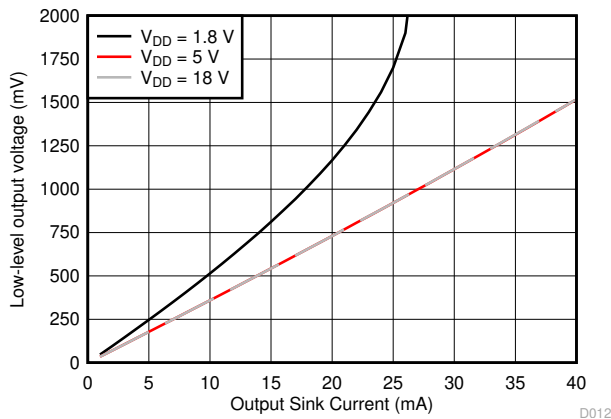


图 7-12. Output Voltage Low ( $V_{OL}$ ) vs Output Sink Current ( $85^\circ\text{C}$ )

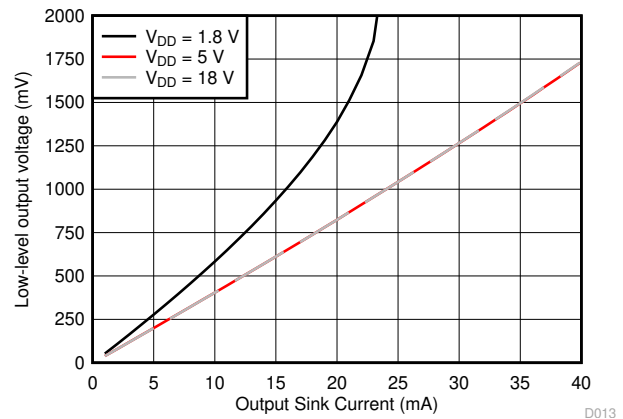


图 7-13. Output Voltage Low ( $V_{OL}$ ) vs Output Sink Current ( $125^\circ\text{C}$ )

## 8 Detailed Description

### 8.1 Overview

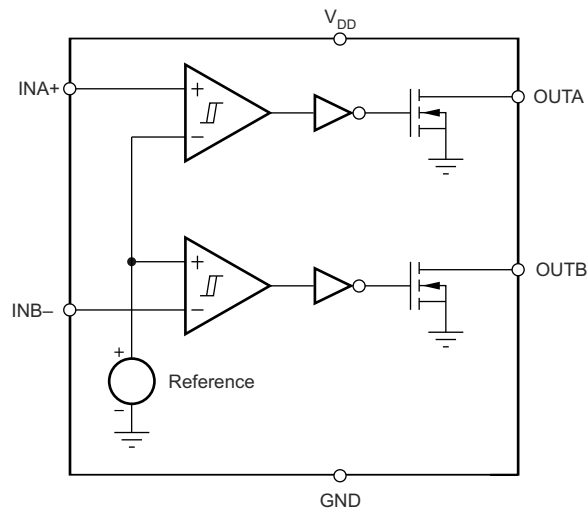
The TLV6700-Q1 device combines two comparators for overvoltage and undervoltage detection. The TLV6700-Q1 has a wide-supply voltage range (1.8 V to 18 V) with a high-accuracy rising-input threshold of 400 mV (1% over temperature) and built-in hysteresis. The outputs are also rated to 18 V, independent of supply voltage, and can sink up to 40 mA.

The TLV6700-Q1 is designed to assert the output signals, as shown in 表 8-1. Each input terminal can be set to monitor any voltage above 0.4 V using an external resistor divider network. Each input pin has very low input leakage current, allowing the use of large resistor dividers without sacrificing system accuracy. With the use of two input terminals of different polarities, the TLV6700-Q1 forms a window comparator. The relationship between the inputs and the outputs is shown in 表 8-1. Broad voltage thresholds can be supported that allow the device to be used in a wide array of applications.

表 8-1. TLV6700 Truth Table

CONDITION	OUTPUT	OUTPUT STATE
$INA+ > V_{IT+}$	OUTA high	Output A high impedance
$INA+ < V_{IT-}$	OUTA low	Output A sinking
$INB- > V_{IT+}$	OUTB low	Output B sinking
$INB- < V_{IT-}$	OUTB high	Output B high impedance

### 8.2 Functional Block Diagram



### 8.3 Feature Description

#### 8.3.1 Inputs (INA+, INB - )

The TLV6700-Q1 device combines two comparators. Each comparator has one external input (inverting and noninverting); the other input is connected to the internal reference. The comparator rising threshold is designed and trimmed to be equal to the reference voltage (400 mV). Both comparators also have a built-in falling hysteresis that makes the device less sensitive to supply rail noise and ensures stable operation.

The comparator inputs can swing from ground to 6.5 V, regardless of the device supply voltage used. Although not required in most cases, good analog design practice is to place a 1-nF to 10-nF bypass capacitor at the comparator input for extremely noisy applications to reduce sensitivity to transients and layout parasitics.

For comparator A, the corresponding output (OUTA) is driven to logic low when the input INA+ voltage drops below  $(V_{IT+} - V_{hys})$ . When the voltage exceeds  $V_{IT+}$ , the output (OUTA) goes to a high-impedance state; see 图 7-1.

For comparator B, the corresponding output (OUTB) is driven to logic low when the voltage at input INB - exceeds  $V_{IT+}$ . When the voltage drops below  $V_{IT+} - V_{hys}$  the output (OUTB) goes to a high-impedance state; see 图 7-1. Together, these comparators form a window-detection function as discussed in the 节 8.3.3 section.

### 8.3.2 Outputs (OUTA, OUTB)

In a typical TLV6700-Q1 application, the outputs are connected to a GPIO input of the processor (such as a digital signal processor [DSP], central processing unit [CPU], field-programmable gate array [FPGA], or application-specific integrated circuit [ASIC]).

The TLV6700-Q1 device provides two open-drain outputs (OUTA and OUTB). Pullup resistors must be used to hold these lines high when the output goes to high impedance (not asserted). By connecting pullup resistors to the proper voltage rails, the outputs can be connected to other devices at the correct interface-voltage levels. The TLV6700-Q1 outputs can be pulled up to 18 V, independent of the device supply voltage. By using wired-OR logic, OUTA and OUTB can merge into one logic signal that goes low if either outputs are asserted because of a fault condition.

表 8-1 and the 节 8.3.1 section describe how the outputs are asserted or deasserted. See 图 7-1 for a timing diagram that describes the relationship between threshold voltages and the respective output.

### 8.3.3 Window Comparator

The inverting and noninverting configuration of the comparators forms a window-comparator detection circuit using a resistor divider network, as illustrated in 图 8-1 and 图 8-2. The input terminals can monitor any system voltage above 400 mV with the use of a resistor divider network. The INA+ and INB - terminals monitor for undervoltage and overvoltage conditions, respectively.

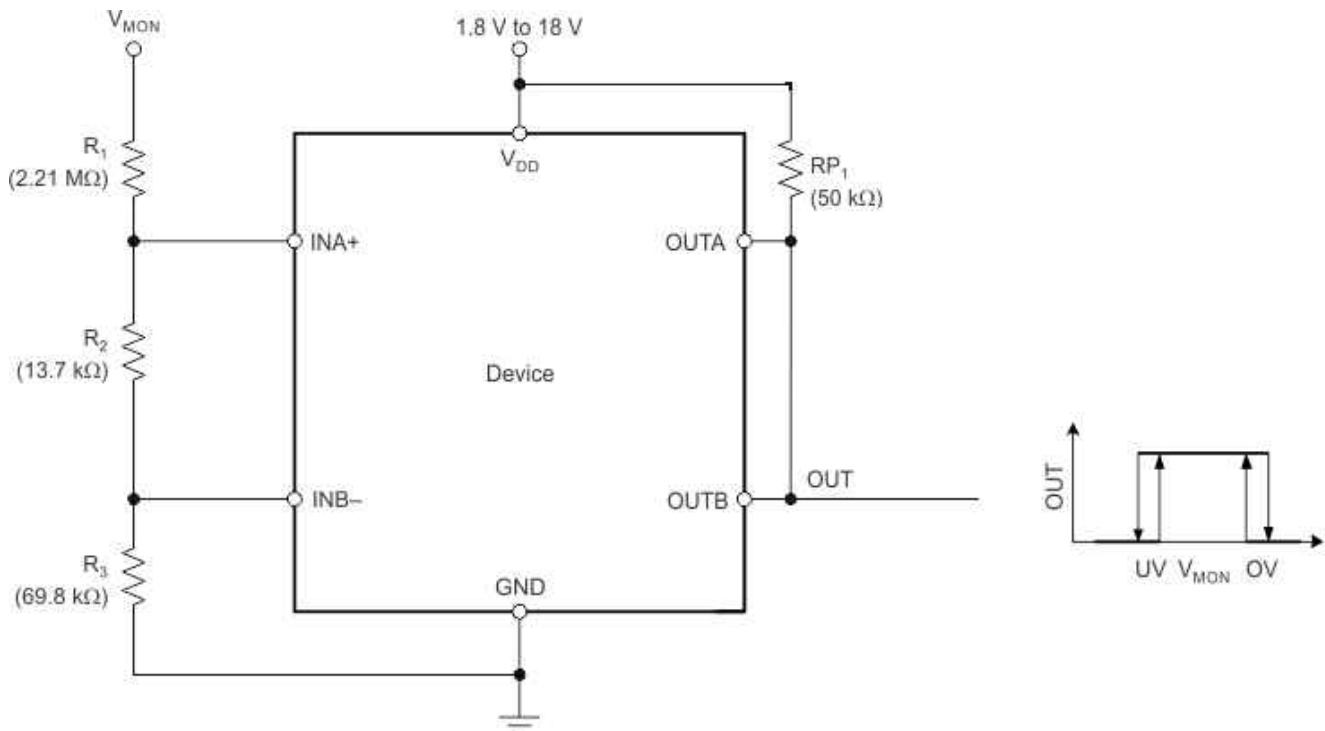


图 8-1. Window Comparator Block Diagram

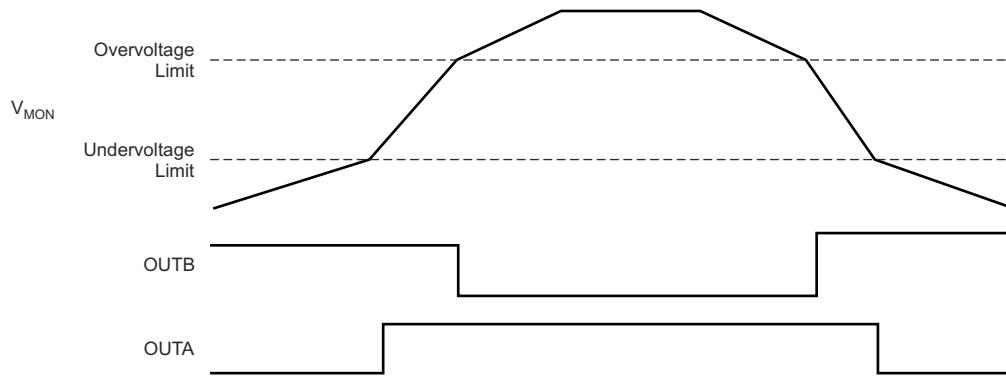


图 8-2. Window Comparator Timing Diagram

### 8.3.4 Immunity to Input Terminal Voltage Transients

The TLV6700-Q1 device is relatively immune to short voltage transient spikes on the input terminals. Sensitivity to transients depends on both transient duration and amplitude; see the *Minimum Pulse Duration vs Threshold Overdrive Voltage* curve (图 7-7) in the 节 7.9 section.

## 8.4 Device Functional Modes

### 8.4.1 Normal Operation ( $V_{DD} > UVLO$ )

When the voltage on  $V_{DD}$  is greater than 1.8 V for at least 150  $\mu$ s, the OUTA and OUTB signals correspond to the voltage on INA+ and INB – as listed in 表 8-1.

### 8.4.2 Undervoltage Lockout ( $V_{(POR)} < V_{DD} < UVLO$ )

When the voltage on  $V_{DD}$  is less than the device UVLO voltage, and greater than the power-on reset voltage,  $V_{(POR)}$ , the OUTA and OUTB signals are asserted and high impedance, respectively, regardless of the voltage on INA+ and INB –.

### 8.4.3 Power-On Reset ( $V_{DD} < V_{(POR)}$ )

When the voltage on  $V_{DD}$  is lower than the required voltage to internally pull the asserted output to GND ( $V_{(POR)}$ ), both outputs are in a high-impedance state.

## 9 Application and Implementation

### 备注

以下应用部分的信息不属于 TI 组件规范，TI 不担保其准确性和完整性。客户应负责确定 TI 组件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

### 9.1 Application Information

The TLV6700-Q1 device is a wide-supply voltage window comparator that operates over a  $V_{DD}$  range of 1.8 V to 18 V. The device has two high-accuracy comparators with an internal 400-mV reference and two open-drain outputs rated to 18 V for overvoltage and undervoltage detection. The device can be used either as a window comparator or as two independent voltage monitors. The monitored voltages are set with the use of external resistors.

#### 9.1.1 $V_{PULLUP}$ to a Voltage Other Than $V_{DD}$

The outputs are often tied to  $V_{DD}$  through a resistor. However, some applications may require the outputs to be pulled up to a higher or lower voltage than  $V_{DD}$  to correctly interface with the input terminals of other devices.

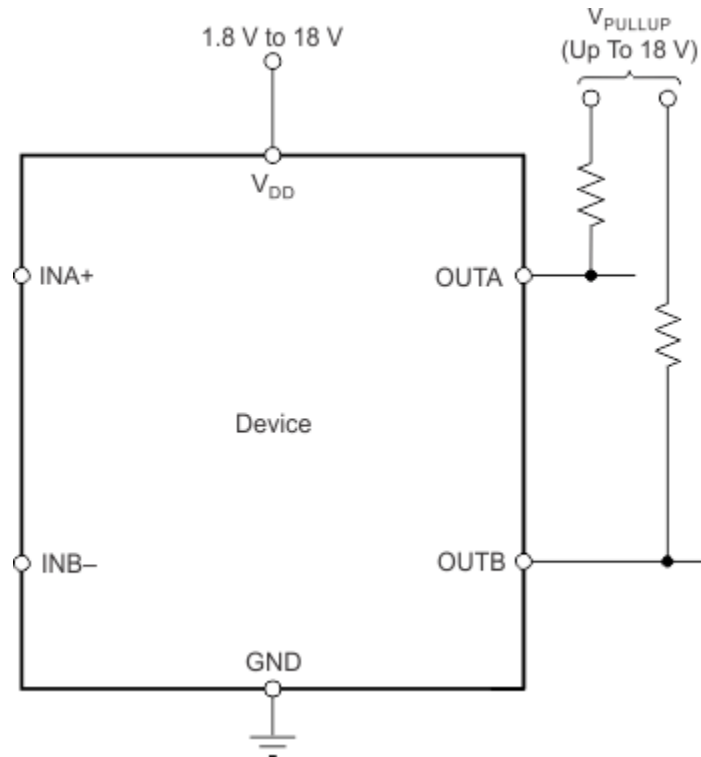


图 9-1. Interfacing to Voltages Other Than  $V_{DD}$

### 9.1.2 Monitoring $V_{DD}$

Many applications monitor the same rail that is powering  $V_{DD}$ . In these applications the resistor divider is simply connected to the  $V_{DD}$  rail.

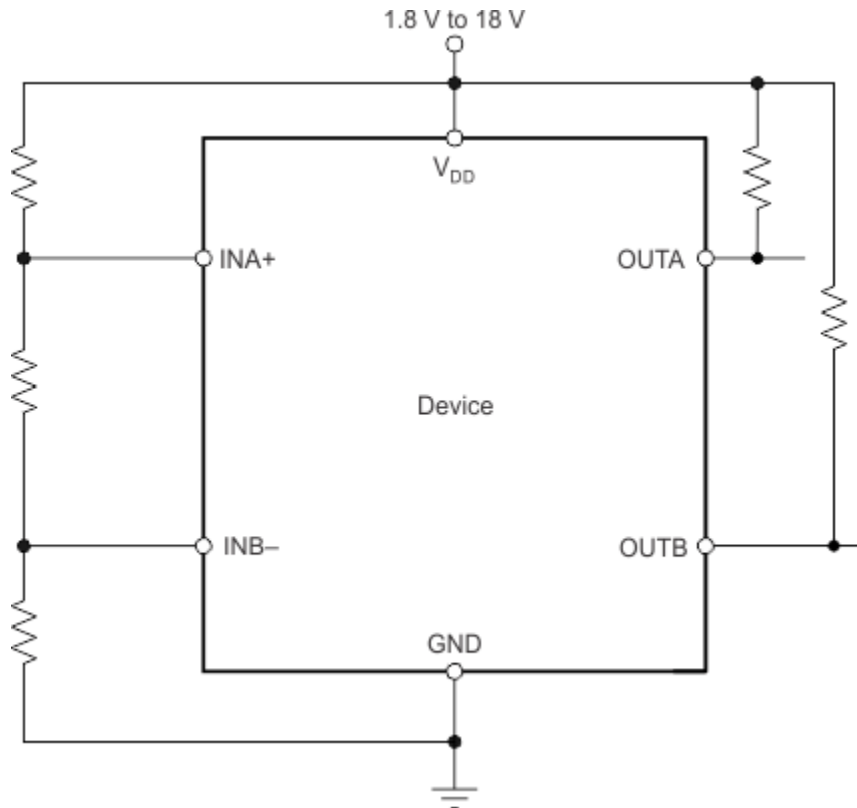
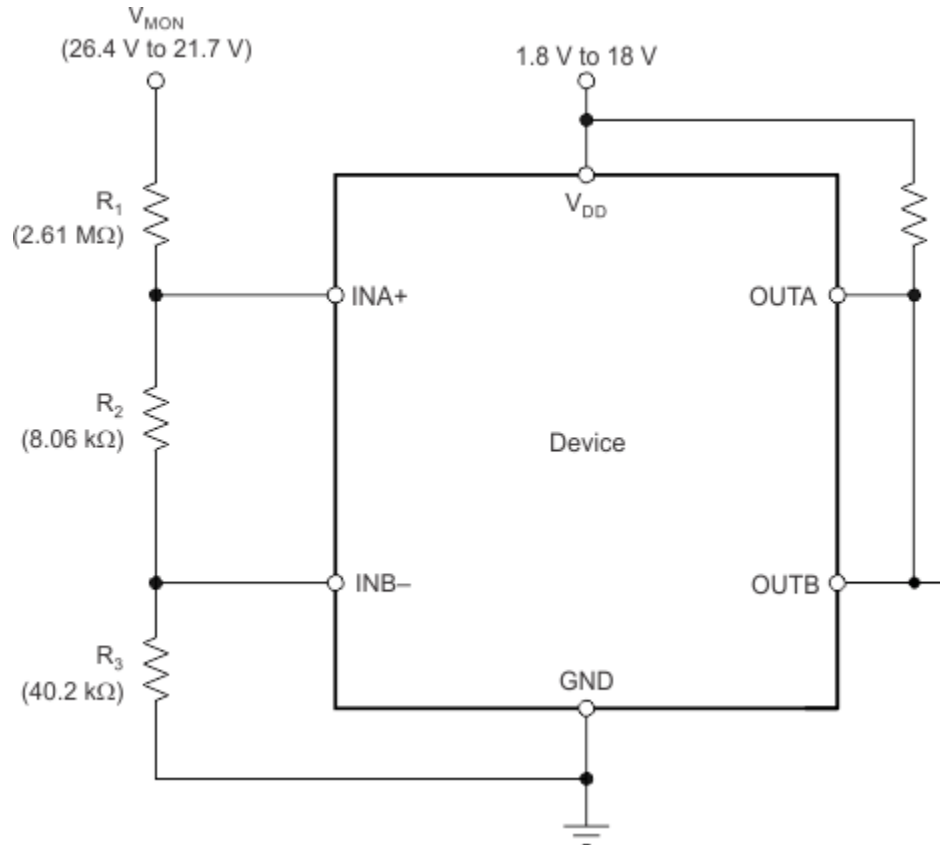


图 9-2. Monitoring the Same Voltage as  $V_{DD}$

### 9.1.3 Monitoring a Voltage Other Than $V_{DD}$

Some applications monitor rails other than the one that is powering  $V_{DD}$ . In these types of applications the resistor divider used to set the desired thresholds is connected to the rail that is being monitored.



The inputs can monitor a voltage higher than  $V_{DDmax}$  with the use of an external resistor divider network.

**图 9-3. Monitoring a Voltage Other Than  $V_{DD}$**

## 9.2 Typical Application

The TLV6700-Q1 device is a wide-supply voltage window comparator that operates over a  $V_{DD}$  range of 1.8 to 18 V. The monitored voltages are set with the use of external resistors, so the device can be used either as a window comparator or as two independent overvoltage and undervoltage monitors.

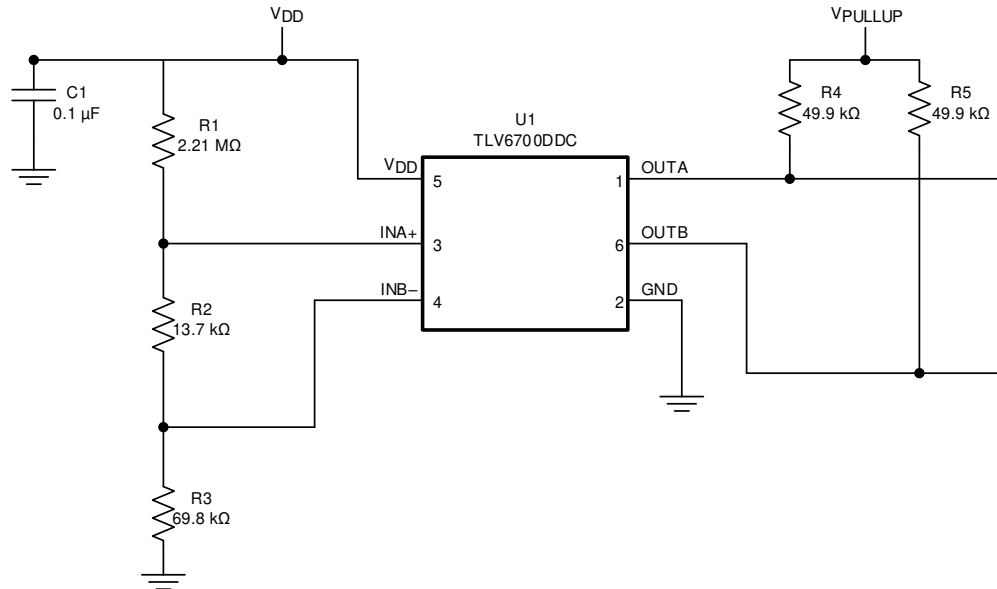


图 9-4. Typical Application Schematic

### 9.2.1 Design Requirements

For this design example, use the values summarized in 表 9-1 as the input parameters.

表 9-1. Design Parameters

PARAMETER	DESIGN REQUIREMENT	DESIGN RESULT
Monitored voltage	12-V nominal rail with maximum rising and falling thresholds of $\pm 10\%$	$V_{MON(UV)} = 10.99 \text{ V (8.33\%)} \pm 2.94\%$ , $V_{MON(OV)} = 13.14 \text{ V (8.33\%)} \pm 2.94\%$

### 9.2.2 Detailed Design Procedure

#### 9.2.2.1 Resistor Divider Selection

Use 方程式 1 through 方程式 4 to calculate the resistor divider values and target threshold voltages.

$$R_T = R_1 + R_2 + R_3 \quad (1)$$

Select a value for  $R_T$  such that the current through the divider is approximately 100 times higher than the input current at the INA+ and INB - terminals. The resistors can have high values to minimize current consumption as a result of low-input bias current without adding significant error to the resistive divider. See the application note *Optimizing Resistor Dividers at a Comparator Input (SLVA450)* for details on sizing input resistors.

Use 方程式 2 to calculate the value of  $R_3$ .

$$R_3 = \frac{R_T}{V_{MON(OV)}} \times V_{IT+} \quad (2)$$

where:

$V_{MON(OV)}$  is the target voltage at which an overvoltage condition is detected



Use 方程式 3 或 方程式 4 to calculate the value of  $R_2$ .

$$R_2 = \left[ \frac{R_T}{V_{MON(\text{no UV})}} \times V_{IT+} \right] - R_3 \quad (3)$$

where:

$V_{MON(\text{no UV})}$  is the target voltage at which an undervoltage condition is removed as  $V_{MON}$  rises

$$R_2 = \left[ \frac{R_T}{V_{MON(\text{UV})}} \times (V_{IT+} - V_{\text{hys}}) \right] - R_3 \quad (4)$$

where:

$V_{MON(\text{UV})}$  is the target voltage at which an undervoltage condition is detected

The worst-case tolerance can be calculated by referring to Equation 13 in application report [SLVA450, Optimizing Resistor Dividers at a Comparator Input](#) (available for download at [www.ti.com](http://www.ti.com)). An example of the rising threshold error,  $V_{MON(\text{OV})}$ , is given in 方程式 5.

$$\% \text{ ACC} = \% \text{ TOL}(V_{IT+(\text{INB})}) + 2 \times \left[ 1 - \frac{V_{IT+(\text{INB})}}{V_{MON(\text{OV})}} \right] \times \% \text{ TOL}_R = 1\% + 2 \times \left[ 1 - \frac{0.4}{13.2} \right] \times 1\% = 2.94\% \quad (5)$$

### 9.2.2.2 Pullup Resistor Selection

To ensure proper voltage levels, the pullup resistor value is selected by ensuring that the pullup voltage divided by the resistor does not exceed the sink-current capability of the device. This confirmation is calculated by verifying that the pullup voltage minus the output-leakage current ( $I_{\text{kg}(\text{OD})}$ ) multiplied by the resistor is greater the desired logic-high voltage. These values are specified in the [表 7.5](#) table.

Use 方程式 6 to calculate the value of the pullup resistor.

$$\frac{(V_{\text{HI}} - V_{\text{PU}})}{I_{\text{kg}(\text{OD})}} \geq R_{\text{PU}} \geq \frac{V_{\text{PU}}}{I_{\text{O}}} \quad (6)$$

### 9.2.2.3 Input Supply Capacitor

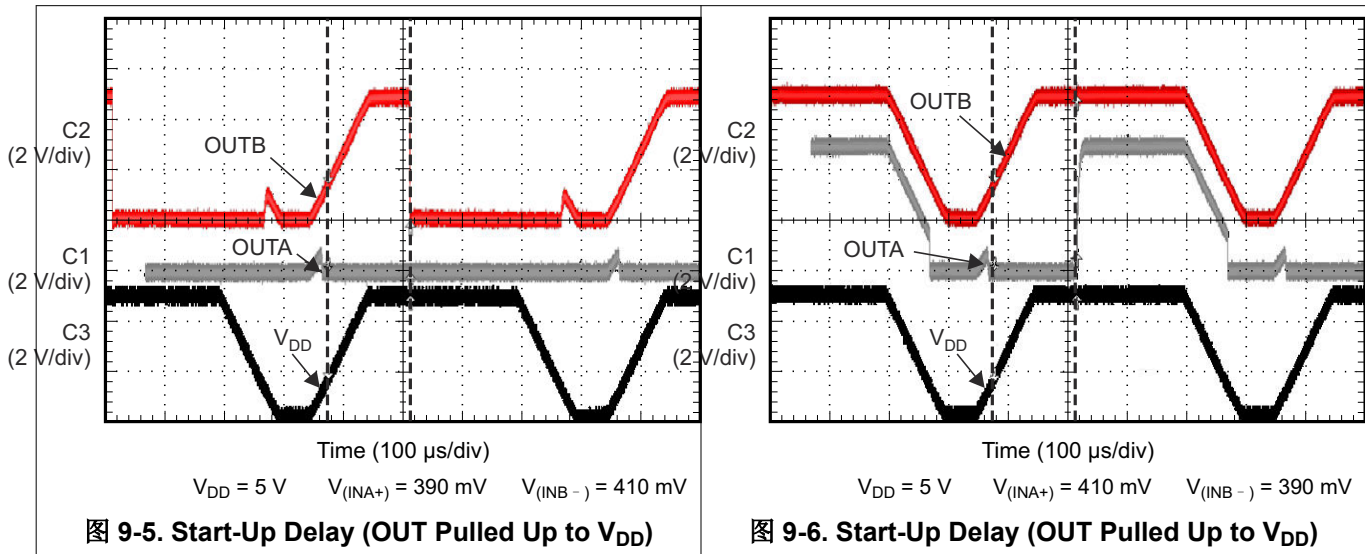
Although an input capacitor is not required for stability, connecting a 0.1- $\mu\text{F}$  low equivalent series resistance (ESR) capacitor across the  $V_{\text{DD}}$  terminal and GND terminal is good analog design practice. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated, or if the device is not located close to the power source.

### 9.2.2.4 Input Capacitors

Although not required in most cases, for extremely noisy applications, placing a 1-nF to 10-nF bypass capacitor from the comparator inputs (INA+, INB - ) to the GND terminal is good analog design practice. This capacitor placement reduces device sensitivity to transients.

### 9.2.3 Application Curves

At  $T_J = 25^\circ\text{C}$



### 9.3 Do's and Don'ts

It is good analog design practice to have a 0.1- $\mu\text{F}$  decoupling capacitor from  $V_{DD}$  to GND.

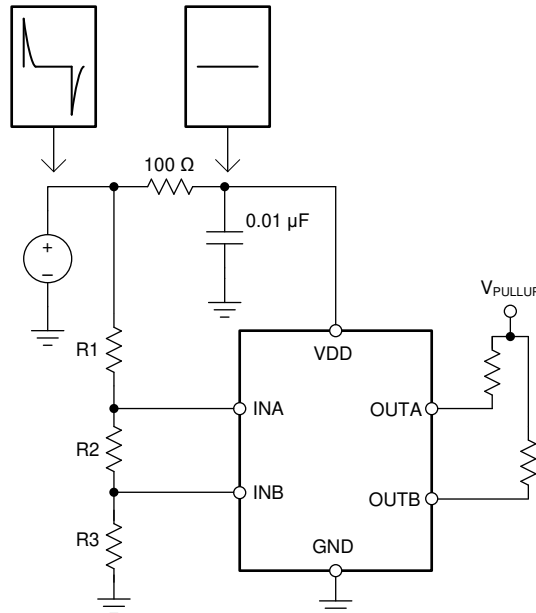
If the monitored rail is noisy, connect decoupling capacitors from the comparator inputs to GND.

Do not use resistors for the voltage divider that cause the current through them to be less than 100 times the input current of the comparators without also accounting for the effect to the accuracy.

Do not use pullup resistors that are too small, because the larger current sunk by the output then exceeds the desired low-level output voltage ( $V_{OL}$ ).

## 10 Power Supply Recommendations

The TLV6700-Q1 has a 20 V absolute maximum rating on the VDD pin, with a recommended operating condition of 18V. If the voltage supply that is providing power to VDD is susceptible to any large voltage transient that may exceed 20 V, or if the supply exhibits high voltage slew rates greater than 1 V/ $\mu$ s, take additional precautions. Place an RC filter between the supply and VDD to filter any high-frequency transient surges on the VDD pin. A 100- $\Omega$  resistor and 0.01- $\mu$ F capacitor is required in these cases, as shown in [图 10-1](#).



**图 10-1. Using an RC Filter to Remove High-Frequency Disturbances on VDD**

## 11 Layout

### 11.1 Layout Guidelines

Placing a 0.1- $\mu$ F capacitor close to the  $V_{DD}$  terminal to reduce the input impedance to the device is good analog design practice. The pullup resistors can be separated if separate logic functions are needed (as shown in [Figure 11-1](#)) or both resistors can be tied to a single pullup resistor if a logical AND function is desired.

### 11.2 Layout Example

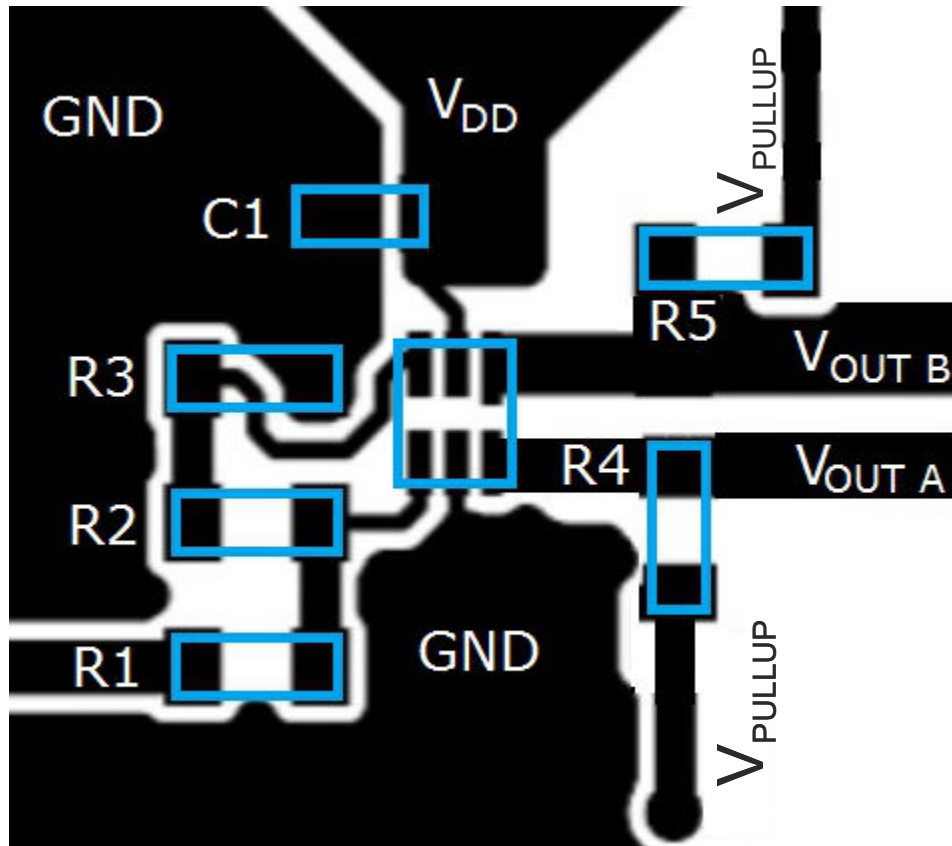


图 11-1. TLV6700 Layout Schematic

## 12 Device and Documentation Support

### 12.1 Device Support

#### 12.1.1 Development Support

The [DIP Adapter Evaluation Module](#) allows conversion of the SOT-23-6 package to a standard DIP-6 pinout for ease of prototyping and bench evaluation.

### 12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 12.3 支持资源

[TI E2E™ 支持论坛](#)是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《[使用条款](#)》。

### 12.4 Trademarks

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ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 12.6 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV6700QDDCRQ1	ACTIVE	SOT-23-THIN	DDC	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2D11	<a href="#">Samples</a>
TLV6700QDSESRQ1	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	K6	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

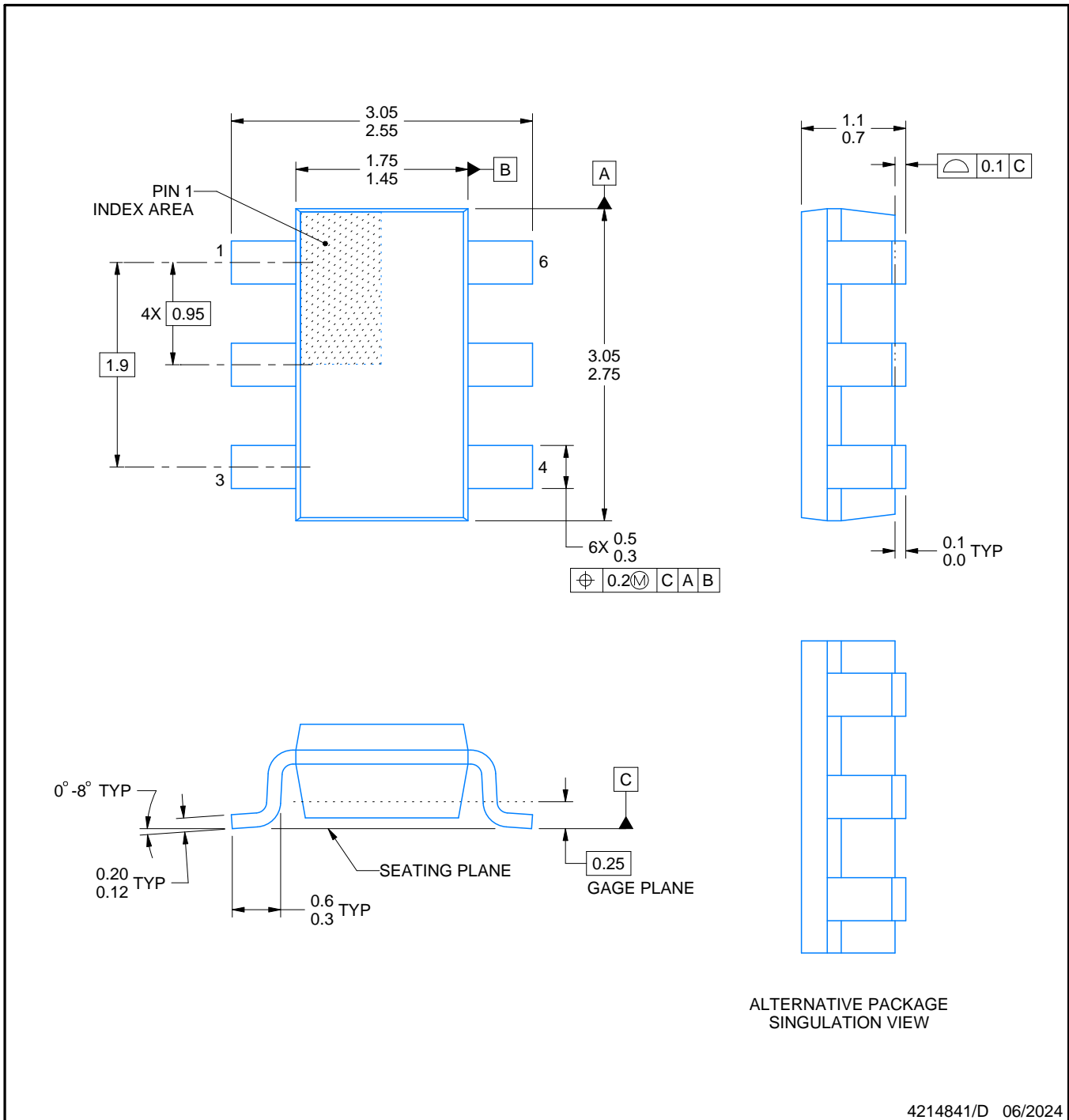
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV6700QDDCRQ1	SOT-23-THIN	DDC	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV6700QDSERQ1	WSON	DSE	6	3000	180.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2



**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV6700QDDCRQ1	SOT-23-THIN	DDC	6	3000	213.0	191.0	35.0
TLV6700QDSERQ1	WSON	DSE	6	3000	213.0	191.0	35.0



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NOTES:

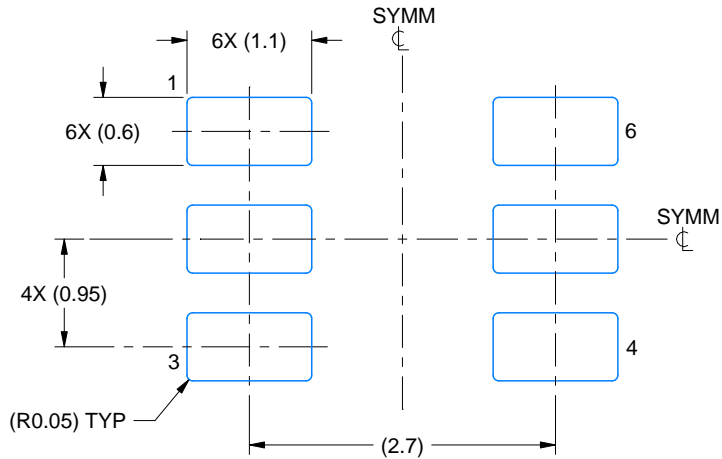
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.

# EXAMPLE BOARD LAYOUT

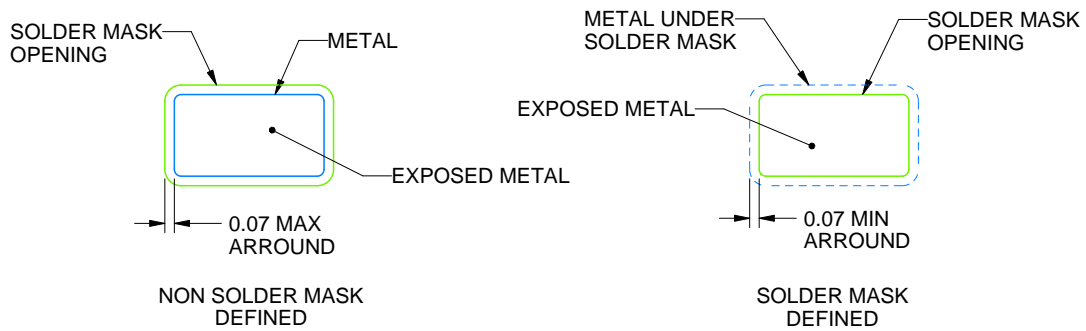
DDC0006A

SOT-23 - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPLODED METAL SHOWN  
SCALE:15X



SOLDEMASK DETAILS

4214841/D 06/2024

NOTES: (continued)

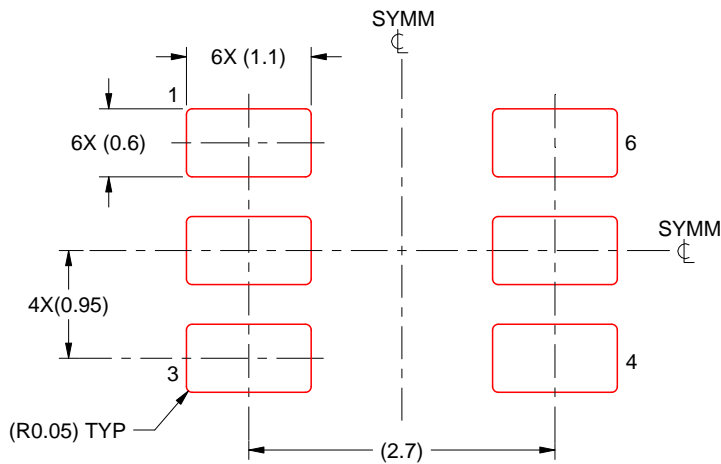
- 4. Publication IPC-7351 may have alternate designs.
- 5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DDC0006A

SOT-23 - 1.1 max height

SMALL OUTLINE TRANSISTOR

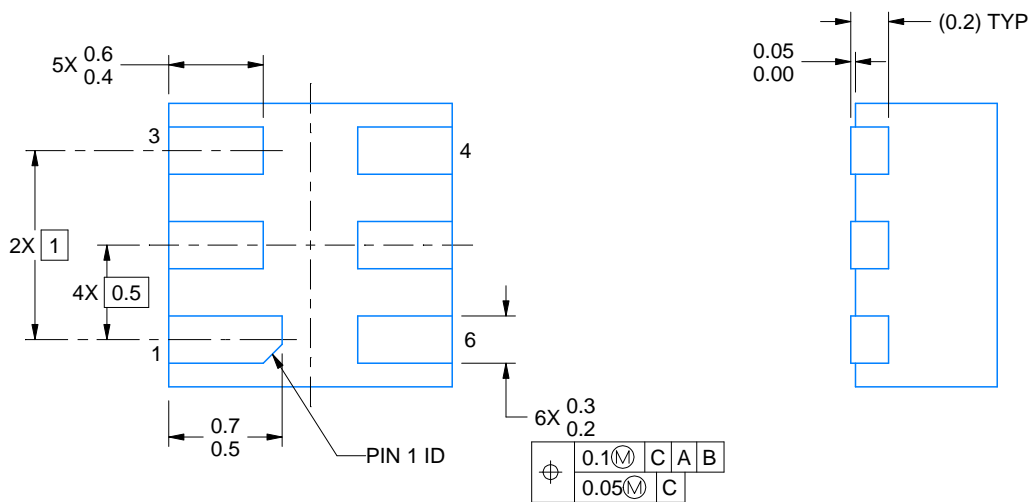
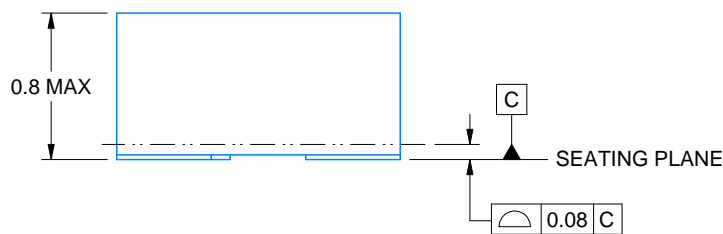
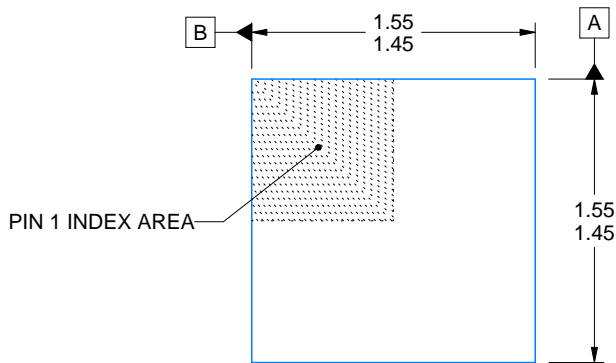


SOLDER PASTE EXAMPLE  
BASED ON 0.125 THICK STENCIL  
SCALE:15X

4214841/D 06/2024

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.



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NOTES:

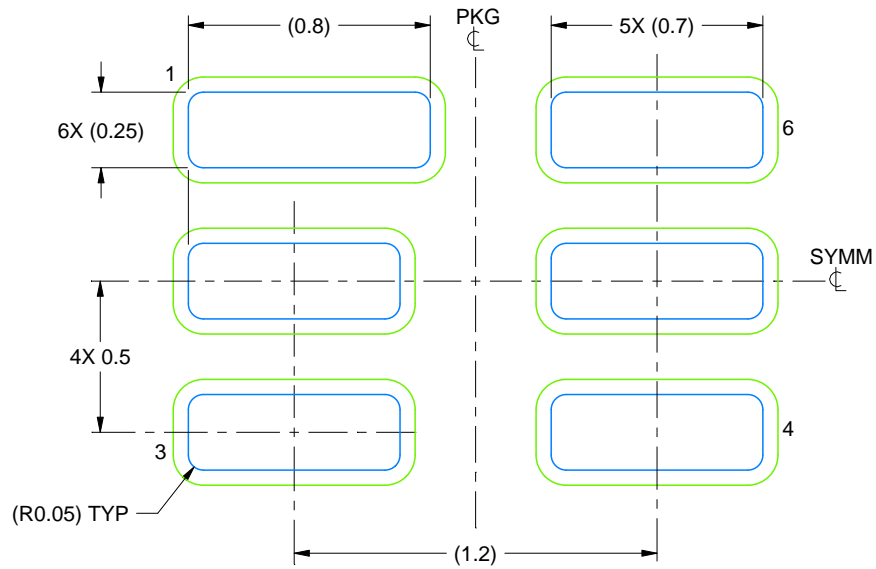
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

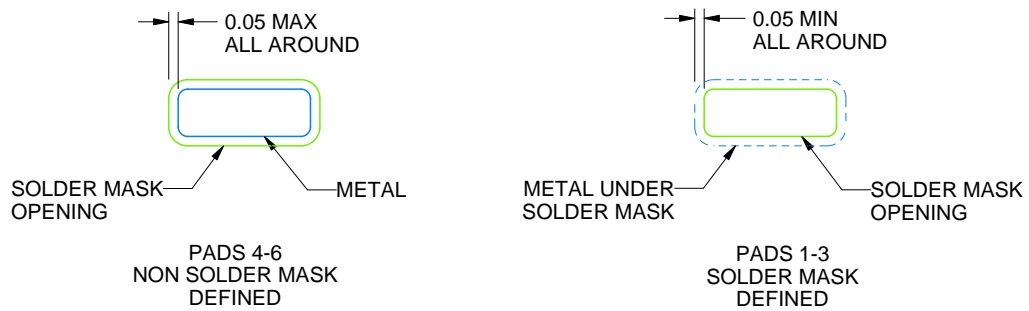
DSE0006A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
SCALE:40X



SOLDER MASK DETAILS

4220552/B 01/2024

NOTES: (continued)

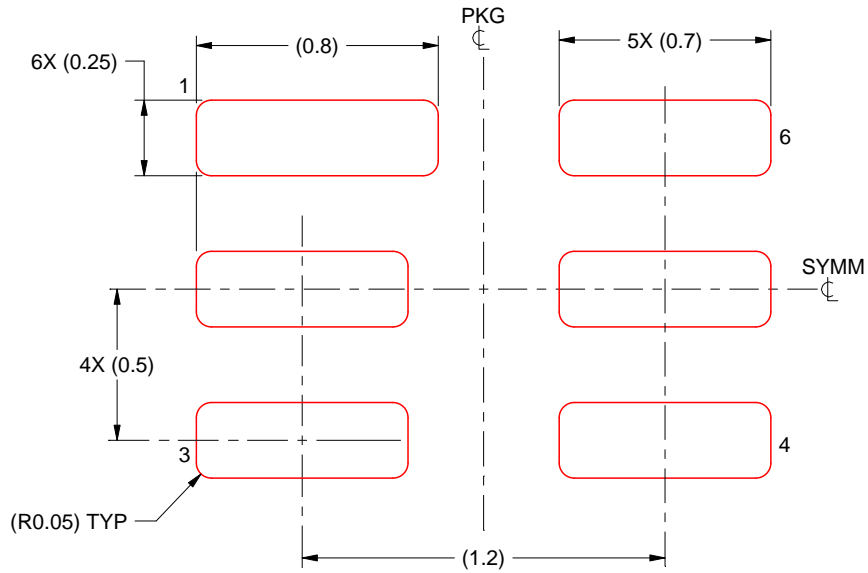
3. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/slua271](http://www.ti.com/lit/slua271)).

# EXAMPLE STENCIL DESIGN

DSE0006A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:40X

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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