具有超低 EMI 的 TPA3137D2 6W 无电感器立体声 (BTL) D 类音频放大器

1 特性

- 电源电压为 12V、总谐波失真 + 噪声 (THD+N) 为 10%、负载为 6Ω 时的功率为 2 × 6W/通道
- 电源电压为 13V、总谐波失真 + 噪声 (THD+N) 为 10%、负载为 8Ω 时的功率为 2 × 6W/通道
- 高达 90% 的高效 D 类运行（负载为 8Ω），无需散热器
- 1W/4Ω/1kHz 时的 THD+N < 0.05%
- 宽电源电压范围允许在 4.5V至 14.4V 范围内运行
- 无电感运行
- EMI 性能增强，具备扩展频谱
- SpeakerGuard™扬声器保护包括功率限制器和直流保护
- 可靠的引脚至引脚、引脚接地以及引脚至电源短路保护和热保护
- 26dB 固定增益
- 单端或差分模拟输入
- 启动时无喀哒声和噼啪声

2 应用

- 电视
- 蓝牙/无线扬声器
- 迷你扬声器
- USB 扬声器
- 消费类音频设备

3 说明

TPA3137D2 器件是一款高效 D 类音频功率放大器，适用于以高达 6W 的功率驱动阻抗为 6Ω 或 8Ω（每通道）的桥接式立体声扬声器。

借助采用扩展频谱控制方案的高级 EMI 抑制技术，既能实现在输出端使用成本较低的铁氧体磁珠滤波器，同时能够满足 EMC 要求，降低了系统成本。
TPA3137D2 器件不仅针对短路和过载提供全面的保护，而且 SpeakerGuard™扬声器保护电路包括一个功率限制器和一个直流检测电路，可以保护所连接的扬声器。直流检测及引脚至引脚、引脚接地和引脚至电源短路保护电路可以防止扬声器在生产过程中发生输出直流和引脚短路。同时充分保护输出，防止 GND、PVCC、输出至输出短路。短路保护和热保护具有自动恢复功能。

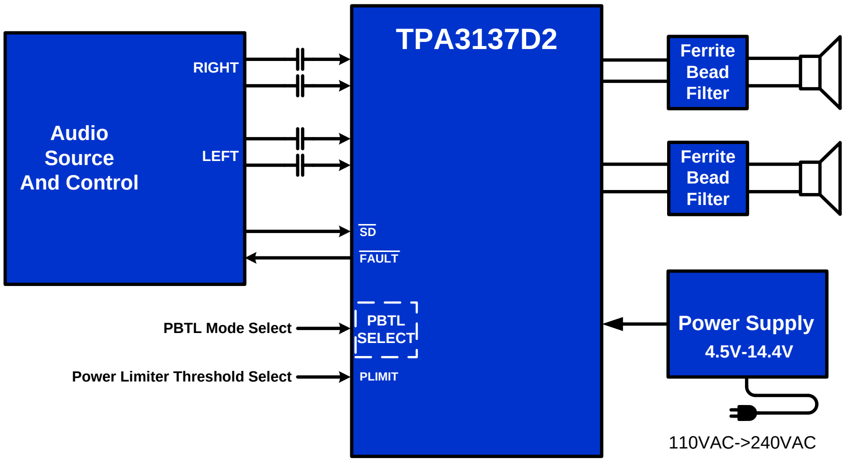
TPA3137D2 器件可驱动阻抗低至 4Ω 的立体声扬声器。TPA3137D2 的效率在负载为 8Ω 时高达 90%，无需外部散热器，而且 TPA3137D2 将在双层印刷电路板 (PCB) 上实现全功率输出。

器件信息[(1)]

器件型号	封装	封装尺寸（标称值）
TPA3137D2	HTSSOP (28)	9.70mm × 4.40mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。

简化原理图



English Data Sheet: SLOS956

目录

4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision A (June 2016) to Revision B **Page**

- Changed the Supply Voltage (AVCC to GND, PVCC to GND) MAX value From: 16 V To: 20 V in the *Absolute Maximum Ratings* 5

Changes from Original (June 2016) to Revision A **Page**

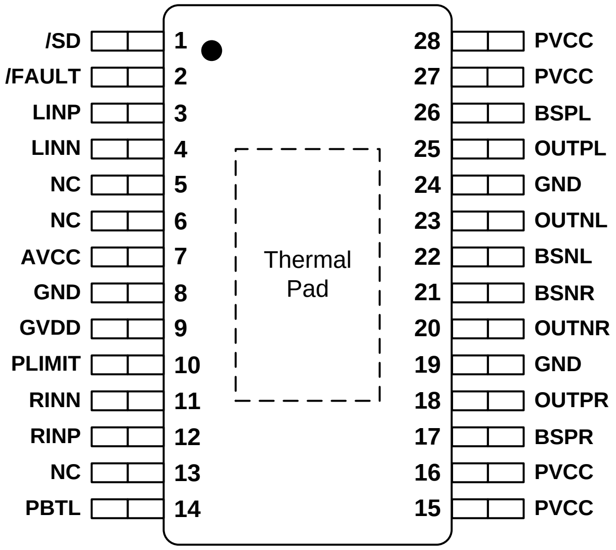
- 已更改 “2 × 8W/通道”至“2 × 6W/通道”（6Ω 负载） 特性 1
- 已更改 8W 至 6W（ 说明）。 1
- Updated Thermal Characteristics 6

5 Device Comparison Table

DEVICE NAME	DESCRIPTION
TPA3113D2	6-W Filter-Free Class-D Stereo Amplifier with SpeakerGuard™
TPA3144D2	6-W Inductor-Free Class-D Stereo Amplifier with Ultra Low EMI and AGL

6 Pin Configuration and Functions

PWP Package
28-Pin HTSSOP
(Top View)



Pin Functions

PIN		I/O/P[1]	DESCRIPTION
NAME	NUMBER		
$\overline{\text{SD}}$	1	I	Shutdown logic input for audio amp (LOW = outputs Hi-Z, HIGH = outputs enabled). TTL logic levels with compliance to AVCC.
$\overline{\text{FAULT}}$	2	O	Open drain output used to display short circuit or dc detect fault status. Voltage compliant to AVCC. Short circuit faults can be set to auto-recovery by connecting $\overline{\text{FAULT}}$ pin to $\overline{\text{SD}}$ pin. Otherwise, both short circuit faults and dc detect faults must be reset by cycling PVCC.
LINP	3	I	Positive audio input for left channel. Biased at 3 V.
LINN	4	I	Negative audio input for left channel. Biased at 3 V.
NC	5, 6, 13	I	No Connect Pin. Can be shorted to PVCC or shorted to GND or left open.
AVCC	7	P	Analog supply
GND	8	P	Analog signal ground.
GVDD	9	O	High-side FET gate drive supply. Nominal voltage is 7 V.
PLIMIT	10	I	Power Limiter Control pin
RINN	11	I	Negative audio input for right channel. Biased at 3 V.
RINP	12	I	Positive audio input for right channel. Biased at 3 V.

(1) I = Input, O = Output, P = Power

Pin Functions (continued)

PIN		I/O/P[1]	DESCRIPTION
NAME	NUMBER		
PBTL	14	I	Parallel BTL mode select pin. L=Stereo BTL mode, H=Mono PBTL mode
PVCC	15, 16	P	Power supply for right channel H-bridge. Right channel and left channel power supply inputs are connected internally.
BSPR	17	I	Bootstrap I/O for right channel, positive high-side FET.
OUTPR	18	O	Class-D H-bridge positive output for right channel.
GND	19	P	Power ground for the H-bridges.
OUTNR	20	O	Class-D H-bridge negative output for right channel.
BSNR	21	I	Bootstrap I/O for right channel, negative high-side FET.
BSNL	22	I	Bootstrap I/O for left channel, negative high-side FET.
OUTNL	23	O	Class-D H-bridge negative output for left channel.
GND	24	P	Power ground for the H-bridges.
OUTPL	25	O	Class-D H-bridge positive output for left channel.
BSPL	26	I	Bootstrap I/O for left channel, positive high-side FET.
PVCC	27, 28	P	Power supply for left channel H-bridge. Right channel and left channel power supply inputs are connected internally.
Thermal Pad		P	Connect to GND for best thermal and electrical performance.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage	AVCC to GND, PVCC to GND	–0.3	20	V
Input current	To any pin except supply pins		10	mA
Voltage	$\overline{\text{SD}}$, $\overline{\text{FAULT}}$ to GND(2)	–0.3	AVCC + 0.3	V
			10	V/ms
Voltage	RINN, RINP, LINN, LINP	–0.3	6.3	V
Minimum load resistance, R_L	BTL, PVCC > 12 V	4.8		Ω
	BTL, PVCC ≤ 12 V	3.2		
	PBTL, PVCC > 12 V	2.5		
	PBTL, PVCC ≤ 12 V	1.8		
Continuous total power dissipation		See the Thermal Information Table		
Operating free-air temperature range, T_A(3)		–40	85	°C
Temperature range		–65	150	°C
Storage temperature range, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The voltage slew rate of these pins must be restricted to no more than 10 V/ms. For higher slew rates, use a 100 kΩ resister in series with the pins.

(3) The TPA3137D2 incorporates an exposed thermal pad on the underside of the chip. This acts as a heatsink, and it must be connected to a thermally dissipating plane for proper power dissipation. Failure to do so may result in the device going into thermal protection shutdown. See TI Technical Briefs SLMA002 for more information about using the TSSOP thermal pad.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±1000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 (2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
V_{CC}	Supply voltage	PVCC, AVCC	TPA3136	4.5	14.4	V
V_{IH}	High-level input voltage	$\overline{\text{SD}}$, PBTL		2	AVCC	V
V_{IL}	Low-level input voltage	$\overline{\text{SD}}$, PBTL			0.8	V
V_{OL}	Low-level output voltage	$\overline{\text{FAULT}}$, $R_{PULL\text{-}UP}$=100 k, PVCC=14.4 V			0.8	V
I_{IH}	High-level input current	$\overline{\text{SD}}$, PBTL, V_I = 2 V, AVCC = 12 V			50	μA
I_{IL}	Low-level input current	$\overline{\text{SD}}$, PBTL, V_I = 0.8 V, AVCC = 12 V			5	μA
T_A	Operating free-air temperature(1)			–40	85	°C
T_J	Operating junction temperature(1)			-40	150	°C

(1) The TPA3137D2 incorporates an exposed thermal pad on the underside of the chip. This acts as a heatsink, and it must be connected to a thermally dissipating plane for proper power dissipation. Failure to do so may result in the device going into thermal protection shutdown. See TI Technical Briefs SLMA002 for more information about using the TSSOP thermal pad.

7.4 Thermal Information

THERMAL METRIC(1)		TPA3137D2	UNIT
		PWP (HTSSOP)	
		28 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	30.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	33.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	17.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	7.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

T_A = 25°C, AV_{CC} = PV_{CC} = 12 V, R_L = 6 Ω (unless otherwise noted).(1) Over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DC CHARACTERISTICS							
$\lvert V_{OS} \rvert$	Class-D output offset voltage (measured differentially)	V_I = 0 V, Gain = 26 dB			1.5	15	mV
I_{CC}	Quiescent supply current	$\overline{SD}$ = 2 V, no load, 300 ohm Ferrite Bead + 1nF Output Filter			35	40	mA
$I_{CC(SD)}$	Quiescent supply current in shutdown mode	$\overline{SD}$ = 0.8 V, no load			40	60	µA
$r_{DS(on)}$	Drain-source on-state resistance	I_O = 500 mA, T_J = 25°C Excluding Metal and Bond Wire Resistance	High Side		240		mΩ
			Low side		240		
G	Gain			25	26	27	dB
t_{on}	Turn-on time	$\overline{SD}$ = 2 V			14		ms
t_{OFF}	Turn-off time	$\overline{SD}$ = 0.8 V			2.5		µs
GVDD	Gate drive supply	I_{GVDD} = 2 mA		6.4	6.9	7.4	V
t_{DCDET}	DC detect time	V_{RINN} = 3.1 V and V_{RINN} = 2.9 V, or V_{RINN} = 2.9 V and V_{RINN} = 3.1 V			950		ms
AC CHARACTERISTICS							
PSRR	Power supply ripple rejection	200-mV_{PP} ripple at 1 kHz, Gain = 26 dB, Inputs ac-coupled to GND			–65		dB
P_O	Continuous output power	THD+N = 10%, f = 1 kHz			6		W
P_O	Continuous output power	THD+N = 10%, f = 1 kHz, PV_{CC} = 13 V, R_L = 8 Ω			6		W
P_O	Continuous output power, PBTL (mono)	THD+N = 10%, f = 1 kHz, PV_{CC} = 13 V, R_L = 4 Ω			12		W
THD+N	Total harmonic distortion + noise	f = 1 kHz, P_O = 5 W (half-power)			0.06%		
V_n	Output integrated noise	20 Hz to 22 kHz, A-weighted filter, Gain = 26 dB			91		µV
					–81		dBV
	Crosstalk	V_O = 1 Vrms, Gain = 26 dB, f = 1 kHz			–75		dB
SNR	Signal-to-noise ratio	Maximum output at THD+N < 1%, f = 1 kHz, Gain = 26 dB, A-weighted			102		dB
OTE	Thermal trip point				150		°C
	Thermal hysteresis				15		°C

(1) Using the TPA3137D2 EVM (SLOU444), unless otherwise noted.

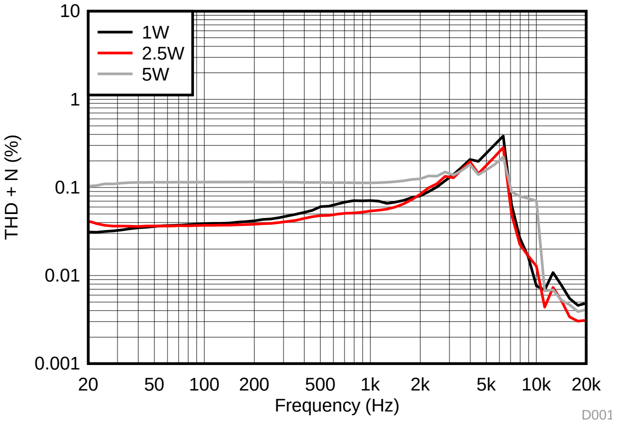
7.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		MIN	NOM	MAX	UNIT
$f_{OSC, SS}$	Oscillator frequency, Spread Spectrum ON	255	315	355	kHz

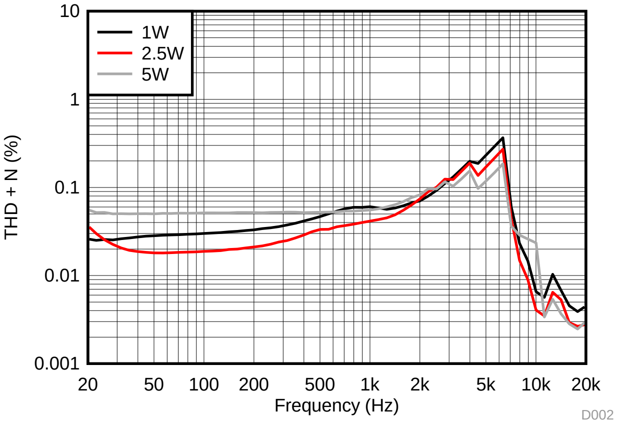
7.7 Typical Characteristics

All Measurements taken at 26dB closed loop gain, 1-kHz audio, T_A= 25°C unless otherwise noted. Measurements were made with AES17 filter using the TPA3137D2 EVM, which is available at ti.com.



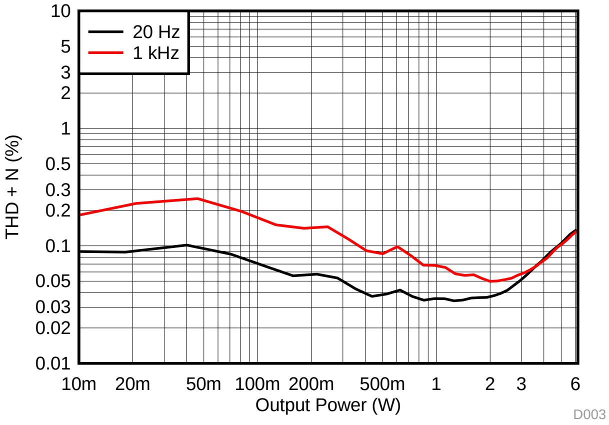
AVCC=PVCC = 12 V, Load = 6 Ω + 47 µH, 1 W, 2.5 W, 5 W

Figure 1. Total Harmonic Distortion vs Frequency (BTL)



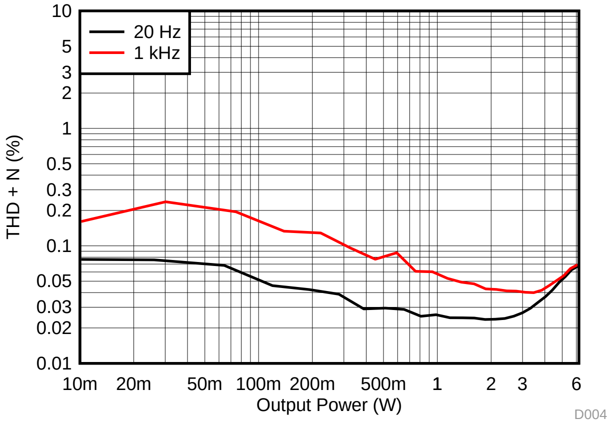
AVCC=PVCC = 13 V, Load = 8 Ω + 66 µH, 1 W, 2.5 W, 5 W

Figure 2. Total Harmonic Distortion vs Frequency (BTL)



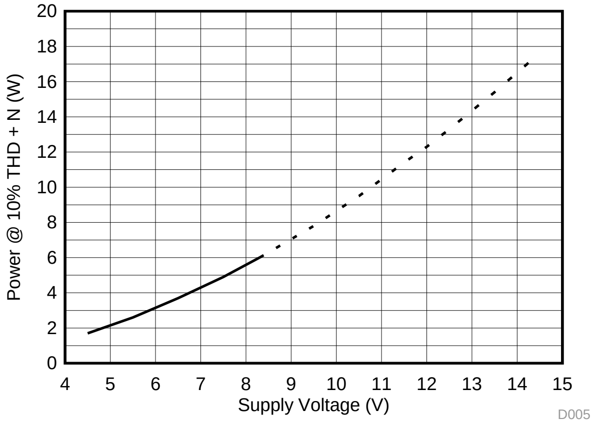
AVCC=PVCC = 12 V, Load = 6 Ω + 47 µH, 20 Hz, 1 kHz

Figure 3. Total Harmonic Distortion + Noise vs Output Power (BTL)



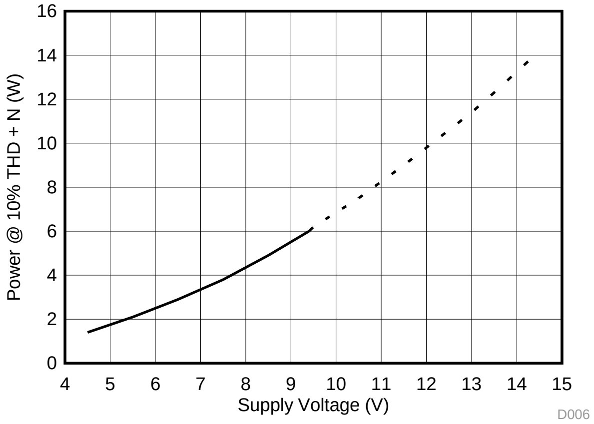
AVCC=PVCC = 13 V, Load = 8 Ω + 66 µH, 20 Hz, 1 kHz

Figure 4. Total Harmonic Distortion + Noise vs Output Power (BTL)



AVCC=PVCC = 4.5 V to 14.4 V, Load = 6 Ω + 47 µH

Figure 5. Output Power vs Supply Voltage (BTL)

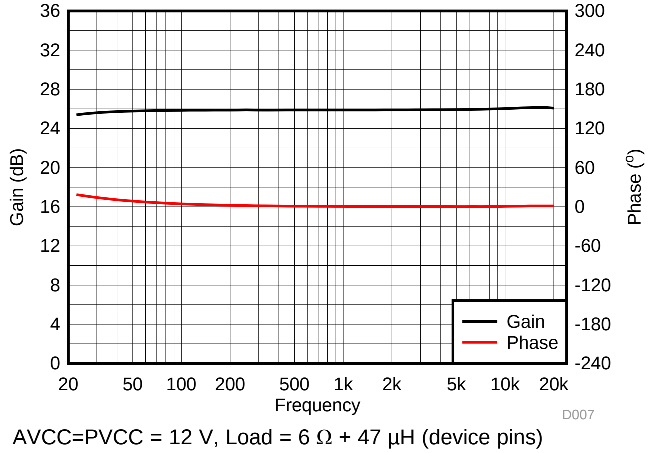


AVCC=PVCC = 4.5 V to 14.4 V, Load = 8 Ω + 66 µH

Figure 6. Output Power vs Supply Voltage (BTL)

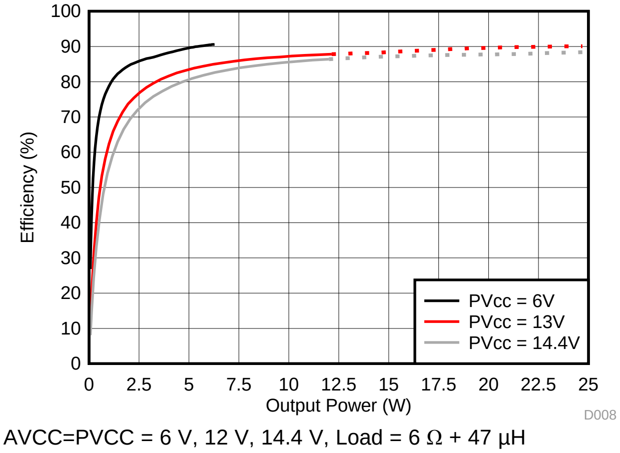
Typical Characteristics (continued)

All Measurements taken at 26dB closed loop gain, 1-kHz audio, T_A= 25°C unless otherwise noted. Measurements were made with AES17 filter using the TPA3137D2 EVM, which is available at ti.com.



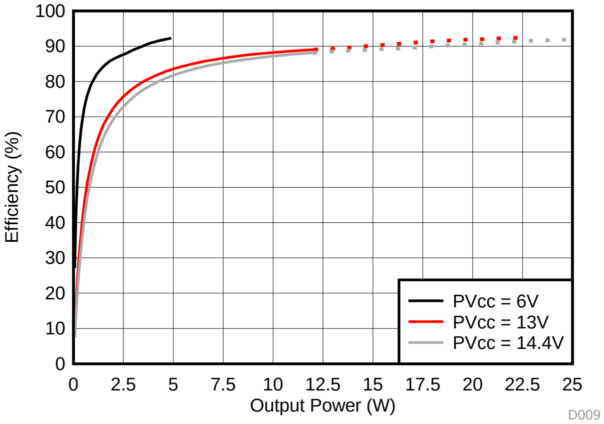
AVCC=PVCC = 12 V, Load = 6 Ω + 47 µH (device pins)

Figure 7. Gain/Phase vs Frequency (BTL)



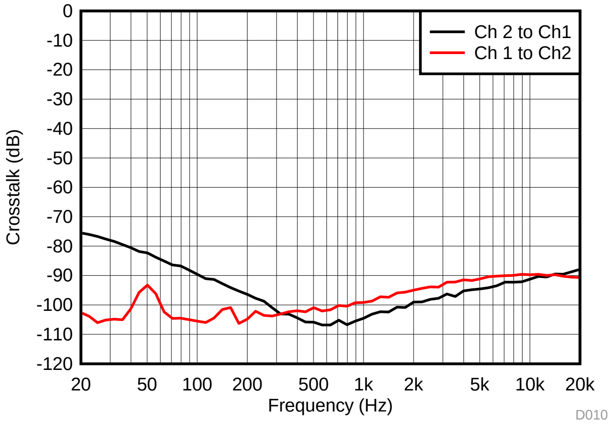
AVCC=PVCC = 6 V, 12 V, 14.4 V, Load = 6 Ω + 47 µH

Figure 8. Efficiency vs Output Power (BTL)



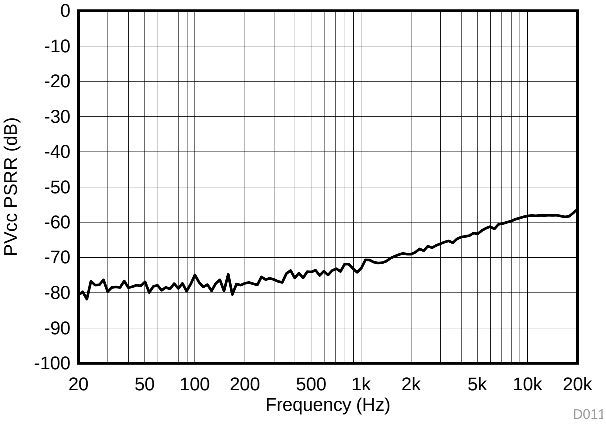
AVCC=PVCC= 6 V, 13 V, 14.4 V, Load = 8 Ω + 66 µH

Figure 9. Efficiency vs Output Power (BTL)



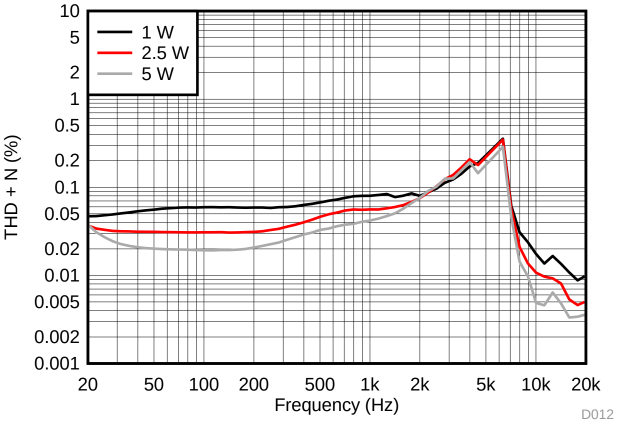
AVCC=PVCC = 12 V, 1 W, Load = 6 Ω + 47 µH

Figure 10. Crosstalk vs Frequency (BTL)



AVCC=PVCC = 12 V, Load = 4 Ω + 33 µH

Figure 11. Supply Ripple Rejection Ratio vs Frequency (BTL)

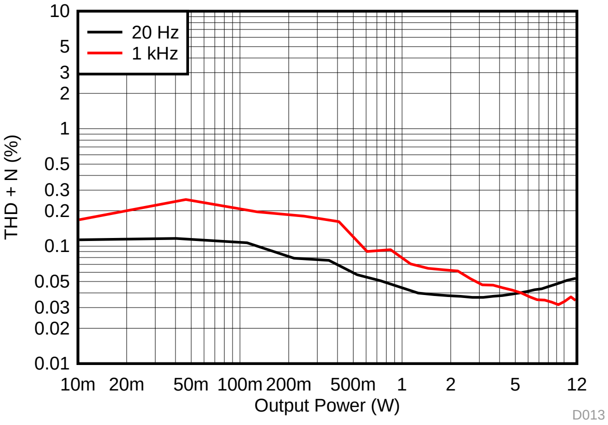


AVCC=PVCC = 13 V, Load = 4 Ω + 33 µH, 1 W, 2.5 W, 5 W

Figure 12. Total Harmonic Distortion + Noise vs Frequency (PBTL)

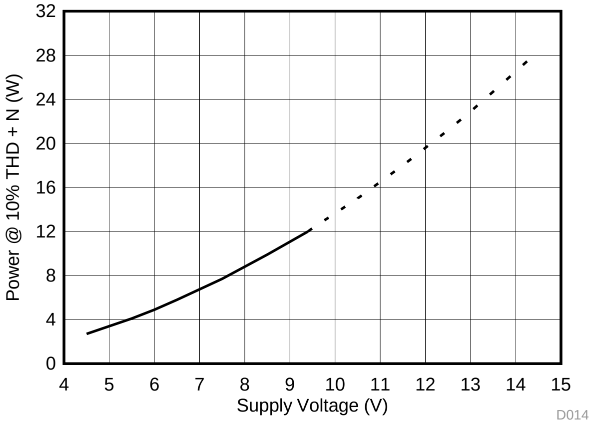
Typical Characteristics (continued)

All Measurements taken at 26dB closed loop gain, 1-kHz audio, T_A= 25°C unless otherwise noted. Measurements were made with AES17 filter using the TPA3137D2 EVM, which is available at ti.com.



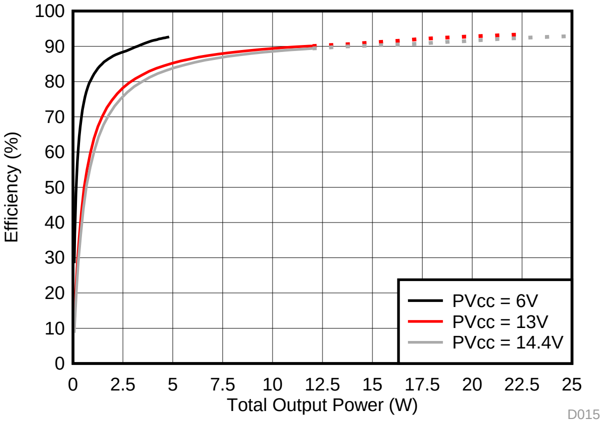
AVCC=PVCC = 13 V, Load = 4 Ω + 33 µH, 20 Hz, 1 kHz

Figure 13. Total Harmonic Distortion + Noise vs Output Power (PBTL)



AVCC=PVCC = 4.5 V to 14.4 V, Load = 4 Ω + 33 µH

Figure 14. Output Power vs Supply Voltage (PBTL)



AVCC=PVCC = 6 V, 13 V, 14.4 V, Load = 4 Ω + 33 µH

Figure 15. Efficiency vs Output Power (PBTL)

8 Parameter Measurement Information

All parameters are measured according to the conditions described in the *Specifications* section.

Most audio analyzers will not give correct readings of Class-D amplifiers' performance due to their sensitivity to out of band noise present at the amplifier output. An AES-17 pre analyzer filter is recommended to use for Class-D amplifier measurements. In absence of such filter, a 30-kHz low-pass filter (10 Ω + 47 nF) can be used to reduce the out of band noise remaining on the amplifier outputs.

9 Detailed Description

9.1 Overview

To facilitate system design, the TPA3137D2 needs only a single power supply between 4.5 V and 14.4 V for operation. An internal voltage regulator provides suitable voltage levels for the gate driver, digital, and low-voltage analog circuitry. Additionally, all circuitry requiring a floating voltage supply, as in the high-side gate drive, is accommodated by built-in bootstrap circuitry with integrated boot strap diodes requiring only an external capacitor for each half-bridge.

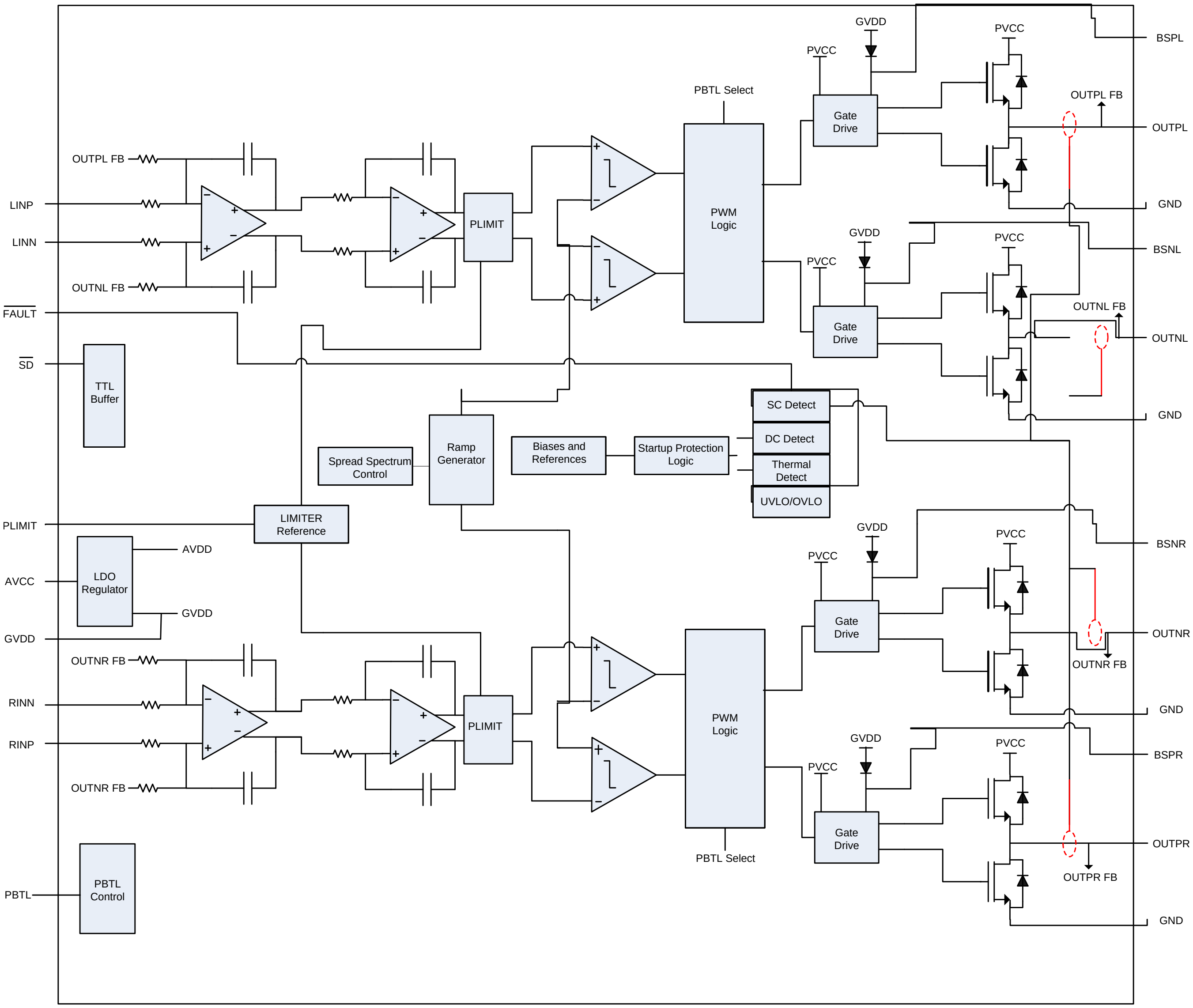
The audio signal path, including the gate drive and output stage, is designed as identical, independent full-bridges. All decoupling capacitors should be placed as close to their associated pins as possible. In general, the physical loop with the power supply pins, decoupling capacitors and GND return path to the device pins must be kept as short as possible and with as little area as possible to minimize induction (see reference board documentation for additional information).

For a properly functioning bootstrap circuit, a small ceramic capacitor must be connected from each bootstrap pin (BSXX) to the power-stage output pin (OUTXX). When the power-stage output is low, the bootstrap capacitor is charged through an internal diode connected between the gate-drive power-supply pin (GVDD) and the bootstrap pins. When the power-stage output is high, the bootstrap capacitor potential is shifted above the output potential and thus provides a suitable voltage supply for the high-side gate driver. In an application with PWM switching frequencies in the range of 315 kHz, use ceramic capacitors with at least 220-nF capacitance, size 0603 or 0805, for the bootstrap supply. These capacitors ensure sufficient energy storage, even during clipped low frequency audio signals, to keep the high-side power stage FET (LDMOS) fully turned on during the remaining part of its ON cycle.

Special attention should be paid to the power-stage power supply; this includes component selection, PCB placement, and routing. For optimal electrical performance, EMI compliance, and system reliability, each PVCC pin should be decoupled with ceramic capacitors that are placed as close as possible to each supply pin. It is recommended to follow the PCB layout of the TPA3137D2 reference design. For additional information on recommended power supply and required components, see the application diagrams in this data sheet.

The PVCC power supply should have low output impedance and low noise. The power-supply ramp and $\overline{\text{SD}}$ release sequence is not critical for device reliability as facilitated by the internal power-on-reset circuit, but it is recommended to release $\overline{\text{SD}}$ after the power supply is settled for minimum turn on audible artifacts.

9.2 Functional Block Diagram



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9.3 Feature Description

9.3.1 Fixed Analog Gain

The analog gain of the TPA3137D2 is fixed to 26 dB.

9.3.2 $\overline{\text{SD}}$ Operation

The TPA3137D2 device employs a shutdown mode of operation designed to reduce supply current (I_{CC}) to the absolute minimum level during periods of nonuse for power conservation. The $\overline{\text{SD}}$ input pin should be held high (see specification table for trip point) during normal operation when the amplifier is in use. Pulling $\overline{\text{SD}}$ low causes the outputs to mute and the amplifier to enter a low-current state. Never leave $\overline{\text{SD}}$ unconnected, because amplifier operation would be unpredictable.

For the best power-off pop performance, place the amplifier in the shutdown mode prior to removing the power supply voltage.

9.3.3 PLIMIT

The PLIMIT operation will, if selected, limit the output voltage level to a voltage level below the supply rail. In this case, the amplifier operates as if it was powered by a lower supply voltage, and thereby limiting the output power by voltage clipping. PLIMIT threshold is set by the PLIMIT pin voltage.

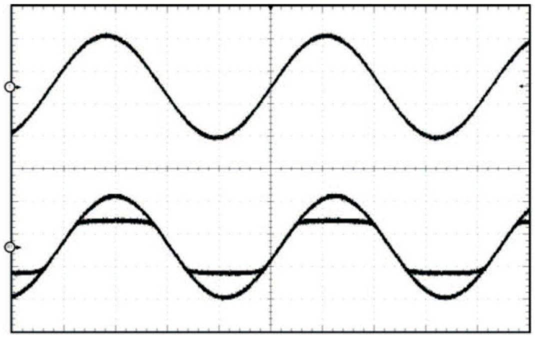


Figure 16. PLIMIT Circuit Operation

The PLIMIT circuit sets a limit on the output peak-to-peak voltage. The limiting is done by limiting the duty cycle to a fixed maximum value. The limit can be thought of as a "virtual" voltage rail which is lower than the supply connected to PVCC. The "virtual" rail is approximately four times the voltage at the PLIMIT pin. The output voltage can be used to calculate the maximum output power for a given maximum input voltage and speaker impedance.

Feature Description (continued)

$$P_{OUT} = \frac{\left(\left(\frac{R_L}{R_L + 2 \times R_S}\right) \times V_P\right)^2}{2 \times R_L} \quad \text{for unclipped power}$$

where

- P_{OUT} (10%THD) = 1.25 × P_{OUT} (unclipped)
- R_L is the load resistance.
- R_S is the total series resistance including $R_{DS(on)}$, and output filter resistance.
- V_P is the peak amplitude, which is limited by "virtual" voltage rail. (1)

9.3.4 Spread Spectrum and De-Phase Control

The TPA3137D2 device has built-in spread spectrum control of the oscillator frequency and de-phase of the PWM outputs to improve EMI performance. The spread spectrum schemes is internally fixed is always turned on.

De-phase inverts the phase of the output PWM such that the idle output PWM waveforms of the two audio channels are inverted. De-phase does not affect the audio signal, or its polarity.

9.3.5 GVDD Supply

The GVDD Supply is used to power the gates of the output full bridge transistors. Add a 1-µF capacitor to ground at this pin.

9.3.6 DC Detect

The TPA3137D2 device has circuitry which will protect the speakers from DC current which might occur due to defective capacitors on the input or shorts on the printed circuit board at the inputs. A DC detect fault will be reported on the $\overline{\text{FAULT}}$ pin as a low state. The DC Detect fault will also cause the amplifier to shutdown by changing the state of the outputs to Hi-Z.

A DC Detect Fault is issued when the output differential duty-cycle of either channel exceeds 14% (for example, +57%, –43%) for more than 950 msec at the same polarity. This feature protects the speaker from large DC currents or AC currents less than 2 Hz. To avoid nuisance faults due to the DC detect circuit, hold the $\overline{\text{SD}}$ pin low at power-up until the signals at the inputs are stable. Also, take care to match the impedance seen at the positive and negative inputs to avoid nuisance DC detect faults.

The minimum differential input voltage required to trigger the DC detect is 130 mV. The inputs must remain at or above the voltage listed in the table for more than 950 msec to trigger the DC detect.

9.3.7 PBTL Select

The TPA3137D2 device offers the feature of parallel BTL operation with two outputs of each channel connected directly. If the PBTL (pin 14) is tied high, the positive and negative outputs of each channel (left and right) are synchronized and in phase. To operate in this PBTL (mono) mode, tie PBTL pin to VCC and apply the input signal to the RINP and RINN inputs and place the speaker between the LEFT and RIGHT outputs with OUTPL connected to OUTNL and OUTPR connected to OUTNR to parallel the output half bridges for highest power efficiency. For an example of the PBTL connection, see the schematic in the *Typical Applications* section.

9.3.8 Short-Circuit Protection and Automatic Recovery Feature

The TPA3137D2 device has protection from overcurrent conditions caused by a short circuit on the output stage. The short circuit protection fault is reported on the $\overline{\text{FAULT}}$ pin as a low state. The amplifier outputs are switched to a Hi-Z state when the short circuit protection latch is engaged. The latch can be cleared by cycling the $\overline{\text{SD}}$ pin through the low state.

If automatic recovery from the short circuit protection latch is desired, connect the $\overline{\text{FAULT}}$ pin directly to the $\overline{\text{SD}}$ pin. This allows the $\overline{\text{FAULT}}$ pin function to automatically drive the $\overline{\text{SD}}$ pin low which clears the short-circuit protection latch.

Feature Description (continued)

9.3.9 Thermal Protection

Thermal protection on the TPA3137D2 device prevents damage to the device when the internal die temperature exceeds 150°C. There is a ±15°C tolerance on this trip point from device to device. Once the die temperature exceeds the thermal trip point, the device enters into the shutdown state and the outputs are disabled. This is a latched fault.

Thermal protection faults are reported on the $\overline{\text{FAULT}}$ pin.

If automatic recovery from the thermal protection latch is desired, connect the $\overline{\text{FAULT}}$ pin directly to the $\overline{\text{SD}}$ pin. This allows the $\overline{\text{FAULT}}$ pin function to automatically drive the $\overline{\text{SD}}$ pin low which clears the thermal protection latch.

9.4 Device Functional Modes

The TPA3137D2 device is running in **BD-modulation.**

This is a modulation scheme that allows operation without the classic LC reconstruction filter when the amp is driving an inductive load with short speaker wires. Each output is switching from 0 volts to the supply voltage. The OUTPx and OUTNx are in phase with each other with no input so that there is little or no current in the speaker. The duty cycle of OUTPx is greater than 50% and OUTNx is less than 50% for positive output voltages. The duty cycle of OUTPx is less than 50% and OUTNx is greater than 50% for negative output voltages. The voltage across the load sits at 0 V throughout most of the switching period, reducing the switching current, which reduces any I^2R losses in the load.

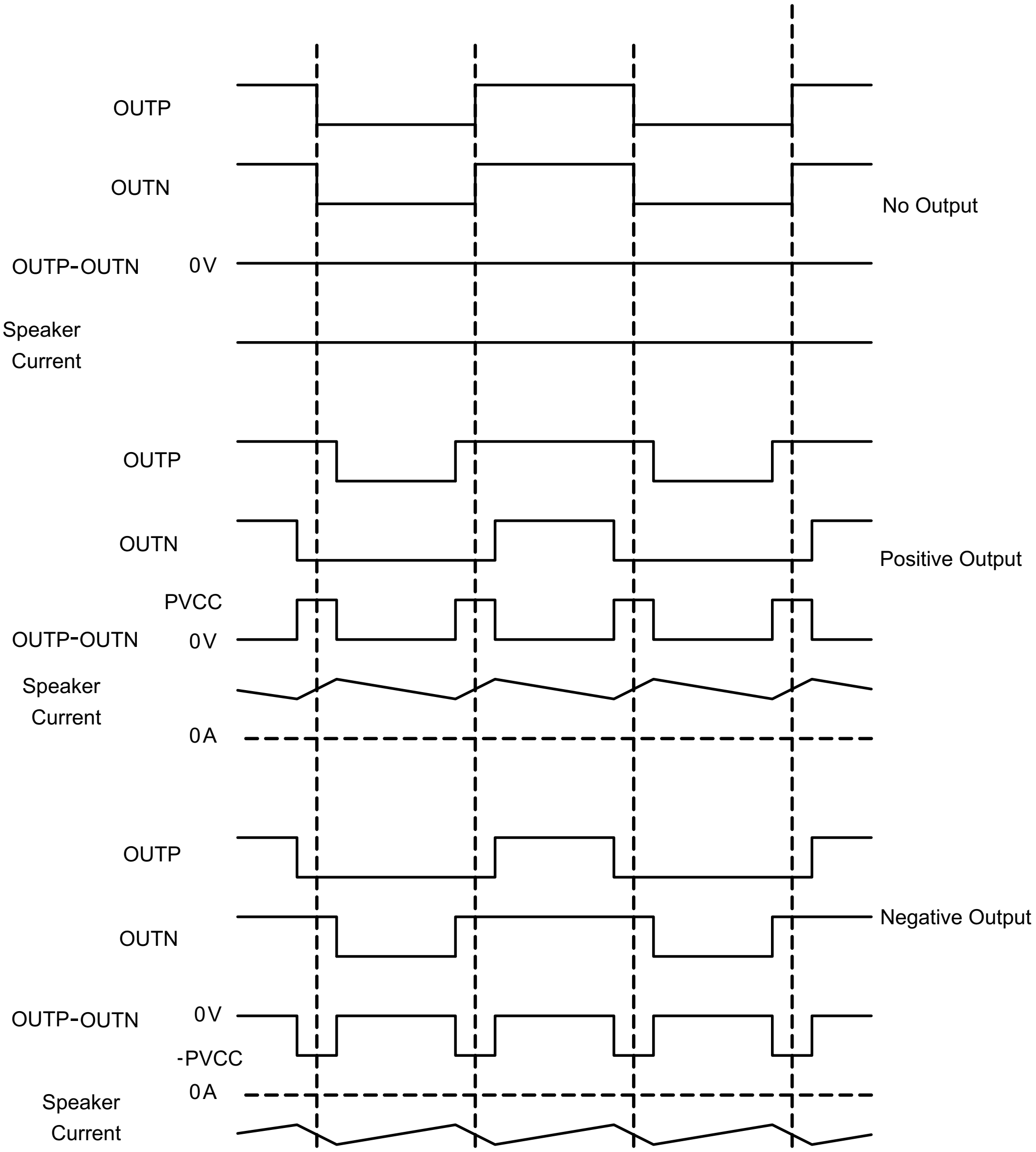


Figure 17. BD Mode Modulation

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The TPA3137D2 device is designed for use in inductor free applications with limited distance wire length) between amplifier and speakers like in TV sets, sound docks and Bluetooth speakers. The TPA3137D2 device can either be configured in stereo or mono mode, depending on output power conditions. Depending on output power requirements and necessity for (speaker) load protection, the built in PLIMIT circuit can be used to control system power, see functional description of these features.

10.2 Typical Applications

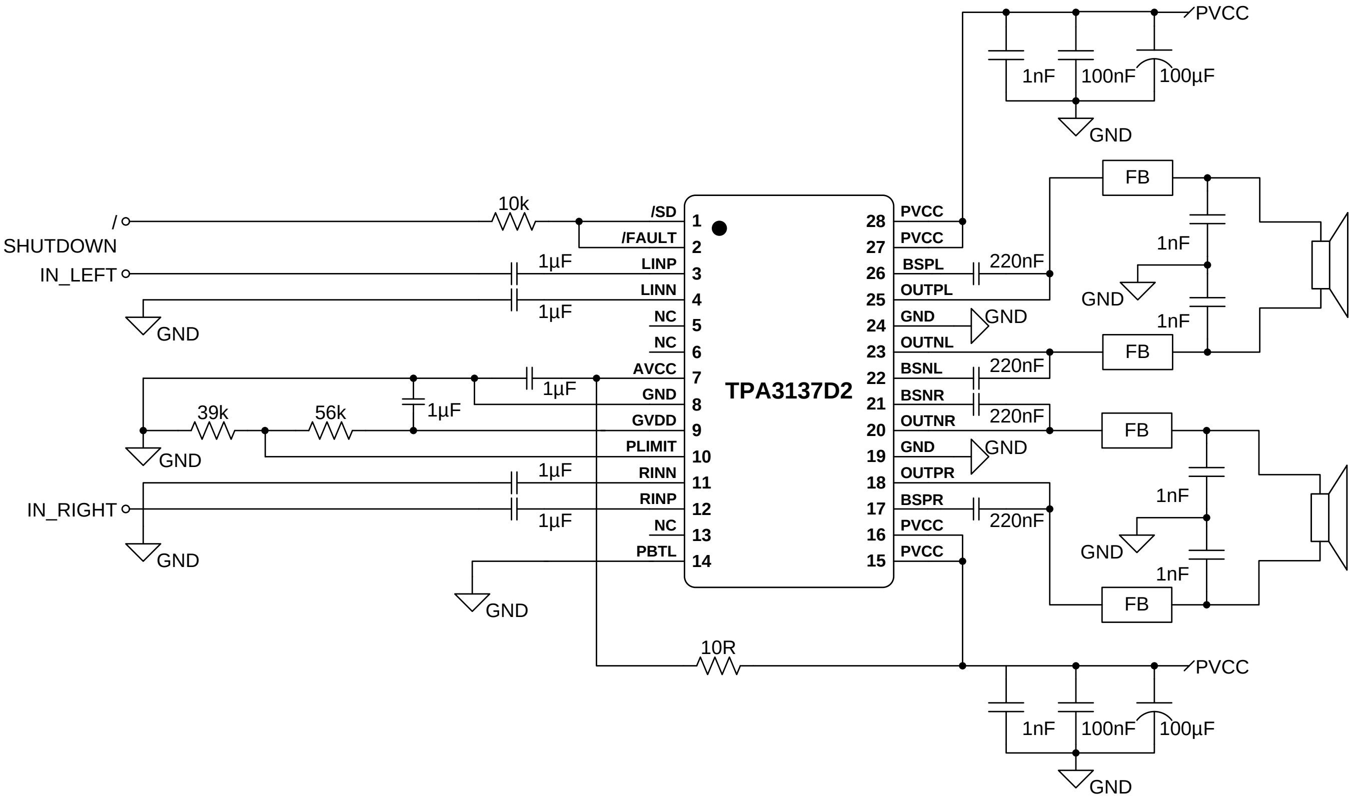


Figure 18. Stereo Class-D Amplifier with BTL Output and Single-Ended Inputs with Spread Spectrum Modulation

Typical Applications (continued)

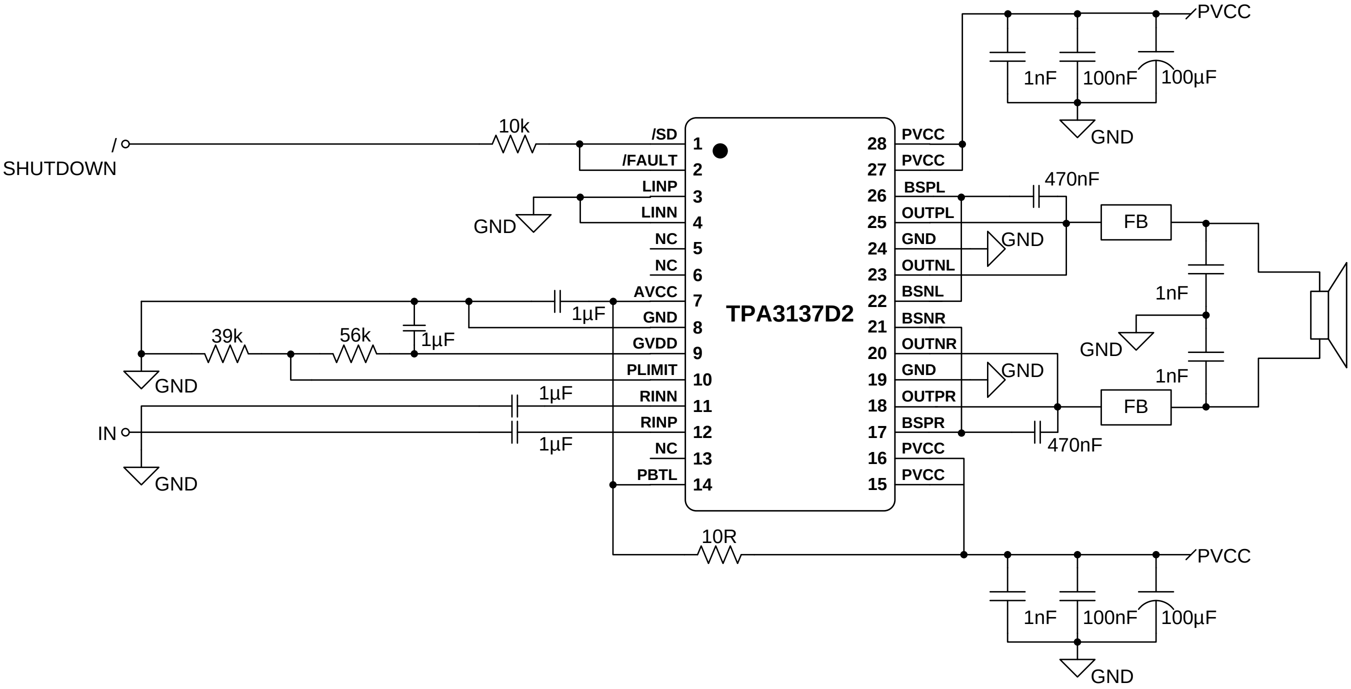


Figure 19. Stereo Class-D Amplifier with PBTL Output and Single-Ended Input with Spread Spectrum Modulation

10.2.1 Design Requirements

10.2.1.1 PCB Material Recommendation

FR-4 Glass Epoxy material with 1 oz. (35 µm) is recommended for use with the TPA3137D2. The use of this material can provide for higher power output, improved thermal performance, and better EMI margin (due to lower PCB trace inductance). It is recommended to use several GND underneath the device thermal pad for thermal coupling to a bottom side copper GND plane for best thermal performance.

10.2.1.2 PVCC Capacitor Recommendation

The large capacitors used in conjunction with each full-bridge, are referred to as the PVCC Capacitors. These capacitors should be selected for proper voltage margin and adequate capacitance to support the power requirements. In practice, with a well designed system power supply, 100 µF, 16 V will support most applications with 12-V power supply. 25-V capacitor rating is recommended for power supply voltage higher than 12 V. For The PVCC capacitors should be low ESR type because they are used in a circuit associated with high-speed switching.

10.2.1.3 Decoupling Capacitor Recommendations

In order to design an amplifier that has robust performance, passes regulatory requirements, and exhibits good audio performance, good quality decoupling capacitors should be used. In practice, X7R should be used in this application.

The voltage of the decoupling capacitors should be selected in accordance with good design practices. Temperature, ripple current, and voltage overshoot must be considered. This fact is particularly true in the selection of the ceramic capacitors that are placed on the power supply to each full-bridge. They must withstand the voltage overshoot of the PWM switching, the heat generated by the amplifier during high power output, and the ripple current created by high power output. A minimum voltage rating of 16 V is required for use with a 12-V power supply.

Typical Applications (continued)

10.2.2 Detailed Design Procedure

A rising-edge transition on $\overline{\text{SD}}$ input allows the device to start switching. It is recommended to ramp the PVCC voltage to its desired value before releasing $\overline{\text{SD}}$ for minimum audible artifacts.

The device is non-inverting the audio signal from input to output.

The GVDD pin is not recommended to be used as a voltage source for external circuitry.

10.2.2.1 Ferrite Bead Filter Considerations

Using the Advanced Emissions Suppression Technology in the TPA3137D2 amplifier it is possible to design a high efficiency Class-D audio amplifier while minimizing interference to surrounding circuits. It is also possible to accomplish this with only a low-cost ferrite bead filter. In this case it is necessary to carefully select the ferrite bead used in the filter.

One important aspect of the ferrite bead selection is the type of material used in the ferrite bead. Not all ferrite material is alike, so it is important to select a material that is effective in the 10 to 100 MHz range which is key to the operation of the Class-D amplifier. Many of the specifications regulating consumer electronics have emissions limits as low as 30 MHz. It is important to use the ferrite bead filter to block radiation in the 30-MHz and above range from appearing on the speaker wires and the power supply lines which are good antennas for these signals. The impedance of the ferrite bead can be used along with a small capacitor with a value in the range of 1000 pF to reduce the frequency spectrum of the signal to an acceptable level. For best performance, the resonant frequency of the ferrite bead/ capacitor filter should be less than 10 MHz.

Also, it is important that the ferrite bead is large enough to maintain its impedance at the peak currents expected for the amplifier. Some ferrite bead manufacturers specify the bead impedance at a variety of current levels. In this case it is possible to make sure the ferrite bead maintains an adequate amount of impedance at the peak current the amplifier will see. If these specifications are not available, it is also possible to estimate the bead's current handling capability by measuring the resonant frequency of the filter output at low power and at maximum power. A change of resonant frequency of less than fifty percent under this condition is desirable. Examples of ferrite beads which have been tested and work well with the TPA3137D2 device include NFZ2MSM series from Murata.

A high quality ceramic capacitor is also needed for the ferrite bead filter. A low ESR capacitor with good temperature and voltage characteristics will work best.

Additional EMC improvements may be obtained by adding snubber networks from each of the class-D outputs to ground. Suggested values for a simple RC series snubber network would be 68 Ω in series with a 100-pF capacitor although design of the snubber network is specific to every application and must be designed taking into account the parasitic reactance of the printed circuit board as well as the audio amp. Take care to evaluate the stress on the component in the snubber network especially if the amp is running at high PVCC. Also, make sure the layout of the snubber network is tight and returns directly to the GND or the thermal pad beneath the chip.

10.2.2.2 Efficiency: LC Filter Required with the Traditional Class-D Modulation Scheme

The main reason that the traditional class-D amplifier needs an output filter is that the switching waveform results in maximum current flow. This causes more loss in the load, which causes lower efficiency. The ripple current is large for the traditional modulation scheme, because the ripple current is proportional to voltage multiplied by the time at that voltage. The differential voltage swing is $2 \times V_{CC}$, and the time at each voltage is half the period for the traditional modulation scheme. An ideal LC filter is needed to store the ripple current from each half cycle for the next half cycle, while any resistance causes power dissipation. The speaker is both resistive and reactive, whereas an LC filter is almost purely reactive.

The TPA3137D2 modulation scheme has little loss in the load without a filter because the pulses are short and the change in voltage is V_{CC} instead of $2 \times V_{CC}$. As the output power increases, the pulses widen, making the ripple current larger. Ripple current could be filtered with an LC filter for increased efficiency, but for most applications the filter is not needed.

An LC filter with a cutoff frequency less than the class-D switching frequency allows the switching current to flow through the filter instead of the load. The filter has less resistance but higher impedance at the switching frequency than the speaker, which results in less power dissipation, therefore increasing efficiency.

Typical Applications (continued)

10.2.2.3 When to Use an Output Filter for EMI Suppression

The TPA3137D2 device has been tested with a simple ferrite bead filter for a variety of applications including long speaker wires up to 100 cm and high power. The TPA3137D2 EVM passes FCC Class B specifications under these conditions using twisted speaker wires. The size and type of ferrite bead can be selected to meet application requirements. Also, the filter capacitor can be increased if necessary with some impact on efficiency.

There may be a few circuit instances where it is necessary to add a complete LC reconstruction filter. These circumstances might occur if there are nearby circuits which are sensitive to noise. In these cases, a classic second order Butterworth filter similar to those shown in the following figures can be used.

Some systems have little power supply decoupling from the AC line, but are also subject to line conducted interference (LCI) regulations. These include systems powered by "wall warts" and "power bricks." In these cases, LC reconstruction filters can be the lowest cost means to pass LCI tests. Common mode chokes using low frequency ferrite material can also be effective at preventing line conducted interference.

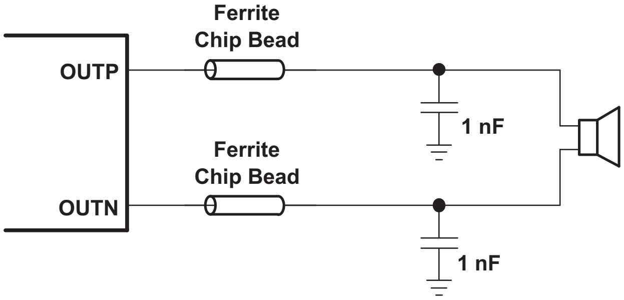


Figure 20. Typical Ferrite Chip Bead Filter (Chip Bead Example: NFZ2MSM series from Murata)

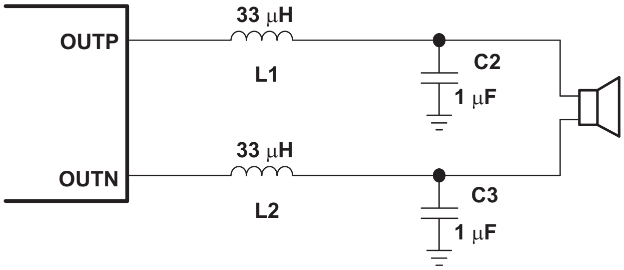


Figure 21. Typical LC Output Filter, Cutoff Frequency of 27 kHz, Speaker Impedance = 8 Ω

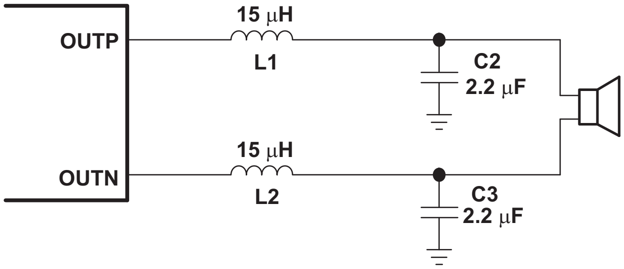
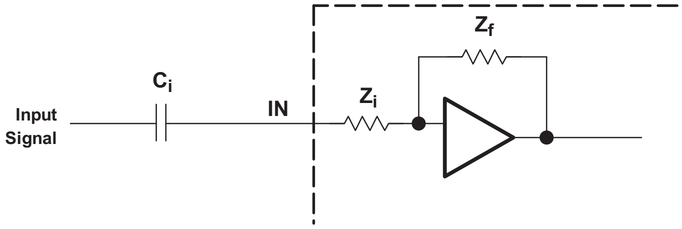


Figure 22. Typical LC Output Filter, Cutoff Frequency of 27 kHz, Speaker Impedance = 6 Ω

10.2.2.4 Input Resistance

The typical input resistance of the amplifier is fixed to 30 kΩ ±20%.

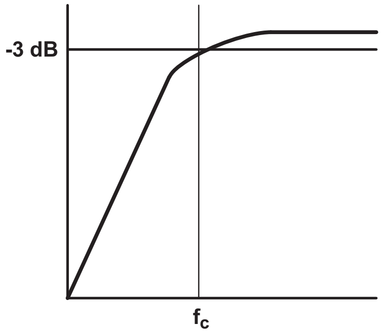
Typical Applications (continued)



10.2.2.5 Input Capacitor, C_i

In the typical application, an input capacitor (C_i) is required to allow the amplifier to bias the input signal to the proper dc level for optimum operation. In this case, C_i and the input impedance of the amplifier (Z_i) form a high-pass filter with the corner frequency determined in Equation 2.

$$f_c = \frac{1}{2\pi\, Z_i\, C_i} \tag{2}$$



The value of C_i is important, as it directly affects the bass (low-frequency) performance of the circuit. Consider the example where Z_i is 30 kΩ and the specification calls for a flat bass response down to 20 Hz. Equation 2 is reconfigured as Equation 3.

$$C_i = \frac{1}{2\pi\, Z_i\, f_c} \tag{3}$$

In this example, C_i is 0.27 µF; so, one would likely choose a value of 0.33 µF as this value is commonly used. A further consideration for this capacitor is the leakage path from the input source through the input network (C_i) and the feedback network to the load. This leakage current creates a dc offset voltage at the input to the amplifier that reduces useful headroom. For this reason, a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the dc level there is held at 3 V, which is likely higher than the source dc level. Note that it is important to confirm the capacitor polarity in the application. Additionally, lead-free solder can create dc offset voltages and it is important to ensure that boards are cleaned properly.

10.2.2.6 BSN and BSP Capacitors

The full H-bridge output stages use only NMOS transistors. Therefore, they require bootstrap capacitors for the high side of each output to turn on correctly. A 0.22-µF ceramic capacitor, rated for at least 25 V, must be connected from each output to its corresponding bootstrap input. Specifically, one 0.22-µF capacitor must be connected from OUTPx to BSPx, and one 0.22-µF capacitor must be connected from OUTNx to BSNx. (See the application circuit diagram in Figure 18.)

The bootstrap capacitors connected between the BSxx pins and corresponding output function as a floating power supply for the high-side N-channel power MOSFET gate drive circuitry. During each high-side switching cycle, the bootstrap capacitors hold the gate-to-source voltage high enough to keep the high-side MOSFETs turned on.

Typical Applications (continued)

10.2.2.7 Differential Inputs

The differential input stage of the amplifier cancels any noise that appears on both input lines of the channel. To use the TPA3137D2 device with a differential source, connect the positive lead of the audio source to the INP input and the negative lead from the audio source to the INN input. To use the TPA3137D2 with a single-ended source, ac ground the INP or INN input through a capacitor equal in value to the input capacitor on INN or INP and apply the audio source to either input. In a single-ended input application, the unused input should be ac grounded at the audio source instead of at the device input for best noise performance. For good transient performance, the impedance seen at each of the two differential inputs should be the same.

The impedance seen at the inputs should be limited to an RC time constant of 1 ms or less if possible. This is to allow the input dc blocking capacitors to become completely charged during the 14-ms power-up time. If the input capacitors are not allowed to completely charge, there is some additional sensitivity to component matching which can result in pop if the input components are not well matched.

10.2.2.8 Using Low-ESR Capacitors

Low-ESR capacitors are recommended throughout this application section. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance, the more the real capacitor behaves like an ideal capacitor.

Typical Applications (continued)

10.2.3 Application Performance Curves

10.2.3.1 EN55013 Radiated Emissions Results

TPA3137D2 EVM, PVCC = 12 V, 8-Ω speakers, P_O = 4 W

Figure 23. Radiated Emission - Horizontal

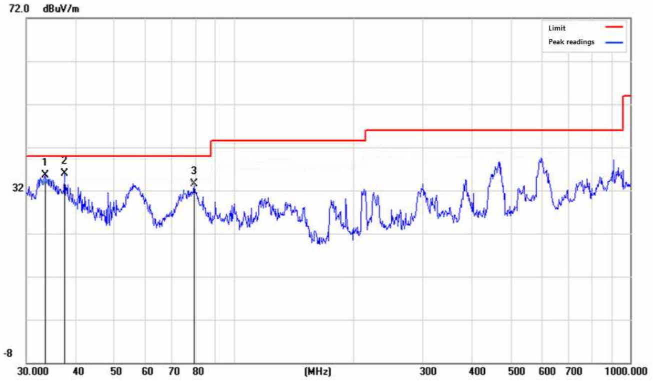


Figure 24. Radiated Emission - Vertical

10.2.3.2 EN55022 Conducted Emissions Results

TPA3137D2 EVM, PVCC = 12 V, 8-Ω speakers, P_O = 4 W

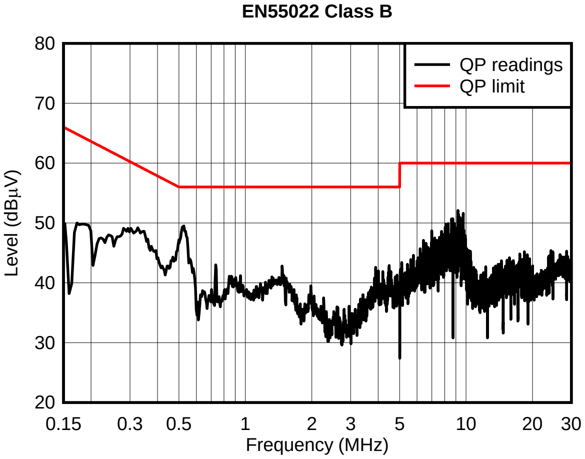


Figure 25. Conducted Emission - Line

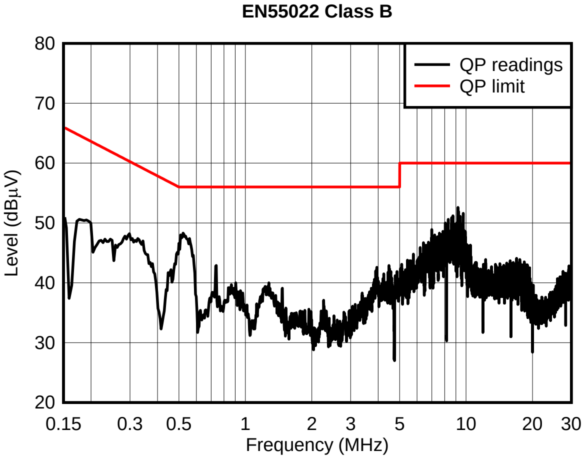


Figure 26. Conducted Emission - Neutral

11 Power Supply Recommendations

11.1 Power Supply Decoupling, C_S

The TPA3137D2 device is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure that the output total harmonic distortion (THD) is as low as possible. Power supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. Optimum decoupling is achieved by using a network of capacitors of different types that target specific types of noise on the power supply leads. For higher frequency transients due to parasitic circuit elements such as bond wire and copper trace inductances as well as lead frame capacitance, a good quality low equivalent-series-resistance (ESR) ceramic capacitor of value between 220 pF and 1000 pF works well. This capacitor should be placed as close to the device PVCC pins and system ground (either GND pins or thermal pad) as possible. For mid-frequency noise due to filter resonances or PWM switching transients as well as digital hash on the line, another good quality capacitor typically 0.1 μF to 1 μF placed as close as possible to the device PVCC leads works best. For filtering lower frequency noise signals, a larger aluminum electrolytic capacitor of 100 μF or greater placed near the audio power amplifier is recommended. The 100-μF capacitor also serves as a local storage capacitor for supplying current during large signal transients on the amplifier outputs. The PVCC pins provide the power to the output transistors, so a 100-μF or larger capacitor should be placed on each PVCC pin. A 1-μF capacitor on the AVCC pin is adequate. Also, a small decoupling resistor between AVCC and PVCC can be used to keep high frequency class-D noise from entering the linear input amplifiers.

12 Layout

12.1 Layout Guidelines

The TPA3137D2 device can be used with a small, inexpensive ferrite bead output filter for most applications. However, since the Class-D switching edges are fast, it is necessary to take care when planning the layout of the printed circuit board. The following suggestions will help to meet EMC requirements.

- Decoupling capacitors—The high-frequency decoupling capacitors should be placed as close to the PVCC and AVCC pins as possible. Large (100-µF or greater) bulk power supply decoupling capacitors should be placed near the TPA3137D2 device on the PVCC supplies. Local, high-frequency bypass capacitors should be placed as close to the PVCC pins as possible. These caps can be connected to the thermal pad directly for an excellent ground connection. Consider adding a small, good quality low ESR ceramic capacitor between 220 pF and 1000 pF and a larger mid-frequency cap of value between 0.1 μF and 1 μF also of good quality to the PVCC connections at each end of the chip.
- Keep the current loop from each of the outputs through the ferrite bead and the small filter cap and back to GND as small and tight as possible. The size of this current loop determines its effectiveness as an antenna.
- Grounding—The AVCC (pin 14) decoupling capacitor should be connected to ground (GND). The PVCC decoupling capacitors should connect to GND. Analog ground and power ground should be connected at the thermal pad, which should be used as a central ground connection or star ground for the TPA3137D2.
- Output filter—The ferrite EMI filter (Figure 20) should be placed as close to the output pins as possible for the best EMI performance. The capacitors used in the ferrite should be grounded to power ground.
- Thermal Pad—The thermal pad must be soldered to the PCB for proper thermal performance and optimal reliability. The dimensions of the thermal pad and thermal land should be 6.46 mm × 2.35 mm. Six rows of solid vias (three vias per row, 0.3302 mm or 13 mils diameter) should be equally spaced underneath the thermal land. The vias should connect to a solid copper plane, either on an internal layer or on the bottom layer of the PCB. The vias must be solid vias, not thermal relief or webbed vias. See the TI Application Report SLMA002 for more information about using the TSSOP thermal pad. For recommended PCB footprints, see figures at the end of this data sheet.

For an example layout, see the TPA3137D2 Evaluation Module (TPA3137D2EVM) User Manual. Both the EVM user manual and the thermal pad application report are available on the TI Web site at http://www.ti.com.

12.2 Layout Example

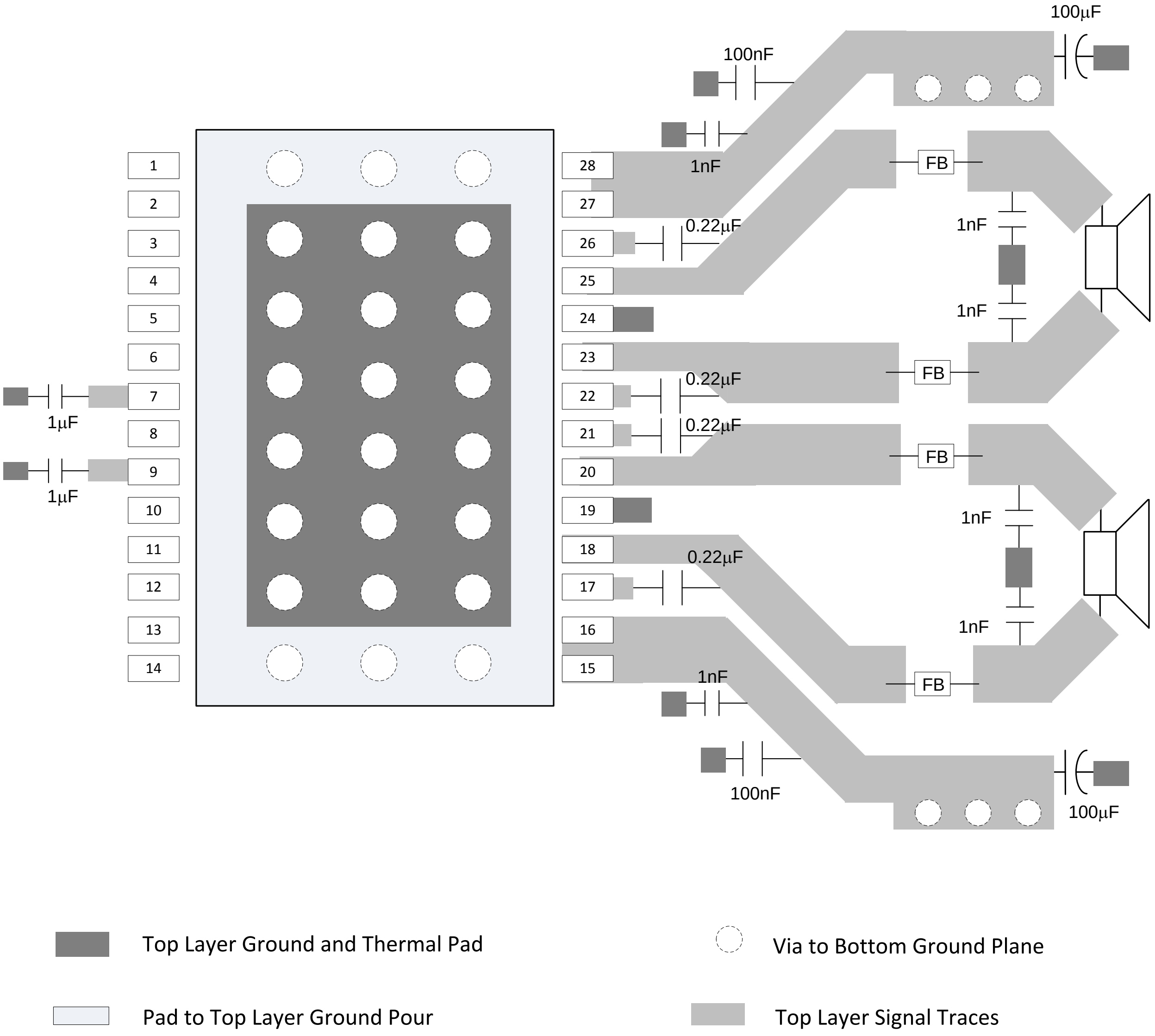


Figure 27. BTL Layout Example

13 器件和文档支持

13.1 器件支持

13.1.1 Third-Party Products Disclaimer

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13.2 文档支持

13.2.1 相关文档

《PowerPAD™ 耐热增强型封装应用报告》（文献编号：SLMA002）

13.3 相关链接

下表列出了快速访问链接。类别包括技术文档、支持和社区资源、工具和软件，以及立即购买的快速链接。

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设计支持	***TI 参考设计支持*** 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

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All other trademarks are the property of their respective owners.

13.7 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

13.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知和修订此文档。如欲获取此数据表的浏览器版本，请参阅左侧的导航。

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPA3137D2PWP	ACTIVE	HTSSOP	PWP	28	50	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPA3137D2	Samples
TPA3137D2PWPR	ACTIVE	HTSSOP	PWP	28	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	TPA3137D2	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

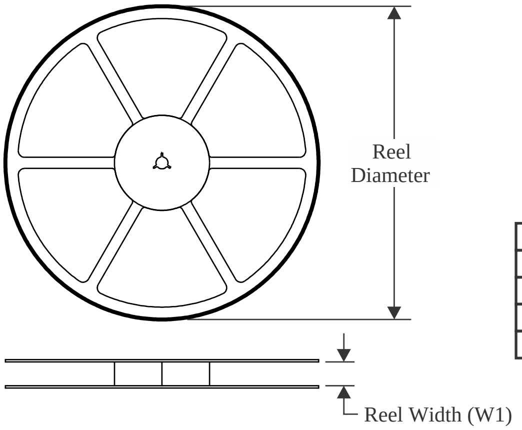
[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

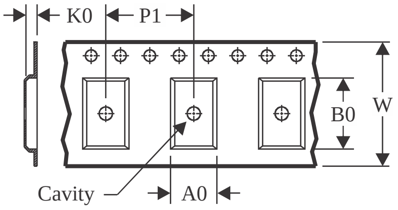
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

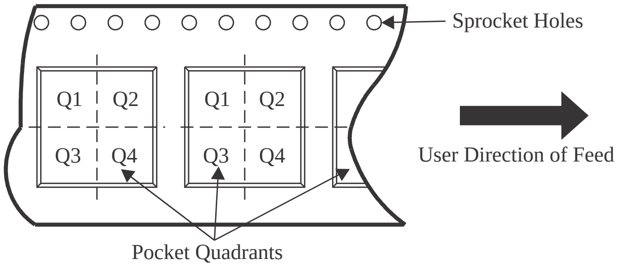


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

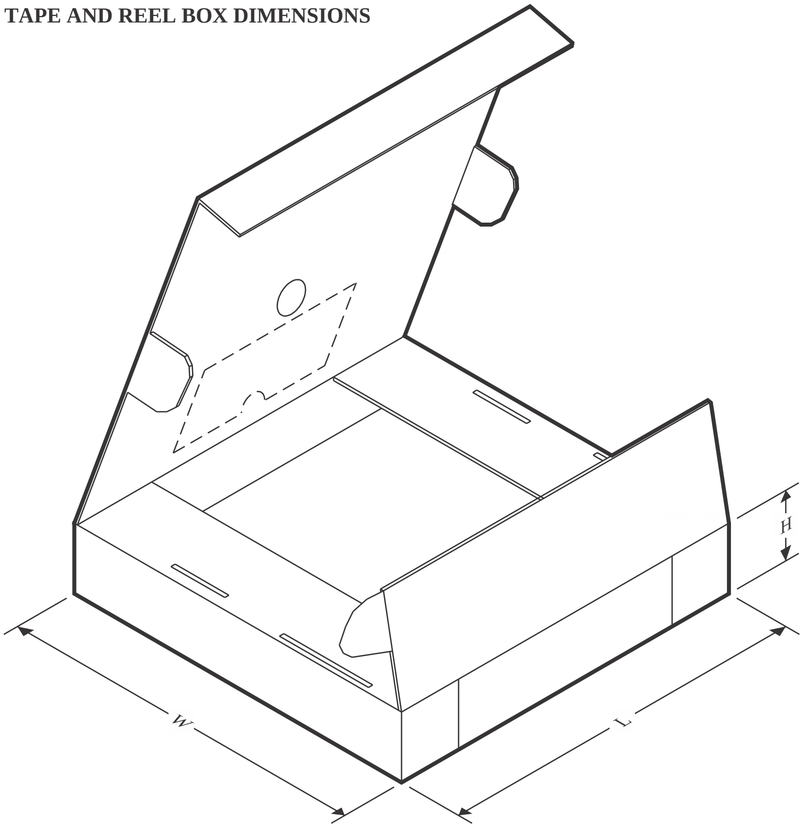
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPA3137D2PWPR	HTSSOP	PWP	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

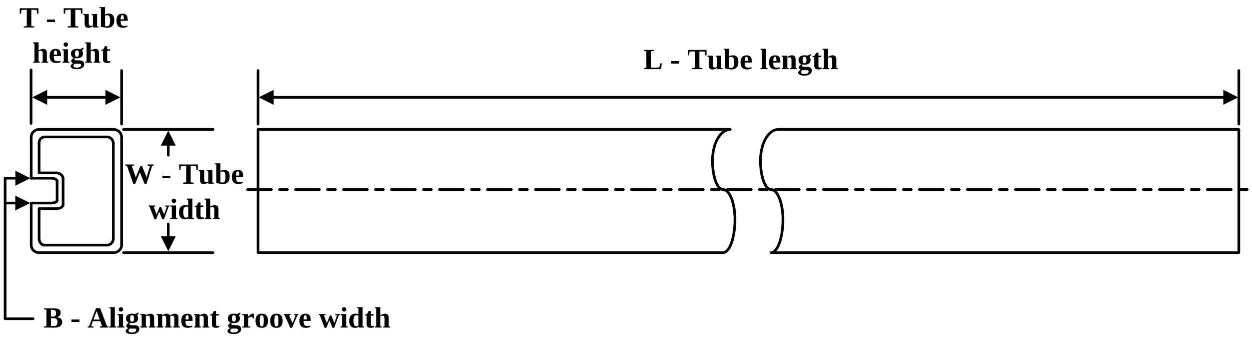
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPA3137D2PWPR	HTSSOP	PWP	28	2000	350.0	350.0	43.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPA3137D2PWP	PWP	HTSSOP	28	50	530	10.2	3600	3.5

GENERIC PACKAGE VIEW

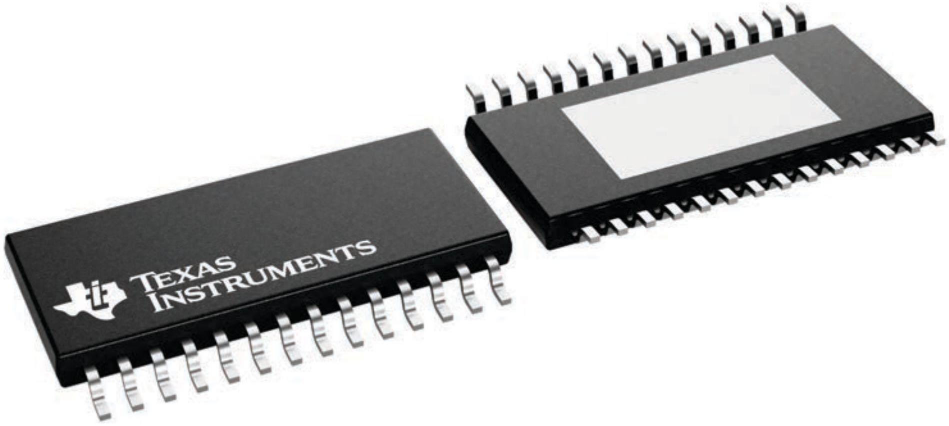
PWP 28

PowerPAD™ TSSOP - 1.2 mm max height

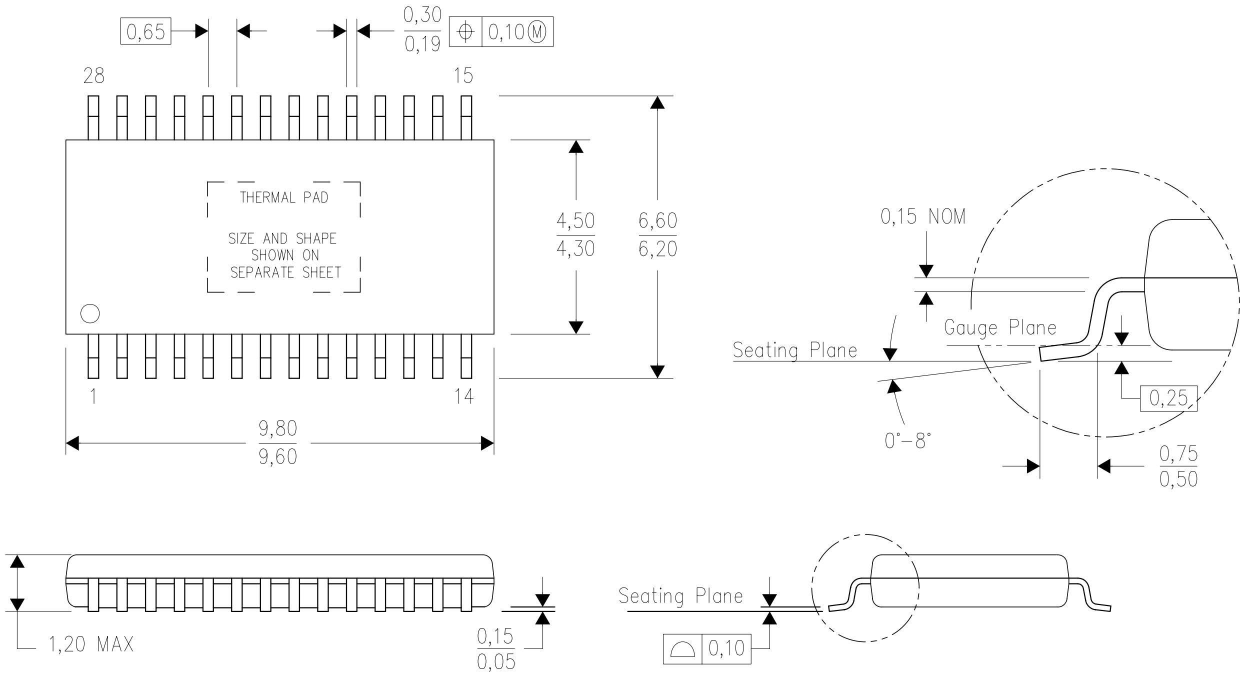
4.4 x 9.7, 0.65 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



PWP (R-PDSO-G28) PowerPAD™ PLASTIC SMALL OUTLINE



4073225-6/I 05/11

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http: //www.ti.com>.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
E. Falls within JEDEC MO-153

PowerPAD is a trademark of Texas Instruments.

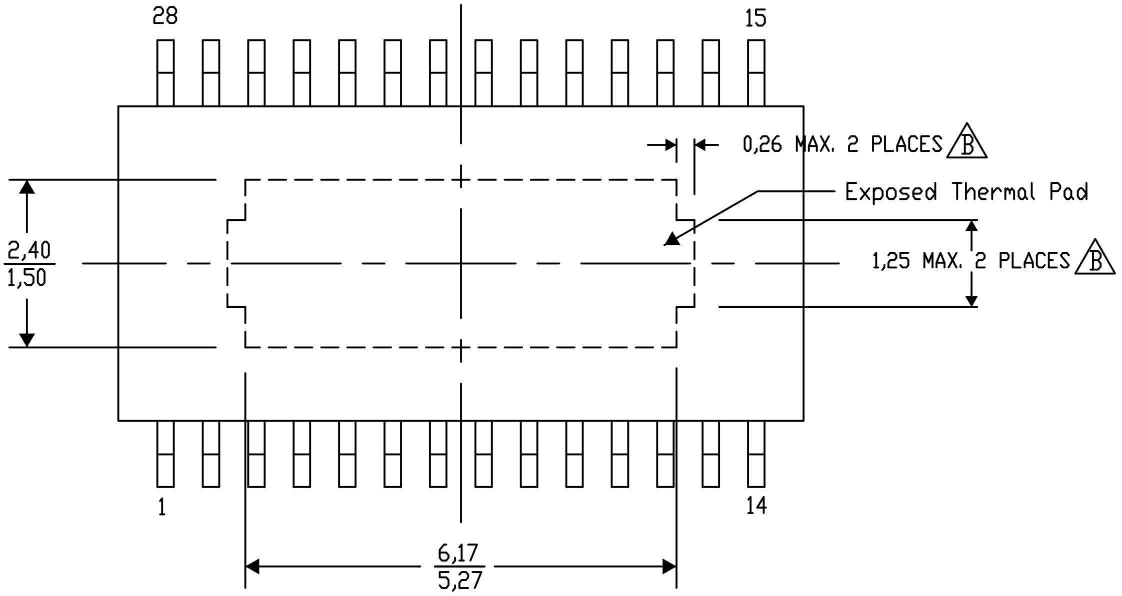
PWP (R-PDSO-G28) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

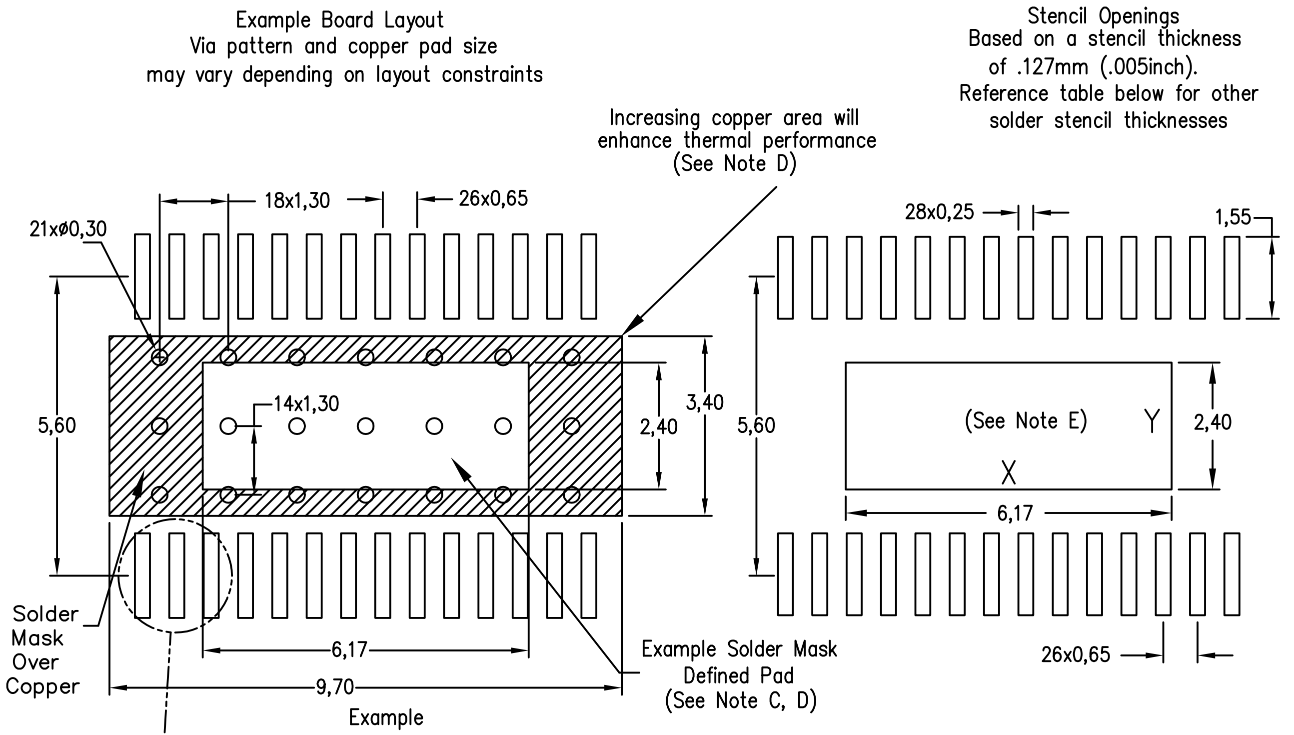
4206332-33/A0 01/16

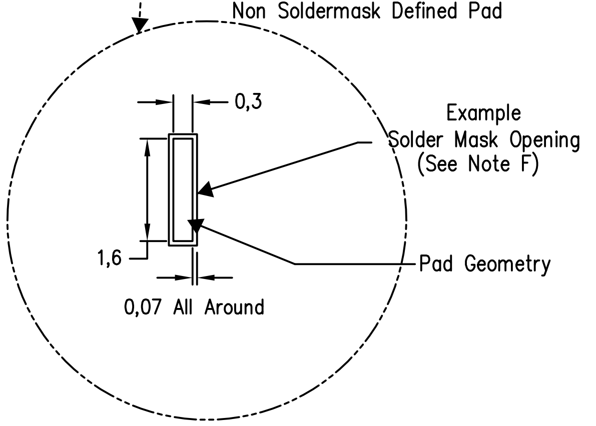
NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments

PWP (R-PDSO-G28) PowerPAD™ PLASTIC SMALL OUTLINE





Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	6.6	2.6
0.127mm	6.17	2.4
0.152mm	5.8	2.3
0.178mm	5.6	2.2

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NOTES:

A. All linear dimensions are in millimeters.

B. This drawing is subject to change without notice.

C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.

D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets.

E. For specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC-7351 is recommended for alternate designs. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil

F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

重要声明和免责声明

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