

# TPS25814 具有集成拉电流电源开关的 USB Type-C® 控制器

## 1 特性

- 符合 USB Type-C 规范
  - 线缆连接和方向检测
  - 集成式 VCONN 开关
  - 26V 耐压 CC 引脚
  - 可配置电流广播
- 集成式 VBUS 供电端口电源开关
  - 5V、3A、36mΩ 电源开关
  - UL 认证组件 (E169910)
  - 欠压和过压保护
  - 高达 3A 的可配置电流限制
- USB type-C 连接器系统软件接口 (USCI) 支持
- 支持工业温度范围
- 面向多端口系统的可选简易电源管理

## 2 应用

- 笔记本电脑和台式机

- 15W USB-C 充电器
- 集线站和集线器

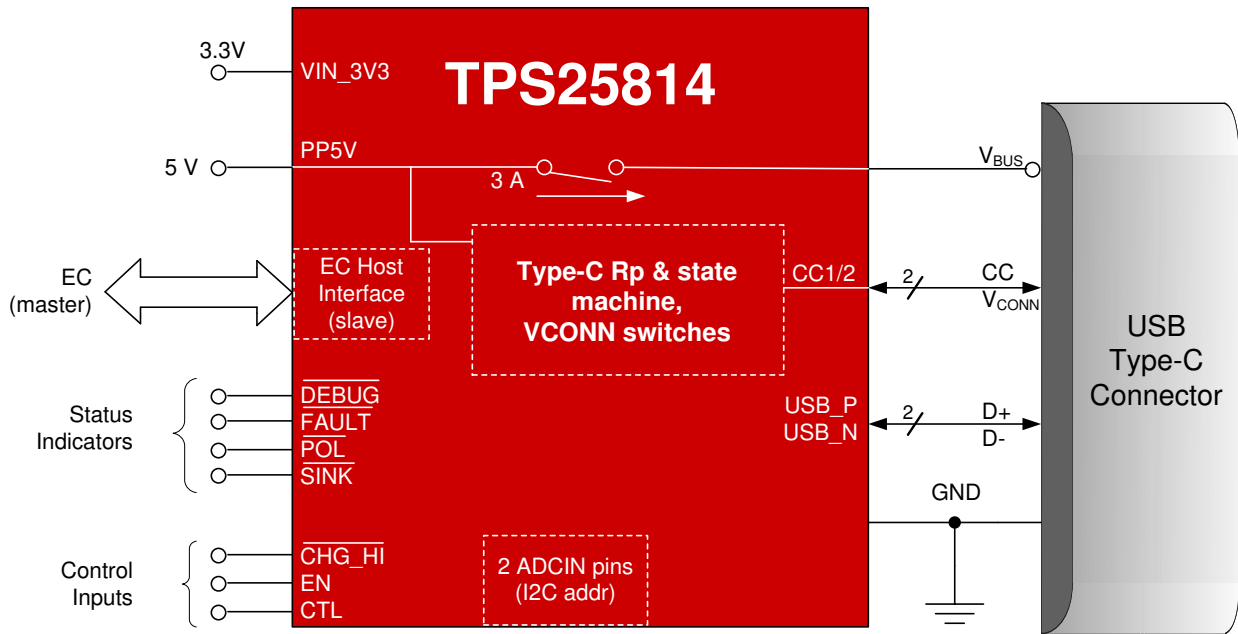
## 3 说明

TPS25814 是一款独立的 USB Type-C 控制器，可为一个 USB Type-C 连接器提供电缆插拔和方向检测功能。在连接电缆时，TPS25814 根据 USB Type-C 规范执行电缆检测。在线缆检测完成后，TPS25814 会启用内部电源路径。状态指示器引脚可用于控制外部多路复用器。

### 器件信息

器件型号 <sup>(1)</sup>	封装	封装尺寸 (标称值)
TPS25814	QFN (RSM)	4.0mm x 4.0mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



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## 4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision * (July 2020) to Revision A (December 2020)	Page
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## 5 Pin Configuration and Functions

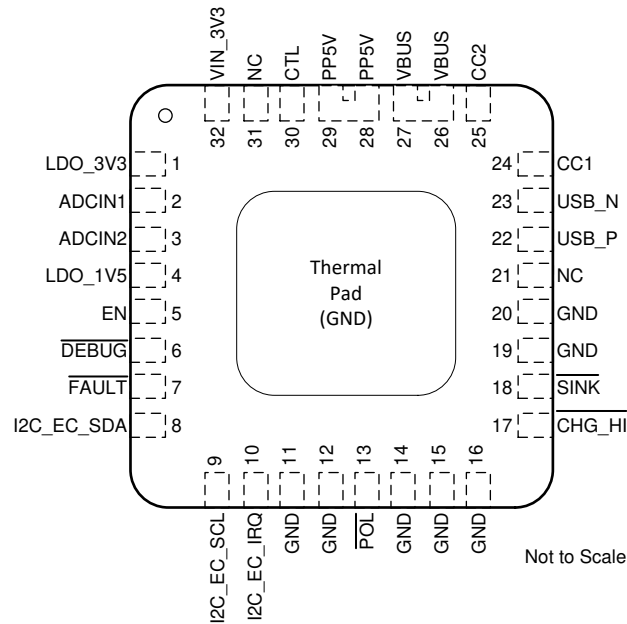


图 5-1. RSM Package 32-pin QFN Top View

表 5-1. Pin Functions

PIN		TYPE <sup>(1)</sup>	RESET	Description
NAME	NO.			
ADCIN1	2	I	Hi-Z	Configuration input. Connect to a resistor divider to LDO_3V3.
ADCIN2	3	I	Hi-Z	Configuration input. Connect to a resistor divider to LDO_3V3.
CC1	24	I/O	Hi-Z	I/O for USB Type-C .
CC2	25	I/O	Hi-Z	I/O for USB Type-C .
CHG_HI	17	I	Hi-Z	Charge logic input to select between minimum or maximum Type-C current advertisement.
CTL	30	I	Hi-Z	This pin controls which BC 1.2 mode is used. Pull to GND for CDP mode. Pull high for DCP mode.
DEBUG	6	O	Hi-Z	Open-drain logic output that is asserted low when a Type-C debug accessory is detected.
EN	5	I	Low	When this pin is pulled low or left floating, the device will be disabled and remain in the Type-C Error Recovery state.
FAULT	7	O	Hi-Z	Open-drain logic output that asserts when an over-current fault is detected.
GND	11,12,14,15,16, 19,20	—	—	Ground. Connect to ground plane.
I2C_EC_SCL	9	I	Hi-Z	I2C slave serial clock input. Tie to pullup voltage through a resistor when used or unused. Connect to Embedded Controller (EC).
I2C_EC_SDA	8	I/O	Hi-Z	I2C slave serial data. Open-drain output. Tie to pullup voltage through a resistor when used or unused. Connect to Embedded Controller (EC).
I2C_EC_IRQ	10	O	Hi-Z	I2C slave interrupt. Active low. Connect to external voltage through a pull-up resistor. May also be used as a general purpose digital output. Connect to Embedded Controller (EC).
LDO_1V5	4	O	—	Output of the CORE LDO. Bypass with capacitance C <sub>LDO_1V5</sub> to GND. This pin cannot source current to external circuits.

表 5-1. Pin Functions (continued)

PIN		TYPE <sup>(1)</sup>	RESET	Description
NAME	NO.			
LDO_3V3	1	O	—	Output of supply switched from VIN_3V3 or VBUS LDO. Bypass with capacitance $C_{LDO\_3V3}$ to GND.
POL	13	O	Hi-Z	Open-drain logic output that gives the information needed to mux the superspeed lines. It is asserted low when CC2 is connected to the cable CC line.
PP5V	28,29	I	—	5-V System Supply to VBUS, supply for CCy pins as VCONN.
SINK	18	O	Hi-Z	Open-drain logic output that asserts low when a Type-C Sink is identified on the CC lines.
USB_N	23	I/O	Hi-Z	I/O for BC 1.2 functionality. Connect to the USB D- line.
USB_P	22	I/O	Hi-Z	I/O for BC 1.2 functionality. Connect to the USB D+ line.
VBUS	26,27	I/O		5-V to 20-V input. Bypass with capacitance $C_{VBUS}$ to GND.
VIN_3V3	32	I	—	Supply for core circuitry and I/O. Bypass with capacitance $C_{VIN\_3V3}$ to GND.
NC	21,31	—	—	This pin has no functionality. Leave floating.

(1) I = input, O = output, I/O = input and output, GPIO = general purpose digital input and output

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT	
Input voltage range <sup>(2)</sup>	PP5V	- 0.3	6	V	
	VIN_3V3	- 0.3	4		
	ADCIN1, ADCIN2	- 0.3	4		
	Source current	VBUS <sup>(4)</sup>	- 0.3	28	V
		CC1, CC2 <sup>(4)</sup>	- 0.5	26	
		SINK, FAULT, CHG_HI, USB_P, USB_N, CTL, POL, DEBUG, EN	-0.3	6.0	
		I2C_EC_SDA, I2C_EC_SCL, I2C_EC_IRQ	- 0.3	4	
Output voltage range <sup>(2)</sup>	LDO_1V5 <sup>(3)</sup>	- 0.3	2	V	
	LDO_3V3 <sup>(3)</sup>	- 0.3	4		
Source current	Source or sink current VBUS	internally limited		A	
	Positive source current on CC1, CC2	1			
	Positive sink current on CC1, CC2 while VCONN switch is enabled	1			
	positive sink current for I2C_EC_SDA, I2C_EC_SCL	internally limited			
	positive source current for LDO_3V3, LDO_1V5	internally limited			
T <sub>J</sub> Operating junction temperature		- 40	175	°C	
T <sub>STG</sub> Storage temperature		- 55	150	°C	

- (1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network GND. Connect the GND pin directly to the GND plane of the board.
- (3) Do not apply voltage to these pins.
- (4) A TVS with a break down voltage falling between the Recommended max and the Abs max value is recommended such as TVS2200.

### 6.2 ESD Ratings

PARAMETER		TEST CONDITIONS	VALUE	UNIT
V <sub>(ESD)</sub>	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	±1000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	±500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT	
V <sub>I</sub>	Input voltage range <sup>(1)</sup>	VIN_3V3	3.0	3.6	V
		PP5V	4.9	5.5	
		VBUS	4	22	

### 6.3 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

			MIN	MAX	UNIT
V <sub>IO</sub>	I/O voltage range <sup>(1)</sup>	I2C_EC_SDA, I2C_EC_SCL, I2C_EC_IRQ, ADCIN1, ADCIN2	0	3.6	V
		SINK, FAULT, CHG_HI, USB_P, USB_N, CTL, POL, DEBUG, EN	0	5.5	
		CC1, CC2	0	5.5	
I <sub>O</sub>	Output current (from PP5V)	VBUS		3	A
		CC1, CC2		315	mA
I <sub>O</sub>	Output current (from VBUS LDO)	current from LDO_3V3		5	mA
T <sub>A</sub>	Ambient operating temperature	I <sub>PP_5V</sub> ≤ 1.5 A, I <sub>PP_CABLE</sub> ≤ 315 mA	-40	105	°C
		I <sub>PP_5V</sub> ≤ 3 A, I <sub>PP_CABLE</sub> ≤ 315 mA	-40	85	
T <sub>J</sub>	Operating junction temperature		-40	125	°C

(1) All voltage values are with respect to network GND. All GND pins must be connected directly to the GND plane of the board.

### 6.4 Recommended Capacitance

over operating free-air temperature range (unless otherwise noted)

PARAMETER <sup>(1)</sup>		VOLTAGE RATING	MIN	NOM	MAX	UNIT
C <sub>VIN_3V3</sub>	Capacitance on VIN_3V3	6.3 V	5	10		μF
C <sub>LDO_3V3</sub>	Capacitance on LDO_3V3	6.3 V	5	10	25	μF
C <sub>LDO_1V5</sub>	Capacitance on LDO_1V5	4 V	4.5		12	μF
C <sub>VBUS</sub>	Capacitance on VBUS	25 V	1	4.7	10	μF
C <sub>PP5V</sub>	Capacitance on PP5V	10 V	120			μF

(1) Capacitance values do not include any derating factors. For example, if 5.0 μF is required and the external capacitor value reduces by 50% at the required operating voltage, then the required external capacitor value would be 10 μF.

### 6.5 Thermal Information

THERMAL METRIC <sup>(1)</sup>		TPS25814	UNIT
		QFN (RSM)	
		32 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	30.5	°C/W
R <sub>θJC (top)</sub>	Junction-to-case (top) thermal resistance	24.5	°C/W
R <sub>θJC</sub>	Junction-to-board (bottom) thermal resistance	2	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	9.8	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	0.2	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	9.7	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

### 6.6 Power Supply Characteristics

Operating under these conditions unless otherwise noted: 3.0 V ≤ V<sub>VIN\_3V3</sub> ≤ 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>VIN_3V3, VBUS</b>						
V <sub>VBUS_UVLO</sub>	VBUS UVLO threshold.	rising	3.6		3.9	V
		falling	3.5		3.8	
		hysteresis		0.1		

## 6.6 Power Supply Characteristics (continued)

Operating under these conditions unless otherwise noted:  $3.0\text{ V} \leq V_{\text{VIN}_3\text{V3}} \leq 3.6\text{ V}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{\text{VIN3V3\_UVLO}}$	voltage required on VIN_3V3 for power on	rising, $V_{\text{VBUS}}=0$	2.56	2.66	2.76	V
		falling, $V_{\text{VBUS}}=0$	2.44	2.54	2.64	
		hysteresis	0.12			
<b>LDO_3V3, LDO_1V5</b>						
$V_{\text{LDO\_3V3}}$	voltage on LDO_3V3	$V_{\text{VIN\_3V3}} = 0\text{V}$ , $10\ \mu\text{A} \leq I_{\text{LOAD}} \leq 18\ \text{mA}$ , $V_{\text{VBUS}} \geq 3.9\text{V}$	3.0	3.4	3.6	V
$R_{\text{LDO\_3V3}}$	Rdson of VIN_3V3 to LDO_3V3	$I_{\text{LDO\_3V3}}=50\text{mA}$	1.4			$\Omega$
$V_{\text{LDO\_1V5}}$	voltage on LDO_1V5	up to maximum internal loading condition.	1.49	1.5	1.65	V

## 6.7 Power Consumption

Operating under these conditions unless otherwise noted:  $3.0\text{ V} \leq V_{\text{VIN}_3\text{V3}} \leq 3.6\text{ V}$ , no GPIO loading

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{\text{VIN\_3V3\_ActSrc}}$	current into VIN_3V3	Active Source mode: $V_{\text{VBUS}}=5.0\text{V}$ , $V_{\text{VIN\_3V3}}=3.3\text{V}$	3			mA
$I_{\text{VIN\_3V3\_IdlSrc}}$	current into VIN_3V3	Idle Source mode: $V_{\text{VBUS}}=5.0\text{V}$ , $V_{\text{VIN\_3V3}}=3.3\text{V}$	1.0			mA
$P_{\text{MstbySrc}}$	Power drawn into PP5V and VIN_3V3 in Modern Standby Source Mode	CCm floating, CCn tied to GND through 5.1k $\Omega$ , $V_{\text{PP5V}} = 5\text{V}$ , $V_{\text{VIN\_3V3}}=3.3\text{V}$ , $I_{\text{VBUS}}=0$ , $T_{\text{J}}=25^{\circ}\text{C}$	4.5			mW
$I_{\text{VIN\_3V3\_SleepSrc}}$	current into VIN_3V3	Sleep source mode: $V_{\text{VBUS}}=0\text{V}$ , $V_{\text{VIN\_3V3}}=3.3\text{V}$	61			$\mu\text{A}$
$I_{\text{PP5V\_Sleep}}$	current into PP5V	Sleep mode: $V_{\text{VBUS}}=0\text{V}$ , $V_{\text{VIN\_3V3}}=3.3\text{V}$	2			$\mu\text{A}$
$I_{\text{PP5V\_ActSrc}}$	current into PP5V	Active Source mode: $V_{\text{VBUS}}=5.0\text{V}$ , $V_{\text{VIN\_3V3}}=3.3\text{V}$ . No external load on VBUS.	0.5			mA

## 6.8 PP\_5V Power Switch Characteristics

Operating under these conditions unless otherwise noted:  $3.0\text{ V} \leq V_{\text{VIN}_3\text{V3}} \leq 3.6\text{ V}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\text{PP\_5V}}$	Resistance from PP5V to VBUS	$I_{\text{LOAD}} = 3\ \text{A}$ , $T_{\text{J}}=25^{\circ}\text{C}$	36 38			m $\Omega$
$R_{\text{PP\_5V}}$	Resistance from PP5V to VBUS	$I_{\text{LOAD}} = 3\ \text{A}$ , $T_{\text{J}}=125^{\circ}\text{C}$	36 53			m $\Omega$
$I_{\text{PP5V\_REV}}$	VBUS to PP5V leakage current	$V_{\text{PP5V}} = 0\text{V}$ , $V_{\text{VBUS}} = 5.5\text{V}$ , PP_5V disabled, $T_{\text{J}} \leq 85^{\circ}\text{C}$ , measure $I_{\text{PP5V}}$	5			$\mu\text{A}$
$I_{\text{PP5V\_FWD}}$	PP5V to VBUS leakage current	$V_{\text{PP5V}} = 5.5\text{V}$ , $V_{\text{VBUS}} = 0\text{V}$ , PP_5V disabled, $T_{\text{J}} \leq 85^{\circ}\text{C}$ , measure $I_{\text{VBUS}}$	15			$\mu\text{A}$
$I_{\text{LIM5V}}$	Current limit setting	1.5A setting	2.3	2.70		A
$I_{\text{LIM5V}}$	Current limit setting	3.0A setting	3.22	3.78		A
$I_{\text{VBUS}}$	PP5V to VBUS current sense accuracy	$3.64\text{A} \geq I_{\text{VBUS}} \geq 1\text{A}$	3.05	3.5	3.75	A/V
$V_{\text{PP\_5V\_RCP}}$	RCP clears and PP_5V starts turning on when $V_{\text{VBUS}} - V_{\text{PP5V}} < V_{\text{PP\_5V\_RCP}}$ . Measure $V_{\text{VBUS}} - V_{\text{PP5V}}$		10	20		mV
$t_{\text{IOS\_PP\_5V}}$	response time to VBUS short circuit	VBUS to GND through 10m $\Omega$ , $C_{\text{VBUS}}=0$	1.15			$\mu\text{s}$

## 6.8 PP\_5V Power Switch Characteristics (continued)

Operating under these conditions unless otherwise noted:  $3.0\text{ V} \leq V_{VIN\_3V3} \leq 3.6\text{ V}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{PP\_5V\_ovp}$	response time to $V_{VBUS} > V_{OVP4RCP}$	Enable PP_5V, $I_{RpDef}$ being drawn from PP5V, configure $V_{OVP4RCP}$ to setting 2, ramp $V_{VBUS}$ from 4V to 20V at 100 V/ms, $C_{PP5V} = 2.5\ \mu\text{F}$ , measure time from OVP detection until reverse current < 100 mA		4.5		$\mu\text{s}$
$t_{PP\_5V\_uvlo}$	response time to $V_{PP5V} < V_{PP5V\_UVLO}$ , PP_VBUS is deemed off when $V_{VBUS} < 0.8\text{ V}$	$R_L = 100\ \Omega$ , no external capacitance on VBUS		4		$\mu\text{s}$
$t_{PP\_5V\_rcp}$	response time to $V_{PP5V} < V_{VBUS} + V_{PP\_5V\_RCP}$	$V_{PP5V} = 5.5\text{ V}$ , $I_{RpDef}$ being drawn from PP5V, enable PP_5V, configure $V_{OVP4RCP}$ to setting 2, ramp $V_{VBUS}$ from 4V to 21.5V at 10 V/ $\mu\text{s}$ , measure $V_{PP5V}$ . $C_{PP5V} = 104\ \mu\text{F}$ , $C_{VBUS} = 10\ \mu\text{F}$ , measure time from RCP detection until reverse current < 100 mA.		0.7		$\mu\text{s}$
$t_{LIM}$	Current limit deglitch time			5.1		ms
$t_{ON}$	from enable signal to VBUS at 90% of final value	$R_L = 100\ \Omega$ , $V_{PP5V} = 5\text{ V}$ , $C_L = 0$	2.3	3.3	4.3	ms
$t_{OFF}$	from disable signal to VBUS at 10% of final value	$R_L = 100\ \Omega$ , $V_{PP5V} = 5\text{ V}$ , $C_L = 0$	0.30	0.45	0.6	ms
$t_{RISE}$	VBUS from 10% to 90% of final value	$R_L = 100\ \Omega$ , $V_{PP5V} = 5\text{ V}$ , $C_L = 0$	1.2	1.7	2.2	ms
$t_{FALL}$	VBUS from 90% to 10% of initial value	$R_L = 100\ \Omega$ , $V_{PP5V} = 5\text{ V}$ , $C_L = 0$	0.06	0.1	0.14	ms

## 6.9 Power Path Supervisory

Operating under these conditions unless otherwise noted:  $3.0\text{ V} \leq V_{VIN\_3V3} \leq 3.6\text{ V}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OVP4RCP}$	VBUS over voltage protection	OVP detected when $V_{VBUS} > V_{OVP4RCP}$ (rising)	5.54	5.8	6.08	V
$V_{OVP4RCP}$	VBUS over voltage protection	falling	5.44		5.94	V
$V_{PP5V\_UVLO}$	Voltage required on PP5V	rising	3.9	4.1	4.3	V
		falling	3.8	4.0	4.2	
		hysteresis		0.1		
$I_{DSCH}$	VBUS discharge current	$V_{VBUS} = 22\text{ V}$ , measure $I_{VBUS}$	4		15	mA

## 6.10 CC Cable Detection Parameters

Operating under these conditions unless otherwise noted:  $3.0\text{ V} \leq V_{VIN\_3V3} \leq 3.6\text{ V}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>Type-C Source (Rp pull-up)</b>						
$V_{OC\_3.3}$	Unattached CCy open circuit voltage while Rp enabled, no load	$V_{LDO\_3V3} > 2.302\text{ V}$ , $R_{CC} = 47\text{ k}\Omega$	1.85			V
$V_{OC\_5}$	Attached CCy open circuit voltage while Rp enabled, no load	$V_{PP5V} > 3.802\text{ V}$ , $R_{CC} = 47\text{ k}\Omega$	2.95			V



## 6.10 CC Cable Detection Parameters (continued)

Operating under these conditions unless otherwise noted:  $3.0\text{ V} \leq V_{\text{VIN}_3\text{V}3} \leq 3.6\text{ V}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{\text{Rev}}$	Unattached reverse current on CCy	$V_{\text{CCy}} = 5.5\text{ V}$ , $V_{\text{CCx}} = 0\text{ V}$ , $V_{\text{LDO}_3\text{V}3\_UVLO} < V_{\text{LDO}_3\text{V}3} < 3.6\text{ V}$ , $V_{\text{PP5V}} = 3.8\text{ V}$ , measure current into CCy			10	$\mu\text{A}$
		$V_{\text{CCy}} = 5.5\text{ V}$ , $V_{\text{CCx}} = 0\text{ V}$ , $V_{\text{LDO}_3\text{V}3\_UVLO} < V_{\text{LDO}_3\text{V}3} < 3.6\text{ V}$ , $V_{\text{PP5V}} = 0$ , $T_J \leq 85^\circ\text{C}$ , measure current into CCy			10	
$I_{\text{RpDef}}$	current source - USB Default	$0 < V_{\text{CCy}} < 1.0\text{ V}$ , measure $I_{\text{CCy}}$	64	80	96	$\mu\text{A}$
$I_{\text{Rp1.5}}$	current source - 1.5A	$4.75\text{ V} < V_{\text{PP5V}} < 5.5\text{ V}$ , $0 < V_{\text{CCy}} < 1.5\text{ V}$ , measure $I_{\text{CCy}}$	166	180	194	$\mu\text{A}$
$I_{\text{Rp3.0}}$	current source - 3.0A	$4.75\text{ V} < V_{\text{PP5V}} < 5.5\text{ V}$ , $0 < V_{\text{CCy}} < 2.45\text{ V}$ , measure $I_{\text{CCy}}$	304	330	356	$\mu\text{A}$

## 6.11 CC VCONN Parameters

Operating under these conditions unless otherwise noted:  $3.0\text{ V} \leq V_{\text{VIN}_3\text{V}3} \leq 3.6\text{ V}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{\text{PP\_CABLE}}$	Rdson of the VCONN path	$V_{\text{PP5V}}=5\text{ V}$ , $I_L = 250\text{ mA}$ , measure resistance from PP5V to CCy			1.2	$\Omega$
$I_{\text{LIMVC}}$	short circuit current limit	$V_{\text{PP5V}}=5\text{ V}$ , $R_L=10\text{ m}\Omega$ , measure $I_{\text{CCy}}$	540	600	660	mA
$I_{\text{CC2PP5V}}$	Reverse leakage current through VCONN FET	VCONN disabled, $T_J \leq 85^\circ\text{C}$ , $V_{\text{CCy}} = 5.5\text{ V}$ , $V_{\text{PP5V}}=0\text{ V}$ , $V_{\text{VBUS}}=5\text{ V}$ , LDO forced to draw from VBUS, measure $I_{\text{CCy}}$			10	$\mu\text{A}$
$V_{\text{VC\_OVP}}$	Over-voltage protection threshold for PP_CABLE	$V_{\text{PP5V}}$ rising	5.6	5.9	6.2	V
$V_{\text{VC\_RCP}}$	Reverse current protection threshold for PP_CABLE, sourcing VCONN through CCx	$V_{\text{PP5V}} \geq 4.9\text{ V}$ , $V_{\text{CCy}} = V_{\text{PP5V}}$ , $V_{\text{CCx}}$ rising	60	200	340	mV
		$V_{\text{PP5V}} \geq 4.9\text{ V}$ , $V_{\text{CCy}} \leq 4\text{ V}$ , $V_{\text{CCx}}$ rising	210	340	470	mV
$t_{\text{VCILIM}}$	Current clamp deglitch time			1.3		ms
$t_{\text{PP\_CABLE\_FSD}}$	Time to disable PP_CABLE after $V_{\text{PP5V}} > V_{\text{VC\_OVP}}$ or $V_{\text{CCx}} - V_{\text{PP5V}} > V_{\text{VC\_RCP}}$	$C_L=0$		0.5		$\mu\text{s}$
$t_{\text{PP\_CABLE\_off}}$	from disable signal to CCy at 10% of final value	$I_L = 250\text{ mA}$ , $V_{\text{PP5V}} = 5\text{ V}$ , $C_L=0$	100	200	300	$\mu\text{s}$
$t_{\text{IOS\_PP\_CABLE}}$	response time to short circuit	$V_{\text{PP5V}}=5\text{ V}$ , for short circuit $R_L = 10\text{ m}\Omega$ .		2		$\mu\text{s}$

## 6.12 Thermal Shutdown Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$T_{\text{SD\_MAIN}}$	Temperature shutdown threshold	Temperature rising	145	160	175	$^\circ\text{C}$
		hysteresis		20		$^\circ\text{C}$
$T_{\text{SD\_PP5V}}$	Temperature controlled shutdown threshold. The PP_5V and PP_CABLE power paths have local sensors that disables them when this temperature is exceeded.	Temperature rising	135	150	165	$^\circ\text{C}$
		hysteresis		10		$^\circ\text{C}$

## 6.13 Input/Output (I/O) Characteristics

Operating under these conditions unless otherwise noted:  $3.0\text{ V} \leq V_{VIN\_3V3} \leq 3.6\text{ V}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>CHG_HI, CTL, EN</b>						
GPIO_VIH	GPIOx high-level input voltage	$V_{LDO\_3V3} = 3.3\text{V}$	1.3			V
GPIO_VIL	GPIOx low-level input voltage	$V_{LDO\_3V3} = 3.3\text{V}$			0.54	V
GPIO_HYS	GPIOx input hysteresis voltage	$V_{LDO\_3V3} = 3.3\text{V}$	0.09			V
GPIO_ILKG	GPIOx leakage current	$V_{GPIOx} = 3.45\text{ V}$	- 1		1	$\mu\text{A}$
GPIO_RPD	GPIOx internal pull-down	pull-down enabled	50	100	150	$\text{k}\Omega$
GPIO_DG	GPIOx input deglitch			20		ns
<b>Status Outputs</b>						
GPIO_VOL	GPIOx output low voltage	$V_{LDO\_3V3} = 3.3\text{V}$ , $I_{GPIOx} = 2\text{mA}$			0.4	V
<b>ADCIN1, ADCIN2</b>						
ADCIN_ILKG	ADCINx leakage current	$V_{ADCINx} = 3.45\text{ V}$ , $V_{VIN\_3V3} = 3.3$	- 1		1	$\mu\text{A}$
$t_{BOOT}$	time from LDO_3V3 going high until ADCINx is read for configuration			10		ms

## 6.14 BC1.2 Characteristics

Operating under these conditions unless otherwise noted:  $3.0\text{ V} \leq V_{VIN\_3V3} \leq 3.6\text{ V}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>Advertisement</b>						
$V_{DX\_SRC}$	Source voltage	$C_{USB\_P} \leq 600\text{ pF}$	0.55	0.6	0.65	V
$V_{DX\_ILIM}$	$V_{DX\_SRC}$ current limit		250		400	$\mu\text{A}$
$I_{DX\_SNK}$	Sink Current	$V_{USB\_P} \geq 250\text{ mV}$	25	75	125	$\mu\text{A}$
$I_{DX\_SNK}$	Sink Current	$V_{USB\_N} \geq 250\text{ mV}$	25	75	125	$\mu\text{A}$
$R_{DCP\_DAT}$	Dedicated Charging Port Resistance	$0.5\text{ V} \leq V_{USB\_P} \leq 0.7\text{ V}$ , $25\text{ }\mu\text{A} \leq I_{USB\_N} \leq 175\text{ }\mu\text{A}$			200	$\Omega$

## 6.15 I2C Requirements and Characteristics

Operating under these conditions unless otherwise noted:  $3.0\text{ V} \leq V_{VIN\_3V3} \leq 3.6\text{ V}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>I2C_EC_IRQ</b>						
OD_VOL_IRQ	Low level output voltage	$I_{OL} = 2\text{ mA}$			0.4	V
OD_LKG_IRQ	Leakage Current	Output is Hi-Z, $V_{I2Cx\_IRQ} = 3.45\text{ V}$	- 1		1	$\mu\text{A}$
<b>SDA and SCL Common Characteristics (Slave)</b>						
$V_{IL}$	Input low signal	$V_{LDO\_3V3} = 3.3\text{V}$ ,			0.54	V
$V_{IH}$	Input high signal	$V_{LDO\_3V3} = 3.3\text{V}$ ,	1.3			V
$V_{HYS}$	Input hysteresis	$V_{LDO\_3V3} = 3.3\text{V}$	0.165			V
$V_{OL}$	Output low voltage	$I_{OL} = 3\text{ mA}$			0.36	V
$I_{LEAK}$	Input leakage current	Voltage on pin = $V_{LDO\_3V3}$	- 3		3	$\mu\text{A}$
$I_{OL}$	Max output low current	$V_{OL} = 0.4\text{ V}$	15			mA
$I_{OL}$	Max output low current	$V_{OL} = 0.6\text{ V}$	20			mA
$t_f$	Fall time from $0.7 \cdot V_{DD}$ to $0.3 \cdot V_{DD}$	$V_{DD} = 1.8\text{V}$ , $10\text{ pF} \leq C_b \leq 400\text{ pF}$	12		80	ns
$t_f$	Fall time from $0.7 \cdot V_{DD}$ to $0.3 \cdot V_{DD}$	$V_{DD} = 3.3\text{V}$ , $10\text{ pF} \leq C_b \leq 400\text{ pF}$	12		150	ns
$t_{SP}$	I2C pulse width suppressed				50	ns
$C_i$	pin capacitance (internal)				10	pF

## 6.15 I2C Requirements and Characteristics (continued)

Operating under these conditions unless otherwise noted:  $3.0\text{ V} \leq V_{\text{VIN } 3\text{V}3} \leq 3.6\text{ V}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$C_b$	Capacitive load for each bus line (external)				400	pF
<b>SDA and SCL Standard Mode Characteristics (Slave)</b>						
$f_{\text{SCLS}}$	Clock frequency for slave	$V_{\text{DD}} = 1.8\text{V or } 3.3\text{V}$			100	kHz
$t_{\text{VD;DAT}}$	Valid data time	Transmitting Data, $V_{\text{DD}} = 1.8\text{V or } 3.3\text{V}$ , SCL low to SDA output valid			3.45	$\mu\text{s}$
$t_{\text{VD;ACK}}$	Valid data time of ACK condition	Transmitting Data, $V_{\text{DD}} = 1.8\text{V or } 3.3\text{V}$ , ACK signal from SCL low to SDA (out) low			3.45	$\mu\text{s}$
<b>SDA and SCL Fast Mode Characteristics (Slave)</b>						
$f_{\text{SCLS}}$	Clock frequency for slave	$V_{\text{DD}} = 1.8\text{V or } 3.3\text{V}$	100		400	kHz
$t_{\text{VD;DAT}}$	Valid data time	Transmitting data, $V_{\text{DD}} = 1.8\text{V}$ , SCL low to SDA output valid			0.9	$\mu\text{s}$
$t_{\text{VD;ACK}}$	Valid data time of ACK condition	Transmitting data, $V_{\text{DD}} = 1.8\text{V or } 3.3\text{V}$ , ACK signal from SCL low to SDA (out) low			0.9	$\mu\text{s}$

### 6.16 Typical Characteristics

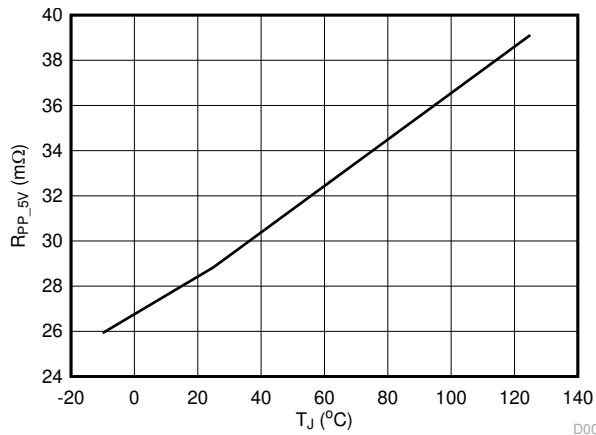


图 6-1. PP\_5Vx Rdson vs. Temperature

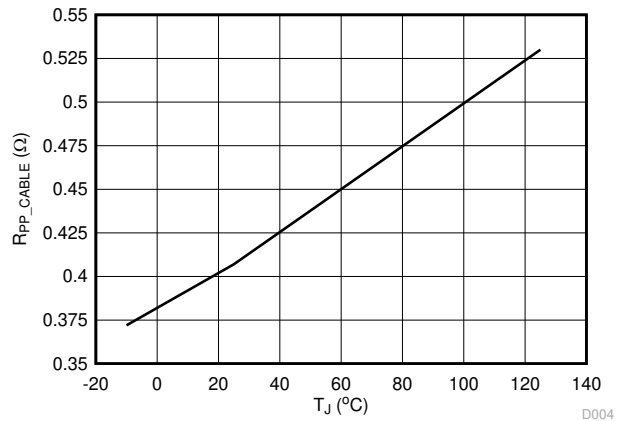


图 6-2. PP\_CABLEx Rdson vs. Temperature

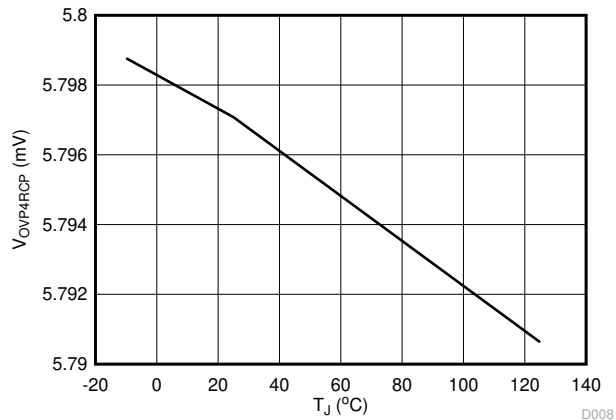


图 6-3. VOVP4RCP vs. Temperature

## 7 Parameter Measurement Information

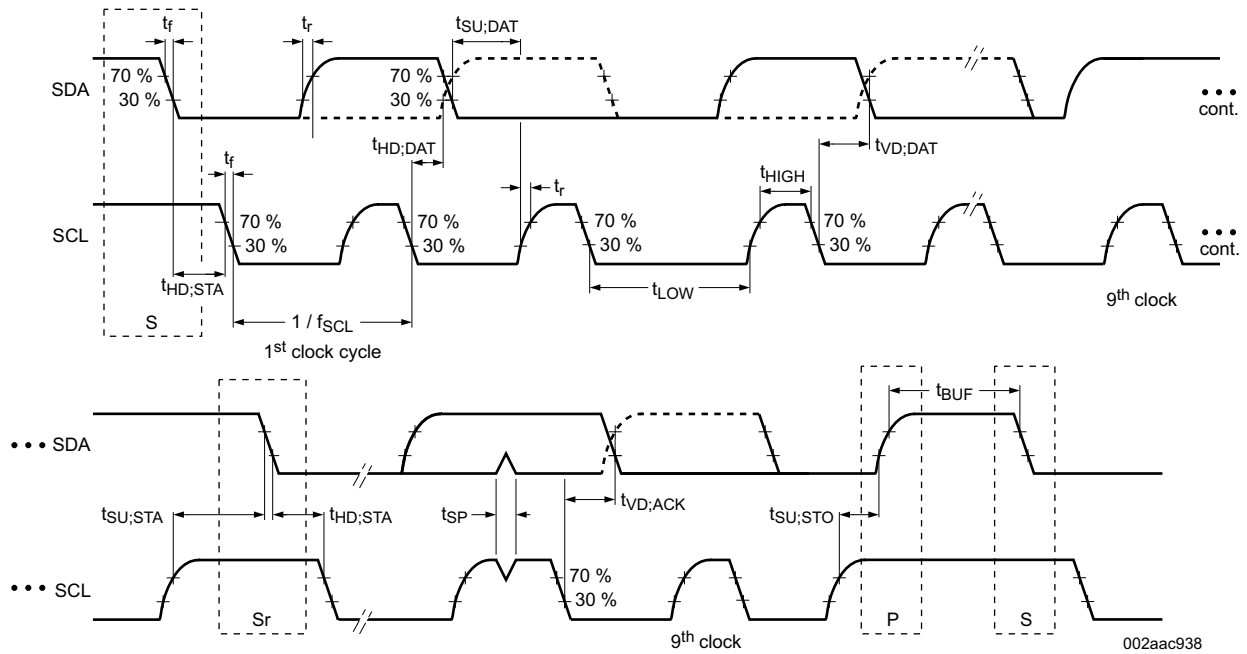


图 7-1. I<sup>2</sup>C Slave Interface Timing

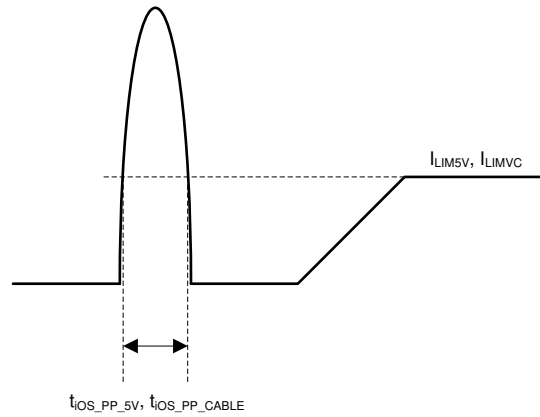


图 7-2. Short-Circuit Response Time for Internal Power Paths PP\_5V and PP\_CABLE

## 8 Detailed Description

### 8.1 Overview

The TPS25814 is a fully-integrated USB Type-C Source management device providing cable plug and orientation detection for USB Type-C receptacle. The TPS25814 may also control an attached super-speed multiplexer to simultaneously support USB data .

The TPS25814 is divided into several main sections: the cable plug and orientation detection circuitry, the port power switches, the power management circuitry and the digital core.

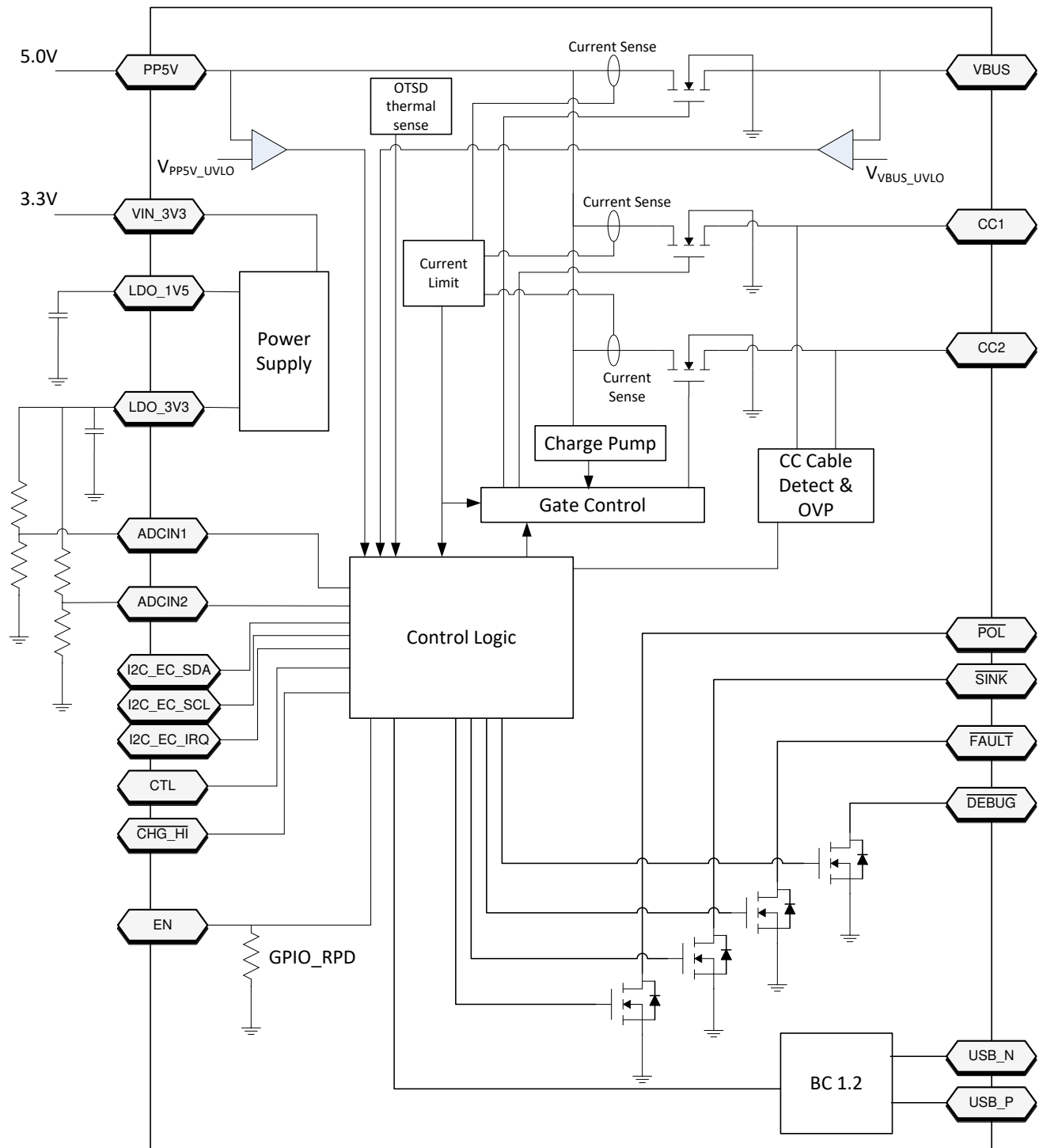
The cable plug and orientation detection analog circuitry automatically detects a USB Type-C cable plug insertion and also automatically detects the cable orientation. For a high-level block diagram of cable plug and orientation detection, a description of its features and more detailed circuitry, see the [Cable Plug and Orientation Detection](#).

The port power switches provide power to the VBUS pin and also to the CC1 or CC2 pins based on the detected plug orientation. For a high-level block diagram of the port power switches, a description of its features and more detailed circuitry, see the [Power Paths](#).

The TPS25814 has a I<sup>2</sup>C slave port to be controlled by host processor (see the [I<sup>2</sup>C Interface](#)).

The TPS25814 also integrates a thermal shutdown mechanism and runs off of accurate clocks provided by the integrated oscillator.

## 8.2 Functional Block Diagram



## 8.3 Feature Description

### 8.3.1 Power Paths

The TPS25814 has internal power paths: PP\_5V and PP\_CABLE. Each power path is described in detail in this section.

#### 8.3.1.1 Internal Sourcing Power Paths

Figure 8-1 shows the TPS25814 internal sourcing power paths. The TPS25814 features two internal 5-V sourcing power paths. The path from PP5V to VBUS is called PP\_5V. The path from PP5V to CCx is called PP\_CABLE. Each path contains current clamping protection, overvoltage protection, UVLO protection and temperature sensing circuitry. PP\_5V may conduct up to 3 A continuously, while PP\_CABLE may conduct up to 315 mA continuously. When disabled, the blocking FET protects the PP5V rail from high-voltage that may appear on VBUS.

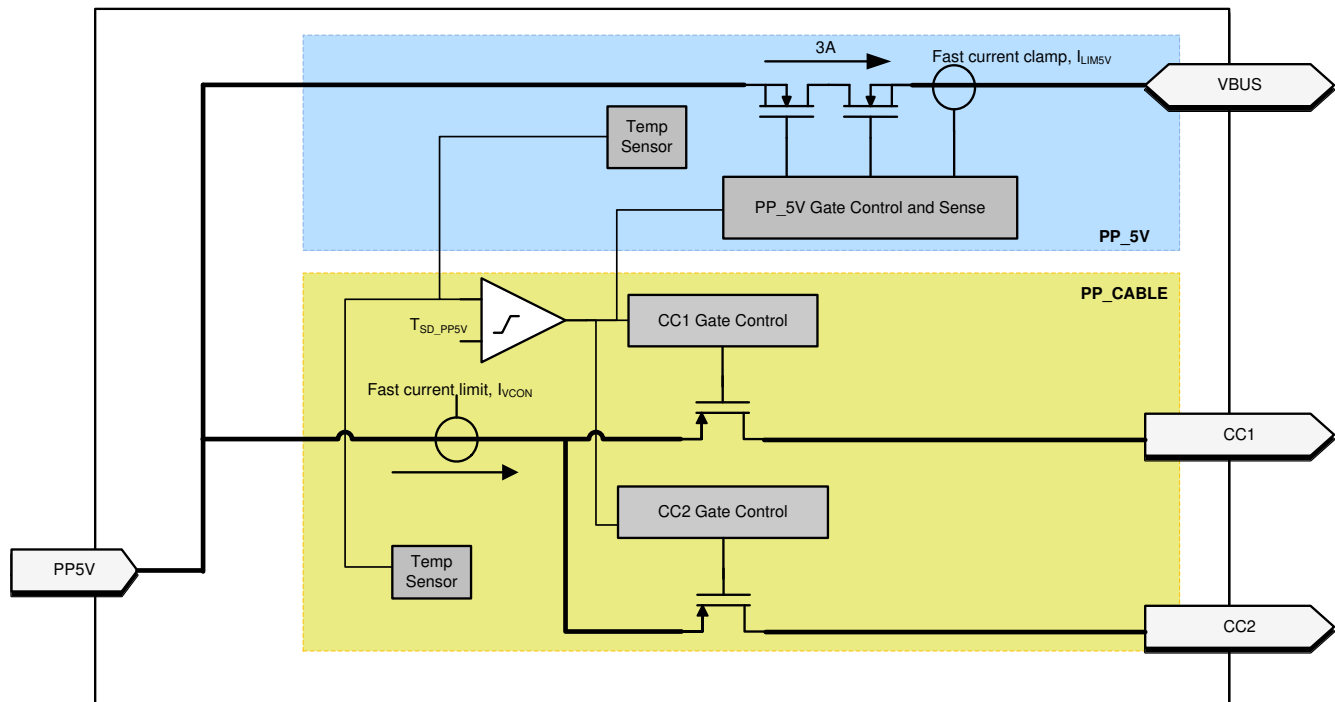


图 8-1. Port Power Switches

##### 8.3.1.1.1 PP\_5V Current Clamping

The current through the internal PP\_5V path are current limited to  $I_{LIM5V}$ . The  $I_{LIM5V}$  value is configured by the  $\overline{CHG\_HI}$  pin as well as ADCIN1 and ADCIN2 pin strapping. When the current through the switch exceeds  $I_{LIM5V}$ , the current limiting circuit activates within  $t_{IOS\_PP\_5V}$  and the path behaves as a constant current source. If the duration of the overcurrent event exceeds  $t_{LIM}$ , the PP\_5V switch is disabled.

##### 8.3.1.1.2 PP\_5V Local Overtemperature Shut Down (OTSD)

When PP\_5V clamps the current, the temperature of the switch will begin to increase. When the local temperature sensors of PP\_5V or PP\_CABLE detect that  $T_J > T_{SD\_PP5V}$  the PP\_5V switch is disabled and the affected port enters the USB Type-C ErrorRecovery state.

##### 8.3.1.1.3 PP\_5V OVP

When the voltage on a port's VBUS pin exceeds  $V_{OVP4RCP}$  while PP\_5V is enabled, then PP\_5V is disabled within  $t_{PP\_5V\_ovp}$  and the port enters into the Type-C ErrorRecovery state.



#### 8.3.1.1.4 PP\_5V UVLO

If the PP5V pin voltage falls below its undervoltage lock out threshold ( $V_{PP5V\_UVLO}$ ) while PP\_5V is enabled, then PP\_5V is disabled within  $t_{PP\_5V\_uvlo}$  and the port that had PP\_5V enabled enters into the Type-C ErrorRecovery state.

#### 8.3.1.1.5 PP\_5Vx Reverse Current Protection

If  $V_{VBUS} - V_{PP5V} > V_{PP\_5V\_RCP}$ , then the PP\_5V path is automatically disabled within  $t_{PP\_5V\_rcp}$ . If the RCP condition clears, then the PP\_5V path is automatically enabled within  $t_{ON}$ .

#### 8.3.1.1.6 PP\_CABLE Current Clamp

When enabled and providing VCONN power the TPS25814 PP\_CABLE power switch clamps the current to  $I_{VCON}$ . When the current through the PP\_CABLE switch exceeds  $I_{VCON}$ , the current clamping circuit activates within  $t_{IOS\_PP\_CABLE}$  and the switch behaves as a constant current source.

#### 8.3.1.1.7 PP\_CABLE Local Overtemperature Shut Down (OTSD)

When PP\_CABLE clamps the current, the temperature of the switch will begin to increase. When the local temperature sensors of PP\_5V or PP\_CABLE detect that  $T_J > T_{SD\_PP5V}$  the PP\_CABLE switch is disabled and latched off within  $t_{PP\_CABLE\_off}$ . The port then enters the USB Type-C ErrorRecovery state.

#### 8.3.1.1.8 PP\_CABLE UVLO

If the PP5V pin voltage falls below its undervoltage lock out threshold ( $V_{PP5V\_UVLO}$ ), then the PP\_CABLE switch is automatically disabled within  $t_{PP\_CABLE\_off}$ .

### 8.3.2 Cable Plug and Orientation Detection

图 8-2 shows the plug and orientation detection block at each CCy pin (CC1, CC2). Each pin has identical detection circuitry.

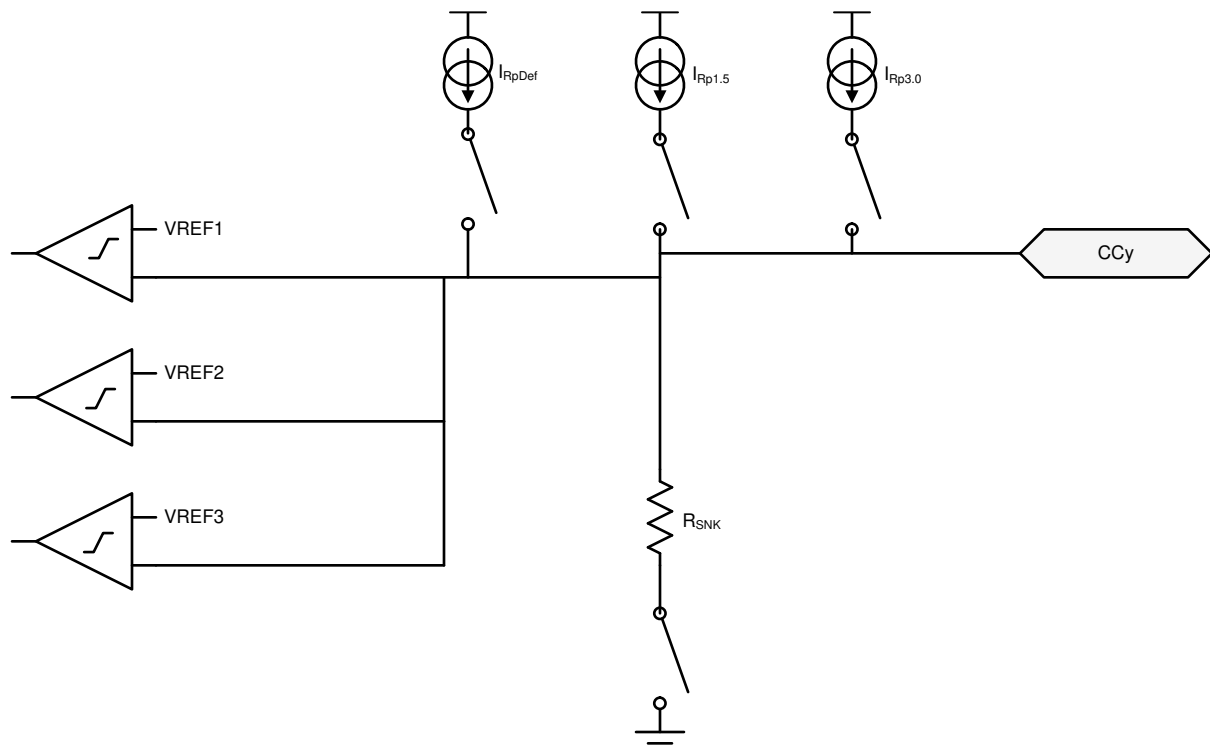


图 8-2. Plug and Orientation Detection Block

### 8.3.2.1 Configured as a Source

When configured as a source, the TPS25814 detects when a cable or a Sink is attached using the CC1 and CC2 pins. When in a disconnected state, the TPS25814 monitors the voltages on these pins to determine what, if anything, is connected. See [USB Type-C Specification](#) for more information.

表 8-1 shows the Cable Detect States for a Source.

表 8-1. Cable Detect States for a Source

CC1	CC2	CONNECTION STATE	RESULTING ACTION
Open	Open	Nothing attached	Continue monitoring both CCy pins for attach. Power is not applied to VBUS or VCONN.
Rd	Open	Sink attached	Monitor CC1 for detach. Power is applied to VBUS but not to VCONN (CC2).
Open	Rd	Sink attached	Monitor CC2 for detach. Power is applied to VBUS but not to VCONN (CC1).
Ra	Open	Powered Cable-No UFP attached	Monitor CC2 for a Sink attach and CC1 for cable detach. Power is not applied to VBUS or VCONN (CC1).
Open	Ra	Powered Cable-No UFP attached	Monitor CC1 for a Sink attach and CC2 for cable detach. Power is not applied to VBUS or VCONN (CC1).
Ra	Rd	Powered Cable-UFP Attached	Provide power on VBUS and VCONN (CC1) then monitor CC2 for a Sink detach. CC1 is not monitored for a detach.
Rd	Ra	Powered Cable-UFP attached	Provide power on VBUS and VCONN (CC2) then monitor CC1 for a Sink detach. CC2 is not monitored for a detach.
Rd	Rd	Debug Accessory Mode attached	Sense either CCy pin for detach.
Ra	Ra	Audio Adapter Accessory Mode attached	Sense either CCy pin for detach.

When a TPS25814 port is configured as a Source, a current  $I_{RpDef}$  is driven out each CCy pin and each pin is monitored for different states. When a Sink is attached to the pin a pull-down resistance of  $R_d$  to GND exists. The current  $I_{RpDef}$  is then forced across the resistance  $R_d$  generating a voltage at the CCy pin. The TPS25814 applies  $I_{RpDef}$  until it closes the switch from PP5V to VBUS, at which time it may change to  $I_{Rp1.5A}$  or  $I_{Rp3.0A}$ .

When the CCy pin is connected to an active cable VCONN input, the pull-down resistance is different ( $R_a$ ). In this case the voltage on the CCy pin will be lower and the TPS25814 recognizes it as an active cable.

The voltage on CCy is monitored to detect a disconnection depending upon which  $R_p$  current source is active. When a connection has been recognized and the voltage on CCy subsequently rises above the disconnect threshold for  $t_{CC}$ , the system registers a disconnection.

### 8.3.3 Overvoltage Protection (CC1, CC2)

The TPS25814 detects when the voltage on the CC1 or CC2 pin is too high or there is reverse current into the PP5V pin and takes action to protect the system. The protective action is to disable PP\_CABLE within  $t_{PP\_CABLE\_FSD}$  and disable the USB PD transmitter.

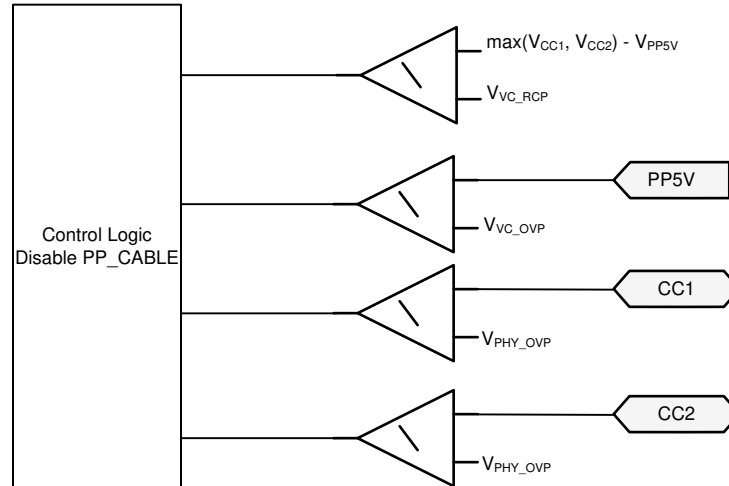


图 8-3. Overvoltage and Reverse Current Protection for CC1 and CC2

### 8.3.4 Default Behavior Configuration (ADCIN1, ADCIN2)

The ADCINx pins must be externally tied to the LDO\_3V3 pin via a resistive divider as shown in the following figure. At power-up the ADC converts the ADCINx voltage and the digital core uses these two values to determine the I<sup>2</sup>C slave address.

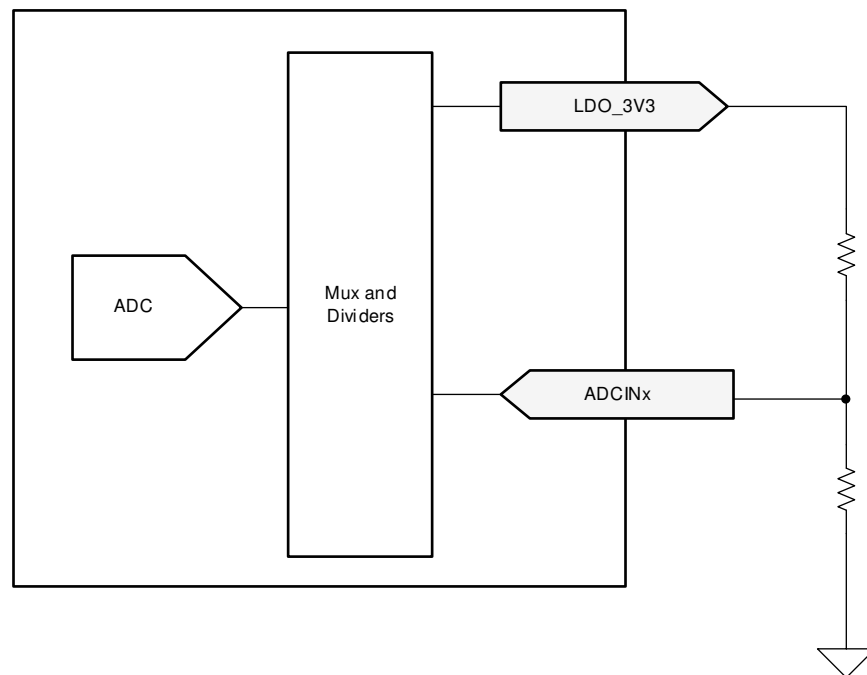


图 8-4. ADCINx Resistor Divider

The device behavior is determined in several ways depending upon the decoded value of the ADCIN1 and ADCIN2 pins. The following table shows the decoded values for different resistor divider ratios. See [Pin Strapping to Configure Default Behavior](#) for details on how the ADCINx configurations determine default device behavior. See [I<sup>2</sup>C Address Setting](#) for details on how ADCINx decoded values affects default I<sup>2</sup>C slave address.

表 8-2. Decoding of ADCIN1 and ADCIN2 Pins

DIV = R <sub>DOWN</sub> / (R <sub>UP</sub> + R <sub>DOWN</sub> )			Without Using R <sub>UP</sub> or R <sub>DOWN</sub>	ADCINx Decoded Value		
MIN	Target	MAX		ADCINx[2]	ADCINx[1]	ADCINx[0]
0	0.0114	0.0228	tie to GND	0	0	0
0.0229	0.0475	0.0722	N/A	0	0	1
0.0723	0.1074	0.1425	N/A	0	1	0
0.1425	0.1899	0.2372	N/A	0	1	1
0.2373	0.3022	0.3671	N/A	1	0	0
0.3672	0.5368	0.7064	tie to LDO_1V5	1	0	1
0.7065	0.8062	0.9060	N/A	1	1	0
0.9061	0.9530	1.0	tie to LDO_3V3	1	1	1

### 8.3.5 BC 1.2 (USB\_P, USB\_N)

The TPS25814 supports BC 1.2 as a Downstream Port using the hardware shown in the following figure.

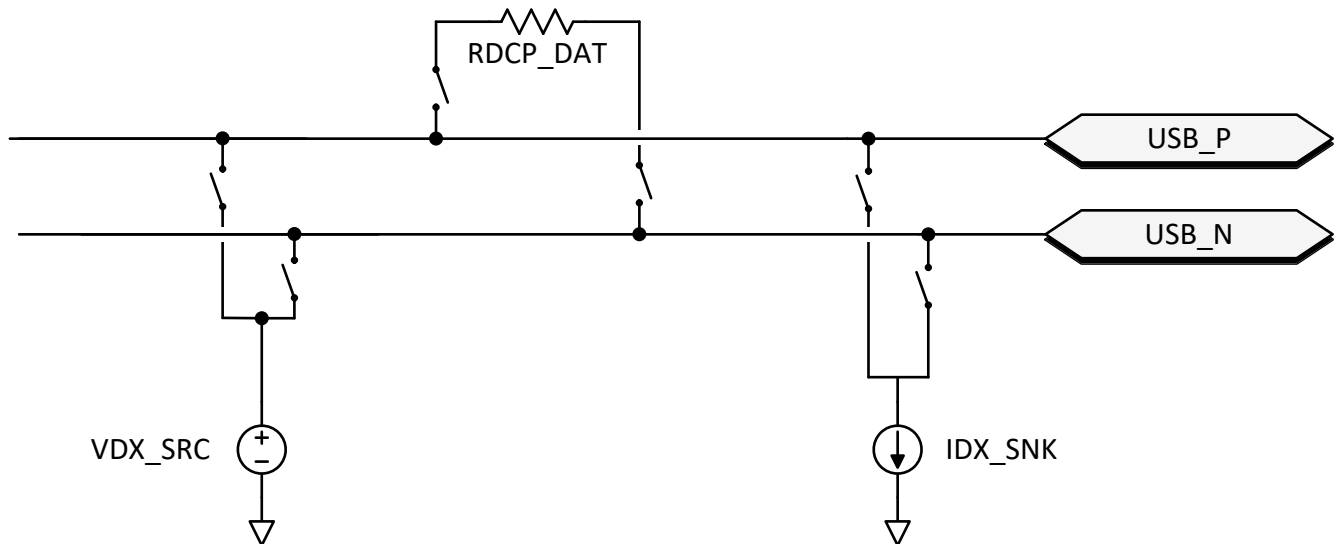


图 8-5. BC1.2 Hardware Components

### 8.3.6 Digital Interfaces

The TPS25814 contains several different digital interfaces which may be used for communicating with other devices. The available interfaces include one I<sup>2</sup>C Slave, and additional inputs and outputs.

#### 8.3.6.1 Fault Indicators ( $\overline{FAULT}$ )

When the PP\_5Vx power path is clamping the current, the  $\overline{FAULT}$  pin is asserted. It is de-asserted when the sink is unplugged or when the TPS25814 enters the Error Recovery state due to an OTSD event.

#### 8.3.6.2 Sink Attachment Indicator ( $\overline{SINK}$ )

When the TPS25814 detects a valid sink attachment it asserts the  $\overline{SINK}$  pin. The pin is de-asserted when the sink is detached or the TPS25814 enters the Error Recovery state due to an OTSD event.

#### 8.3.6.3 Polarity Indicator ( $\overline{POL}$ )

When the  $\overline{SINK}$  pin is asserted, the TPS25814 will also assert the  $\overline{POL}$  pin if CC2 is connected to the CC wire in the plug. This pin will be de-asserted upon detachment of the sink.  $\overline{POL}$  can connect to the FLIP pin of the TUSB1046 for example.

### 8.3.6.4 Power Management ( $\overline{\text{CHG\_HI}}$ )

The TPS25814 will adjust its current advertisement and its current limit when the  $\overline{\text{CHG\_HI}}$  pin changes state. When the  $\overline{\text{CHG\_HI}}$  pin is high, the TPS25814 will limit its current advertisement to the minimum current value. When the pin is low, the maximum current is advertised. The ADCIN2 pin is used to configure the minimum and maximum current (see [Pin Strapping to Configure Default Behavior](#)). To enable this behavior, the ADCIN1 must be set to enable SPM (see [Pin Strapping to Configure Default Behavior](#)). Note that until the  $\overline{\text{SINK}}$  pin is asserted, the TPS25814 will set its Type-C current advertisement to USB default current.

表 8-3.  $\overline{\text{CHG\_HI}}$  usage

ADCIN1[0]	CHG_HI pin state	Current Advertisement and Current Limit
1	Low	Maximum Current (1.5 A or 3.0 A depending on ADCIN2)
1	High	Minimum Current (USB default or 1.5 A depending on ADCIN2)
0	High or Low	Maximum Current (1.5 A or 3.0 A depending on ADCIN2)

### 8.3.6.5 Battery Charging Control (CTL)

The system can control the mode of the BC 1.2 charging used. The TPS25814 will implement the Dedicated Charging Port (DCP) mode or the Charging Data Port (CDP) mode.

表 8-4. BC 1.2 Mode Control (CTL)

CTL pin state	ADCIN2[0] Decoded Value	BC 1.2 Charging Mode
Low	0 or 1	CDP
High	0	DCP
High	1	DCP Auto Mode1

### 8.3.6.6 Debug Accessory Detection ( $\overline{\text{DEBUG}}$ )

If the TPS25814 detects the attachment of a Type-C debug accessory (Rd, Rd), then it will assert the  $\overline{\text{DEBUG}}$  pin low. Otherwise this pin is Hi-Z.

### 8.3.6.7 Disable the Port (EN)

The system may force the TPS25814 to disable the port by forcing the EN pin low. This forces the TPS25814 into the Type-C Error Recovery state. Note that the TPS25814 has an internal pull-down on this pin (GPIO\_RPD).

### 8.3.6.8 I<sup>2</sup>C Interface

The TPS25814 features an I<sup>2</sup>C interface that each use an I<sup>2</sup>C I/O driver like the one shown in [图 8-6](#). This I/O consists of an open-drain output and in input comparator with de-glitching.

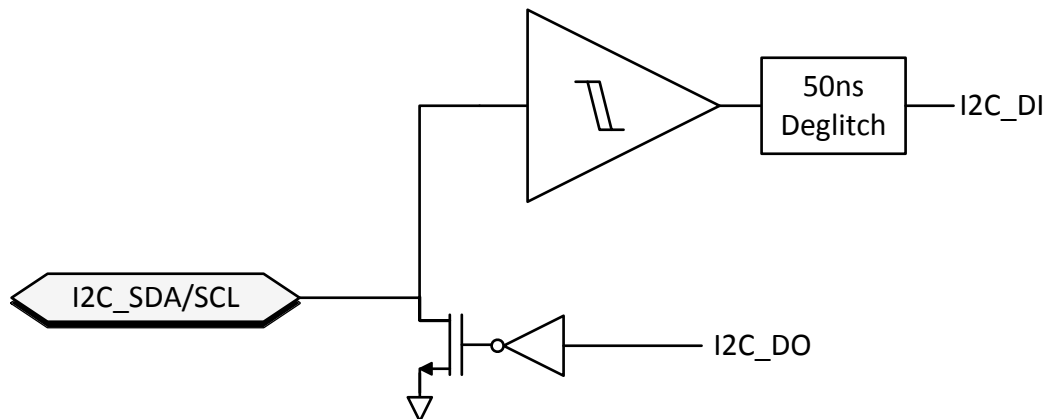


图 8-6. I<sup>2</sup>C Buffer

### 8.3.7 I<sup>2</sup>C Interface

The TPS25814 has an I<sup>2</sup>C slave interface port: I2C\_EC . I<sup>2</sup>C port I2C\_EC is comprised of the I2C\_EC\_SDA, I2C\_EC\_SCL, and I2C\_EC\_IRQ pins. These interfaces provide general status information about the TPS25814, as well as the ability to control the TPS25814 behavior, and providing information about connections detected at the USB-C receptacle.

表 8-5. I<sup>2</sup>C Summary

I2C Bus	Type	Typical Usage
I2C_EC	Slave	Connect to an Embedded Controller (EC).

#### 8.3.7.1 I<sup>2</sup>C Interface Description

The TPS25814 supports Standard and Fast mode I<sup>2</sup>C interfaces. The bidirectional I<sup>2</sup>C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a supply through a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

A master sending a Start condition, a high-to-low transition on the SDA input and output, while the SCL input is high initiates I<sup>2</sup>C communication. After the Start condition, the device address byte is sent, most significant bit (MSB) first, including the data direction bit (R/W).

After receiving the valid address byte, this device responds with an acknowledge (ACK), a low on the SDA input/output during the high of the ACK-related clock pulse. On the I<sup>2</sup>C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period as changes in the data line at this time are interpreted as control commands (Start or Stop). The master sends a Stop condition, a low-to-high transition on the SDA input and output while the SCL input is high.

Any number of data bytes can be transferred from the transmitter to receiver between the Start and the Stop conditions. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit. The device that acknowledges must pull down the SDA line during the ACK clock pulse, so that the SDA line is stable low during the high pulse of the ACK-related clock period. When a slave receiver is addressed, it must generate an ACK after each byte is received. Similarly, the master must generate an ACK after each byte that it receives from the slave transmitter. Setup and hold times must be met to ensure proper operation.

A master receiver signals an end of data to the slave transmitter by not generating an acknowledge (NACK) after the last byte has been clocked out of the slave. The master receiver holding the SDA line high does this. In this event, the transmitter must release the data line to enable the master to generate a Stop condition.

图 8-7 shows the start and stop conditions of the transfer. 图 8-8 shows the SDA and SCL signals for transferring a bit. 图 8-9 shows a data transfer sequence with the ACK or NACK at the last clock pulse.

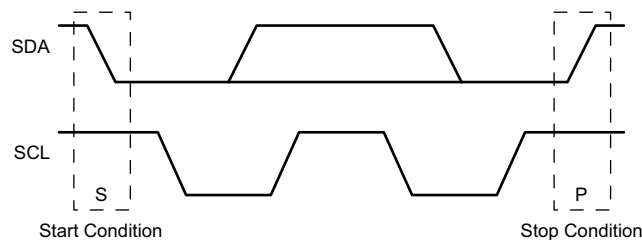


图 8-7. I<sup>2</sup>C Definition of Start and Stop Conditions

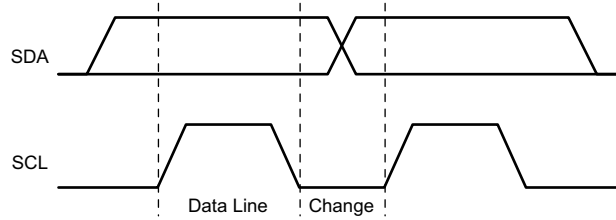


图 8-8. I<sup>2</sup>C Bit Transfer

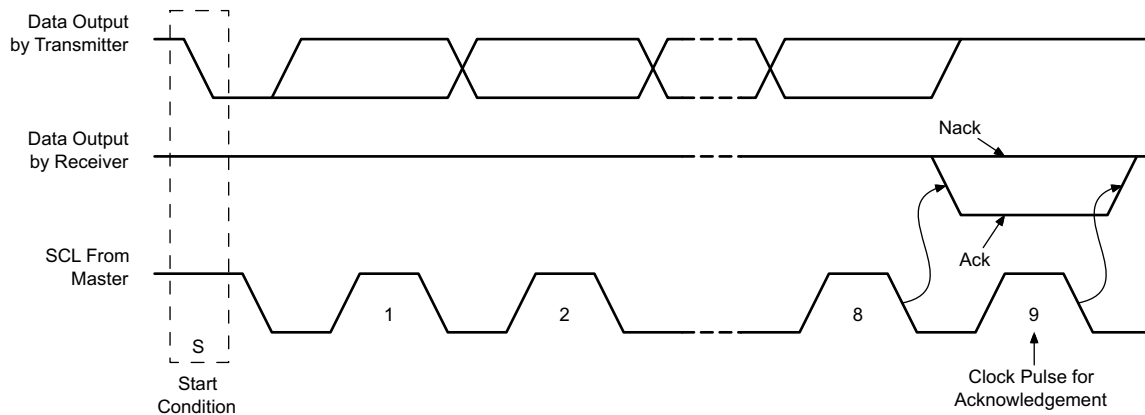


图 8-9. I<sup>2</sup>C Acknowledgment

### 8.3.7.2 I<sup>2</sup>C Clock Stretching

The TPS25814 features clock stretching for the I<sup>2</sup>C protocol. The TPS25814 slave I<sup>2</sup>C port may hold the clock line (SCL) low after receiving (or sending) a byte, indicating that it is not yet ready to process more data. The master communicating with the slave must not finish the transmission of the current bit and must wait until the clock line actually goes high. When the slave is clock stretching, the clock line remains low.

The master must wait until it observes the clock line transitioning high plus an additional minimum time (4  $\mu$ s for standard 100-kbps I<sup>2</sup>C) before pulling the clock low again.

Any clock pulse may be stretched but typically it is the interval before or after the acknowledgment bit.

### 8.3.7.3 I<sup>2</sup>C Address Setting

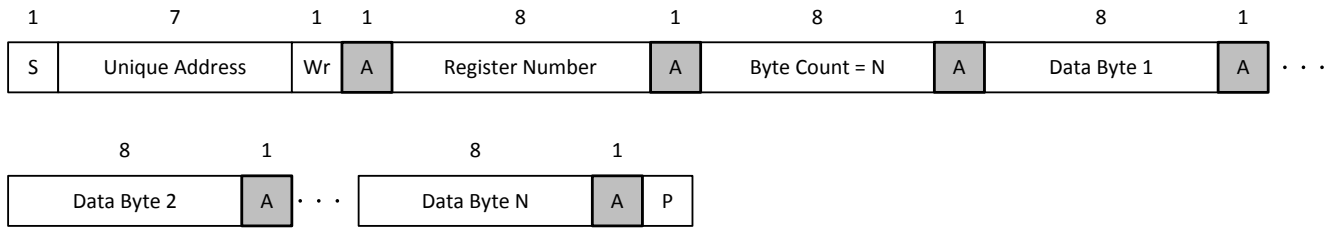
The host should only use I2C\_EC\_SCL/SDA for loading a patch bundle. Once the boot process is complete, each port has a unique slave address on the I2C\_EC\_SCL/SDA bus as selected by the ADCINx pins.

表 8-6. I<sup>2</sup>C Default Slave Address for I2C\_EC\_SCL/SDA.

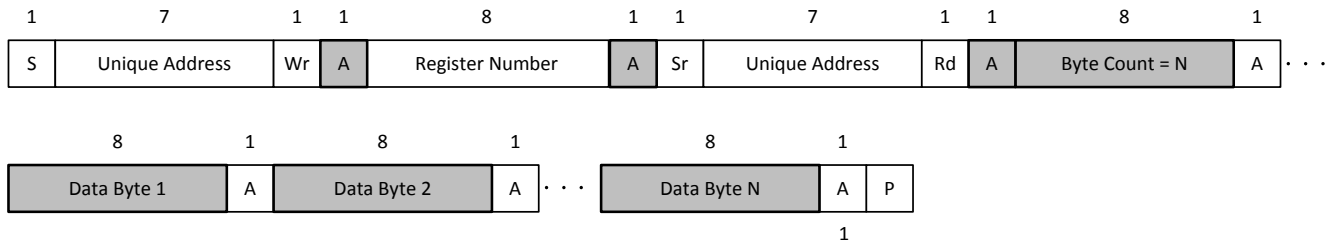
ADCIN1 Decoding		Slave Address							
ADCIN1[1]	ADCIN1[0]	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	1	0	0	0	0	0	R/W
0	1	0	1	0	0	0	0	1	R/W
1	0	0	1	0	0	0	1	0	R/W
1	1	0	1	0	0	0	1	1	R/W

### 8.3.7.4 Unique Address Interface

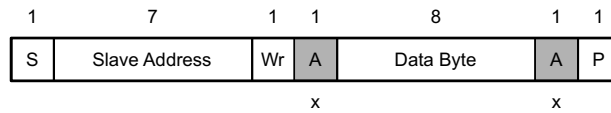
The Unique Address Interface allows for complex interaction between an I<sup>2</sup>C master and a single TPS25814. The I<sup>2</sup>C Slave sub-address is used to receive or respond to Host Interface protocol commands. 图 8-10 and 图 8-11 show the write and read protocol for the I<sup>2</sup>C slave interface, and a key is included in 图 8-12 to explain the terminology used. The key to the protocol diagrams is in the SMBus Specification and is repeated here in part.





**图 8-10. I<sup>2</sup>C Unique Address Write Register Protocol**



**图 8-11. I<sup>2</sup>C Unique Address Read Register Protocol**



- S Start Condition
- SR Repeated Start Condition
- Rd Read (bit value of 1)
- Wr Write (bit value of 0)
- x Field is required to have the value x
- A Acknowledge (this bit position may be 0 for an ACK or 1 for a NACK)
- P Stop Condition
-  Master-to-Slave
-  Slave-to-Master
- Continuation of protocol

**图 8-12. I<sup>2</sup>C Read/Write Protocol Key**



## 8.4 Device Functional Modes

### 8.4.1 Pin Strapping to Configure Default Behavior

During the boot procedure, the device will read the ADCINx pins and set the configurations based on the table below.

**表 8-7. Device Configuration using ADCIN1**

ADCIN1 Decoded Value <sup>(1)</sup>			I <sup>2</sup> C Address Index <sup>(2)</sup>	SPM Enabled
ADCIN1[2]	ADCIN1[1]	ADCIN1[0]		
0	0	0	#1	no
0	0	1	#2	
0	1	0	#3	
0	1	1	#4	
1	0	0	#1	yes
1	0	1	#2	
1	1	0	#3	
1	1	1	#4	

(1) See 表 8-6 to see the exact meaning of I<sup>2</sup>C Address Index.

(2) See 表 8-2 for how to configure a given ADCINx decoded value.

**表 8-8. Device Configuration using ADCIN2**

ADCIN2 Decoded Value <sup>(1)</sup>			Minimum Current <sup>(2)</sup>	Maximum Current	DCP Mode
ADCIN2[2]	ADCIN2[1]	ADCIN2[0]			
0	0	0	USB Default	1.5A	DCP
0	0	1			DCP Auto Mode 1
0	1	0		3A	DCP
0	1	1			DCP Auto Mode 1
1	0	0	1.5A	1.5A	DCP
1	0	1			DCP Auto Mode 1
1	1	0		3A	DCP
1	1	1			DCP Auto Mode 1

(1) See 表 8-2 for how to configure a given ADCINx decoded value.

(2) Requires SPM to be enabled via ADCIN1.

### 8.4.2 Power States

The TPS25814 may operate in one of three different power states: Active, Idle, or Sleep. The Modern Standby mode is a special case of the Idle mode. The functionality available in each state is summarized in the following table. The device will automatically transition between the three power states based on the circuits that are active and required, see the following figure. In the Sleep State the TPS25814 will detect a Type-C connection. Transitioning between the Active mode to the Idle mode requires a period of time (T) without any of the following activity:

- Change in CC status.
- GPIO input event.
- I<sup>2</sup>C transactions.
- Voltage alert.
- Fault alert.

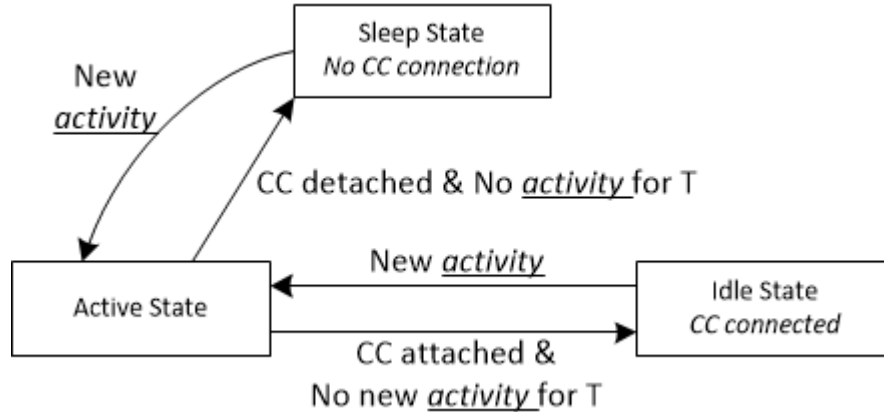


图 8-13. Flow Diagram For Power States

表 8-9. Power Consumption States.

	Active Source Mode <sup>(1)</sup>	Idle Source Mode <sup>(2)</sup>	Modern Standby Source Mode <sup>(4)</sup>	Sleep Mode <sup>(3)</sup>
PP_5V	enabled	enabled	enabled	disabled
PP_CABLE	enabled	enabled	disabled	disabled
external CC1 termination	Rd	Rd	Rd	open
external CC2 termination	open	open	open	open

(1) This mode is used for:  $I_{VIN\_3V3,ActSrc}$ (2) This mode is used for:  $I_{VIN\_3V3,IdlSrc}$ (3) This mode is used for:  $I_{VIN\_3V3,SleepSrc}$ (4) This mode is used for:  $P_{MstbySrc}$ 

### 8.4.3 Schottky for Current Surge Protection

To prevent the possibility of large ground currents into the TPS25814 during sudden disconnects due to inductive effects in a cable, it is recommended that a Schottky diode be placed from VBUS to ground as shown in 图 8-14.

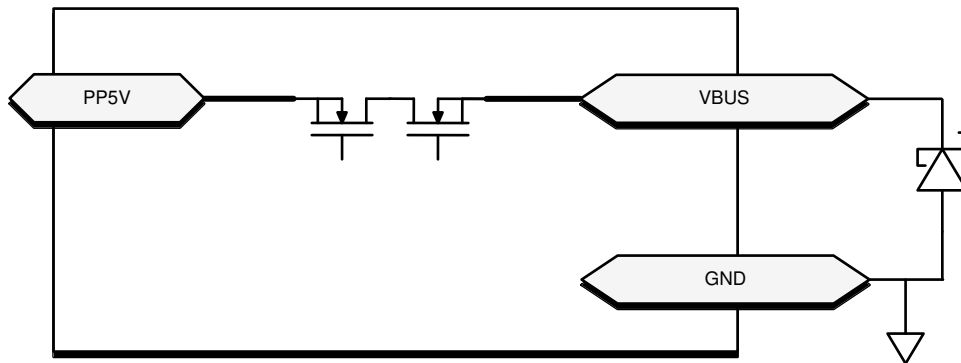


图 8-14. Schottky for Current Surge Protection

### 8.4.4 Thermal Shutdown

The TPS25814 features a central thermal shutdown as well as independent thermal sensors for each internal power path. The central thermal shutdown monitors the overall temperature of the die and disables all functions except for supervisory circuitry when die temperature goes above a rising temperature of  $T_{SD\_MAIN}$ . The temperature shutdown has a hysteresis of  $T_{SDH\_MAIN}$  and when the temperature falls back below this value, the device resumes normal operation.

The power path thermal shutdown monitors the temperature of each internal PP5V-to-VBUS power path and disables both power paths and the VCONN power path when either exceeds  $T_{SD\_PP5V}$ . Once the temperature falls by at least  $T_{SDH\_PP5V}$  the path can be configured to resume operation or remain disabled until re-enabled by firmware.

## 9 Application and Implementation

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### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

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### 9.1 Application Information

The TPS25814 is a Type-C DFP controller that supports all Type-C DFP required functions. The TPS25814 Only applies power to VBUS when it detects that a UFP is attached and removes power when it detects the UFP is detached. The device exposes its identity via its CC pin advertising its current capability based on the CHG\_HI pin settings. The TPS25814 also limits its advertised current internally and provides robust protection to a fault on the system VBUS power rail.


After a connection is established by the TPS25814, the device is capable of providing VCONN to power circuits in the cable plug on the CC pin that is not connected to the CC wire in the cable. VCONN is internally current limited and is supplied by PP5V.

The TPS25814 is also capable of supporting BC 1.2 compliant charging schemes of a Charging Data Port (CDP) and a Dedicated Charging Port (DCP). The CTL pin changes which charging modes are activated to the connected portable device.

The following design procedure can be used to implement a full featured Type-C DFP.

### 9.2 Typical Application

#### 9.2.1 Type C DFP Port Implementation with Embedded Controller

 9-1 shows a Type-C DFP implementation where the TPS25814 is connected to an embedded controller. The embedded controller will have the ability to communicate with the TPS25814 via I<sup>2</sup>C, as well as change the charge current advertisement and BC 1.2 charging scheme.

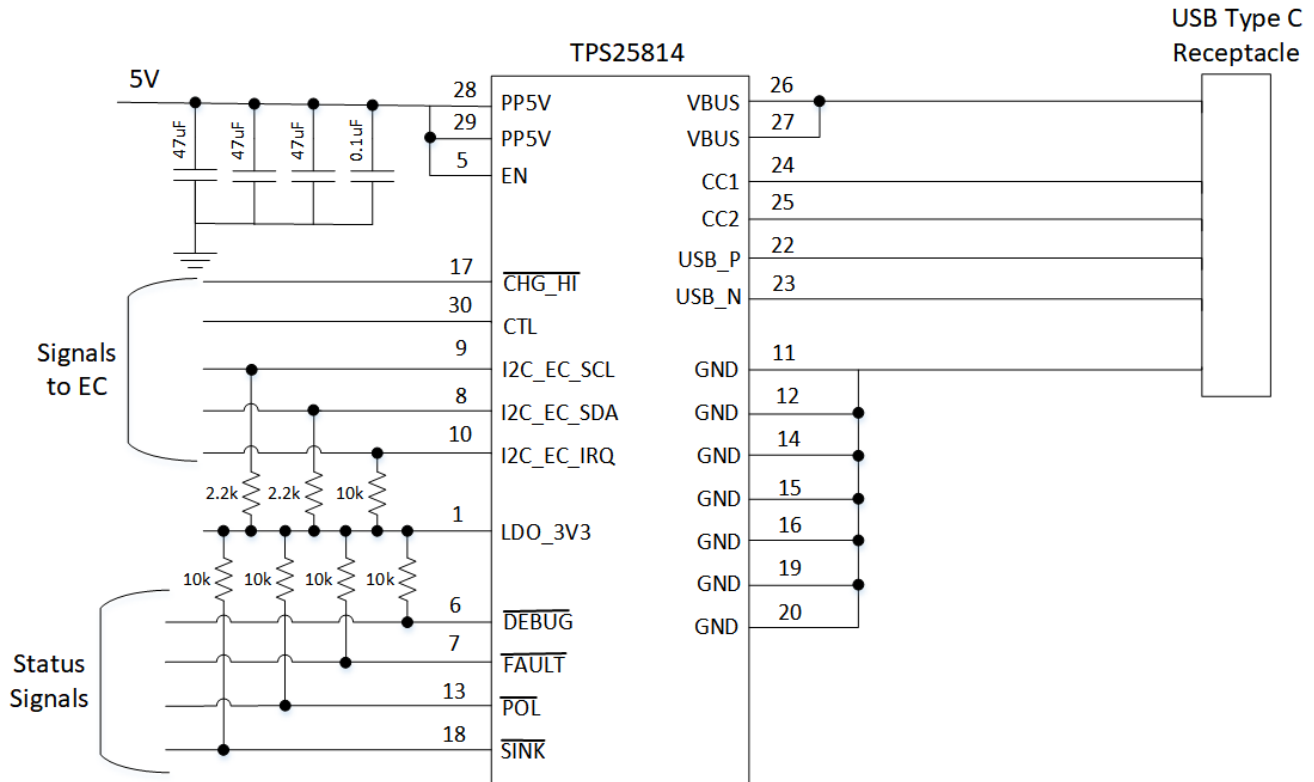


图 9-1. Type C DFP Port Implementation

### 9.2.1.1 Detailed Design Procedure

#### 9.2.1.1.1 Type-C Connector VBUS Capacitors

The first level of protection starts at the Type-C connector and the VBUS pin capacitors. These capacitors help filter out high frequency noise but can also help absorb short voltage transients. Each VBUS pin should have a 10-nF capacitor rated at or above 25 V and placed as close to the pin as possible. The GND pin on the capacitors should have very short path to GND on the connector. The derating factor of ceramic capacitors should be taken into account as they can lose more than 50% of their effective capacitance when biased. Adding the VBUS capacitors can help reduce voltage spikes by 2 V to 3 V.

#### 9.2.1.1.2 VBUS Schottky and TVS Diodes

Schottky diodes are used on VBUS to help absorb large GND currents when a Type-C cable is removed while drawing high current. The inductance in the cable will continue to draw current on VBUS until the energy stored is dissipated. Higher currents could cause the body diodes on IC devices connected to VBUS to conduct. When the current is high enough it could damage the body diodes of IC devices. Ideally, a VBUS Schottky diode should have a lower forward voltage so it can turn on before any other body diodes on other IC devices. Schottky diodes on VBUS also help during hard shorts to GND which can occur with a faulty Type-C cable or damaged Type-C PD device. VBUS could ring below GND which could damage devices hanging off of VBUS. The Schottky diode will start to conduct once VBUS goes below the forward voltage. When the TPS25814 is the only device connected to VBUS, place the Schottky Diode close to the VBUS pin of the TPS25814.

TVS Diodes help suppress and clamp transient voltages. Most TVS diodes can fully clamp around 10 ns and can keep the VBUS at their clamping voltage for a period of time. Looking at the clamping voltage of TVS diodes after they settle during a transient will help decide which TVS diode to use. The peak power rating of a TVS diode must be able to handle the worst case conditions in the system.

9.2.1.1.3 VBUS Snubber Circuit

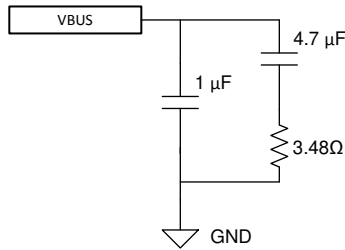


图 9-2. VBUS Snubber

Another method of clamping the USB Type-C VBUS is to use a VBUS RC Snubber. An RC Snubber is smaller than a TVS diode, and typically more cost effective as well. An RC Snubber works by modifying the characteristic of the total RLC response in the USB Type-C cable hot-plug from being under-damped to critically-damped or over-damped. So rather than clamping the overvoltage directly, it changes the hot-plug response from under-damped to critically-damped, so the voltage on VBUS does not ring at all; so the voltage is limited, but without requiring a clamping element like a TVS diode.

However, the USB Type-C and Power Delivery specifications limit the range of capacitance that can be used on VBUS for the RC snubber. VBUS capacitance must have a minimum 1 µF and a maximum of 10 µF. The RC snubber values chosen support up to 4 m USB Type-C cable (maximum length allowed in the USB Type-C specification) being hot plugged, is to use 4.7- µ F capacitor in series with a 3.48- Ω resistor. In parallel with the RC Snubber a 1- µ F capacitor is used, which always ensures the minimum USB Type-C VBUS capacitance specification is met. This circuit is shown in 图 9-2.

9.2.1.2 Application Curves

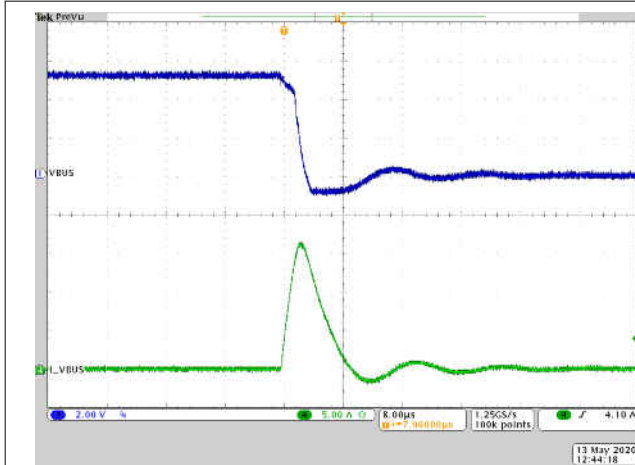


图 9-3. VBUS Short to Ground (Zoomed In)

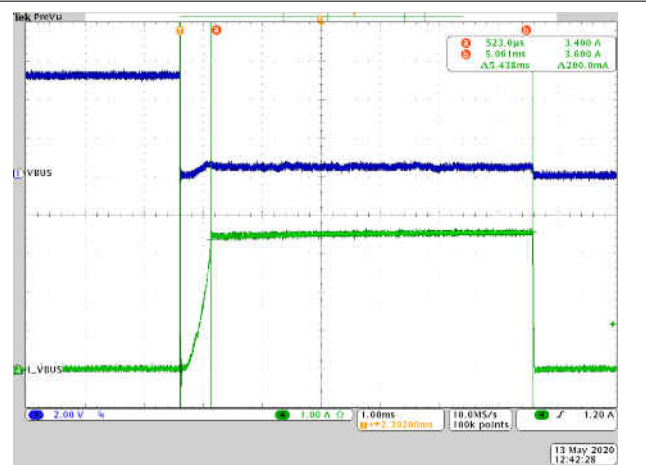


图 9-4. VBUS Short to Ground (Zoomed Out)

## 10 Power Supply Recommendations

### 10.1 3.3-V Power

#### 10.1.1 VIN\_3V3 Input Switch

The VIN\_3V3 input is the main supply of the TPS25814 device. The VIN\_3V3 switch is a uni-directional switch from VIN\_3V3 to LDO\_3V3, not allowing current to flow backwards from LDO\_3V3 to VIN\_3V3. This switch is on when the 3.3 V supply is available. The recommended capacitance  $C_{VIN\_3V3}$  (see the Recommended Capacitance in the [Specifications](#) section) should be connected from the VIN\_3V3 pin to the GND pin).

### 10.2 1.5-V Power

The internal circuitry is powered from 1.5 V. The 1.5-V LDO steps the voltage down from LDO\_3V3 to 1.5 V. The 1.5-V LDO provides power to all internal low-voltage digital circuits which includes the digital core, and memory. The 1.5-V LDO also provides power to all internal low-voltage analog circuits. Connect the recommended capacitance  $C_{LDO\_1V5}$  (see the Recommended Capacitance in the [Specifications](#) section) from the LDO\_1V5 pin to the GND pin.

### 10.3 Recommended Supply Load Capacitance

The Recommended Capacitance in the [Specifications](#) section lists the recommended board capacitances for the various supplies. The typical capacitance is the nominally rated capacitance that must be placed on the board as close to the pin as possible. The maximum capacitance must not be exceeded on pins for which it is specified. The minimum capacitance is minimum capacitance allowing for tolerances and voltage derating ensuring proper operation.

## 11 Layout

### 11.1 Layout Guidelines

Proper routing and placement will maintain signal integrity for high speed signals and improve the heat dissipation from the TPS25814 power path. The combination of power and high speed data signals are easily routed if the following guidelines are followed. It is a best practice to consult with board manufacturing to verify manufacturing capabilities.

#### 11.1.1 Top TPS25814 Placement and Bottom Component Placement and Layout

When the TPS25814 is placed on top and its components on bottom the solution size will be at its smallest.

### 11.2 Layout Example

Follow the differential impedances for Super / High Speed signals defined by their specifications (DisplayPort - AUXN/P and USB2.0). All I/O will be fanned out to provide an example for routing out all pins, not all designs will utilize all of the I/O on the TPS25814.

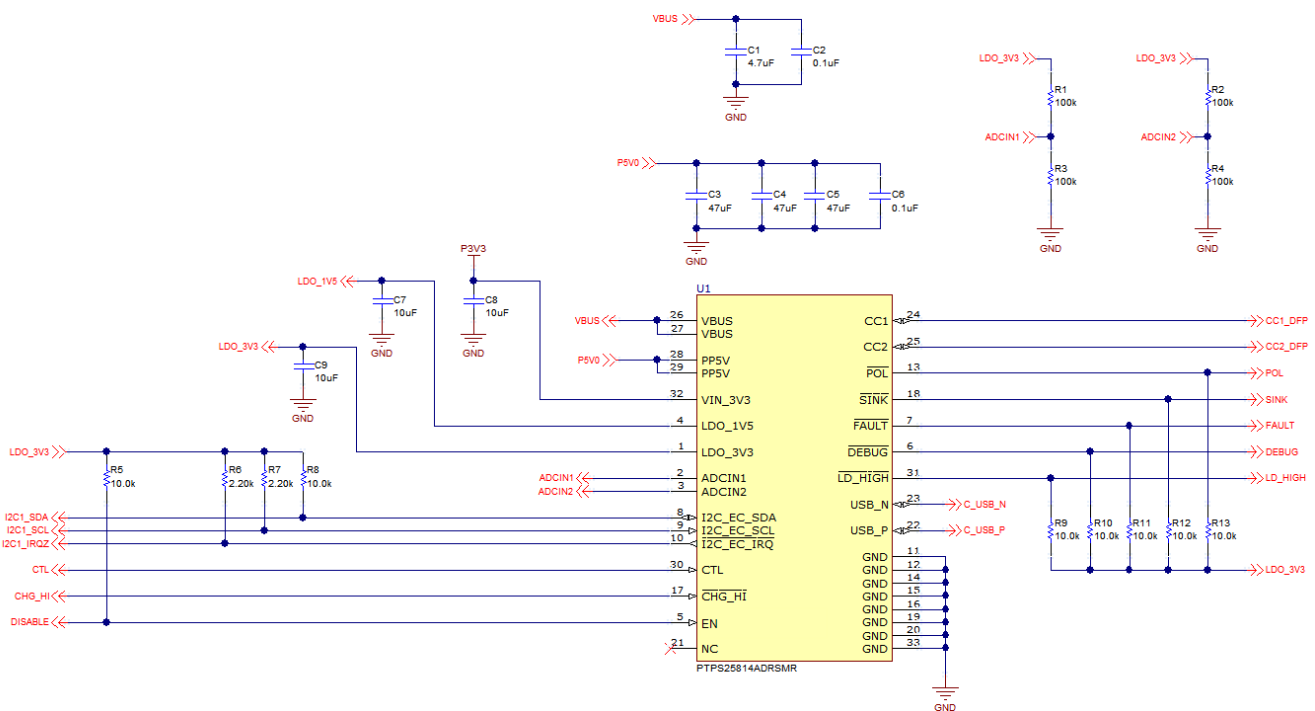


图 11-1. Example Schematic

### 11.3 Component Placement

Top and bottom placement is used for this example to minimize solution size. The TPS25814 is placed on the top side of the board and the majority of its components are placed on the bottom side. When placing the components on the bottom side, it is recommended that they are placed directly under the TPS25814. When placing the VBUS and PPHV capacitors it is easiest to place them with the GND terminal of the capacitors to face outward from the TPS25814 or to the side since the drain connection pads on the bottom layer should not be connected to anything and left floating. All other components that are for pins on the GND pad side of the TPS25814 should be placed where the GND terminal is underneath the GND pad.

The CC capacitors should be placed on the same side as the TPS25814 close to the respective CC1 and CC2 pins. Do NOT via to another layer in between the CC pins to the CC capacitor, placing a via after the CC capacitor is recommended.

The ADCIN1/2 voltage divider resistors can be placed where convenient.



The figures below show the placement in 2-D and 3-D.

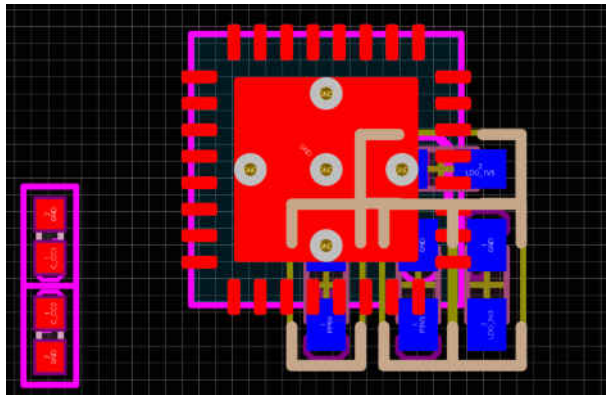


图 11-2. Top View Layout

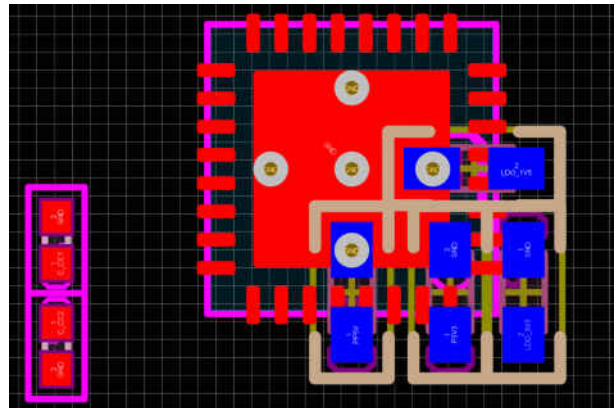


图 11-3. Bottom View Layout

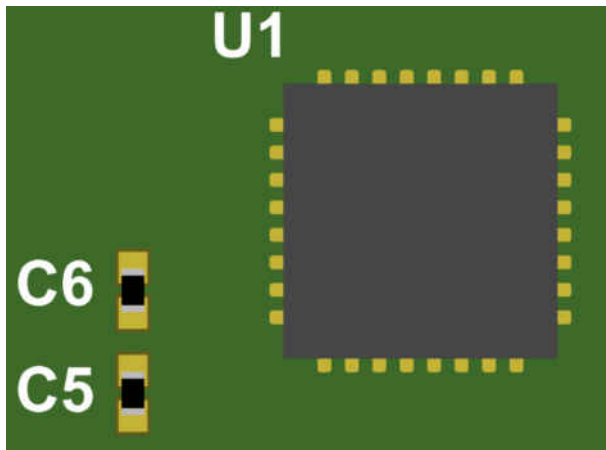


图 11-4. Top View 3-D

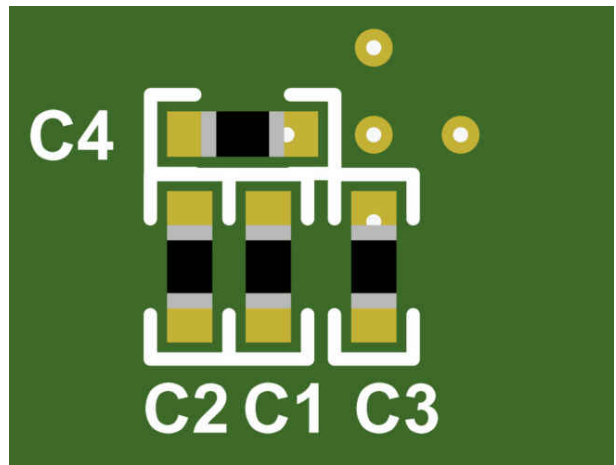


图 11-5. Bottom View 3-D

#### 11.4 Routing and View Placement

On the top side, create pours for PP5V and VBUS. Connect PP5V and VBUS from the top layer to the bottom layer using at least 6, 8-mil hole and 16-mil diameter vias. See [图 11-6](#) for the recommended via sizing. The via placement and copper pours are highlighted in [图 11-7](#).



图 11-6. Recommended Minimum Via Sizing

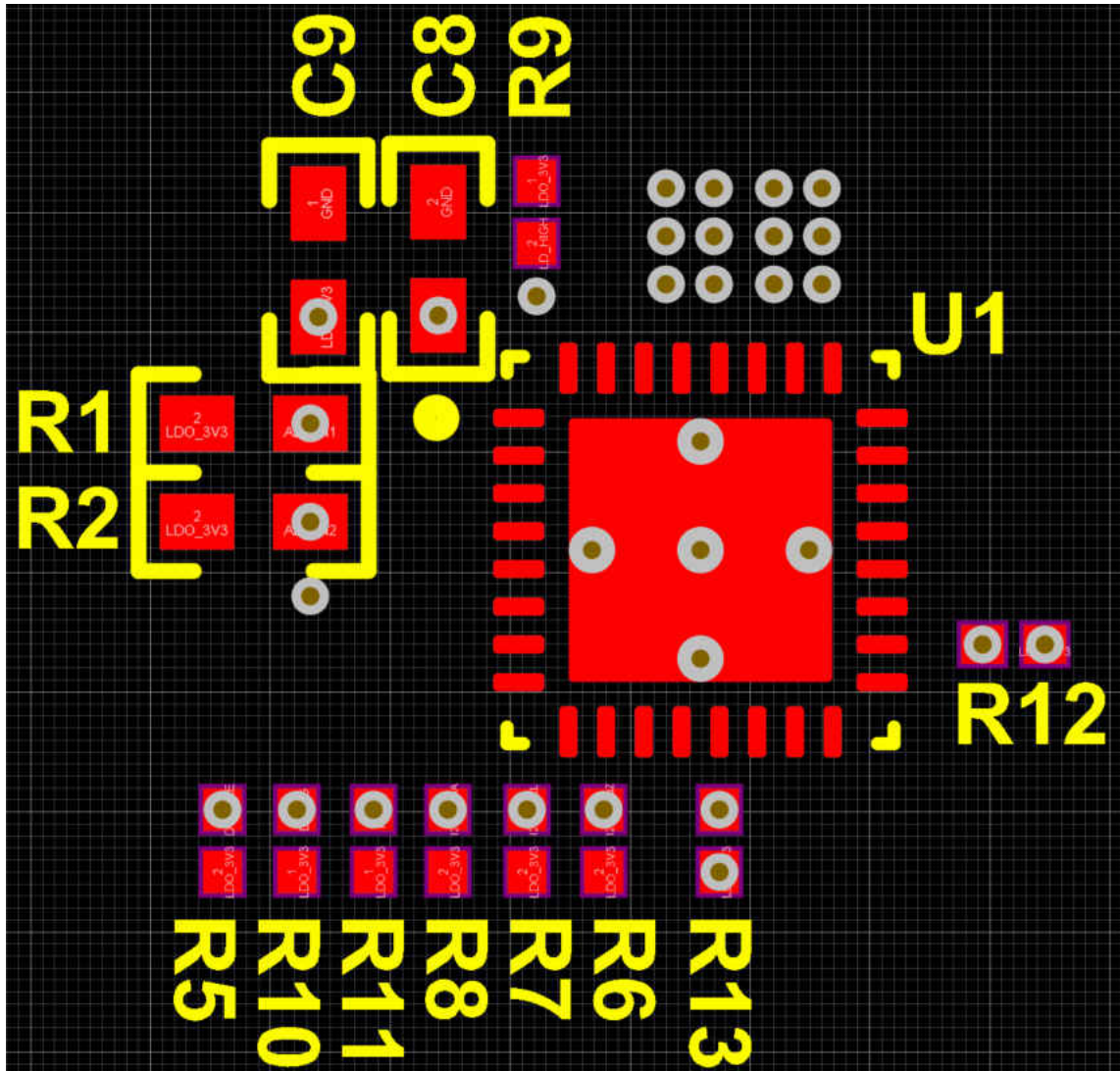


图 11-7. Via Placement - Top Layer

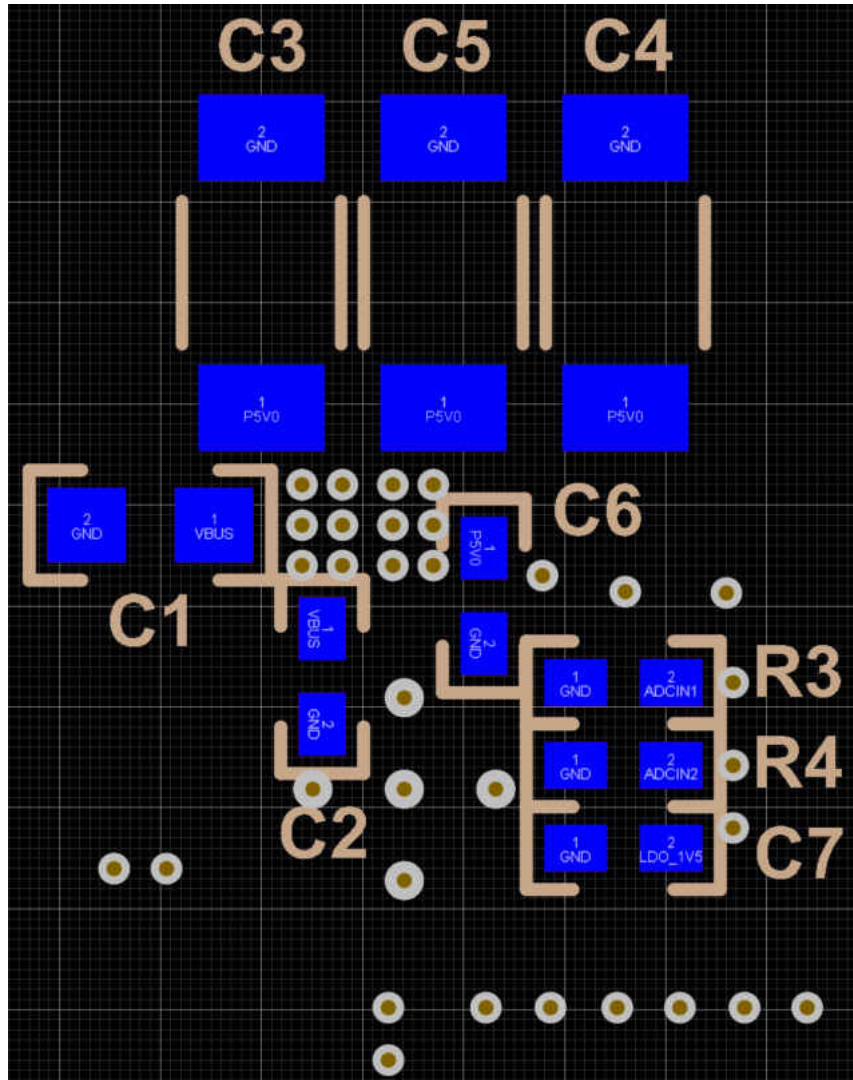


图 11-8. Via Placement - Bottom Layer

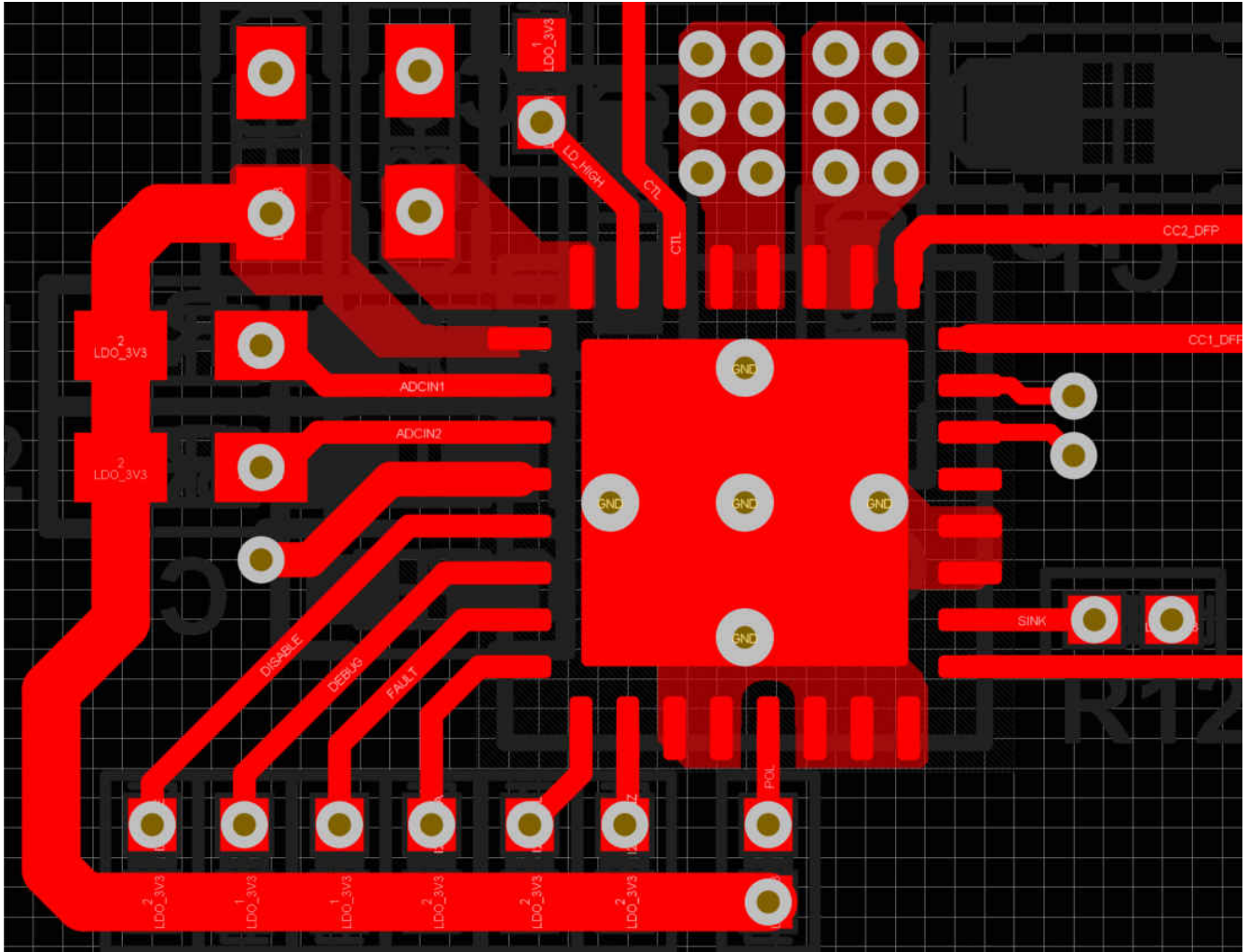


图 11-9. Routing - Top Layer

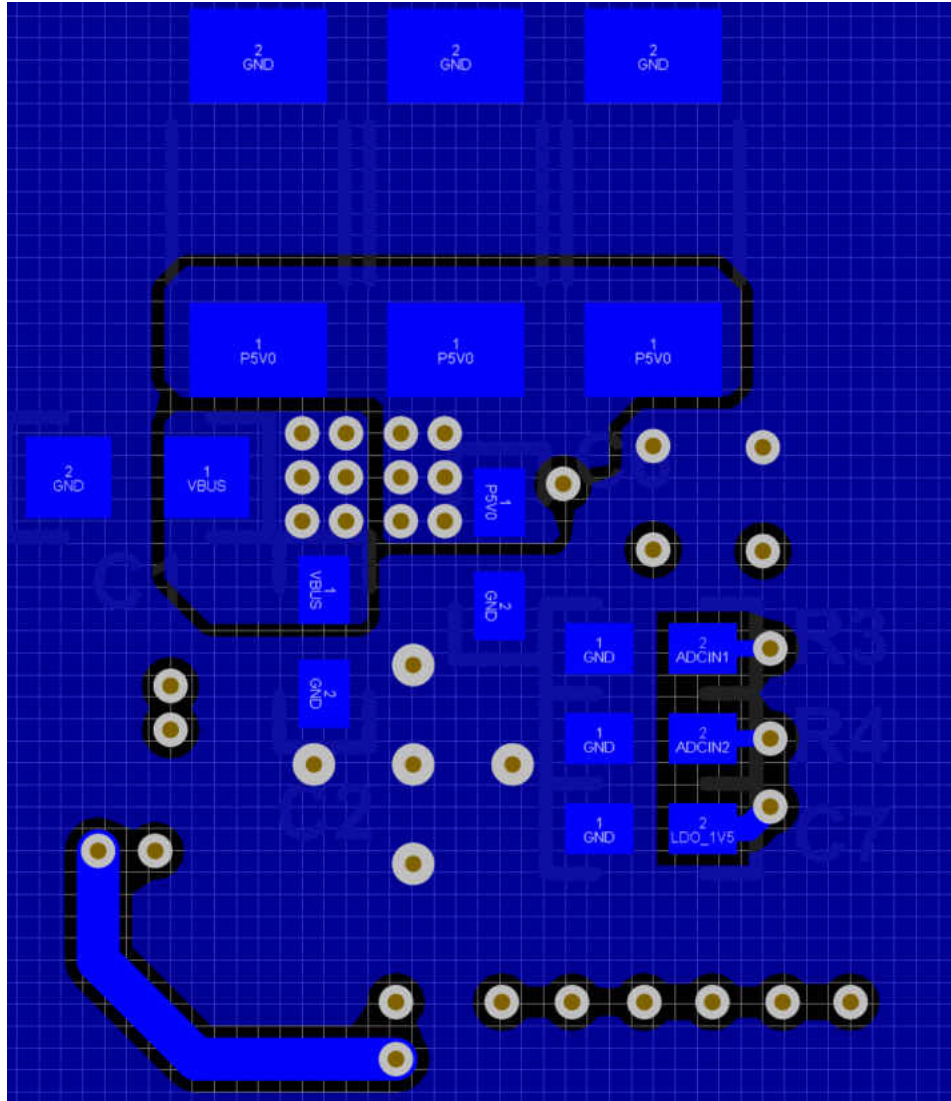


图 11-10. Routing - Bottom Layer

## 12 Device and Documentation Support

### 12.1 Device Support

#### 12.1.1 第三方产品免责声明

TI 发布的与第三方产品或服务有关的信息，不能构成与此类产品或服务或保修的适用性有关的认可，不能构成此类产品或服务单独或与任何 TI 产品或服务一起的表示或认可。

### 12.2 Documentation Support

#### 12.2.1 Related Documentation

- [USB-PD Specifications](#)
- [USB Power Delivery Specification](#)

### 12.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

### 12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

### 12.5 静电放电警告



静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

### 12.6 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS25814RSMR	ACTIVE	VQFN	RSM	32	3000	RoHS & Green	NIPDAU   NIPDAUAG	Level-2-260C-1 YEAR	-40 to 105	25814	Samples

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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## GENERIC PACKAGE VIEW

**RSM 32**

**VQFN - 1 mm max height**

4 x 4, 0.4 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4224982/A



# RSM0032B



# PACKAGE OUTLINE

## VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



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**NOTES:**

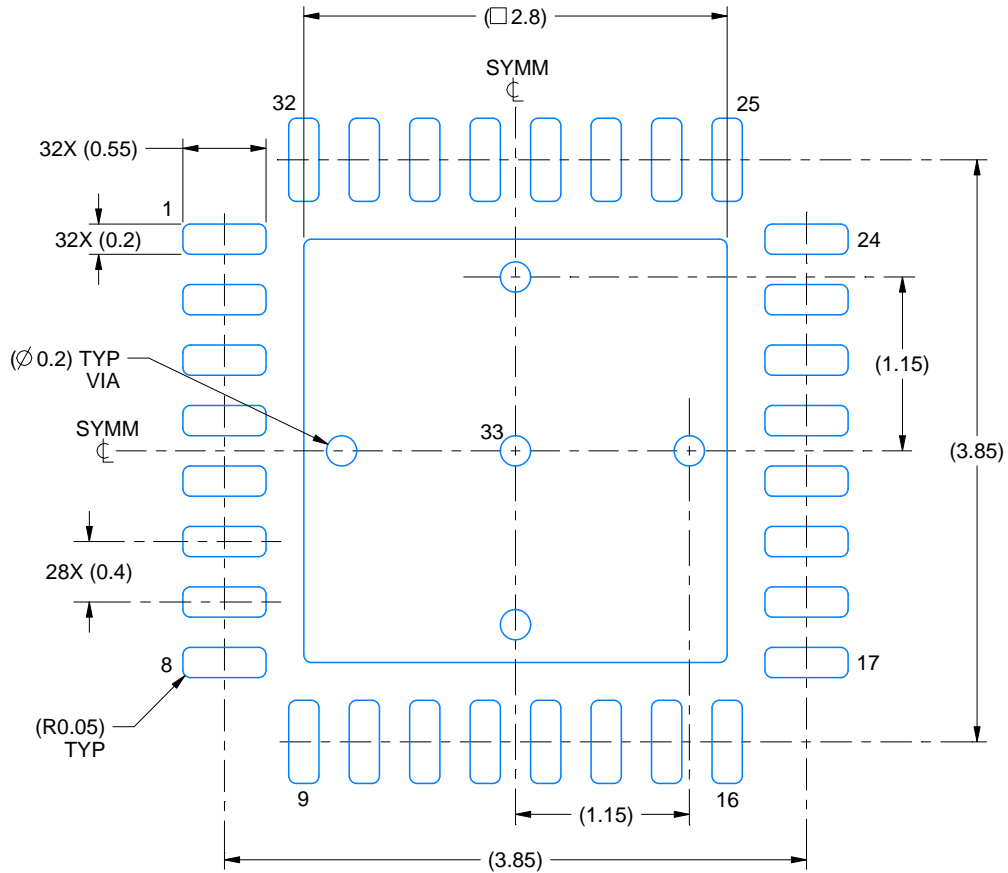
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

RSM0032B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:20X



SOLDER MASK DETAILS

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NOTES: (continued)

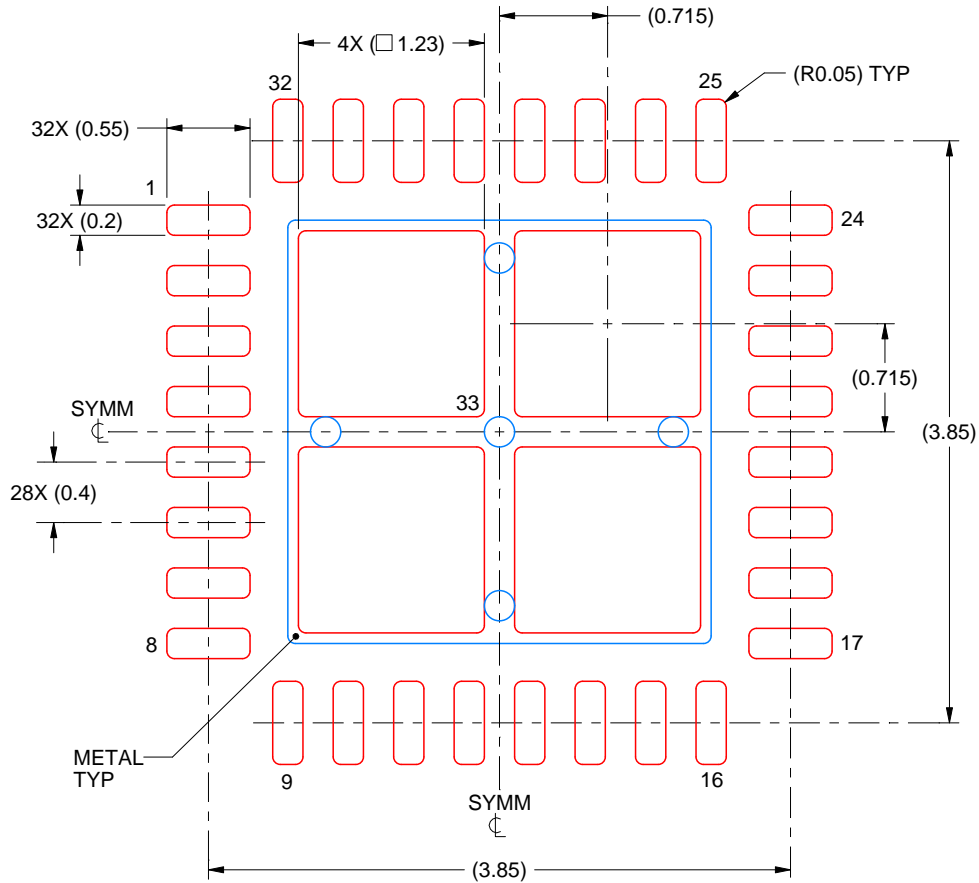
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RSM0032B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



**SOLDER PASTE EXAMPLE**  
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 33:  
77% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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