TEXAS INSTRUMENTS
TPS3700-Q1
ZHCSCB4C – MARCH 2014 – REVISED MARCH 2021

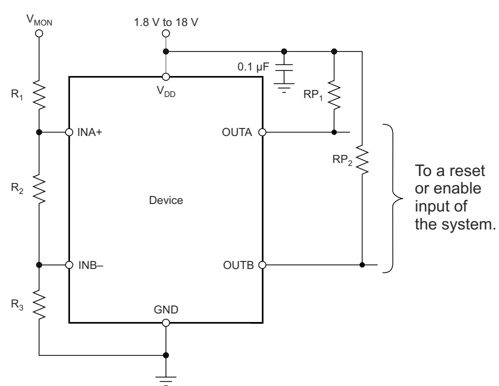
TPS3700-Q1 用于过压和欠压监控、具有内部基准的汽车类高压 (18V) 窗口电压检测器

1 特性

- 符合汽车应用要求
- 具有符合 AEC-Q100 标准的下列特性：
  - 器件温度等级 1：–40°C 至 125°C 环境工作温度范围
  - 器件人体放电模型 (HBM) 静电防护 (ESD) 分类等级 H2
  - 器件 CDM ESD 分类等级 C6
- 提供功能安全
  - 可提供用于功能安全系统设计的文档
- 宽电源电压范围：1.8V 至 18V
- 可调节阈值：低至 400mV
- 针对过压和欠压检测的开漏输出
- 低静态电流：5.5 µA（典型值）
- 高阈值精度：
  - 过温时为 1%
  - 0.25%（典型值）
- 内部迟滞：5.5mV（典型值）
- 采用薄型 SOT23-6 和 WSON 封装

2 应用

- 高级驾驶辅助系统 (ADAS)
- ADAS 域控制器
- 数字驾驶舱
- 汽车信息娱乐系统和仪表组
- 混合动力电动汽车/电动汽车 OBC 和无线充电器
- 工业机器人



简化原理图

3 说明

TPS3700-Q1 宽电源窗口电压检测器可在 1.8V 至 18V 的电压范围内运行。此器件具有两个带有内部 400mV 基准的高精度比较器和两个用于过压和欠压检测的额定值为 18V 的开漏输出。TPS3700-Q1 器件可以用作一个窗口电压检测器，也可以用作两个单独的电压监测器。通过外部电阻器可以设置监控电压。如需高达 65V 的更宽输入电压范围，请参阅 TPS37A-Q1 或 TPS38A-Q1 器件。

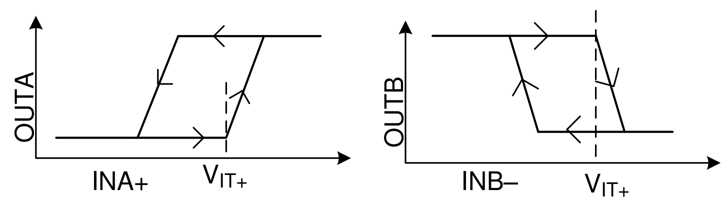
当 INA+ 端子上的电压下降至低于 (V_{IT+} - V_{hys}) 时，OUTA 端子被驱动至低电平，而当电压返回到各自阈值 (V_{IT+}) 之上时，OUTA 端子变为高电平。当 INB- 端子上的电压上升至高于 V_{IT+}时，OUTB 端子被驱动至低电平，而当电压下降至低于各自的阈值 (V_{IT+} - V_{hys}) 时，OUTB 端子变为高电平。TPS3700-Q1 器件中的两个比较器包括用于滤波的内置滞后来抑制短时毛刺脉冲，从而确保无故障触发的稳定输出运行。

TPS3700-Q1 器件采用薄型 SOT-6 封装和 1.5mm x 1.5mm WSON-6 封装，额定工作结温范围为 -40°C 至 125°C。

器件信息

订货编号	封装 (1)	封装尺寸
TPS3700-Q1	SOT23 (6)	2.90mm × 1.60mm
	WSON (6)	1.50mm x 1.50mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



输出与输入阈值和迟滞

Table of Contents

1 特性........ 1
2 应用........ 1
3 说明........ 1
4 Revision History........ 2
5 Pin Configuration and Functions........ 3
6 Specifications........ 4
6.1 Absolute Maximum Ratings........ 4
6.2 ESD Ratings........ 4
6.3 Recommended Operating Conditions........ 4
6.4 Thermal Information........ 4
6.5 Electrical Characteristics........ 5
6.6 Timing Requirements........ 6
6.7 Timing Diagram........ 6
6.8 Switching Characteristics........ 6
6.9 Typical Characteristics........ 7
7 Detailed Description........ 9
7.1 Overview........ 9
7.2 Functional Block Diagram........ 9
7.3 Feature Description........ 9
7.4 Device Functional Modes........ 11
8 Application and Implementation........ 12
8.1 Application Information........ 12
8.2 Typical Application........ 15
9 Power Supply Recommendations........ 17
10 Layout........ 18
10.1 Layout Guidelines........ 18
10.2 Layout Example........ 18
11 Device and Documentation Support........ 19
11.1 Documentation Support........ 19
11.2 Trademarks........ 19
11.3 静电放电警告........ 19
11.4 术语表........ 19
12 Mechanical, Packaging, and Orderable Information........ 19

4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision B (July 2017) to Revision C (March 2021) **Page**

- 向功能安全型器件添加了要点........ 1
- 添加了指向 TI.com 应用页面的链接........ 1
- 更新了整个文档中的表格、图和交叉参考的编号格式，将器件信息中的器件型号更正为 GPN........ 1
- Moved Storage temperature range here in the Absolute Maximum Ratings from the section previously called handling ratings (which also included ESD ratings) when the ESD ratings section was updated per the latest format........ 4
- Corrected table formatting, descriptions and the notes in ESD Ratings section per the latest standards........ 4
- Corrected Input Voltage Max on INA+, INB- from 6 V to 6.5 V to match the device capability........ 4
- Added missing Thermal Information for the DSE package........ 4
- Added the missing max start-up delay spec and corrected corresponding note 2........ 5

Changes from Revision A (April 2014) to Revision B (July 2017) **Page**

- 向“器件信息”表添加了 WSON 封装........ 1
- Added WSON Package to Pin Configuration and Function table........ 3

Changes from Revision * (March 2014) to Revision A (April 2014) **Page**

- 将器件状态从*产品预发布* 更改为*量产数据*........ 1

5 Pin Configuration and Functions

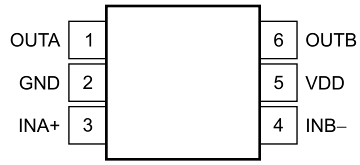


图 5-1. DDC Package SOT-6 Top View

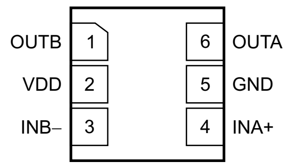


图 5-2. DSE Package WSON-6 Top View

表 5-1. Pin Functions

PIN			I/O	DESCRIPTION
NAME	DDC	DSE		
GND	2	5	—	Ground
INA+	3	4	I	This pin is connected to the voltage to be monitored with the use of an external resistor divider. When the voltage at this terminal drops below the threshold voltage (V_{IT+} – V_{HYS}), OUTA is driven low.
INB –	4	3	I	This pin is connected to the voltage to be monitored with the use of an external resistor divider. When the voltage at this terminal exceeds the threshold voltage (V_{IT+}), OUTB is driven low.
OUTA	1	6	O	INA+ comparator open-drain output. OUTA is driven low when the voltage at this comparator is below (V_{IT+} – V_{HYS}). The output goes high when the sense voltage returns above the respective threshold (V_{IT+}).
OUTB	6	1	O	INB – comparator open-drain output. OUTB is driven low when the voltage at this comparator exceeds V_{IT+}. The output goes high when the sense voltage returns below the respective threshold (V_{IT+} – V_{HYS}).
VDD	5	2	I	Supply voltage input. Connect a 1.8-V to 18-V supply to VDD to power the device. Good analog design practice is to place a 0.1-μF ceramic capacitor close to this pin.

6 Specifications

6.1 Absolute Maximum Ratings

Over operating temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
Voltage[2]	V_{DD}	–0.3	20	V
	OUTA, OUTB	–0.3	20	V
	INA+, INB–	–0.3	7	V
Current	Output terminal current		40	mA
Operating junction temperature, T_J		–40	125	°C
Storage temperature range, T_{stg}		-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to network ground terminal.

6.2 ESD Ratings

			VALUE	UNIT
V_{ESD}	Electrosatic discharge	Human body model (HBM), per AEC Q100-002[1]	±2500	V
		Charge device model (CDM), per AEC Q100-011	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

Over operating temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{DD}	Supply voltage		1.8	18	V
V_I	Input voltage	INA+, INB–	0	6.5	V
V_O	Output voltage	OUTA, OUTB	0	18	V

6.4 Thermal Information

THERMAL METRIC[1]		TPS3700-Q1		UNIT
		DDC (SOT)	DSE (WSON)	
		6 pins	6 pins	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	174.0	160.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	81.5	101.9	
$R_{\theta JB}$	Junction-to-board thermal resistance	47.2	68.8	
ψ_{JT}	Junction-to-top characterization parameter	22.0	5.4	
ψ_{JB}	Junction-to-board characterization parameter	46.9	68.6	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Over the operating temperature range of T_J = –40°C to 125°C, and 1.8 V < V_{DD} < 18 V, unless otherwise noted. Typical values are at T_J = 25°C and V_{DD} = 5 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{DD}	Supply voltage range		1.8		18	V
$V_{(POR)}$	Power-on reset voltage[(1)]	V_{OL}max = 0.2 V, $I_{(OUTA/B)}$ = 15 µA			0.8	V
V_{IT+}	Positive-going input threshold voltage	V_{DD} = 1.8 V	396	400	404	mV
		V_{DD} = 18 V	396	400	404	mV
V_{IT-}	Negative-going input threshold voltage	V_{DD} = 1.8 V	387	394.5	400	mV
		V_{DD} = 18 V	387	394.5	400	mV
V_{hys}	Hysteresis voltage (hys = V_{IT+} – V_{IT-})			5.5	12	mV
$I_{(INA+)}$ $I_{(INB-)}$	Input current (at the INA+ or INB – terminal)	V_{DD} = 1.8 V and 18 V, V_I = 6.5 V	–25	1	25	nA
		V_{DD} = 1.8 V and 18 V, V_I = 0.1 V	–15	1	15	nA
V_{OL}	Low-level output voltage	V_{DD} = 1.3 V, I_O = 0.4 mA			250	mV
		V_{DD} = 1.8 V, I_O = 3 mA			250	mV
		V_{DD} = 5 V, I_O = 5 mA			250	mV
$I_{lkg(OD)}$	Open-drain output leakage-current	V_{DD} = 1.8 V and 18 V, V_O = V_{DD}			300	nA
		V_{DD} = 1.8 V, V_O = 18 V			300	nA
I_{DD}	Supply current	V_{DD} = 1.8 V, no load		5.5	11	µA
		V_{DD} = 5 V		6	13	µA
		V_{DD} = 12 V		6	13	µA
		V_{DD} = 18 V		7	13	µA
	Startup delay[(2)]			150	450	µs
UVLO	Undervoltage lockout[(4)]	V_{DD} falling	1.3		1.7	V

(1) The lowest supply voltage (V_{DD}) at which output is active; $t_{r(VDD)}$ > 15 µs/V. Below $V_{(POR)}$, the output cannot be determined.
(2) During power on, V_{DD} must exceed 1.8 V for 450 µs (max) before the output is in a correct state.
(3) High-to-low and low-to-high refers to the transition at the input terminals (INA+ and INB –).
(4) When V_{DD} falls below UVLO, OUTA is driven low and OUTB goes to high impedance. The outputs cannot be determined below $V_{(POR)}$.

6.6 Timing Requirements

Over operating temperature range (unless otherwise noted)

			MIN	TYP	MAX	UNIT
t_{PHL}	High-to-low propagation delay[3]	V_{DD} = 5 V, 10-mV input overdrive, R_P = 10 kΩ, V_{OH} = 0.9 × V_{DD}, V_{OL} = 400 mV See 图 6-1		18		μs
t_{PLH}	Low-to-high propagation delay[3]	V_{DD} = 5 V, 10-mV input overdrive, R_P = 10 kΩ, V_{OH} = 0.9 × V_{DD}, V_{OL} = 400 mV See 图 6-1		29		μs

6.7 Timing Diagram

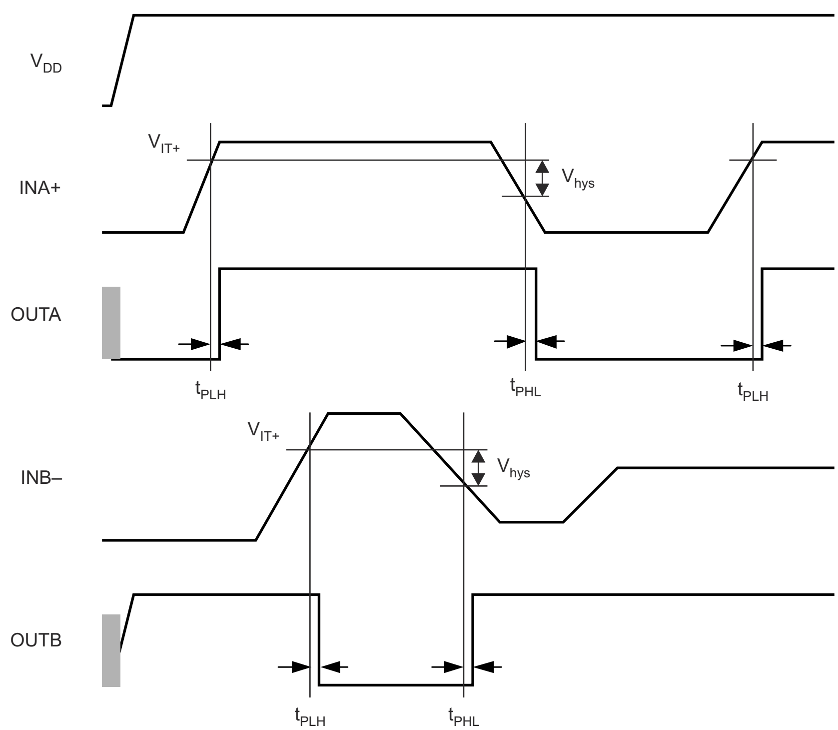


图 6-1. Timing Diagram

6.8 Switching Characteristics

Over operating temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Output rise time	V_{DD} = 5 V, 10-mV input overdrive, R_P = 10 kΩ, V_O = (0.1 to 0.9) × V_{DD}		2.2		μs
t_f	Output fall time	V_{DD} = 5 V, 10-mV input overdrive, R_P = 10 kΩ, V_O = (0.1 to 0.9) × V_{DD}		0.22		μs

6.9 Typical Characteristics

At T_J = 25°C and V_{DD} = 5 V, unless otherwise noted.

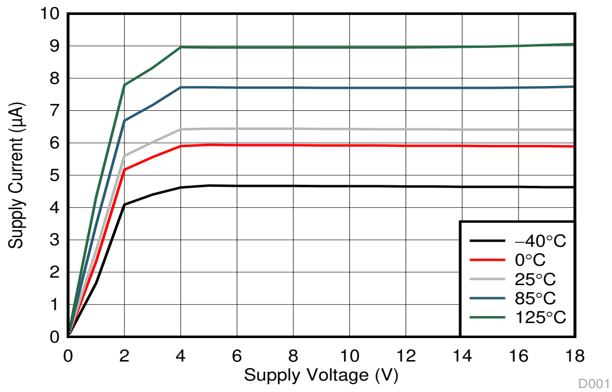


图 6-2. Supply Current (I_{DD}) vs Supply Voltage (V_{DD})

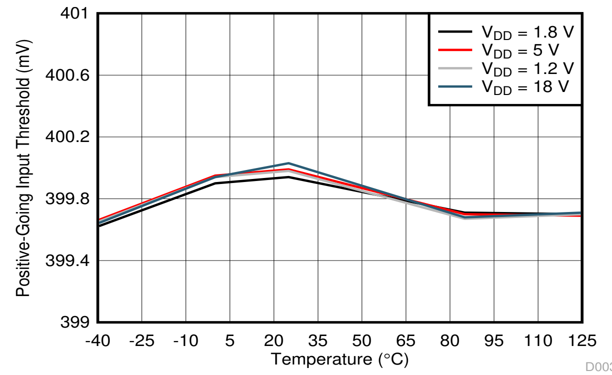


图 6-3. Rising Input Threshold Voltage (V_{IT+}) vs Temperature

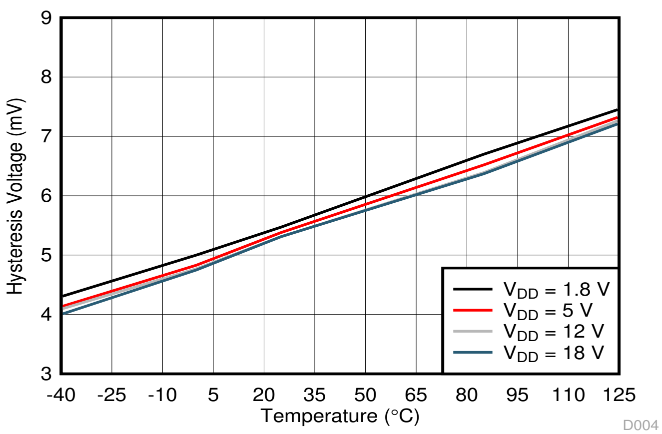


图 6-4. Hysteresis (V_{hys}) vs Temperature

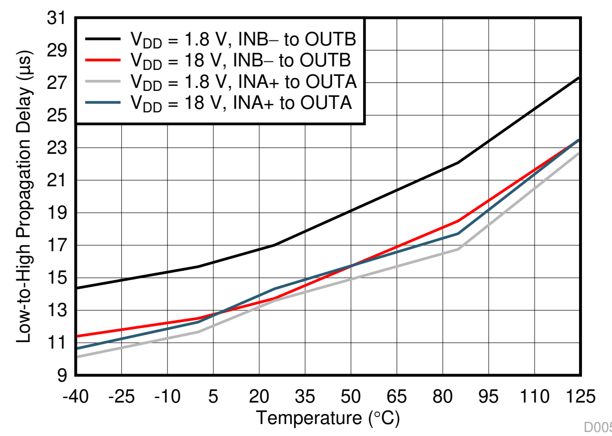


图 6-5. Propagation Delay vs Temperature (High-to-Low Transition at the Inputs)

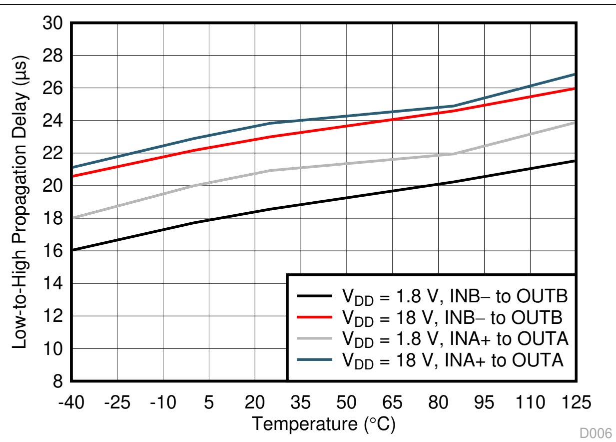
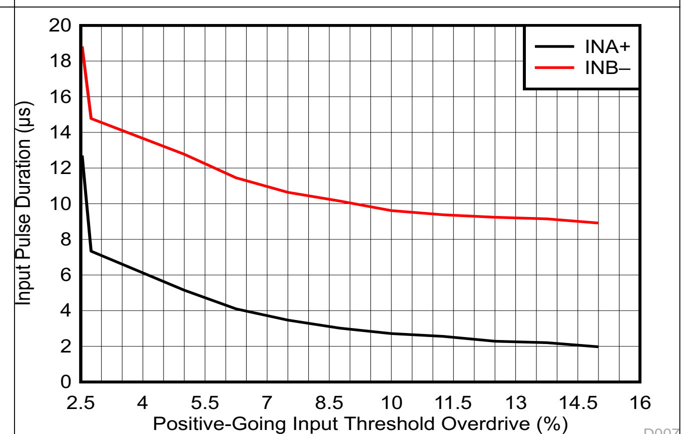


图 6-6. Propagation Delay vs Temperature (Low-to-High Transition at the Inputs)



INA+ = negative spike below V_{IT-}

INB– = positive spike above V_{IT+}

图 6-7. Minimum Pulse Width vs Threshold Overdrive Voltage

6.9 Typical Characteristics (continued)

At T_J = 25°C and V_{DD} = 5 V, unless otherwise noted.

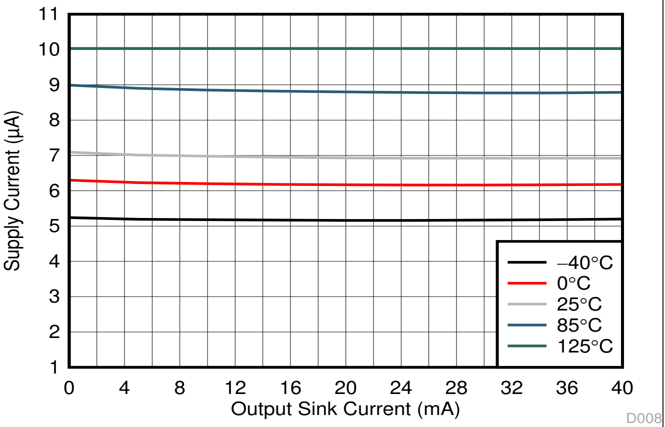


图 6-8. Supply Current (I_{DD}) vs Output Sink Current

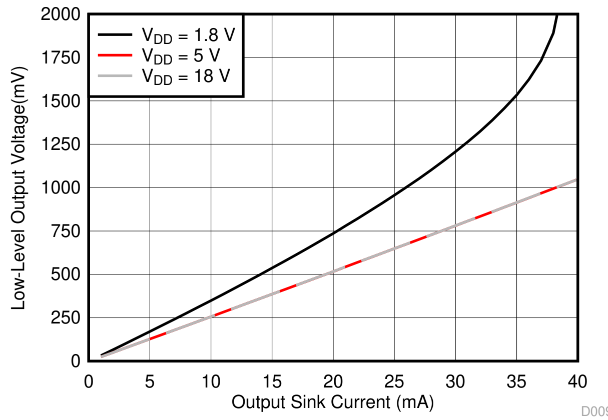


图 6-9. Output Voltage Low (V_{OL}) vs Output Sink Current (– 40°C)

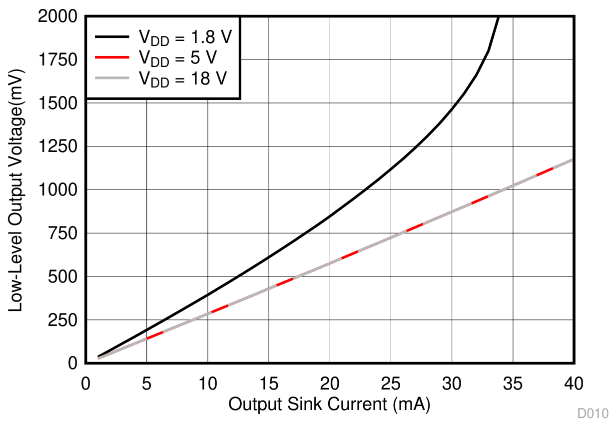


图 6-10. Output Voltage Low (V_{OL}) vs Output Sink Current (0°C)

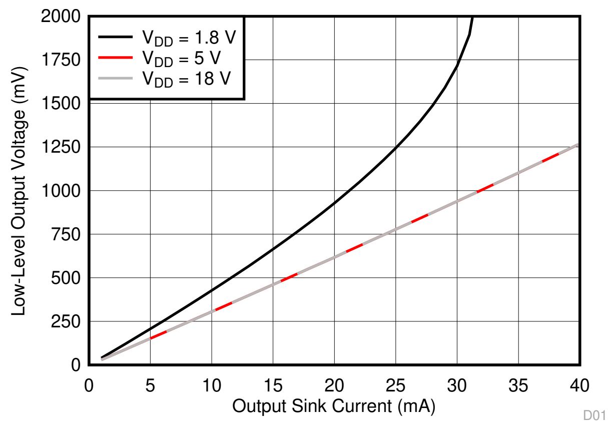


图 6-11. Output Voltage Low (V_{OL}) vs Output Sink Current (25°C)

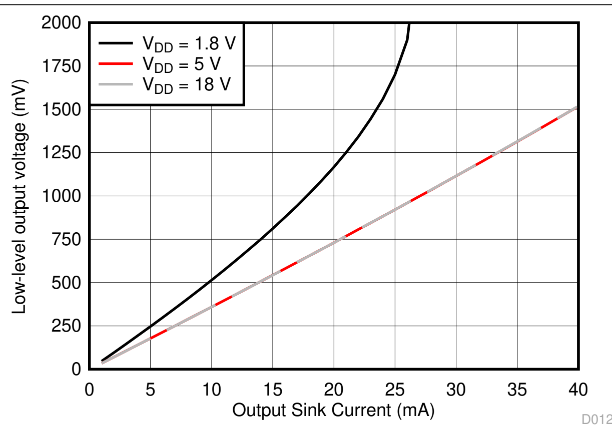


图 6-12. Output Voltage Low (V_{OL}) vs Output Sink Current (85°C)

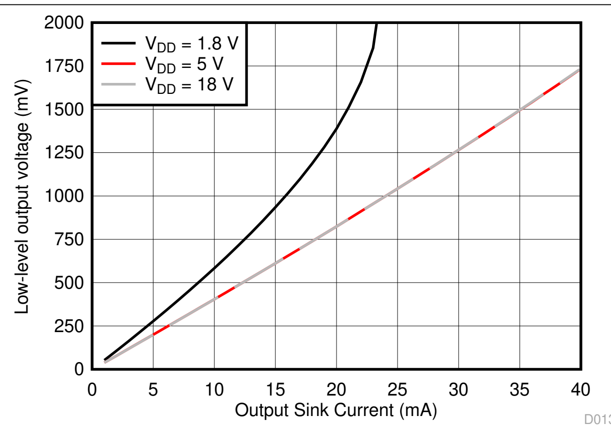


图 6-13. Output Voltage Low (V_{OL}) vs Output Sink Current (125°C)

7 Detailed Description

7.1 Overview

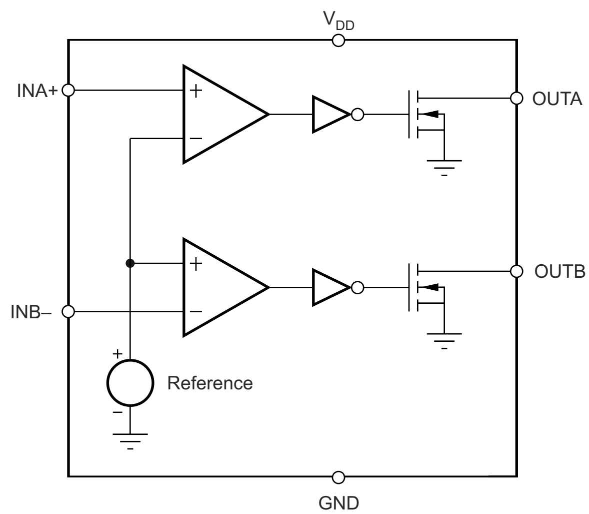
The TPS3700-Q1 device combines two comparators for overvoltage and undervoltage detection. The TPS3700-Q1 device is a wide-supply voltage range (1.8 to 18 V) device with a high-accuracy rising input threshold of 400 mV (1% over temperature) and built-in hysteresis. The outputs are also rated to 18 V and can sink up to 40 mA.

The TPS3700-Q1 device is designed to assert the output signals, as shown in 表 7-1. Each input terminal can be set to monitor any voltage above 0.4 V using an external resistor divider network. With the use of two input terminals of different polarities, the TPS3700-Q1 device forms a window voltage detector. Broad voltage thresholds can be supported that allow the device to be used in a wide array of applications.

表 7-1. TPS3700-Q1 Truth Table

CONDITION	OUTPUT	STATUS
INA+ > V_{IT+}	OUTA high	Output A not asserted
INA+ < V_{IT-}	OUTA low	Output A asserted
INB – > V_{IT+}	OUTB low	Output B asserted
INB – < V_{IT-}	OUTB high	Output B not asserted

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Inputs (INA+, INB –)

The TPS3700-Q1 device combines two comparators. Each comparator has one external input (inverting and noninverting); the other input is connected to the internal reference. The comparator rising threshold is designed and trimmed to be equal to the reference voltage (400 mV). Both comparators also have a built-in falling hysteresis that makes the device less sensitive to supply rail noise and ensures stable operation.

The INA+ and INB- inputs can swing from ground to 6.5 V, regardless of the device supply voltage used. Although not required in most cases, it is good analog design practice to place a 1-nF to 10-nF bypass capacitor at the comparator input for extremely noisy applications in order to reduce sensitivity to transients and layout parasitics.

For comparator A, the corresponding output (OUTA) is driven to logic low when the input INA+ voltage drops below (V_{IT+} – V_{hys}). When the voltage exceeds V_{IT+}, the output (OUTA) goes to a high-impedance state; see 图 6-1.

For comparator B, the corresponding output (OUTB) is driven to logic low when the voltage at input INB – exceeds V_{IT+}. When the voltage drops below V_{IT+} – V_{hys} the output (OUTB) goes to a high-impedance state; see 图 6-1 . Together, these comparators form a window-detection function as discussed in the 节 7.3.3 section.

7.3.2 Outputs (OUTA, OUTB)

In a typical TPS3700-Q1 application, the outputs are connected to a reset or enable input of the processor (such as a digital signal processor [DSP], central processing unit [CPU], field-programmable gate array [FPGA], or application-specific integrated circuit [ASIC]) or the outputs are connected to the enable input of a voltage regulator (such as a DC-DC or low-dropout regulator [LDO]).

The TPS3700-Q1 device provides two open-drain outputs (OUTA and OUTB). Pullup resistors must be used to hold these lines high when the output goes to high impedance (not asserted). By connecting pullup resistors to the proper voltage rails, the outputs can be connected to other devices at the correct interface-voltage levels. The TPS3700-Q1 outputs can be pulled up to 18 V, independent of the device supply voltage. To ensure proper voltage levels, some thought should be given while choosing the pullup resistor values. The pullup resistor value is determined by V_{OL}, sink-current capability, and output-leakage current ($I_{lkg(OD)}$). These values are specified in the 节 6.5 table. By using wired-AND logic, OUTA and OUTB can merge into one logic signal.

表 7-1 and the 节 7.3.1 section describe how the outputs are asserted or de-asserted. See 图 6-1 for a timing diagram that describes the relationship between threshold voltages and the respective output.

7.3.3 Window Voltage Detector

The inverting and noninverting configuration of the comparators forms a window voltage detector circuit using a resistor divider network, as shown in 图 7-1 and 图 7-2. The input terminals can monitor any system voltage above 400 mV with the use of a resistor divider network. The INA+ and INB – terminals monitor for undervoltage and overvoltage conditions, respectively.

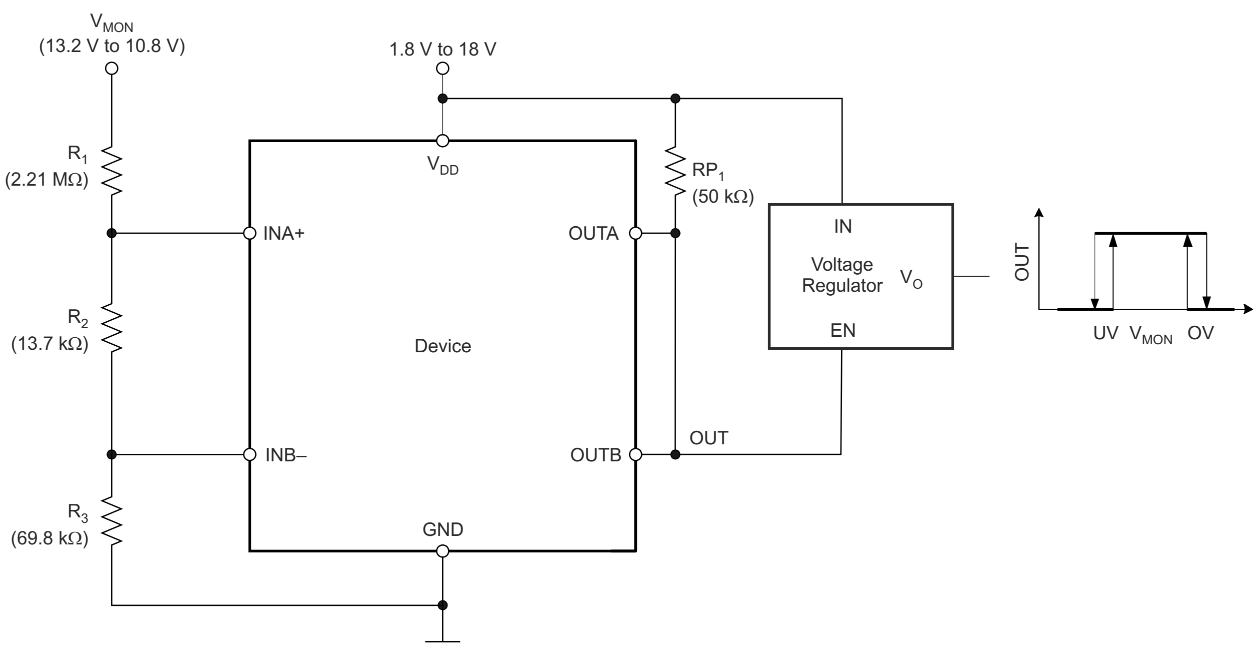


图 7-1. Window Voltage Detector Block Diagram

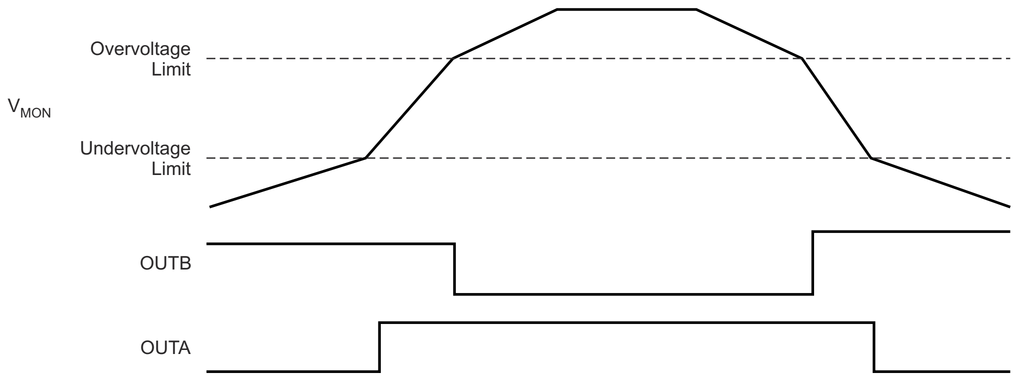


图 7-2. Window Voltage Detector Timing Diagram

7.3.4 Immunity to Input Terminal Voltage Transients

The TPS3700-Q1 device is relatively immune to short voltage transient spikes on the input terminals. Sensitivity to transients is dependent on both transient duration and amplitude; see the *Minimum Pulse Width vs Threshold Overdrive Voltage* curve (图 6-7) in the 节 6.9 section.

7.4 Device Functional Modes

The TPS3700-Q1 has a single functional mode, which is on when V_{DD} is greater than 1.8 V.

8 Application and Implementation

8.1 Application Information

The TPS3700-Q1 device is a wide-supply voltage window voltage detector that operates over a V_{DD} range of 1.8-V to 18-V. The device has two high-accuracy comparators with an internal 400-mV reference and two open-drain outputs rated to 18 V for overvoltage and undervoltage detection. The device can be used either as a window voltage detector or as two independent voltage monitors. The monitored voltages are set with the use of external resistors.

8.1.1 V_{PULLUP} to a Voltage Other Than V_{DD}

The outputs are often tied to V_{DD} through a resistor. However some applications may require the outputs to be pulled up to a higher or lower voltage than V_{DD} in order to correctly interface with the reset and enable the terminal of other devices.

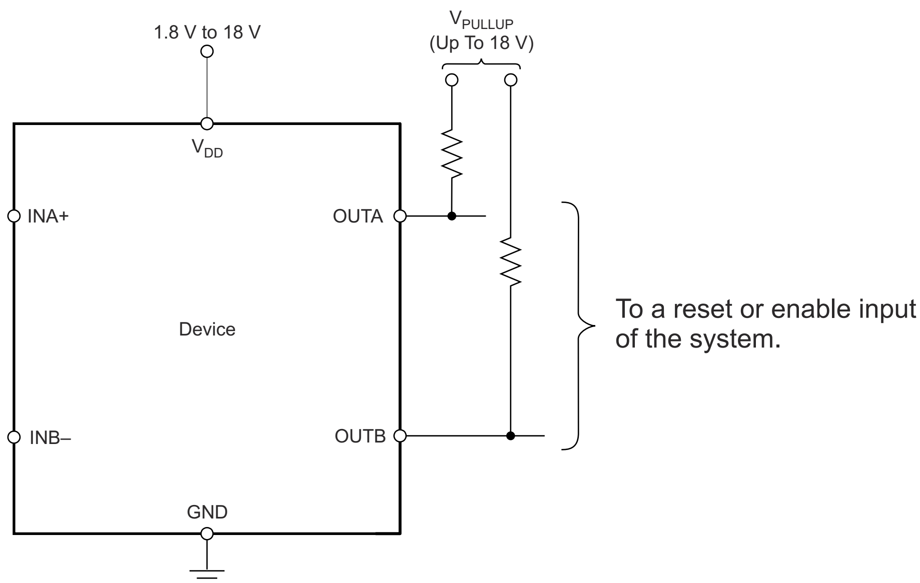


图 8-1. Interfacing to Voltages Other Than V_{DD}

8.1.2 Monitoring V_{DD}

Many applications monitor the same rail that is powering V_{DD}. In these applications the resistor divider is simply connected to the V_{DD} rail.

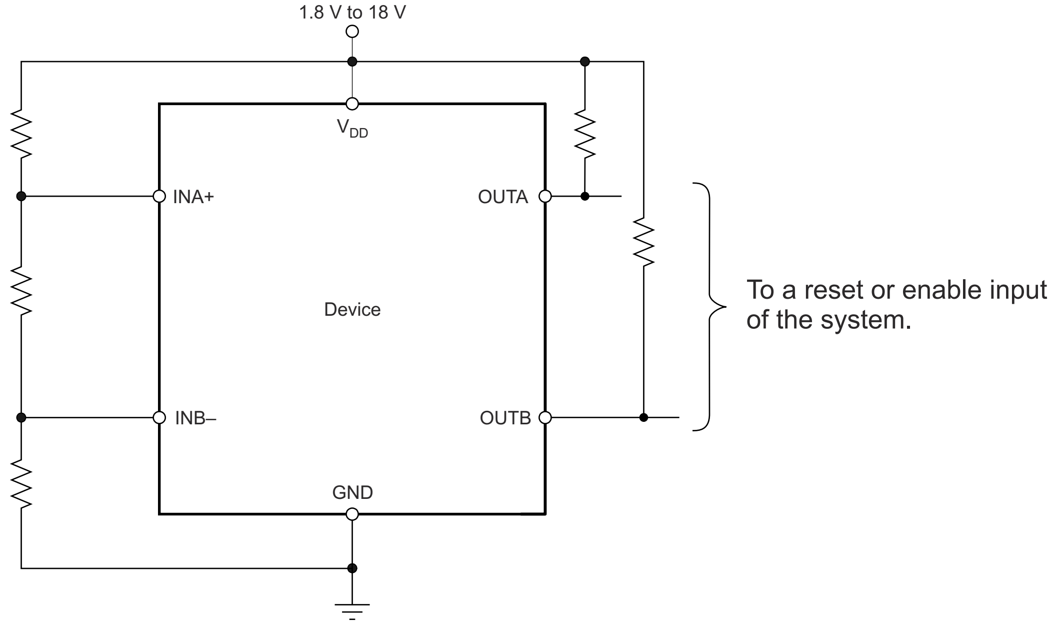
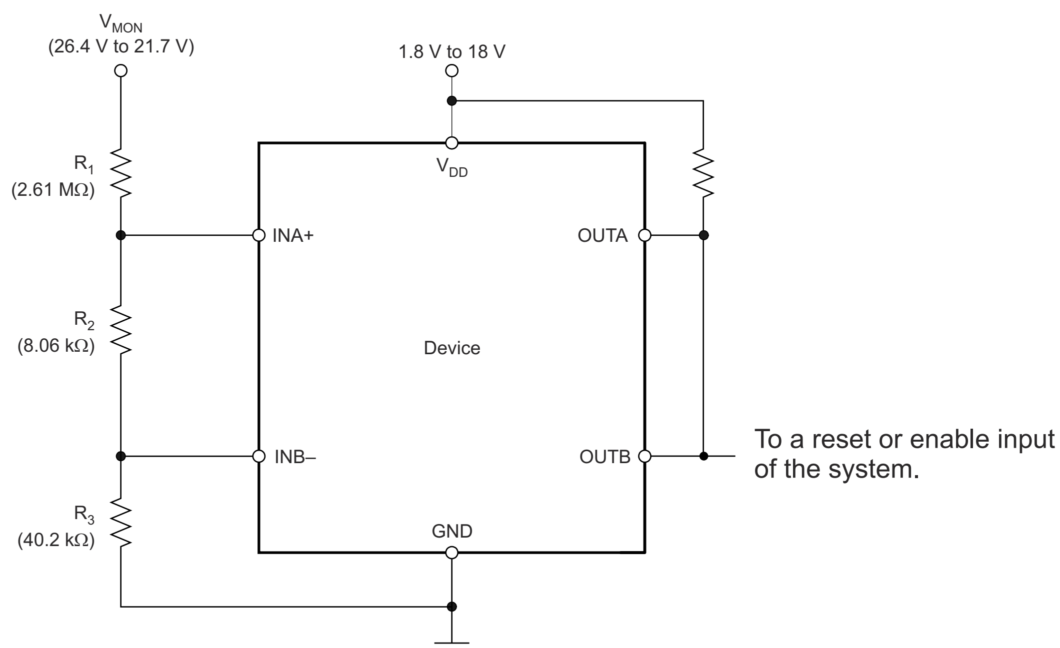


图 8-2. Monitoring the Same Voltage as V_{DD}

8.1.3 Monitoring a Voltage Other Than V_{DD}

Some applications monitor rails other than the one that is powering V_{DD}. In these types of applications the resistor divider used to set the desired thresholds in connected to the rail that is being monitored.

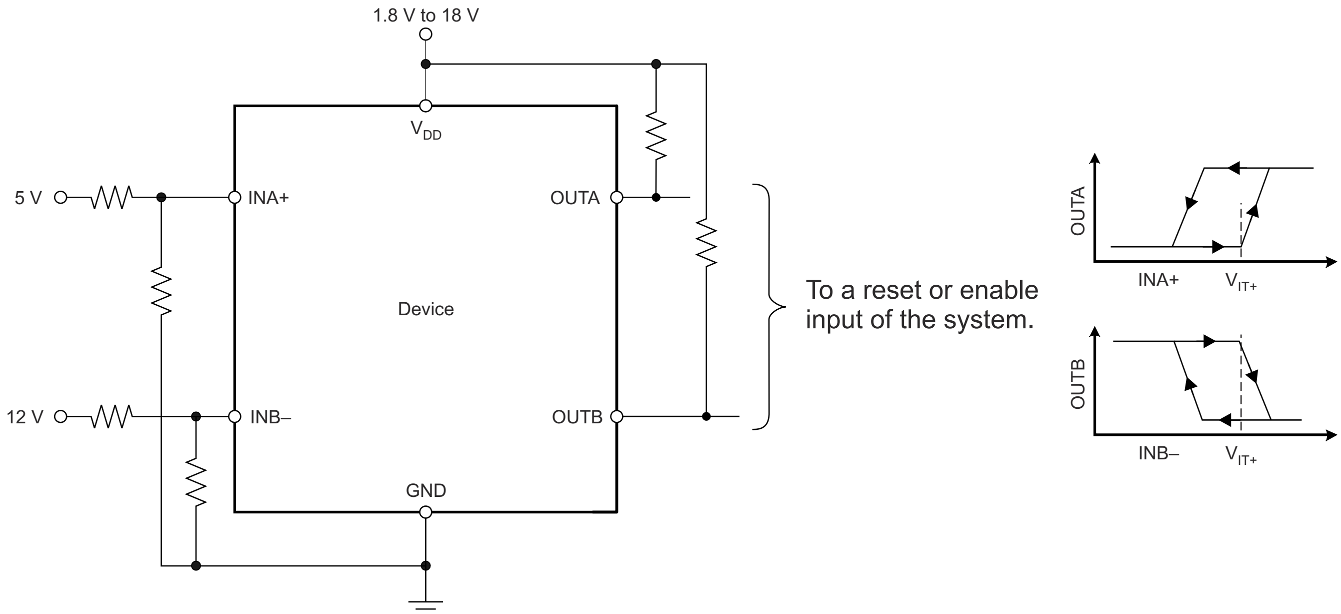


NOTE: The inputs can monitor a voltage higher than V_{DD}max with the use of an external resistor divider network.

图 8-3. Monitoring a Voltage Other Than V_{DD}

8.1.4 Monitoring Overvoltage and Undervoltage for Separate Rails

Some applications may want to monitor for overvoltage conditions on one rail while also monitoring for undervoltage conditions on a different rail. In those applications two independent resistor dividers will need to be used.



NOTE: In this case, OUTA is driven low when an undervoltage condition is detected at the 5-V rail and OUTB is driven low when an overvoltage condition is detected at the 12-V rail.

图 8-4. Monitoring Overvoltage for One Rail and Undervoltage for a Different Rail

8.2 Typical Application

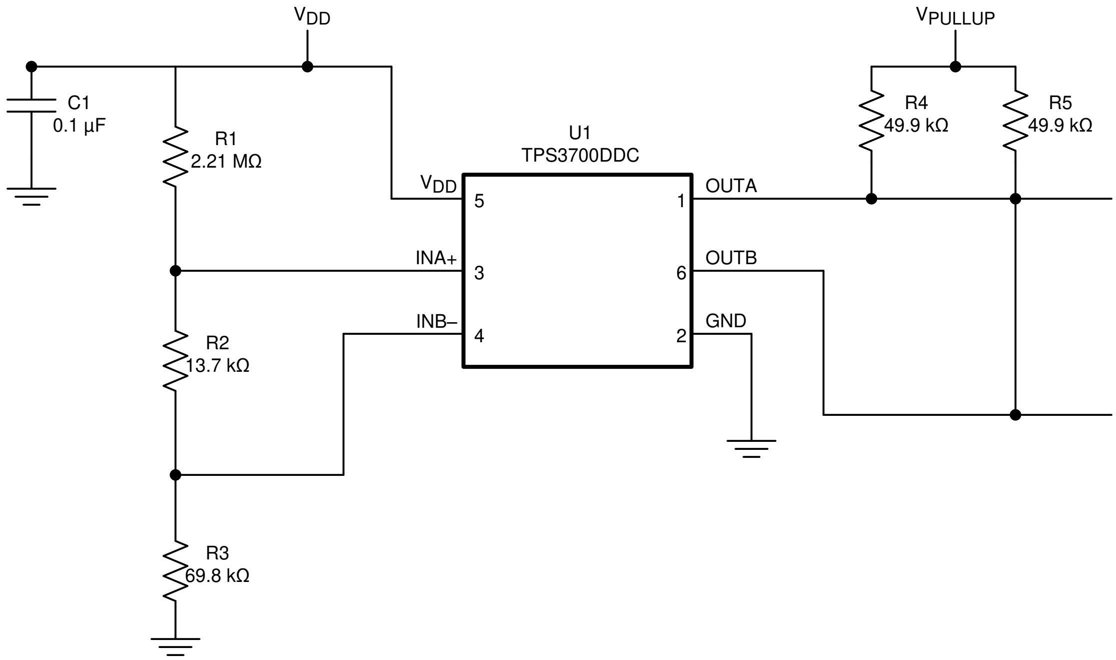


图 8-5. Typical Application Schematic

8.2.1 Design Requirements

8.2.1.1 Input Supply Capacitor

Although an input capacitor is not required for stability, connecting a 0.1-μF low equivalent series resistance (ESR) capacitor across the V_{DD} terminal and GND terminal is good analog design practice. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated, or if the device is not located close to the power source.

8.2.1.2 Input Capacitors

Although not required in most cases, for extremely noisy applications, placing a 1-nF to 10-nF bypass capacitor from the comparator inputs (INA+, INB–) to the GND terminal is good analog design practice. This capacitor placement reduces device sensitivity to transients.

8.2.2 Detailed Design Procedure

Use 方程式 1 through 方程式 4 to calculate the resistor divider values and target threshold voltage.

$$R_T = R_1 + R_2 + R_3 \quad (1)$$

Select a value for R_T such that the current through the divider is approximately 100-times higher than the input current at the INA+ and INB– terminals. The resistors can have high values to minimize current consumption as a result of low-input bias current without adding significant error to the resistive divider. See the application note *Optimizing Resistor Dividers at a Comparator Input* (SLVA450) for details on sizing input resistors.

Use 方程式 2 to calculate the value of R_3.

$$R_3 = \frac{R_T}{V_{MON(OV)}} \times V_{IT+} \quad (2)$$

where

- $V_{MON(OV)}$ is the target voltage at which an overvoltage condition is detected

Use 方程式 3 or 方程式 4 to calculate the value of R_2.

$$R_2 = \left[\frac{R_T}{V_{MON}\,(\text{no UV})} \times V_{IT+} \right] - R_3 \tag{3}$$

where

- $V_{MON(no\ UV)}$ is the target voltage at which an undervoltage condition is removed as V_{MON} rises

$$R_2 = \left[\frac{R_T}{V_{MON(UV)}} \times (V_{IT+} - V_{hys}) \right] - R_3 \tag{4}$$

where:

$V_{MON(UV)}$ is the target voltage at which an undervoltage condition is detected

•

8.2.3 Application Curves

T_J = 25°C

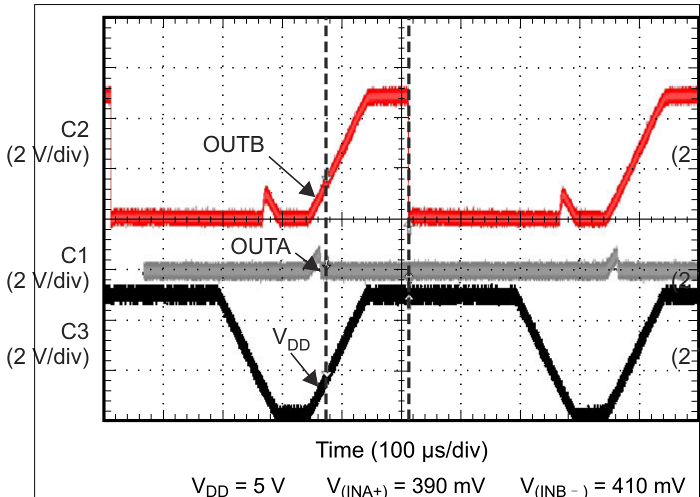


图 8-6. Startup Delay (Outputs Pulled Up to V_{DD})

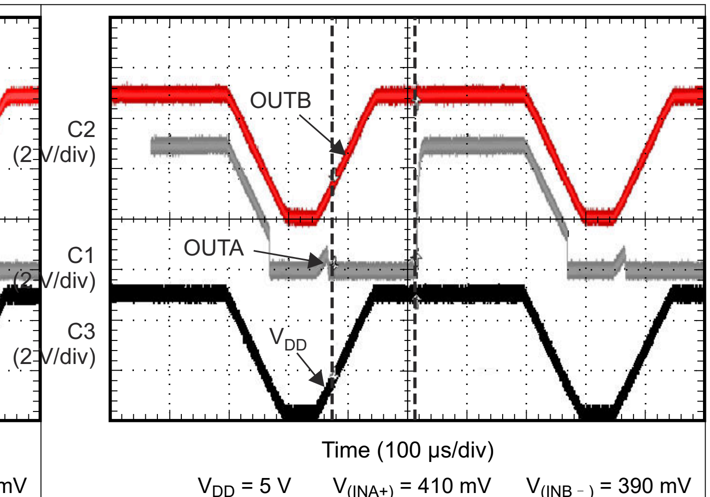


图 8-7. Startup Delay (Outputs Pulled Up to V_{DD})

9 Power Supply Recommendations

These devices are designed to operate from an input voltage supply range between 1.8 V and 18 V.

10 Layout

10.1 Layout Guidelines

Placing a 0.1-μF capacitor close to the V_{DD} terminal to reduce the input impedance to the device is good analog design practice. The pullup resistors can be separated if separate logic functions are needed (see 图 10-1) or both resistors can be tied to a single pullup resistor if a logical AND function is desired.

10.2 Layout Example

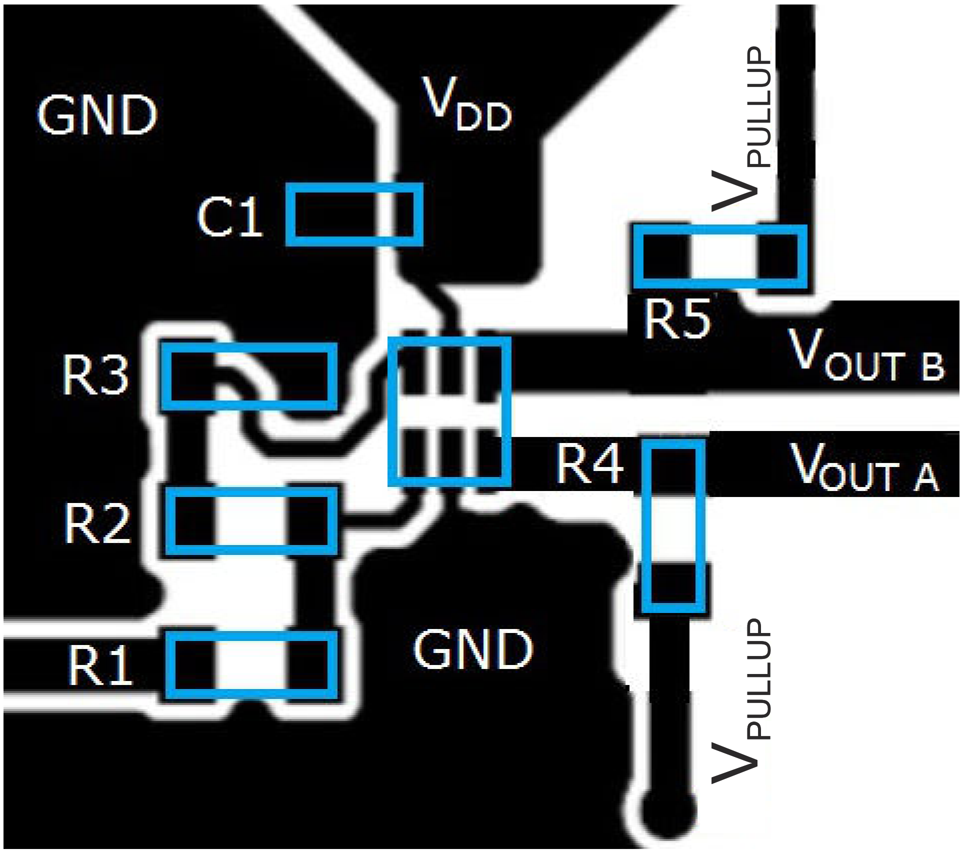


图 10-1. TPS3700-Q1 Layout Example

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- *Using the TPS3700 as a Negative Rail Over- and Undervoltage Detector*, SLVA600
- *Optimizing Resistor Dividers at a Comparator Input*, SLVA450
- *TPS3700EVM-114 Evaluation Module*, SLVU683

11.2 Trademarks

所有商标均为其各自所有者的财产。

11.3 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.4 术语表

TI 术语表　本术语表列出并解释了术语、首字母缩略词和定义。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS3700QDDCRQ1	ACTIVE	SOT-23-THIN	DDC	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PD7Q	Samples
TPS3700QDSERQ1	ACTIVE	WSON	DSE	6	3000	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	5O	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

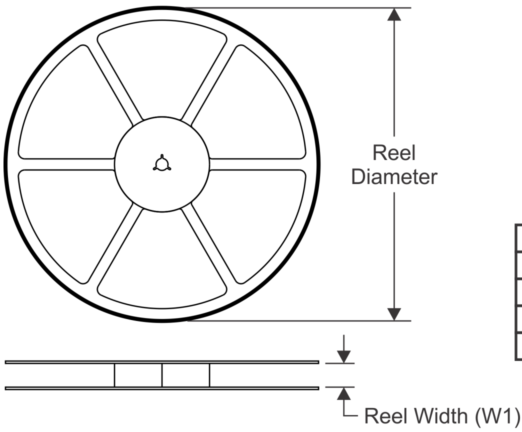
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

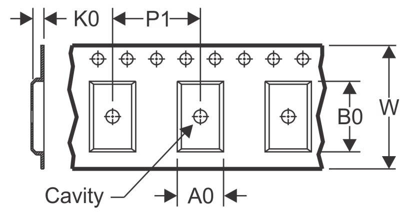
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

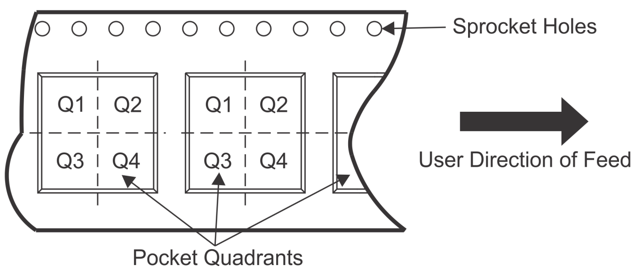


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

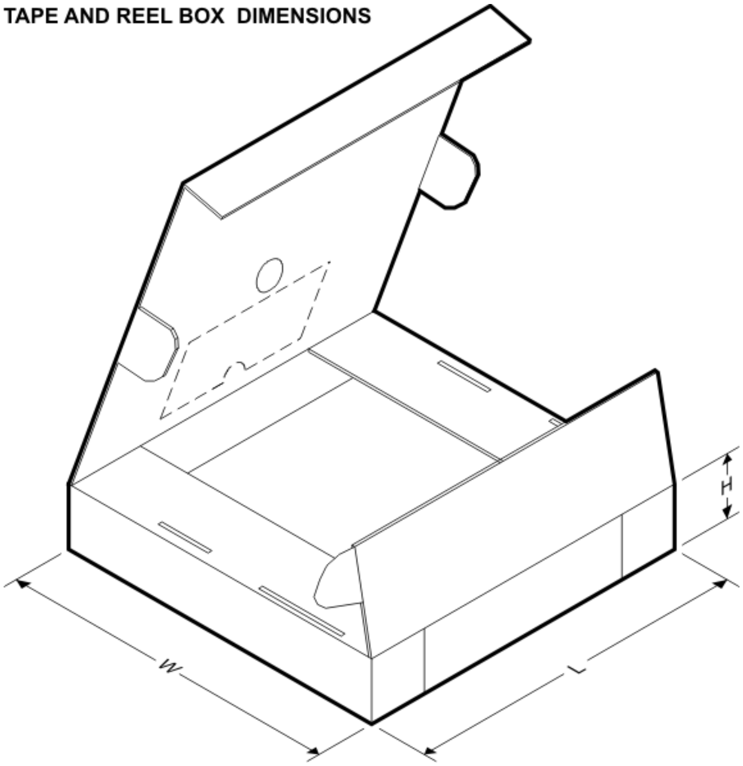
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

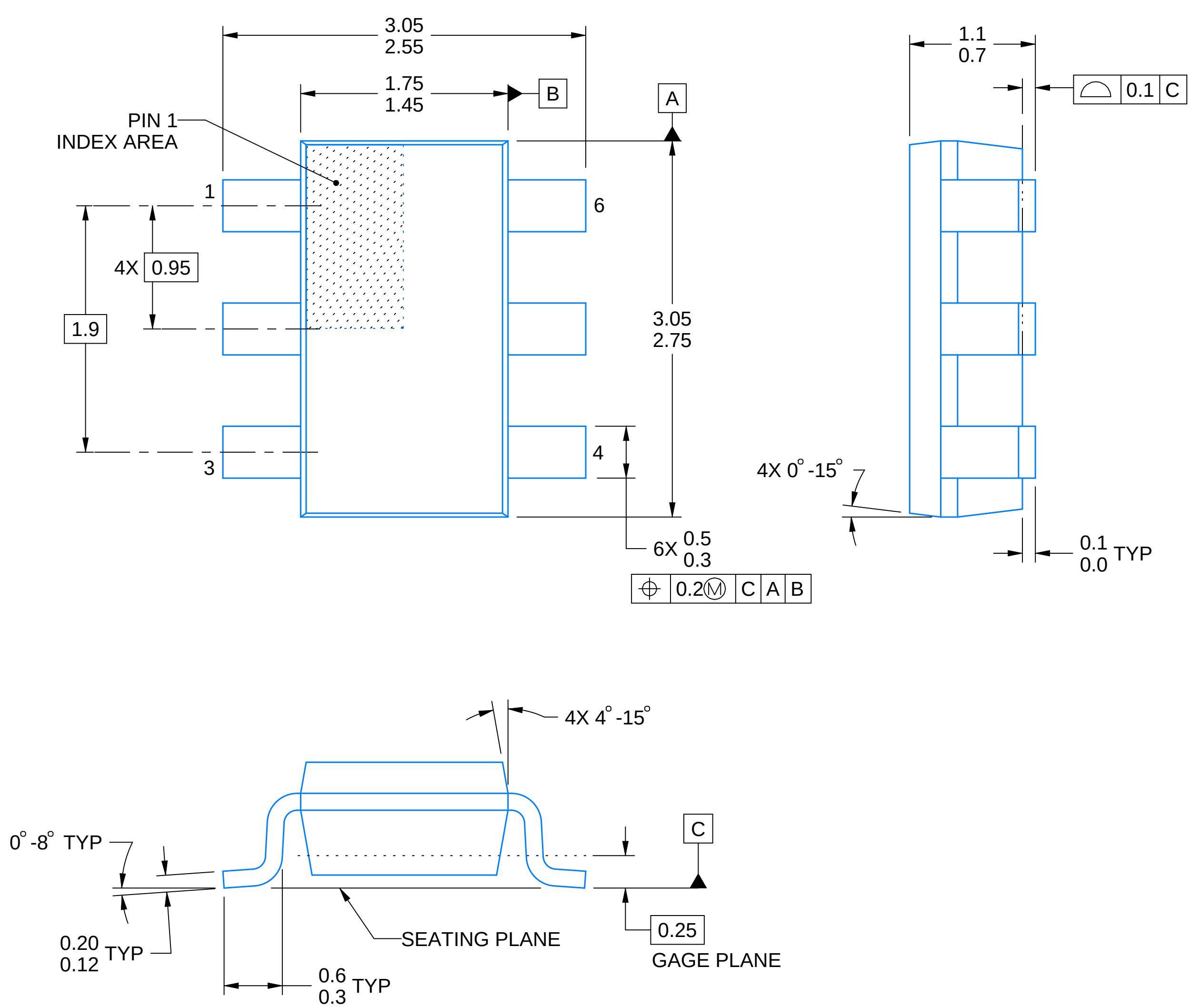
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3700QDDCRQ1	SOT-23-THIN	DDC	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3700QDSERQ1	WSON	DSE	6	3000	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

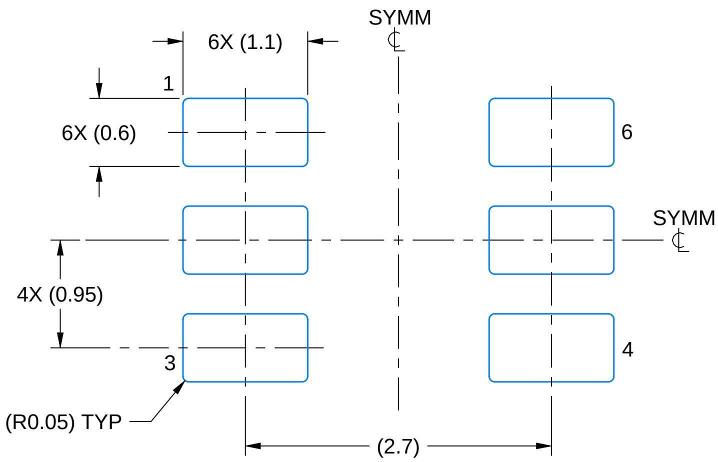
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3700QDDCRQ1	SOT-23-THIN	DDC	6	3000	213.0	191.0	35.0
TPS3700QDSERQ1	WSON	DSE	6	3000	213.0	191.0	35.0



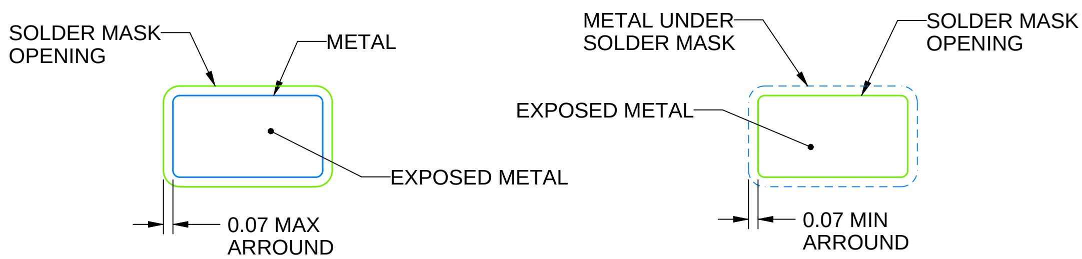
4214841/E 08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.



LAND PATTERN EXAMPLE
EXPLOSED METAL SHOWN
SCALE:15X



NON SOLDER MASK DEFINED

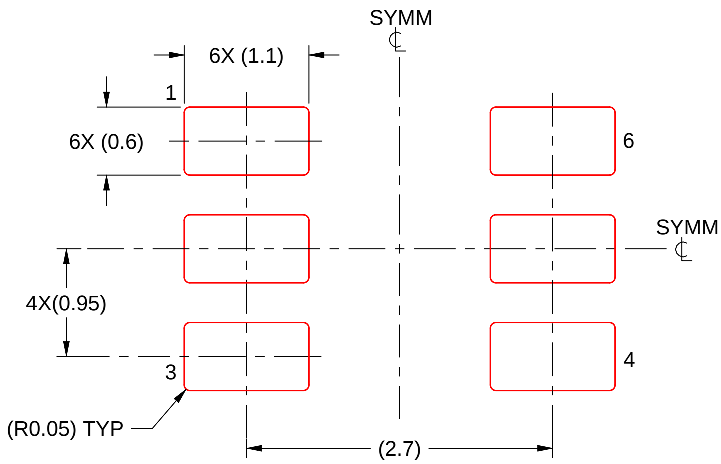
SOLDER MASK DEFINED

SOLDERMASK DETAILS

4214841/E 08/2024

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

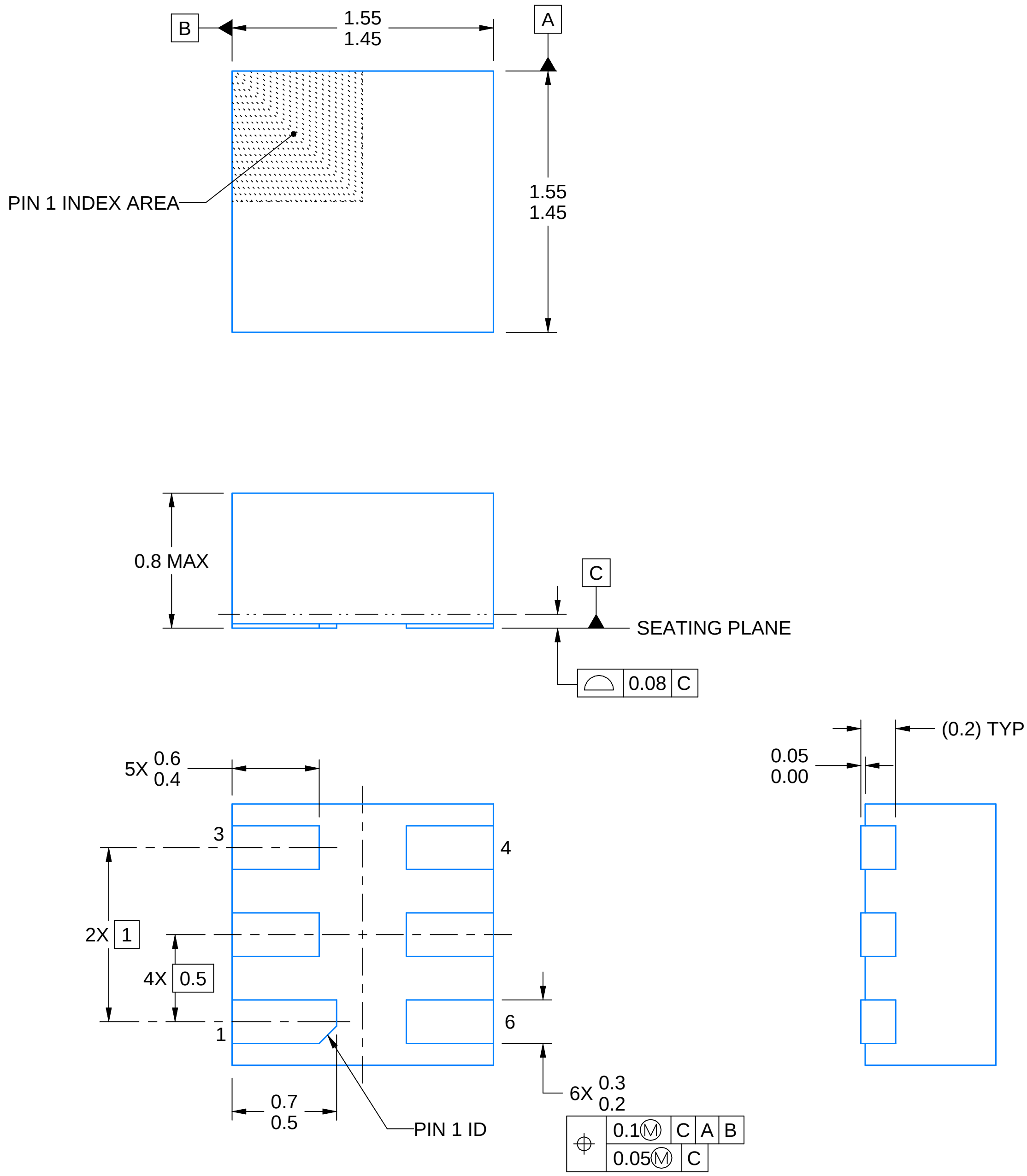


SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

4214841/E 08/2024

NOTES: (continued)

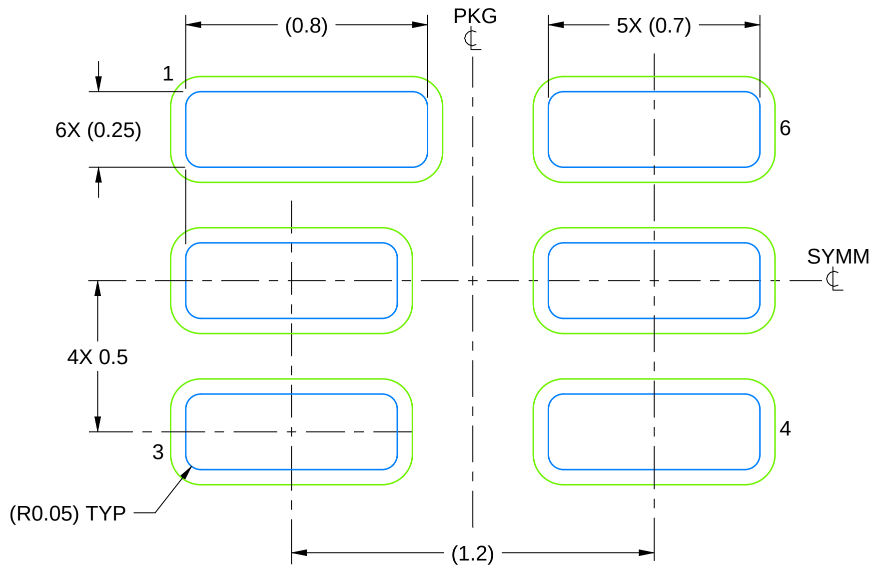
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.



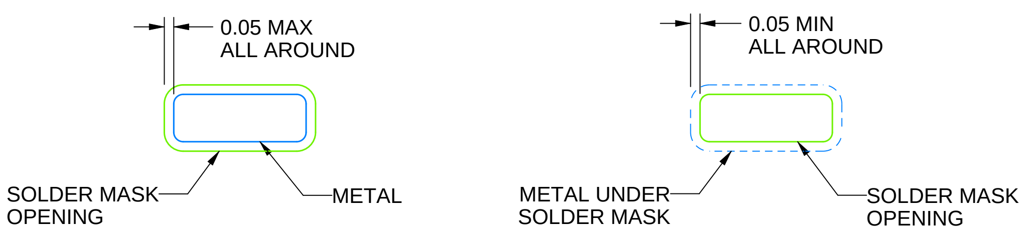
4220552/B 01/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:40X



PADS 4-6
NON SOLDER MASK
DEFINED

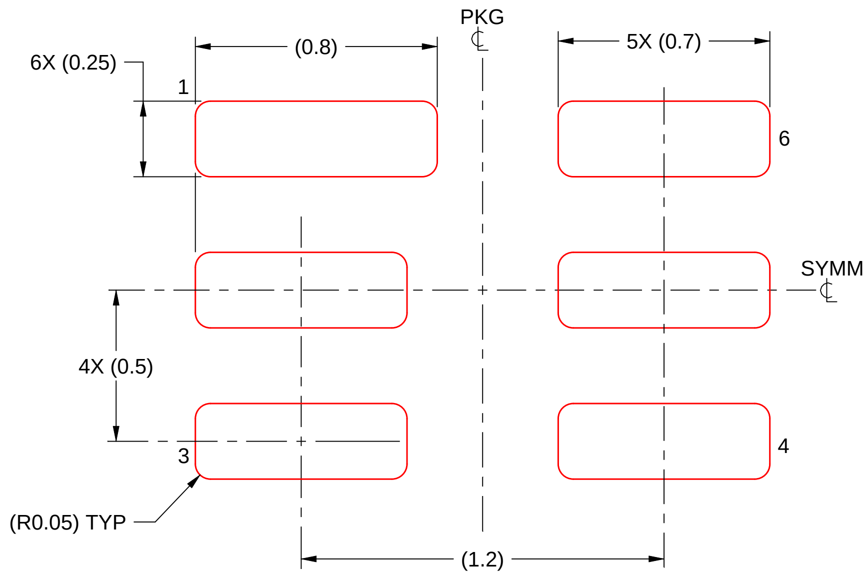
PADS 1-3
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220552/B 01/2024

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:40X

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要声明和免责声明

TI"按原样"提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 TI 的销售条款或 ti.com 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265