TPS54116-Q1 2.95V 至 6V 输入、4A 降压转换器和 1A 拉/灌电流 DDR 终端稳压器

1 特性

- 具有符合 AEC-Q100 标准的下列结果：
  - 器件温度 1 级：-40℃ 至 +125℃ 的环境运行温度范围
  - 器件人体模型 (HBM) 静电放电 (ESD) 分类等级 2
  - 器件组件充电模式 (CDM) ESD 分类等级 C6
- 单片 DDR2、DDR3 和 DDR3L 存储器电源解决方案
- 4A 同步降压转换器
  - 集成了 33mΩ 高侧和 25mΩ 低侧金属氧化物半导体场效应晶体管 (MOSFET)
  - 固定频率电流模式控制
  - 可调频率范围：100kHz 至 2.5MHz
  - 与一个外部时钟同步
  - 整个温度范围内的电压基准为 0.6V ± 1%
  - 可调逐周期峰值电流限制
  - 针对预偏置输出的单调性启动
- 直流精度为 ±20mV 的 1A 拉/灌电流终端低压降 (LDO) 稳压器
  - 与 2 × 10µF 多层陶瓷电容 (MLCC) 电容一起工作时保持稳定
  - 10mA 拉/灌电流缓冲参考输出稳定在 VDDQ 的 49% 至 51% 之间
- 独立使能引脚，欠压闭锁 (UVLO) 和迟滞均可调
- 热关断
- 运行温度 (T_J) 范围：-40°C 至 150°C
- 24 引脚 4mm x 4mm 超薄四方扁平无引线 (WSON) 封装

2 应用

- 嵌入式计算系统中的 DDR2、DDR3、DDR3L 和 DDR4 存储器电源
- SSTL_18、SSTL_15、SSTL_135、SSTL_12 和 HSTL 终端
- 信息娱乐和仪表板
- 先进的驾驶员辅助系统 (ADAS)

3 说明

TPS54116-Q1 器件是一款功能全面的 6V、4A 同步降压转换器，其配有两个集成型 MOSFET 以及带 VTTREF 缓冲参考输出的 1A 拉/灌电流双倍数据速率 (DDR) VTT 终端稳压器。

TPS54116-Q1 降压稳压器通过集成 MOSFET 和减小电感尺寸来最大限度减小解决方案尺寸，开关频率最高达 2.5MHz。开关频率可设置在中波频段以上以满足噪声敏感型 应用 的需求，而且能够与外部时钟同步。同步整流使频率在整个输出负载范围内保持为固定值。效率通过集成 25mΩ 低侧 MOSFET 和 33mΩ 高侧 MOSFET 得到了最大限度的提升。逐周期峰值电流限制在过流状态下保护器件，并且可通过 ILIM 引脚上的电阻进行调整，从而针对小尺寸电感进行优化。

VTT 终端稳压器仅利用 2 × 10µF 的陶瓷输出电容即可保持快速瞬态响应，从而减少外部组件数量。TPS54116-Q1 使用 VTT 进行远程感测，从而实现最佳的稳压效果。

该器件可利用使能引脚进入关断模式，从而使电源电流降至 1µA。欠压闭锁阈值可通过任一使能引脚上的电阻网络进行设置。VTT 和 VTTREF 输出被 ENLDO 禁用时会进行放电。

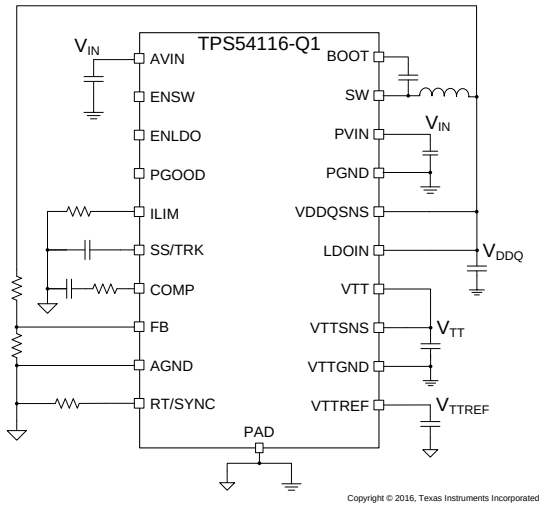
该器件具备全集成特性，并且采用小尺寸的 4mm × 4mm 耐热增强型 WQFN 封装，最大限度地减小了 IC 尺寸。

器件信息(1)

器件型号	封装	封装尺寸（标称值）
TPS54116-Q1	WQFN (24)	4.00mm x 4.00mm

(1) 如需了解所有可用封装，请见数据表末尾的可订购产品附录。

简化电路原理图



目录

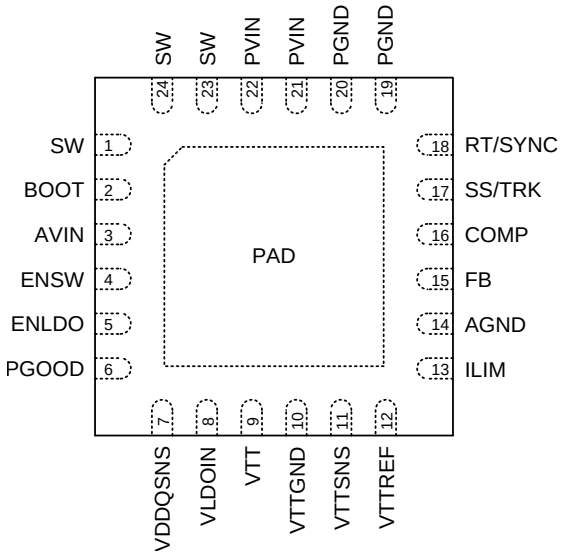
4 修订历史记录

Changes from Original (August 2016) to Revision A **Page**

- Changed pin 18 From: RT/CLK To: RT/SYNC in the *Pin Functions* table ... 4
- Changed $R_{(RT/CLK)}$ To: $R_{(RT/SYNC)}$ in 图 16 and 图 17 ... 9
- Changed "The RT/CLK is typically 0.5 V.." To: "The RT/SYNC is typically 0.5 V.." in *Constant Switching Frequency and Timing Resistor (RT/SYNC)* ... 20

5 Pin Configuration and Functions

RTW Package
WQFN 24 Pins
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
SW	1, 23, 24	O	Switching node of the buck converter.
BOOT	2	I	Bootstrap capacitor node for high-side MOSFET gate driver of the buck converter. Connect the bootstrap capacitor from this pin to the SW pin.
AVIN	3	I	The input supply pin to the IC, powering the control circuits of both the buck converter and DDR termination regulator. Connect AVIN to a supply voltage between 2.95 V and 6 V.
ENSW	4	I	Buck converter enable pin with internal pull-up current source. Floating this pin will enable the IC. Pull below 1.17 V to enter low current standby mode. Pull below 0.4 V to enter shutdown mode. The ENSW pin can be used to implement adjustable under-voltage lockout (UVLO) using two resistors.
ENLDO	5	I	VTT LDO enable pin with internal pull-up current source. Floating this pin will enable the IC. Pull below 1.17 V to enter low current standby mode. Pull below 0.4 V to enter shutdown mode. The ENLDO pin can be used to implement adjustable under-voltage lockout (UVLO) using two resistors.
PGOOD	6	O	Power good indicator for the buck regulator. This pin is an open-drain output. A 10-kΩ pull-up resistor is recommended between PGOOD and AVIN or an external logic supply pin.
VDDQSNS	7	I	VDDQ sense input to generate VDDQ/2 reference for VTTREF.
LDOIN	8	I	Power supply input for VTT LDO. Connected VDDQ in typical application. Alternatively this pin can be used for split-rail configuration to reduce power dissipation when sourcing current to the VTT output by powering the VTT LDO with a lower voltage.
VTT	9	O	1-A LDO output. Connect 2 x 10-µF ceramic capacitors to VTTGND for stability.
VTTGND	10	I	Power ground for VTT LDO.
VTTSNS	11	I	VTT LDO voltage feedback.
VTTREF	12	O	Buffered low-noise VTT reference output. Connect to a 0.22 µF or larger ceramic capacitor to AGND for stability.
ILIM	13	I	Programmable current limit pin. An internal amplifier holds this pin at a fixed voltage then sets the high-side MOSFET peak current limit based on the value of an external resistor to AGND.
AGND	14	I	Analog signal ground of the IC. AGND should be connected to PGND via a single point on the PCB, typically to the thermal pad.

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
FB	15	I	Error amplifier inverting input and feedback pin for voltage regulation of the buck converter. Connect this pin to the center of a resistor divider to set the output voltage of the buck converter. The resistor divider should go from the regulated output voltage to AGND.
COMP	16	I	Output of the internal transconductance error amplifier for the buck converter. The feedback loop compensation network is connected from this pin to AGND.
SS/TRK	17	I	Soft-start programming pin. A capacitor between the SS/TRK pin and AGND pin sets soft-start time. The voltage on this pin overrides the internal reference allowing it to be used for tracking and sequencing.
RT/SYNC	18	I	Resistor Timing and External Clock. An internal amplifier holds this pin at a fixed voltage when using an external resistor to AGND to set the switching frequency. If the pin is pulled above the upper threshold, a mode change occurs and the pin becomes a synchronization input. The internal amplifier is disabled and the pin is a high impedance clock input. If clocking edges stop, the internal amplifier is re-enabled and the operating mode returns to resistor frequency programming.
PGND	19, 20	I	Power ground of the buck regulator. PGND should be connected to AGND via a single point on PCB board, typically to the thermal pad.
PVIN	21, 22	I	The input supply pin for power MOSFETs. Connect PVIN to a supply voltage between 2.95 V and 6 V.
PAD		–	The exposed thermal pad must be electrically connected to AGND and PGND on the printed circuit board for proper operation. Connect to the largest possible copper area for best thermal performance.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Voltage Range	PVIN, AVIN, ENSW, ENLDO, PGOOD	-0.3	7	V
	FB, COMP, SS/TRK, ILIM	-0.3	3	V
	RT/SYNC	-0.3	6	V
	BOOT with respect to SW	-0.3	7	V
	LDOIN, VTTSNS, VDDQSNS	-0.3	3.6	V
	SW	-0.6	7	V
	SW, 10-ns transient	-4	10	V
	VTT, VTTREF	-0.3	3.6	V
Current Range	RT/SYNC	-100	100	µA
	PGOOD	-5	5	mA
Operating junction temperature		-40	150	°C
Storage temperature, T_{stg}		-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{(AVIN)}$, $V_{(PVIN)}$	Input voltage	2.95	6	V
V_{OUT}	Buck output voltage	0.6	4.5	V
I_{OUT}	Buck output current	0	4	A
$V_{(VDDQSNS)}$	VDDQSNS input voltage	1	3.5	V
$V_{(LDOIN)}$	LDOIN input voltage	VTT + VDO	3.5	V
$V_{(VTT)}$, $V_{(VTTREF)}$	VTT and VTTREF output voltage	0.5	3.5	V

6.4 Thermal Information

THERMAL METRIC(1)		TPS54116-Q1 RTW (WQFN) 24 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	36.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	35.0	
$R_{\theta JB}$	Junction-to-board thermal resistance	14.3	
ψ_{JT}	Junction-to-top characterization parameter	0.4	
ψ_{JB}	Junction-to-board characterization parameter	14.4	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4.6	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

TJ = -40°C to 150°C, AVIN = PVIN = 2.95 V to 6 V, VLDOIN = VDDQSNS (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (AVIN and PVIN PINS)						
	AVIN and PVIN operating		2.95		6	V
	AVIN internal UVLO threshold	AVIN rising		2.7	2.8	V
	AVIN internal UVLO hysteresis			0.05	0.12	V
	Iq shutdown	$V_{(ENSW)}$ = $V_{(ENLDO)}$ = 0 V, $V_{(VDDQSNS)}$ = 1.8 V, TJ = 25°C		1	3.5	µA
	Iq operating — LDO and buck enabled	$V_{(ENSW)}$ = $V_{(ENLDO)}$ = $V_{(AVIN)}$ = 5 V, $V_{(FB)}$ = 0.7 V, $V_{(VDDQSNS)}$ = 1.8 V, TJ = 25°C		650	800	µA
	Iq operating — LDO enabled, buck disabled	$V_{(ENLDO)}$ = $V_{(AVIN)}$ = 5 V, $V_{(ENSW)}$ = 0 V, $V_{(VDDQSNS)}$ = 1.8 V, TJ = 25°C		190	300	µA
	Iq operating — LDO disabled, buck enabled	$V_{(ENSW)}$ = $V_{(AVIN)}$ = 5 V, $V_{(ENLDO)}$ = 0 V, $V_{(FB)}$ = 0.7 V, $V_{(VDDQSNS)}$ = 1.8 V, TJ = 25°C		570	700	µA
ENABLE (ENSW and ENLDO PINS)						
$V_{ENRISING}$	ENLDO rising threshold	ENLDO voltage ramping up		1.20		V
$V_{ENFALLING}$	ENLDO falling threshold	ENLDO voltage ramping down		1.17		
	ENLDO input current above voltage threshold	$V_{(ENLDO)}$ = Enable threshold + 50 mV		-4.4		µA
I_p	ENLDO input current below voltage threshold	$V_{(ENLDO)}$ = Enable threshold - 50 mV		-1.7		
I_h	ENLDO hysteresis current			-2.7		
$V_{ENRISING}$	ENSW rising threshold	ENSW voltage ramping up		1.20		V
$V_{ENFALLING}$	ENSW falling threshold	ENSW voltage ramping down		1.17		
	ENSW input current above voltage threshold	$V_{(ENSW)}$ = Enable threshold + 50 mV		-4.4		µA
I_p	ENSW input current below voltage threshold	$V_{(ENSW)}$ = Enable threshold - 50 mV		-1.7		
I_h	ENSW hysteresis current			-2.7		
	Input current above voltage threshold with ENLDO and ENSW connected	$V_{(ENLDO)}$ = $V_{(ENSW)}$ = Enable threshold + 50 mV		-8.5		µA

Electrical Characteristics (continued)

TJ = -40°C to 150°C, AVIN = PVIN = 2.95 V to 6 V, VLDOIN = VDDQSNS (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Input current below voltage threshold with ENLDO and ENSW connected	$V_{(ENLDO)}$ = $V_{(ENSW)}$ = Enable threshold - 50 mV		-3.4		µA
	Hysteresis current with ENLDO and ENSW connected			-5.1		µA
VOLTAGE REFERENCE AND ERROR AMPLIFIER (FB AND COMP PINS)						
V_{REF}	Voltage Reference		0.594	0.6	0.606	V
	FB pin input current			7		nA
gm_{EA}	Error Amp transconductance (gm)	-2 µA < $I_{(COMP)}$ < 2 µA, $V_{(COMP)}$ = 1 V		260	360	µS
	Error Amp source/sink	$V_{(COMP)}$ = 1 V, $V_{(FB)}$ = 100 mV overdrive		22		µA
MOSFETS AND POWER STAGE (SW AND BOOT PINS)						
	High side switch resistance	$V_{(BOOT-SW)}$ = 5 V		33	66	mΩ
		$V_{(BOOT-SW)}$ = 3.3 V		42	84	
	Low side switch resistance	$V_{(PVIN)}$ = 5 V		25	50	mΩ
		$V_{(PVIN)}$ = 3.3 V		30	60	
	BOOT-SW UVLO	$V_{(PVIN)}$ = 2.95 V		2.2		V
	High-side FET current limit	$V_{(PVIN)}$ = 6V, $R_{(ILIM)}$ = 100k	5.2	6.6	8.2	A
	High-side FET current limit	$V_{(PVIN)}$ = 6V, $R_{(ILIM)}$ = 200k	1.5	3	3.8	A
	Low-side FET reverse current limit		2	4.5		A
gm_{PS}	$V_{(COMP)}$ to $I_{(SW)}$peak transconductance	$R_{(ILIM)}$ = 100k		16		A/V
	Minimum pulse width	Measured at 50% points on $V_{(SW)}$, I_{OUT} = 2 A		60		ns
	Minimum pulse width	Measured at 50% points $V_{(SW)}$, $V_{(PVIN)}$ = 5 V, I_{OUT} = 0 A, TJ = -40°C to 125°C		100	125	ns
	Minimum off-time	Prior to skipping off pulses, I_{OUT} = 2 A		60		ns
TIMING RESISTOR AND EXTERNAL CLOCK (RT/SYNC PIN)						
	Switching frequency range using RT mode		100		2500	kHz
	Switching frequency	$R_{(RT/SYNC)}$ = 150 kΩ	370	400	430	kHz
		$R_{(RT/SYNC)}$ = 27 kΩ	1910	2070	2230	kHz
		$V_{(RT/SYNC)}$ > 2.2 V or $V_{(RT/SYNC)}$ < 0.35 V	340	420	480	kHz
	Switching frequency range using SYNC mode		100		2500	kHz
	Minimum SYNC input pulse width		10			ns
	RT/SYNC high threshold			1.5	2.2	V
	RT/SYNC low threshold		0.35	0.4		V
	RT/SYNC rising edge to SW rising edge delay	f_{SW} = 500 kHz	30	45	80	ns
	RT to SYNC lock in time	$R_{(RT/SYNC)}$ = 150 kΩ		55		µs
	SYNC to RT lock in time			60		µs
	Internal RT to SYNC lock in time	Logic high or logic low at RT/SYNC to SYNC signal		55		µs
	SYNC to internal RT lock in time	SYNC signal to logic high or logic low at RT/SYNC		60		µs
SOFT START AND TRACKING (SS/TRK PIN)						
V_{SSTHR}	SS voltage threshold			0.15		V
I_{SS}	Charge Current	$V_{(SS/TRK)}$ < V_{SSTHR}		47		µA
		$V_{(SS/TRK)}$ > V_{SSTHR}	1.5	2.4	3.2	µA
	SS/TRK to FB matching	$V_{(SS/TRK)}$ = 0.3 V		60		mV
	SS/TRK to reference crossover	98% normal		0.85	1	V
	SS/TRK discharge voltage (overload)	$V_{(FB)}$ = 0 V		120		mV
	SS/TRK discharge voltage (fault)	$V_{(FB)}$ = 0 V		5		mV
	SS/TRK discharge current (overload)	$V_{(FB)}$ = 0 V, $V_{(SS/TRK)}$ = 0.4 V		160		µA

Electrical Characteristics (continued)

TJ = -40°C to 150°C, AVIN = PVIN = 2.95 V to 6 V, VLDOIN = VDDQSNS (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	SS/TRK discharge current (AVIN UVLO, ENSW low, thermal fault)	$V_{(AVIN)}$ = 5 V, $V_{(SS/TRK)}$ = 0.4 V		760		µA
POWER GOOD (PGOOD PIN)						
	Threshold	$V_{(FB)}$ falling (fault)		91	95	% V_{REF}
		$V_{(FB)}$ rising (good)		94		
		$V_{(FB)}$ rising (fault)	105	109		
		$V_{(FB)}$ falling (good)		106		
	Hysteresis	$V_{(FB)}$ falling and rising		3		
	Output high leakage	$V_{(FB)}$ = V_{REF}, $V_{(PGOOD)}$ = 5.5 V		5	125	nA
	On resistance	$V_{(AVIN)}$ = 2.95 V		85	170	Ω
	Minimum $V_{(AVIN)}$ for valid output	$V_{(PGOOD)}$ < 0.5 V, $I_{(PGOOD)}$ = 100 µA		1.3	1.7	V
TERMINATION REGULATOR INPUTS (VLDOIN AND VDDQSNS PINS)						
	$V_{(LDOIN)}$ Operating				3.5	V
V_{DO}	DC $V_{(LDOIN)}$ – $V_{(VTT)}$ dropout	1.2 V < $V_{(VDDQSNS)}$ < 2.5 V, $I_{(VTT)}$ = 0.5 A, $V_{(VTT)}$ = $V_{(VTTREF)}$ - 40 mV			0.15	V
V_{DO}	DC $V_{(LDOIN)}$ – $V_{(VTT)}$ dropout	1.2 V < $V_{(VDDQSNS)}$ < 2.5 V, $I_{(VTT)}$ = 1.5 A, $V_{(VTT)}$ = $V_{(VTTREF)}$ - 40 mV			0.45	V
	VLDOIN supply current	$V_{(LDOIN)}$ = 1.8 V, TJ = 25°C			1	µA
	VDDQSNS input current	$V_{(VDDQSNS)}$ = 1.8 V		39	46	µA
VTTREF OUTPUT (VTTREF PIN)						
$V_{(VTTREF)}$	VTTREF output voltage			$V_{(VDDQSNS)}$/2		V
$V_{(VTTREF)TOL}$	VTTREF output voltage difference from $V_{(VDDQSNS)}$/2	$\|I_{(VTTREF)}\|$ < 10 mA, $V_{(VDDQSNS)}$ = 1.8 V	-18		18	mV
		$\|I_{(VTTREF)}\|$ < 10 mA, $V_{(VDDQSNS)}$ = 1.5 V	-15		15	
		$\|I_{(VTTREF)}\|$ < 10 mA, $V_{(VDDQSNS)}$ = 1.2 V	-15		15	
		$\|I_{(VTTREF)}\|$ < 5 mA, $V_{(VDDQSNS)}$ = 1.2 V	-12		12	
$I_{(VTTREF)SRC}$	VTTREF source current limit	$V_{(VDDQSNS)}$ = 1.8 V, $V_{(VTTREF)}$ = 0 V	10	18		mA
$I_{(VTTREF)SNK}$	VTTREF sink current limit	$V_{(VDDQSNS)}$ = 0 V, $V_{(VTTREF)}$ = 1.8 V	10	19		mA
$I_{(VTTREF)DIS}$	VTTREF discharge current	TJ = 25°C, $V_{(VTTREF)}$ = 0.5V, $V_{(ENLDO)}$ = 0 V	0.9	1.1		mA
VTT OUTPUT (VTT PIN)						
$V_{(VTT)}$	VTT output voltage			$V_{(VTTREF)}$		V
$V_{(VTT)TOL}$	VTT output voltage tolerance to VTTREF	$\|I_{(VTT)}\|$≤ 10 mA, 1.2 V ≤ $V_{(VDDQSNS)}$ ≤ 1.8 V	-20		20	mV
		$\|I_{(VTT)}\|$≤ 1 A, 1.2 V ≤ $V_{(VDDQSNS)}$ ≤ 1.8 V	-30		30	
		$\|I_{(VTT)}\|$≤ 1.5 A, 1.2 V ≤ $V_{(VDDQSNS)}$ ≤ 1.8 V	-40		40	
$I_{(VTT)SRC}$	VTT source current limit	$V_{(VDDQSNS)}$ = 1.8 V, $V_{(VTT)}$ = $V_{(VTTSNS)}$ = 0.7 V	1.5	2.5		A
$I_{(VTT)SNK}$	VTT sink current limit	$V_{(VDDQSNS)}$ = 1.8 V, $V_{(VTT)}$ = $V_{(VTTSNS)}$ = 1.1 V	1.5	2.5		A
$I_{(VTTSNS)BIAS}$	VTTSNS input bias current		-0.1		0.1	µA
$I_{(VTT)DIS}$	VTT discharge current	TJ = 25°C, $V_{(VTT)}$ = 0.5 V, $V_{(ENLDO)}$ = 0 V	4.8	6		mA
THERMAL SHUTDOWN						
	Thermal shutdown temperature			175		℃
	Thermal shutdown hysteresis			16		℃

6.6 Typical Characteristics

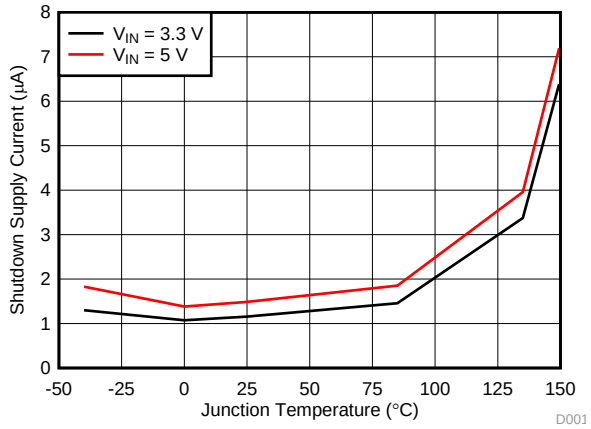


图 1. Shutdown Supply Current vs Temperature

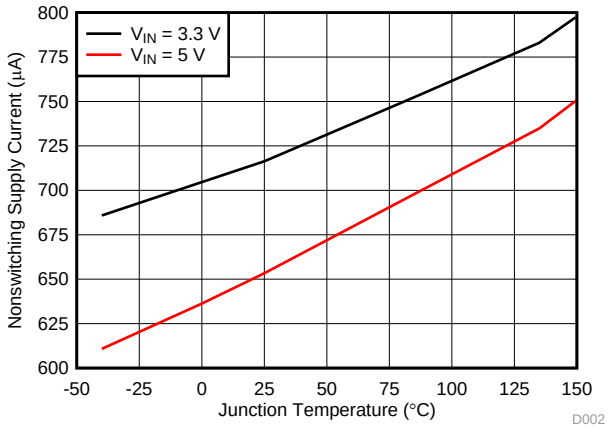


图 2. Non-switching Supply Current - LDO and Buck Enabled vs Temperature

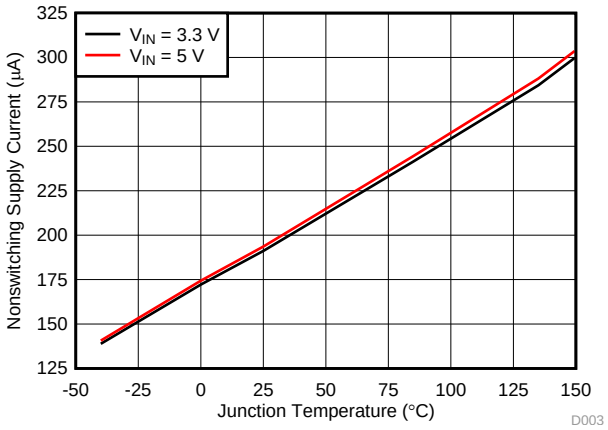


图 3. Non-switching Supply Current - LDO Enabled and Buck Disabled vs Temperature

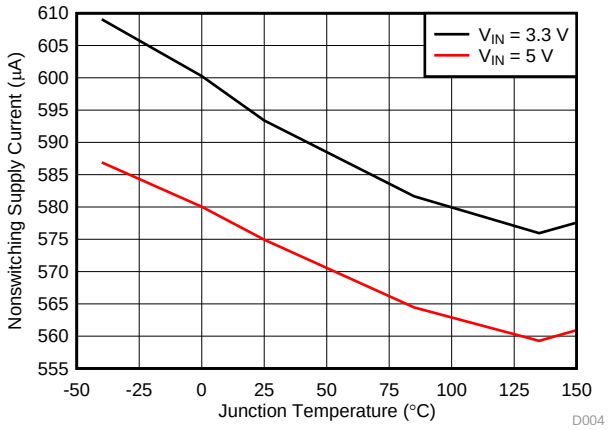


图 4. Non-switching Supply Current - LDO Disabled and Buck Enabled vs Temperature

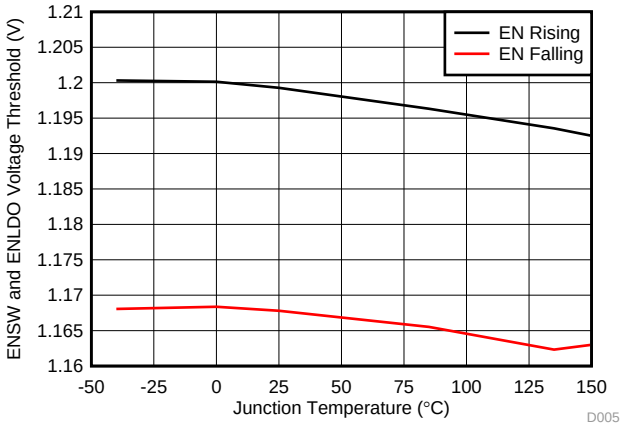


图 5. ENSW and ENLDO Voltage Threshold vs Temperature

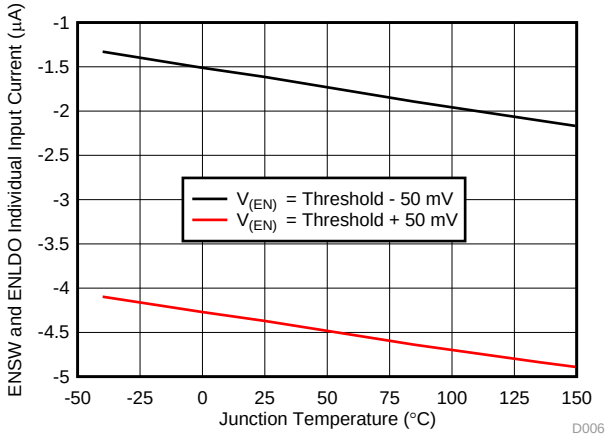


图 6. ENSW and ENLDO Individual Input Current vs Temperature

Typical Characteristics (接下页)

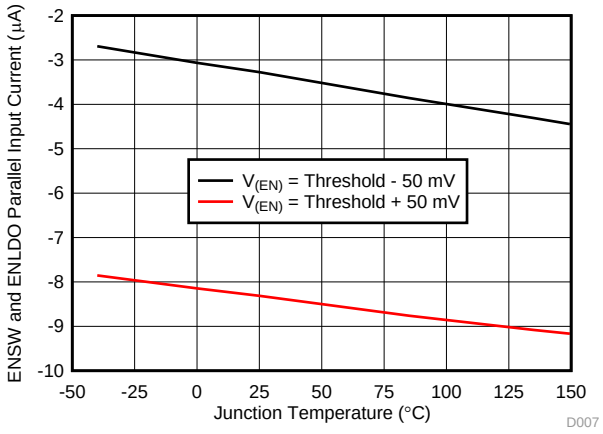


图 7. ENSW and ENLDO Parallel Input Current vs Temperature

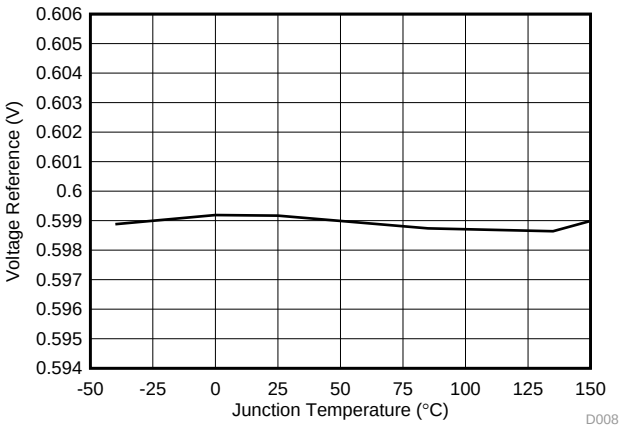


图 8. Voltage Reference vs Temperature

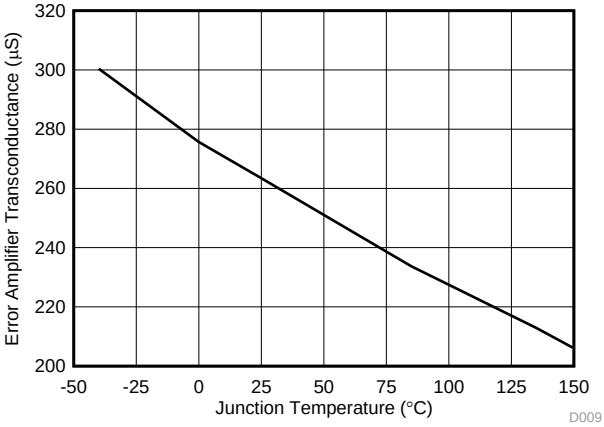


图 9. Error Amplifier Transconductance vs Temperature

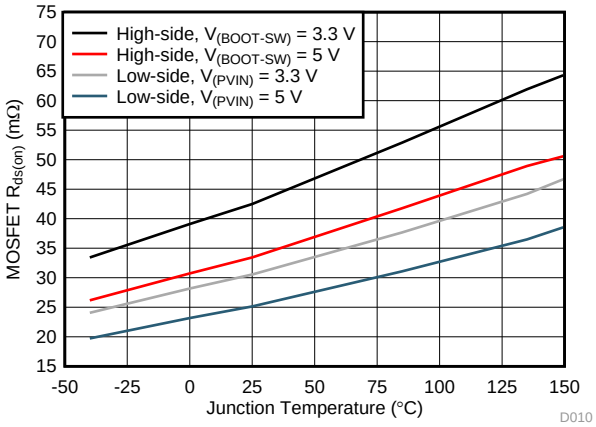


图 10. MOSFET $R_{ds(on)}$ vs Temperature

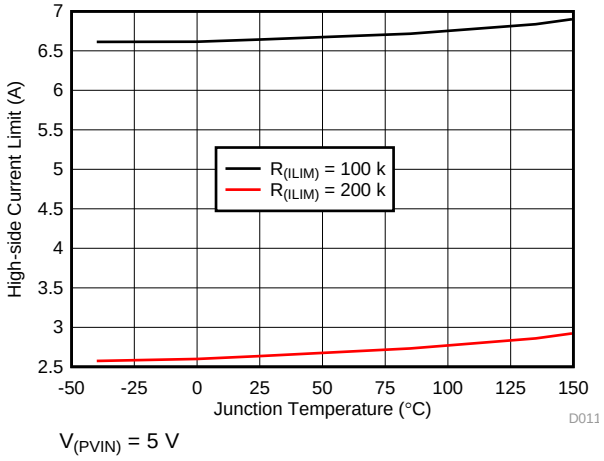


图 11. High-side Current Limit vs Temperature

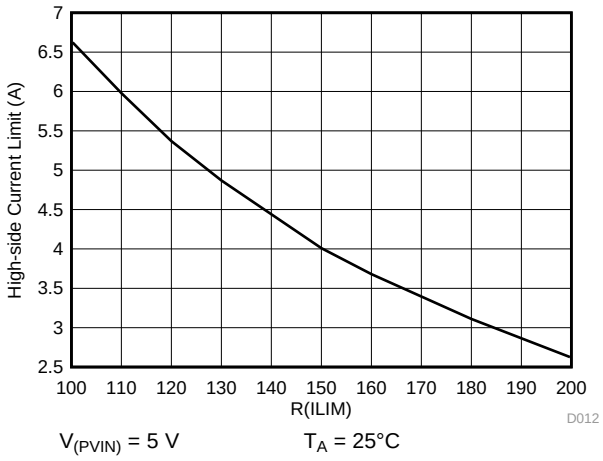


图 12. High-side Current Limit vs R_{ILIM}

Typical Characteristics (接下页)

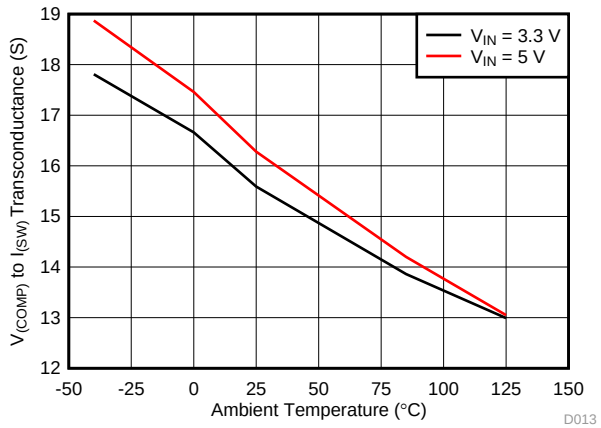


图 13. $V_{(COMP)}$ to $I_{(SW)}$ Transconductance vs Temperature

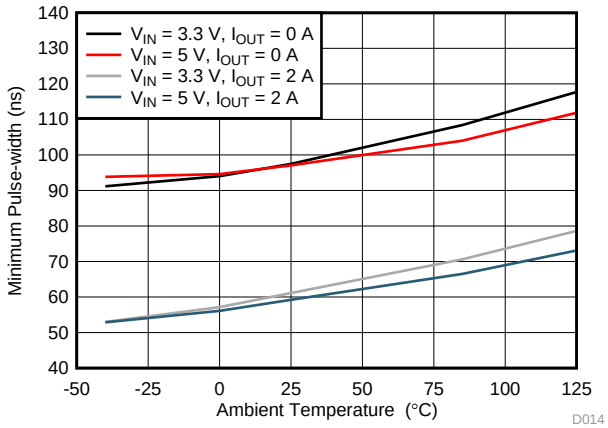
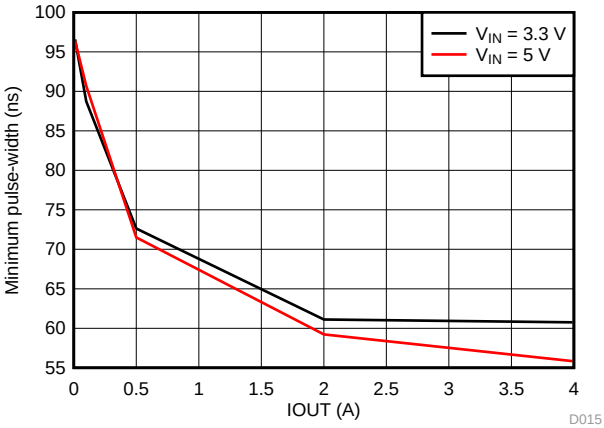
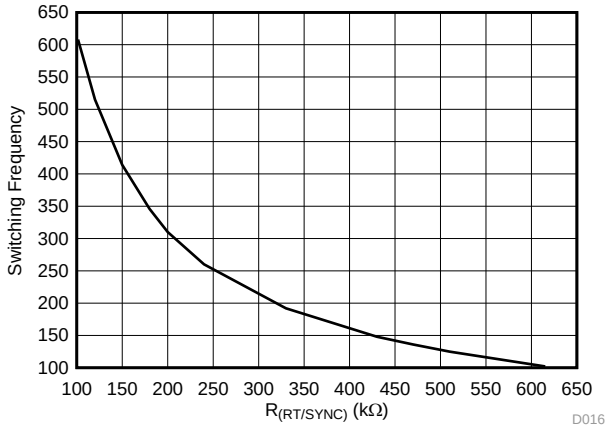


图 14. Minimum Pulse-width vs Temperature



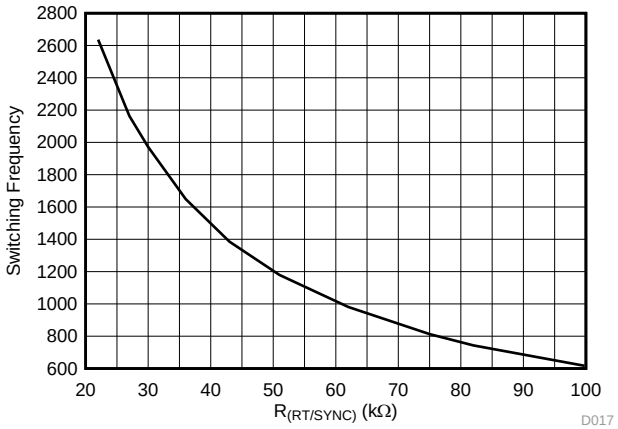
T_A = 25°C

图 15. Minimum pulse-width vs Load Current



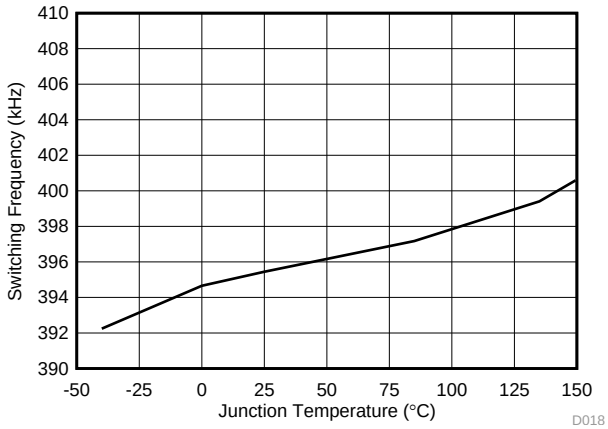
T_A = 25°C

图 16. Switching Frequency vs $R_{(RT/SYNC)}$ Low Range



T_A = 25°C

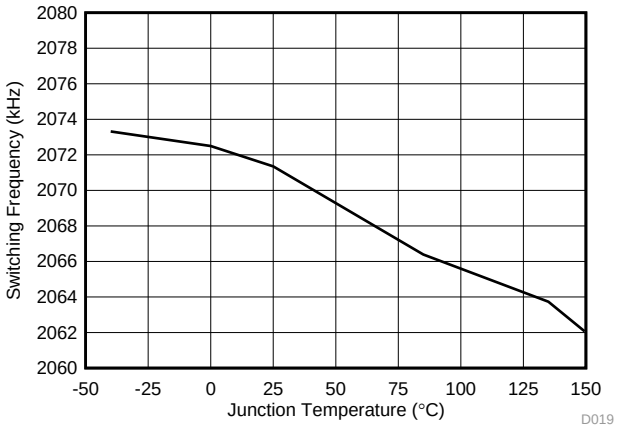
图 17. Switching Frequency vs $R_{(RT/SYNC)}$ High Range



$R_{(RT/SYNC)}$ = 150 kΩ

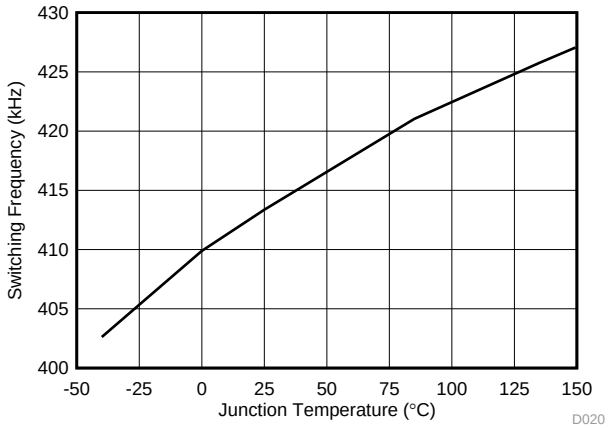
图 18. Switching Frequency vs Temperature

Typical Characteristics (接下页)



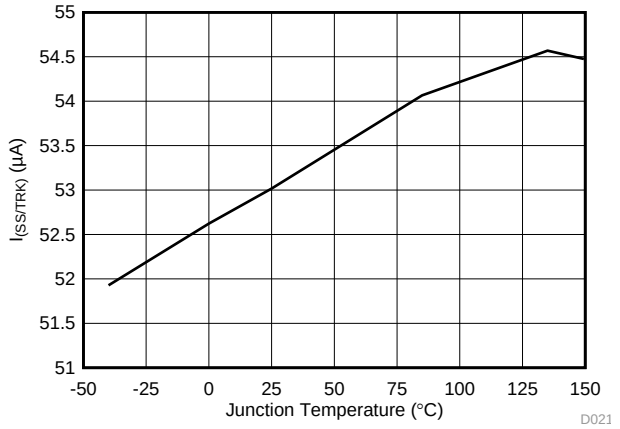
$R_{(RT/SYNC)}$ = 27 kΩ

图 19. Switching Frequency vs Temperature



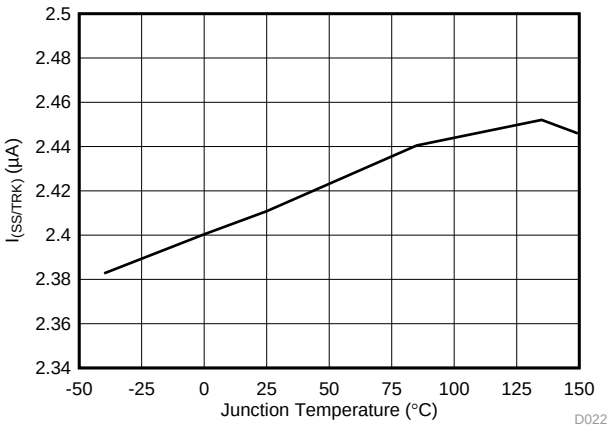
Internal RT

图 20. Switching Frequency vs Temperature



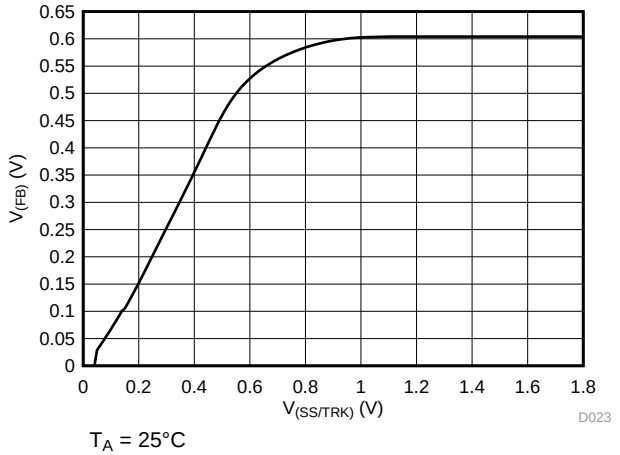
$V_{(SS/TRK)} < V_{SS(THR)}$

图 21. $I_{(SS/TRK)}$ vs Temperature



$V_{(SS/TRK)} > V_{SS(THR)}$

图 22. $I_{(SS/TRK)}$ vs Temperature



T_A = 25°C

图 23. $V_{(FB)}$ vs $V_{(SS/TRK)}$

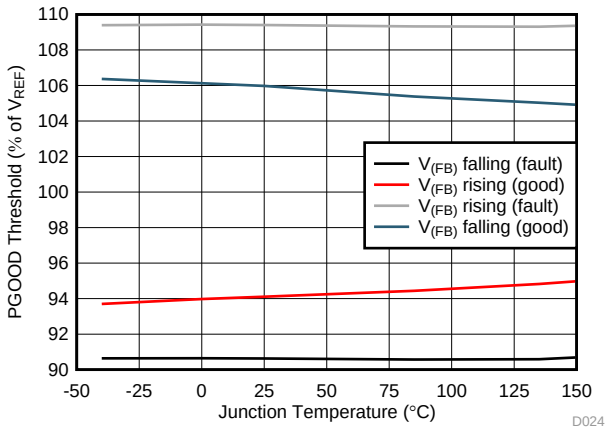
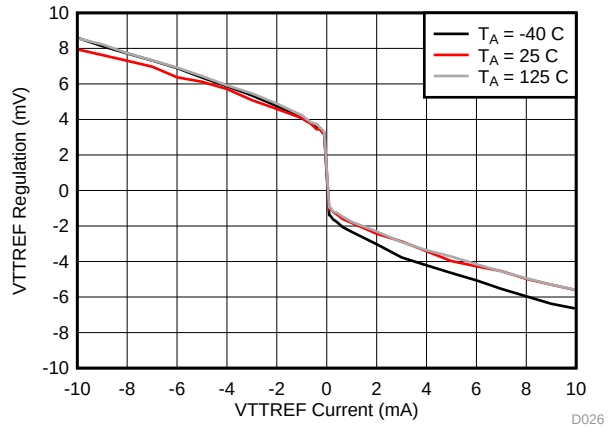


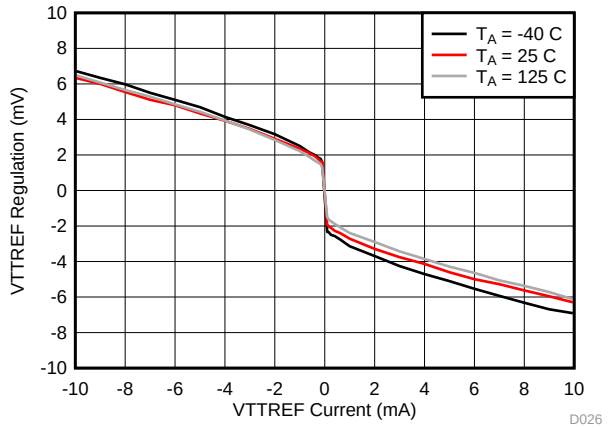
图 24. PGOOD Thresholds vs Temperature

Typical Characteristics (接下页)



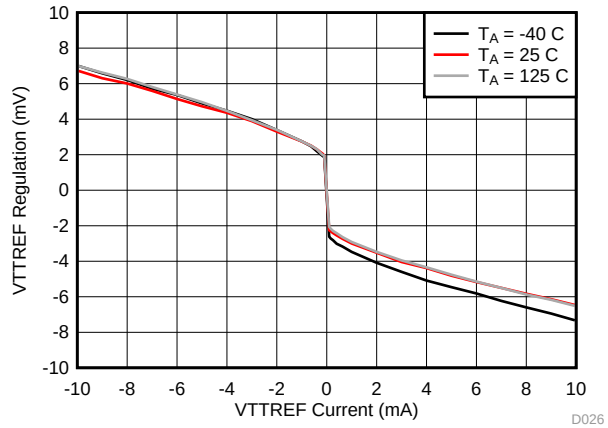
VDDQSNS = 1.8 V V_{IN} = 5 V

图 25. VTTREF Regulation to VDDQSNS/2 vs $I_{(VTTREF)}$



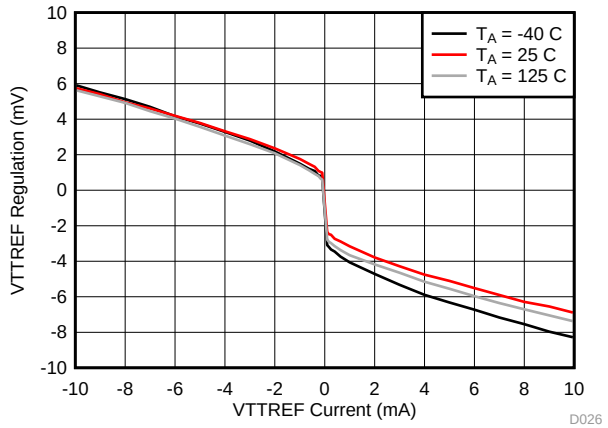
VDDQSNS = 1.5 V V_{IN} = 5 V

图 26. VTTREF Regulation to VDDQSNS/2 vs $I_{(VTTREF)}$



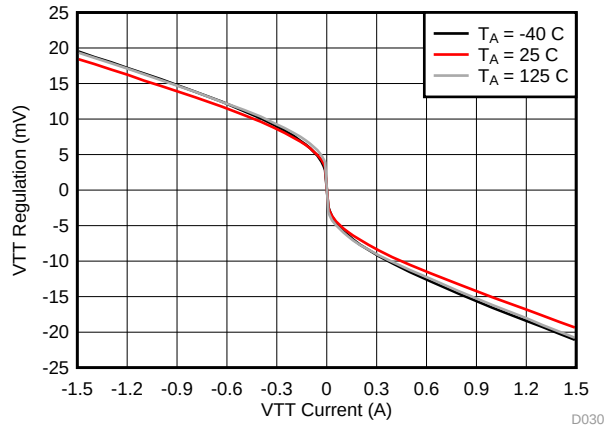
VDDQSNS = 1.35 V V_{IN} = 5 V

图 27. VTTREF Regulation to VDDQSNS/2 vs $I_{(VTTREF)}$



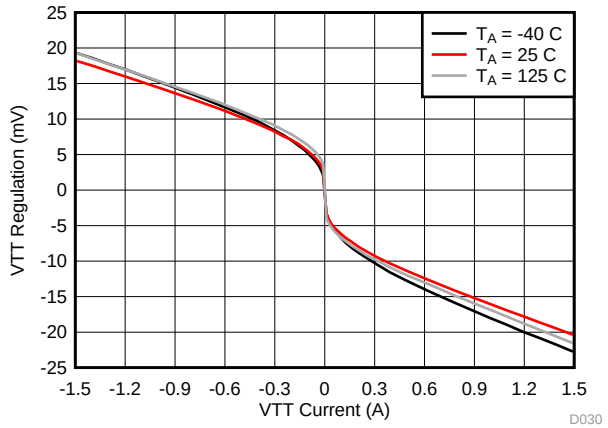
VDDQSNS = 1.2 V V_{IN} = 5 V

图 28. VTTREF Regulation to VDDQSNS/2 vs $I_{(VTTREF)}$



VDDQSNS = 1.8 V V_{IN} = 5 V

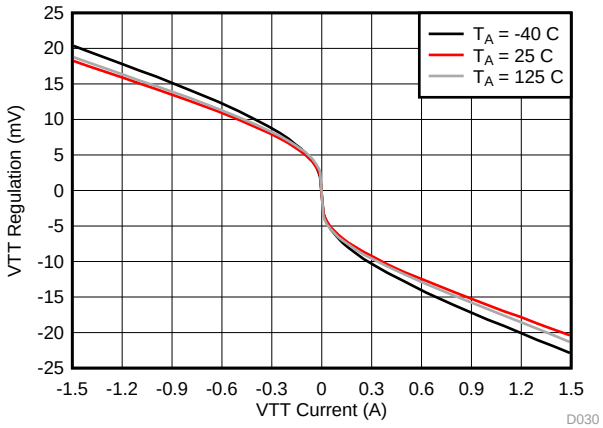
图 29. VTT Regulation to VTTREF vs $I_{(VTT)}$



VDDQSNS = 1.5 V V_{IN} = 5 V

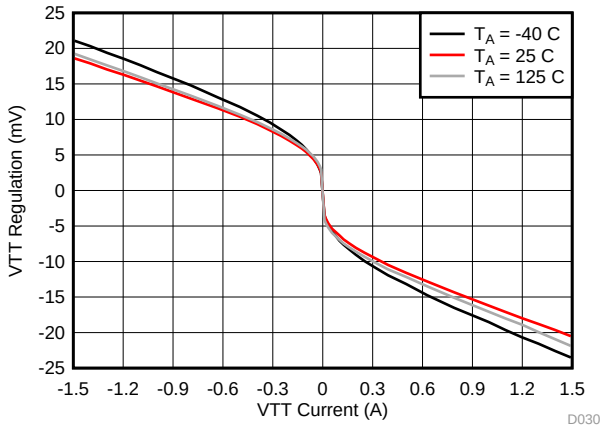
图 30. VTT Regulation to VTTREF vs $I_{(VTT)}$

Typical Characteristics (接下页)



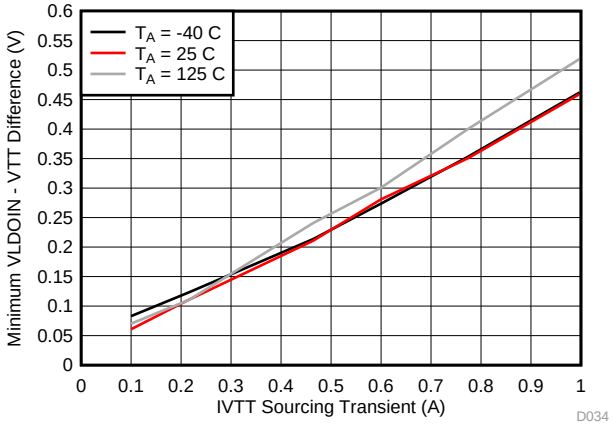
VDDQSNS = 1.35 V　　V_{IN} = 5 V

图 31. VTT Regulation to VTTREF vs $I_{(VTT)}$



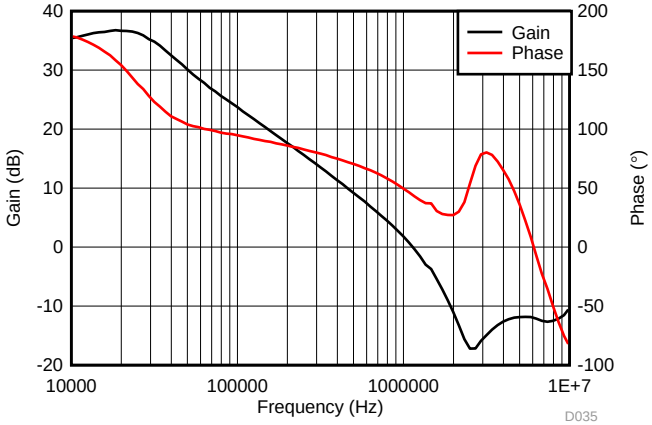
VDDQSNS = 1.2 V　　V_{IN} = 5 V

图 32. VTT Regulation to VTTREF vs $I_{(VTT)}$



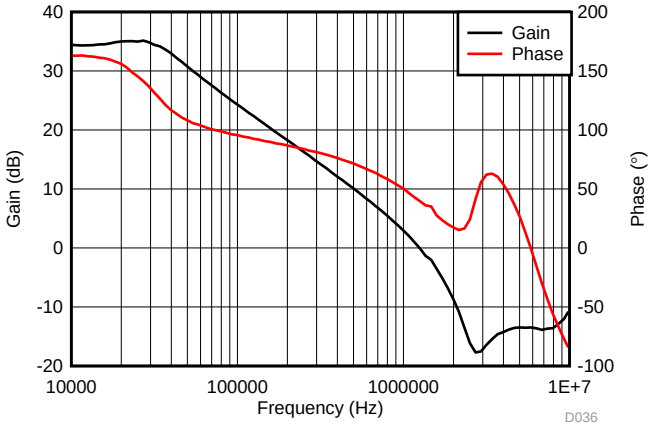
VDDQSNS = 1.5 V　　V_{IN} = 5 V

图 33. VTT Dropout



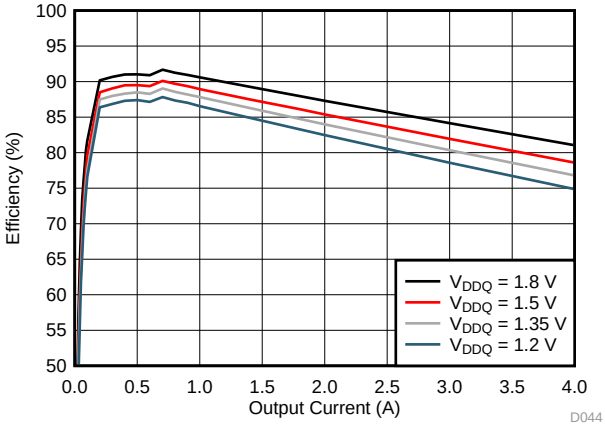
$V_{(VTT)}$ = 1.5 V　　V_{IN} = 5 V　　$I_{(VTT)}$ = +1 A
T_A = 25°C

图 34. VTT Sourcing Frequency Response



$V_{(VTT)}$ = 1.5 V　　V_{IN} = 5 V　　$I_{(VTT)}$ = –1 A
T_A = 25°C

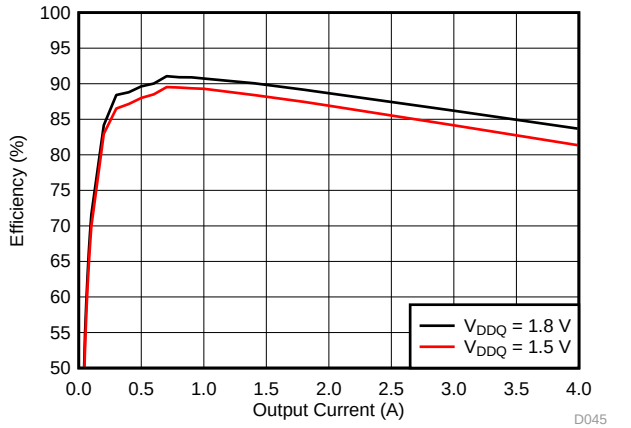
图 35. VTT Sinking Frequency Response



f_{SYNC} = 2.1 MHz　　V_{IN} = 3.3 V　　L = 744373240068
T_A = 25°C

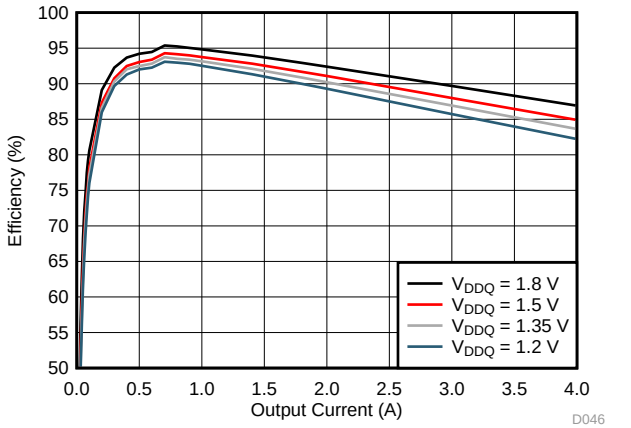
图 36. Efficiency

Typical Characteristics (接下页)



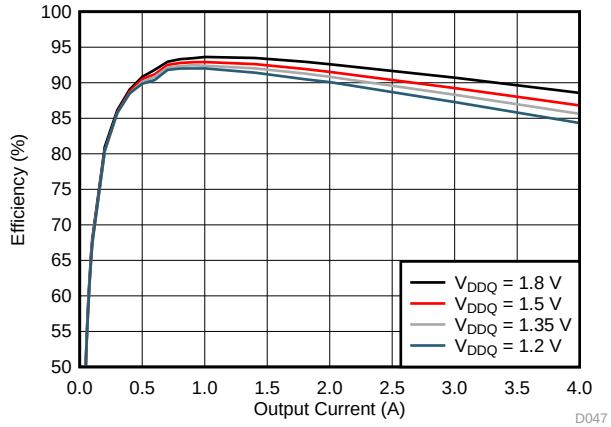
f_{SYNC} = 2.1 MHz V_{IN} = 5 V L = 744373240068
T_A = 25°C

图 37. Efficiency



f_{SYNC} = 400 kHz V_{IN} = 3.3 V L = 744310200
T_A = 25°C

图 38. Efficiency



f_{SYNC} = 400 kHz V_{IN} = 5 V L = 744310200
T_A = 25°C

图 39. Efficiency

7 Detailed Description

7.1 Overview

The TPS54116-Q1 is a 6-V, 4-A, synchronous step-down (buck) converter with two integrated N-channel MOSFETs and integrated 1-A sink/source double data rate (DDR) VTT termination regulator with a VTTREF buffed reference output.

To improve the performance during line and load transients the buck converter implements a constant frequency, peak current mode control which reduces output capacitance and simplifies external frequency compensation design. The wide switching frequency range of 100 kHz to 2500 kHz allows for efficiency and size optimization when selecting the output filter components. The switching frequency is adjusted using a resistor to ground on the RT/SYNC pin. The RT/SYNC pin can also be used to synchronize the power switch turn on to the rising edge of an external clock. The switching frequency can be set using an internal resistor by pulling the RT/SYNC below the low threshold or above the high threshold.

The TPS54116-Q1 has a typical default start-up voltage of 2.7 V. The ENSW pin can be used to enable the buck converter and the ENLDO pin can be used to enable VTT and VTTREF. The ENSW and ENLDO pins have internal pullup current sources that can be used to adjust the input voltage under voltage lockout (UVLO) with two external resistors. In addition, the pullup current provides a default condition when the ENSW or ENLDO pin is floating for the device to operate. The total operating current for the TPS54116-Q1 is typically 650 µA when not switching and under no load. When the device is disabled, the supply current is less than 3.5 µA.

The integrated 33-mΩ and 25-mΩ MOSFETs allow for high-efficiency power supply designs with continuous output currents up to 4 amperes. The TPS54116-Q1 reduces the external component count by integrating the boot recharge diode. The bias voltage for the integrated high-side MOSFET is supplied by a capacitor between the BOOT and SW pins. The boot capacitor voltage is monitored by an UVLO circuit and turns off the high-side MOSFET when the voltage falls below the BOOT-SW UVLO threshold. This BOOT circuit allows the TPS54116-Q1 to operate approaching 100% duty cycle. The output voltage can be stepped down to as low as the 0.60-V reference.

The TPS54116-Q1 features monotonic start-up under prebias conditions. The low-side FET turns on for a short time period every cycle before the output voltage reaches the prebiased voltage. This ensures the boot capacitor has enough charge to turn on the top FET when the output voltage reaches the prebiased voltage.

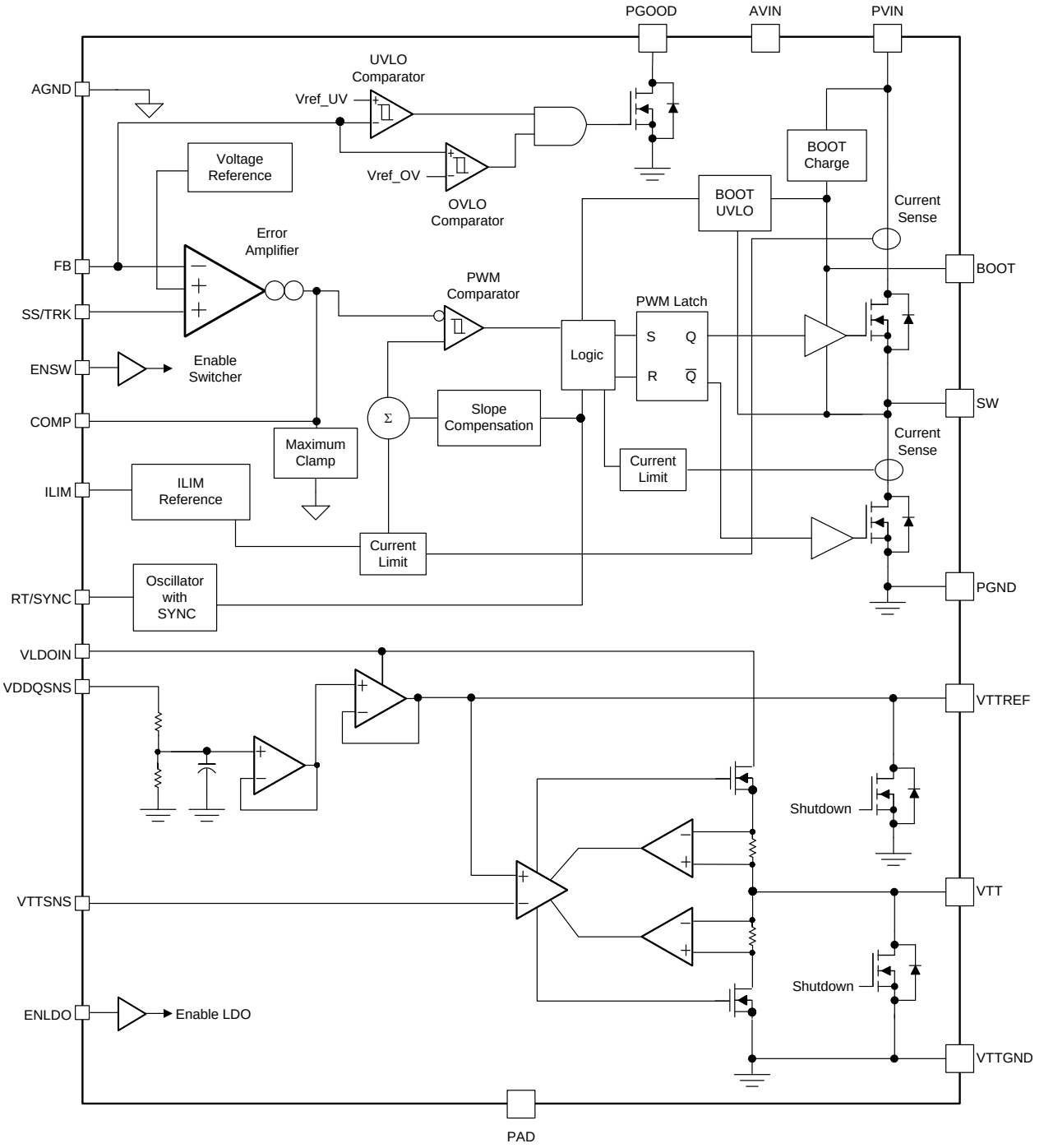
The TPS54116-Q1 has a power good comparator (PGOOD) with 3% hysteresis. Excessive output overvoltage transients are minimized by taking advantage of the overvoltage power good comparator. When the regulated output voltage (as sensed by the FB voltage) is greater than 109% of the nominal voltage, the overvoltage comparator is activated, and the high-side MOSFET is turned off and masked from turning on until the output voltage is lower than 106%.

The SS/TRK (soft-start or tracking) pin is used to minimize inrush currents or provide power supply sequencing during power up. A small value capacitor should be coupled to the pin for soft-start. The SS/TRK pin is discharged before the output power up to ensure a repeatable restart after an over temperature fault, UVLO fault or disabled condition. To optimize the output startup waveform, two levels of SS/TRK output current are implemented.

The TPS54116-Q1 limits the peak inductor current by sensing the current through the high-side MOSFET with cycle-by-cycle protection. The peak current limit is adjusted using a resistor to ground on the ILIM pin. The reverse current through the low-side MOSFET is also limited.

The 10-mA VTTREF buffered reference uses an internal resistor divider to regulate its output within 49% to 51% of VDDQSNS. The 1-A VTT termination regulates to VTTREF and maintains fast transient response with only 2 × 10-µF ceramic output capacitance. Remote sensing of VTT is used for best regulation. The VTT and VTTREF outputs are discharged when disabled with the AVIN UVLO or with ENLDO.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Fixed Frequency PWM Control

The TPS54116-Q1 uses an adjustable fixed frequency, peak current mode control. The output voltage is compared through external resistors on the FB pin to an internal voltage reference by an error amplifier which drives the COMP pin. An internal oscillator initiates the turn on of the high-side power switch. The error amplifier output is compared to the high-side power switch current. When the power switch current reaches the COMP signal level the high-side power switch is turned off and the low-side power switch is turned on. The COMP pin voltage will increase and decrease as the output current increases and decreases. The device implements a current limit by clamping the internal COMP signal.

An internal ramp is used to provide slope compensation to prevent sub-harmonic oscillations. The peak inductor current limit is constant over the full duty cycle range.

7.3.2 Bootstrap Voltage (BOOT) and Low Dropout Operation

The TPS54116-Q1 has an integrated boot regulator and requires a small ceramic capacitor between the BOOT and SW pins to provide the gate drive voltage for the high-side MOSFET. The value of the ceramic capacitor should be 0.1 µF. A ceramic capacitor with an X7R or X5R grade dielectric is recommended because of the stable characteristics over temperature and voltage.

To improve dropout, the TPS54116-Q1 is designed to operate at 100% duty cycle as long as the BOOT-SW voltage is greater than 2.2 V. The high-side MOSFET is turned off using an UVLO circuit, allowing for the low-side MOSFET to conduct, when the BOOT-SW voltage drops below 2.2 V. Because the supply current sourced from the BOOT pin is low, the high-side MOSFET can remain on for more switching cycles than are required to refresh the capacitor, thus the effective duty of the switching regulator is high.

7.3.3 Error Amplifier

The TPS54116-Q1 has a transconductance amplifier for the error amplifier. The error amplifier compares the FB voltage to the lower of the SS/TRK pin voltage or the internal 0.6-V voltage reference. The transconductance (gm_{EA}) of the error amplifier is 260 µA/V during normal operation. During soft-start, the gm_{EA} is reduced to 90 µA/V. The frequency compensation components are added to the COMP pin to ground.

When operating at current limit the COMP pin voltage is clamped to a maximum level to improve response when the load current decreases. When FB is greater than the internal voltage reference or SS/TRK the COMP pin voltage is clamped to a minimum level and the devices enters a high-side skip mode.

7.3.4 Voltage Reference and Adjusting the Output Voltage

The voltage reference system produces a precise ±1% voltage reference over temperature by scaling the output of a temperature stable bandgap circuit. The FB voltage is regulated to the voltage reference. The output voltage is set with a resistor divider from the output node to the FB pin. It is recommended to use divider resistors with 1% tolerance or better. Start with a 10.0 kΩ for the bottom resistor R_{FBB} and use the 公式 1 to calculate R_{FBT}. The maximum recommend resistance value for the bottom resistor is 100 kΩ.

$$R_{FBT} = R_{FBB} \times \left(\frac{V_{OUT}}{V_{REF}} - 1 \right) \quad (1)$$

Feature Description (接下页)

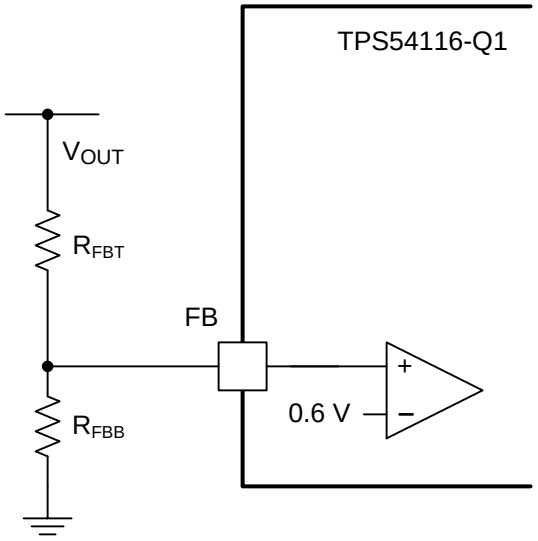


图 40. Voltage Divider Circuit

7.3.5 Enable and Adjusting Undervoltage Lockout

The TPS54116-Q1 is enabled when the AVIN pin voltage exceeds 2.7 V and is disabled when it falls below 2.65 V. If an application requires a higher under-voltage lockout (UVLO) or more hysteresis, use the ENSW or ENLDO pins as shown in 图 41 to adjust the input voltage UVLO by using two external resistors. The EN pin has an internal pull-up current source (I_p) of 1.7 µA that provides the default condition of the TPS54116-Q1 operating when the EN pin floats. Once the EN pin voltage exceeds 1.2 V, an additional 2.7 µA hysteresis current (I_h) is added. When the EN pin is pulled below 1.17 V, the 2.7 µA is removed. This additional current facilitates input voltage hysteresis. It is recommended to use the EN resistors to set the UVLO falling threshold (V_{STOP}) at 2.65V or higher. The rising threshold (V_{START}) should be set to provide enough hysteresis to allow for any input supply variations. 公式 2 can be used to calculate the top resistor in the EN divider and 公式 3 is used to calculate the bottom resistor.

The ENSW and ENLDO can also be tied in parallel. Calculations can be done the same but with the increased EN current of I_p = 3.4 µA and I_h = 5.1 µA.

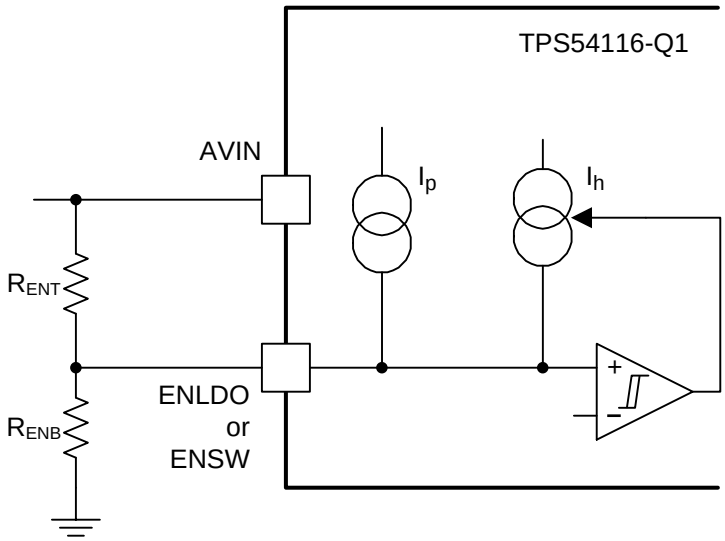


图 41. Adjustable Under Voltage Lock Out

Feature Description (接下页)

$$R_{ENT} = \frac{V_{START} \times \left(\frac{V_{ENFALLING}}{V_{ENRISING}} \right) - V_{STOP}}{I_p \times \left(1 - \frac{V_{ENFALLING}}{V_{ENRISING}} \right) + I_h} \quad (2)$$

$$R_{ENB} = \frac{R_{ENT} \times V_{ENFALLING}}{V_{STOP} - V_{ENFALLING} + R_{ENT} \times \left(I_p + I_h \right)} \quad (3)$$

Where:

- I_h = 2.7 µA
- I_p = 1.7 µA
- $V_{ENRISING}$ = 1.2 V
- $V_{ENFALLING}$ = 1.17 V

7.3.6 Soft Start and Tracking

The TPS54116-Q1 regulates to the lower of the SS/TRK pin and the internal reference voltage. A capacitor on the SS/TRK pin to ground implements a soft start time. Before the SS pin reaches the voltage threshold V_{SSTHR} of 0.15 V, the charge current is about 47 µA. The TPS54116-Q1 internal pull-up current source of 2.4 µA charges the external soft start capacitor after the SS pin voltage exceeds V_{SSTHR}. 公式 4 calculates the required soft start capacitor value where t_{SS} is the desired soft start time for the output voltage to reach 90% its final value in ms and C_{SS} is the required capacitance in nF.

$$C_{SS}\left(nF\right) = 5.3 \times t_{SS}\left(ms\right) \quad (4)$$

If during normal operation, AVIN goes below the UVLO, ENSW pin pulled below 1.17 V, or a thermal shutdown event occurs, the TPS54116-Q1 stops switching. When the AVIN goes above UVLO, ENSW is released or pulled high, or a thermal shutdown is exited, then SS/TRK is discharged to below 5 mV before reinitiating a powering up sequence. The FB voltage will follow the SS/TRK pin voltage with a 60 mV offset up to 90% of the internal voltage reference. When the SS/TRK voltage is greater than 90% of the internal reference voltage the offset increases as the effective system reference transitions from the SS/TRK voltage to the internal voltage reference.

When the COMP pin voltage is clamped by the maximum COMP clamp in an overload condition the soft-start pin is discharged to near the FB voltage. When the overload condition is removed, the soft-start circuit controls the recovery from the fault output level to the nominal regulation voltage. At the beginning of recovery a spike in the output voltage may occur as the COMP voltage transitions to the value determined by the loop.

7.3.7 Start-up into Pre-Biased Output

The TPS54116-Q1 features monotonic startup into pre-biased output. The low-side MOSFET turns on for a very short time period every cycle before the output voltage reaches the pre-biased voltage. This ensures the BOOT-SW cap has enough charge to turn on the high-side MOSFET when the output voltage reaches the pre-biased voltage. The low-side MOSFET reverse current protection provides another layer of protection but it should not be reached due to the implemented prebias function.

7.3.8 Power Good

The PGOOD pin is an open-drain output requiring an external pullup resistor to output a high signal. Once the FB pin is between 94% and 106% of the internal voltage reference, the PGOOD pin is de-asserted and the pin floats. A pull up resistor between the values of 10 kΩ and 100 kΩ to a voltage source that is 6 V or less is recommended. The PGOOD is in a defined state once the AVIN input voltage is greater than 1.3 V but with reduced current sinking capability.

The PGOOD pin is pulled low when the FB is lower than 91% or greater than 109% of the nominal internal reference voltage. The PGOOD is also pulled low if AVIN falls below its UVLO, ENSW pin is pulled low or the TPS54116-Q1 enters thermal shutdown.

Feature Description (接下页)

7.3.9 Sequencing

Many of the common power supply sequencing methods can be implemented using the SS/TRK, ENSW and PGOOD pins. The sequential method can be implemented using an open-drain or collector output of a power on reset pin of another device. An example sequential method is shown in 图 42. PGOOD is connected to the EN pin on the next power supply, which will enable the second power supply once the first supply reaches regulation.

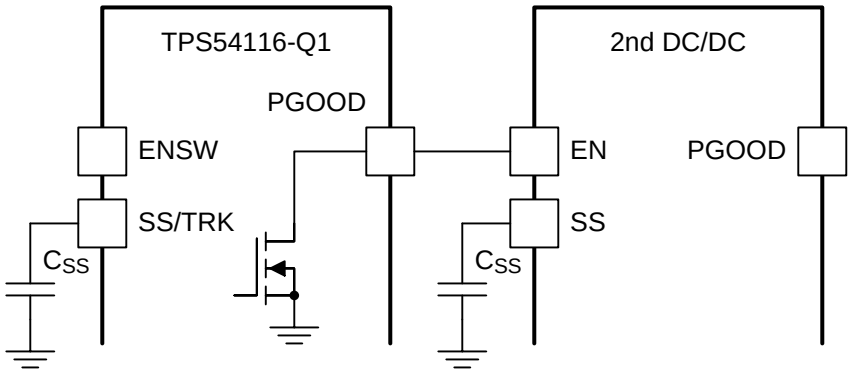


图 42. Sequential Startup Example

7.3.10 Constant Switching Frequency and Timing Resistor (RT/SYNC)

The switching frequency of the TPS54116-Q1 is adjustable over a wide range from 100 kHz to 2500 kHz by placing a maximum of 620 kΩ and minimum of 22 kΩ, respectively, on the RT/SYNC pin. Alternatively the RT/SYNC pin can be tied above the high threshold or below the low threshold to use an internal RT resistor to set the switching frequency to 420 kHz. The RT/SYNC is typically 0.5 V and the current through the resistor sets the switching frequency. To determine the timing resistance for a given switching frequency, refer to the curve in 图 16 and 图 17 or use 公式 5. For a given RT resistor the nominal switching frequency can be calculated with 公式 6. To reduce the solution size one would typically set the switching frequency as high as possible, but tradeoffs of the supply efficiency, maximum input voltage and minimum controllable on time should be considered. The minimum controllable on time is typically 60 ns at 2-A load current and 100 ns at no load, and will limit the maximum operating input voltage or minimum output voltage.

$$R_T\left(k\Omega\right) = \frac{72540}{f_{SW}\left(kHz\right)^{1.033}} \tag{5}$$

$$f_{SW}\left(kHz\right) = \frac{50740}{R_T\left(k\Omega\right)^{0.968}} \tag{6}$$

The RT/SYNC pin can also be used to synchronize the converter to an external system clock. When using the internal RT resistor, the TPS54116-Q1 cannot be synchronized to an external clock. The synchronization frequency range is 100 kHz to 2500 kHz. The rising edge of SW will be synchronized to the rising edge of RT/SYNC. To implement the synchronization feature in a system connect a square wave to the RT/SYNC pin with on-time at least 10 ns. The square wave amplitude at this pin must transition lower than 0.35 V and higher than 2.2 V.

See 图 43 for synchronizing to a high impedance system clock. See 图 44 and 图 45 for synchronizing to a low impedance system clock. A tri-state buffer with its output directly connected to the RT/SYNC pin is the recommended method to accomodate a wide range of external clock frequencies and duty cycles. Alternatively an AC blocking capacitor circuit can be used when synchronizing to frequencies greater than 800 kHz and with clock signals with duty cycle near 50%. When using an AC coupling capacitor to interface with an external clock, RT/SYNC is not actively pulled low by the external clock. As a result the TPS54116-Q1 begins its transition back to RT mode while the external clock is low. When connecting the RT/SYNC pin to the external clock source, it is important to minimize routing connected to the RT/SYNC pin as much as possible to minimize noise sensitivity when operating in RT mode.

Feature Description (接下页)

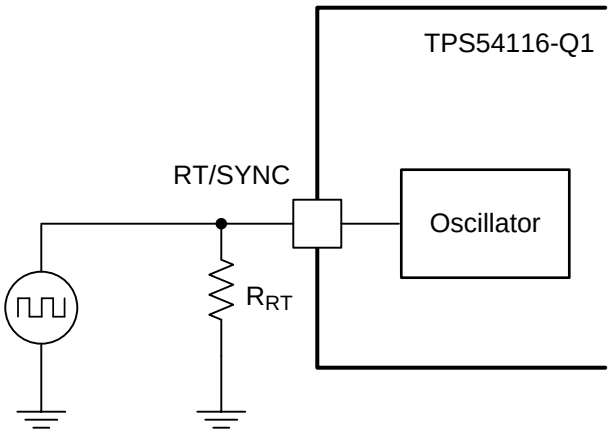


图 43. Synchronizing to a High Impedance System Clock

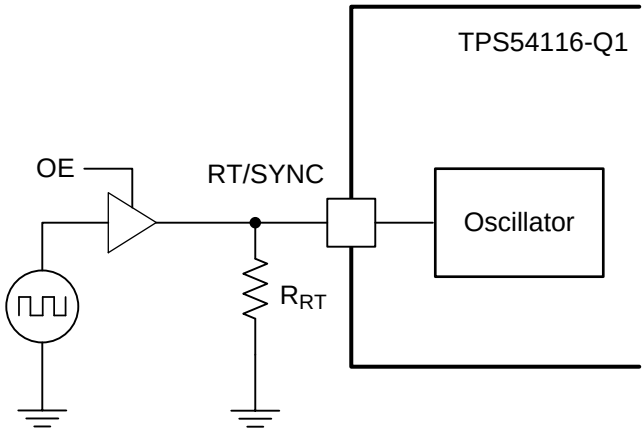


图 44. Interfacing to the RT/SYNC Pin with Buffer

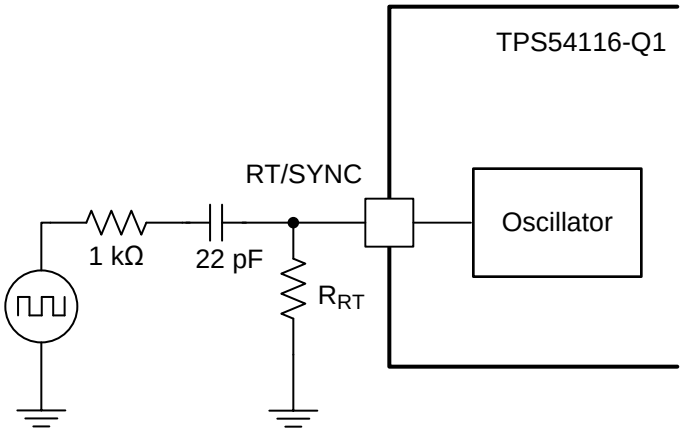


图 45. Interfacing to the RT/SYNC Pin with RC

Feature Description (接下页)

7.3.11 Buck Overcurrent Protection

The TPS54116-Q1 implements current mode control which uses the COMP pin voltage to turn off the high-side MOSFET and turn on the low-side MOSFET on a cycle-by-cycle basis. Each cycle the switch current and the COMP pin voltage are compared, when the peak switch current intersects the COMP voltage the high-side switch is turned off. During overcurrent conditions that pull the output voltage low, the error amplifier will respond by driving the COMP pin high, increasing the switch current. The error amplifier output is clamped internally. This clamp functions as a high-side switch current limit.

A resistor placed from ILIM to AGND sets the peak current limit of the buck converter in the TPS54116-Q1. A 100 kΩ resistor sets it to the maximum value and a 200 kΩ resistor sets it to the minimum value. Any resistor within this range can be used. 图 12 shows the relationship between peak current limit and ILIM resistor. To determine the resistor value for a target current limit use 公式 7.

$$R_{ILIM} = 420 \times I_{limit}^{-0.75} \quad (7)$$

The TPS54116-Q1 also implements low-side current protection by detecting the voltage over the low-side MOSFET. When the converter sinks current through the low-side MOSFET is more than 4.5 A, the control circuit will turn the low-side MOSFET off immediately for the rest of the clock cycle. Under this condition, both the high-side and low-side are off until the start of the next cycle.

7.3.12 Overvoltage Transient Protection

The TPS54116-Q1 incorporates an overvoltage transient protection (OVTP) circuit to minimize voltage overshoot when recovering from output fault conditions or strong unload transients. The OVTP feature minimizes the output overshoot by implementing a circuit to compare the FB pin voltage to OVTP threshold which is 109% of the internal voltage reference. If the FB pin voltage is greater than the OVTP threshold, the high-side MOSFET is disabled preventing current from flowing to the output and minimizing output overshoot. The output voltage can overshoot the 109% threshold as the current in the inductor discharges to 0 A. When the FB voltage drops lower than the OVTP threshold the high-side MOSFET is allowed to turn on the next clock cycle.

7.3.13 VTT Sink and Source Regulator

The TPS54116-Q1 integrates a high-performance, low-dropout (LDO) linear regulator (VTT) that has ultimate fast response to track ½ VDDQSNS within 40 mV at all conditions, and its current capability is 1.5 A peak current for both sink and source directions. Two 10-µF (or greater) ceramic capacitor(s) need to be attached close to the VTT pin for stable operation. X5R grade or better is recommended. To achieve tight regulation with minimum effect of trace resistance, the remote sensing terminal, VTTSNS, should be connected to the positive terminal of the output capacitor(s) as a separate trace from the high current path from the VTT pin.

The device has a dedicated pin, VLDOIN, for VTT power supply to minimize the LDO power dissipation on user application. The minimum VLDOIN voltage is 0.45 V above the ½ VDDQSNS voltage.

7.3.14 VTTREF

The VTTREF pin has a 10 mA sink and source current capability, and regulates to within 49% to 51% of VDDQSNS. A 0.22-µF ceramic capacitor needs to be attached close to the VTTREF terminal for stable operation. X5R grade or better is recommended.

7.3.15 Thermal Shutdown

The device implements an internal thermal shutdown to protect itself if the junction temperature exceeds 175°C. The thermal shutdown has a hysteresis of 16°C. When the junction temperature exceeds thermal trip threshold, thermal shutdown forces the device to stop switching and discharges both VTT and VTTREF. When the die temperature decreases below 159°C, the device reinitiates the power-up sequence by discharging the SS/TRK pin.

7.4 Device Functional Modes

The enable pins and an AVIN UVLO are used to control turn on and turn off of the TPS54116-Q1. The device becomes active when $V_{(AVIN)}$ exceeds the 2.7 V typical UVLO and when either $V_{(ENSW)}$ or $V_{(ENLDO)}$ exceeds 1.20 V typical. The ENSW pin is used to control the turn on and turn off of the buck converter. The ENLDO pin is used to control the turn on and turn off of the VTTREF and VTT outputs of the termination regulator. The ENSW and ENLDO pins both have an internal current source to enable their respective outputs when left floating. Both ENSW and ENLDO need to be pulled low to put the device into a low quiescent current state.

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS54116-Q1 is a fully integrated power solution for DDR2, DDR3 and DDR3L memory supplying VDDQ, VTTREF and VTT as shown in 图 46. It can also be used to power LPDDR2, LPDDR3 and DDR4 memory but an additional power supply is required for VDD1 or VPP as shown in 图 47. The TPS54116-Q1 can supply 4 A for VDDQ and 1 A for VTT. The sourcing current for VTT comes from VDDQ and must be included as part of the total VDDQ load current. Use the following design procedure to select component values for the TPS54116-Q1. This procedure illustrates the design of a high-frequency switching regulator using ceramic output capacitors. Alternatively the WEBENCH® software can be used to generate a complete design. The WEBENCH® software uses an interactive design procedure and accesses a comprehensive database of components when generating a design. This section presents a simplified discussion of the design process.

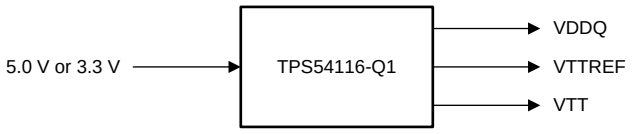


图 46. DDR2, DDR3 and DDR3L Application Block Diagram

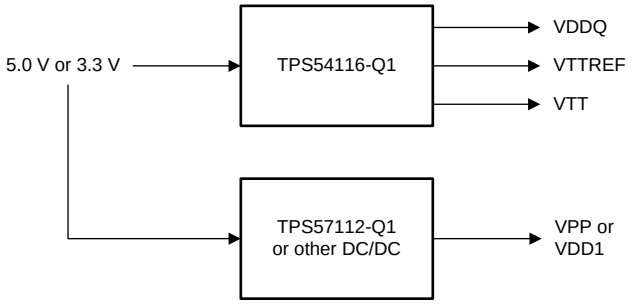


图 47. LPDDR2, LPDDR3 and DDR4 Application Block Diagram

8.2 Typical Application

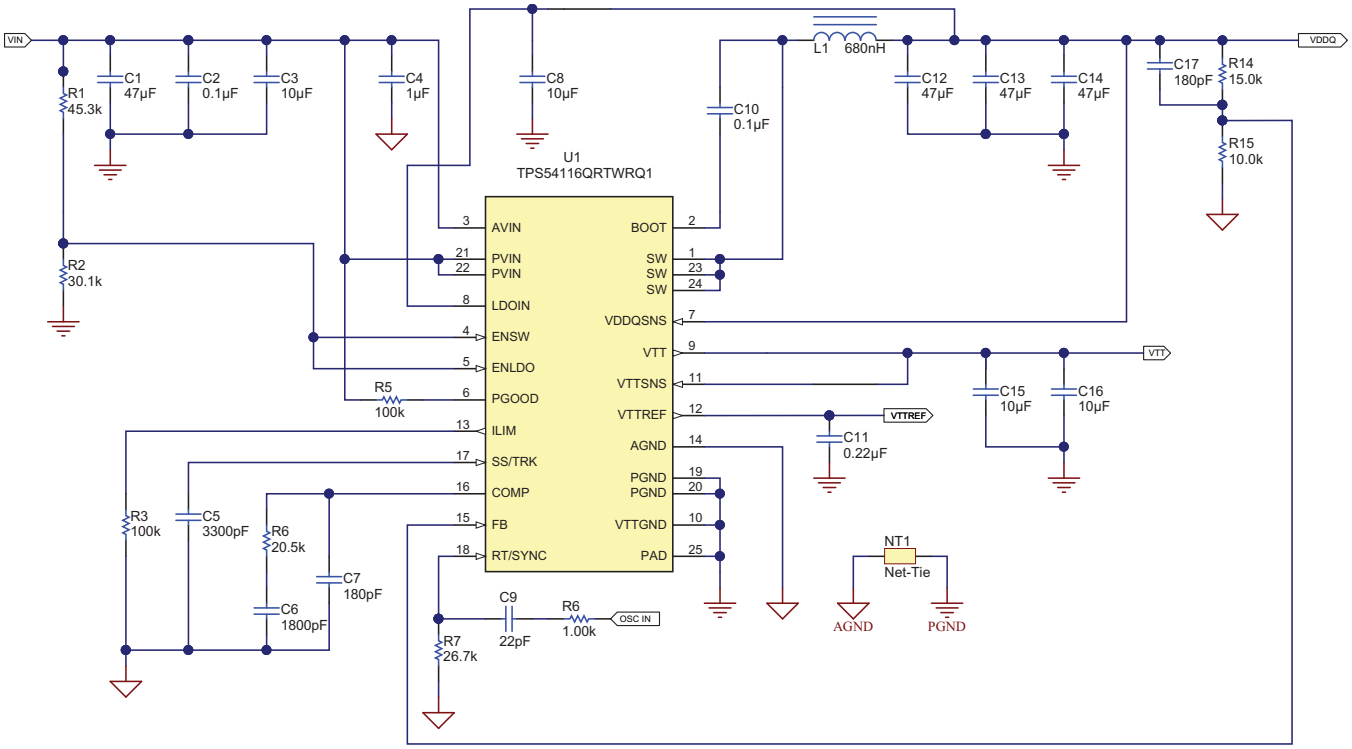


图 48. 3.3-V or 5-V Input, 2.1 MHz fsw, DDR3 Schematic

8.2.1 Design Requirements

表 1. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUES
Input Voltage	5 V nominal, 2.95 V to 5.25 V
Output Voltage	1.5 V
Maximum Output Current (VDDQ)	4 A
Maximum Output Current (VTT)	1 A
Output Voltage Ripple (VDDQ)	0.5% of V_{OUT}
Transient Response 1 A to 3 A load step	ΔV_{OUT} = 4 %
Start Input Voltage (rising VIN)	2.9 V
Stop Input Voltage (falling VIN)	2.6 V

8.2.2 Detailed Design Procedure

8.2.2.1 Switching Frequency

The first step is to decide on a switching frequency for the regulator. The buck converter is capable of running from 100 kHz to 2.5 MHz. Typically the highest switching frequency possible is desired because it will produce the smallest solution size. A high switching frequency allows for lower valued inductors and smaller output capacitors compared to a power supply that switches at a lower frequency. Additionally in applications with EMI requirements, such as automotive, choosing a switching frequency of 2.1 MHz is desired to keep the switching noise above the medium wave band or AM band. They main trade off made with selecting a higher switching frequency is extra switching power loss, which hurt the converter's efficiency.

The maximum switching frequency for a given application is limited by the minimum on-time of the converter and is estimated with 公式 8. For this application with the maximum minimum on-time of 125 ns at no load and 5.25 V maximum input voltage the maximum switching frequency is 2.28 MHz. A switching frequency of 2.1 MHz is selected to stay above the AM band. 公式 9 calculates R14 to be 26.8 kΩ. A standard 1% 26.7 kΩ value was chosen in the design.

$$f_{SW}(max) = \frac{1}{tonmin} \times \frac{V_{OUT}}{V_{IN}(max)} \quad (8)$$

$$R_T(k\Omega) = \frac{72540}{f_{SW}(kHz)^{1.033}} \quad (9)$$

8.2.2.2 Output Inductor Selection

To calculate the value of the output inductor, use 公式 10. K_{IND} is a ratio that represents the amount of inductor ripple current relative to the maximum output current. The inductor ripple current is filtered by the output capacitor. Therefore, choosing high inductor ripple currents impacts the selection of the output capacitor since the output capacitor must have a ripple current rating equal to or greater than the inductor ripple current. Additionally the inductor current ripple is used as part of the PWM control system. Choosing small inductor ripple currents can degrade the transient response performance or introduce jitter in the duty cycle. In general, the inductor ripple value is at the discretion of the designer; however, K_{IND} is normally from 0.1 to 0.3 for the majority of applications giving a peak to peak ripple current range of 0.4 A to 1.2 A. It is recommended to always keep the peak to peak ripple current above 0.4 A because with a current mode control the inductor current ramp is used in the PWM control system.

For this design example, K_{IND} = 0.3 is used and the inductor value is calculated to be 0.43 µH. The next standard value 0.68 µH is selected. It is important that the RMS current and saturation current ratings of the inductor not be exceeded. The RMS and peak inductor current can be found from 公式 12 and 公式 13. For this design, the RMS inductor current is 4.0 A and the peak inductor current is 4.4 A. The chosen inductor is a WE 744373240068. It has a saturation current rating of 10.0 A (20% inductance loss) and a RMS current rating of 5.5 A (40 °C. temperature rise). The series resistance is 16.0 mΩ typical.

The current flowing through the inductor is the inductor ripple current plus the output current. During power up, faults or transient load conditions, the inductor current can increase above the calculated peak inductor current level calculated above. In transient conditions, the inductor current can increase up to the switch current limit of the device. For this reason, the most conservative approach is to specify an inductor with a saturation current rating equal to or greater than the switch current limit rather than the steady-state peak inductor current. Additionally if a hard short on the output occurs in a fault condition the peak inductor current can exceed the current limit and may reach up to 10 A. The peak current limit in this scenario is only limited by the minimum on-time of the TPS54116-Q1 and the parasitic DC voltage drops in the circuit. The peak current during a hard short will vary with the switching frequency and only exceeds the current limit when using the TPS54116-Q1 with higher switching frequencies like 2.1 MHz. To protect the inductor in a hard output short the inductor should be rated for this current.

$$L1 = \frac{Vinmax - Vout}{Io \times Kind} \times \frac{Vout}{Vinmax \times fsw} \quad (10)$$

$$Iripple = \frac{Vinmax - Vout}{L1} \times \frac{Vout}{Vinmax \times fsw} \quad (11)$$

$$ILrms = \sqrt{Io^2 + \frac{1}{12} \times \left(\frac{Vo \times (Vinmax - Vo)}{Vinmax \times L1 \times fsw}\right)^2} \quad (12)$$

$$ILpeak = Iout + \frac{Iripple}{2} \quad (13)$$

8.2.2.3 Output Capacitor

There are three primary considerations for selecting the value of the output capacitor. The output capacitor determines the modulator pole, the output voltage ripple, and how the regulator responds to a large change in load current. The output capacitance needs to be selected based on the more stringent of these three criteria.

The desired response to a large change in the load current is the first criteria and is often the most stringent. The output capacitor needs to supply the increased load current until the regulator responds to the load step. The regulator does not respond immediately to a large, fast increase in the load current such as transitioning from no load to a full load. The regulator usually needs two or more clock cycles for the control loop to sense the change in output voltage and adjust the peak switch current in response to the higher load. The output capacitance must be large enough to supply the difference in current for 2 clock cycles to maintain the output voltage within the specified range. At higher switching frequencies the fastest response time is about 4 µs. 公式 14 shows the minimum output capacitance necessary, where ΔI_{OUT} is the change in output current, tresponse is the regulators response time and ΔV_{OUT} is the allowable change in the output voltage. The minimum of 2/fsw or 4 µs should be used for the response time in the output capacitance calculation. It is important to realize the response to a transient load also depends on the loop compensation and slew rate of the transient load. This calculation assumes the loop compensation is designed for the output filter with the equations later on in this procedure.

For this example, the transient load response is specified as a 4% change in VOUT for a load step of 2 A. Therefore, ΔI_{OUT} is 2 A and ΔV_{OUT} = 0.04 × 1.5 = 60 mV. Using these numbers with a 4 µs response time gives a minimum capacitance of 133 µF. This value does not take the ESR of the output capacitor into account in the output voltage change. For ceramic capacitors, the ESR is usually small enough to be ignored. Aluminum electrolytic and tantalum capacitors have higher ESR that must be considered for load step response.

公式 15 calculates the minimum output capacitance needed to meet the output voltage ripple specification. Where fsw is the switching frequency, Vripple is the maximum allowable output voltage ripple, and Iripple is the inductor ripple current. In this case, the maximum output voltage ripple is 7.5 mV. Under this requirement, 公式 15 yields 6.3 µF.

$$Co > t_{response} \times \frac{\Delta Iout}{\Delta Vout} \tag{14}$$

$$Co > \frac{1}{8 \times fsw} \times \frac{1}{\frac{Voripple}{Iripple}} \tag{15}$$

Where:

- ΔI_{OUT} is the change in output current
- *f*sw is the regulators switching frequency
- ΔV_{OUT} is the allowable change in the output voltage

公式 16 calculates the maximum combined ESR the output capacitors can have to meet the output voltage ripple specification and this shows the ESR should be less than 10 mΩ. In this case ceramic capacitors will be used and the combined ESR of the ceramic capacitors in parallel is much less than 10 mΩ. Capacitors also generally have limits to the amount of ripple current they can handle without failing or producing excess heat. An output capacitor that can support the inductor ripple current must be specified. Some capacitor data sheets specify the RMS (Root Mean Square) value of the maximum ripple current. 公式 17 can be used to calculate the RMS ripple current the output capacitor needs to support. For this application, 公式 17 yields 220 mA. Ceramic capacitors used in this design will have a ripple current rating much higher than 220 mA.

$$Resr < \frac{Voripple}{Iripple} \tag{16}$$

$$Icorms = \frac{Vout \times (Vinmax - Vout)}{\sqrt{12} \times Vinmax \times L1 \times fsw} \tag{17}$$

The value of a ceramic capacitor varies significantly over temperature and the amount of DC bias applied to the capacitor. The capacitance variations due to temperature can be minimized by selecting a dielectric material that is stable over temperature. X5R and X7R ceramic dielectrics are usually selected for power regulator capacitors because they have a high capacitance to volume ratio and are fairly stable over temperature. The output capacitor must also be selected with the DC bias taken into account. The capacitance value of a capacitor decreases as the DC bias across a capacitor increases. For this application example, three 47 µF 10 V 1210 X7R ceramic capacitors each with 8 mΩ of ESR at the fsw are used. The estimated capacitance after derating shown on the capcaitor manufacturer's website with 1.5 V DC bias is 51.4 µF each. With 3 parallel capacitors the total output capacitance is 154 µF and the ESR is 2.7 mΩ.

8.2.2.4 Input Capacitor

The TPS54116-Q1 requires a high quality ceramic, type X5R or X7R, input decoupling capacitor of at least 10 µF of effective capacitance placed across the PVIN and PGND pins and in some applications a bulk capacitance. The effective capacitance includes any DC bias effects. The voltage rating of the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple current rating greater than the maximum RMS input current of the TPS54116-Q1. The RMS input current can be calculated using 公式 18. An input decoupling capacitor of 1 µF must also be placed at the AVIN pin to ensure a stable input voltage to the internal control circuits.

For this example design, a ceramic capacitor with at least a 10 V voltage rating is required to support the maximum input voltage. For this example, one 47 µF 1210 X7R, one 10 µF 0603 X7R and one 0.1 µF 0603 X7R 10 V capacitors in parallel have been selected for the PVIN to PGND pins. Additionally one 1 µF 0603 X5R 10 V capacitor is selected for the AVIN pin. The 0.1 µF at the PVIN pin is used to better bypass the higher frequency content when the high-side MOSFET switches on and off. Based on the capacitor manufacturer's website, the total input capacitance derates to 34 µF at the nominal input voltage of 5 V. The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using 公式 19. Using the design example values, Ioutmax = 4 A, Cin = 34 µF, f_{SW} = 2.1 MHz, yields an input voltage ripple of 14 mV and a rms input ripple current of 1.9 A.

$$\text{Icirms} = \text{Iout} \times \sqrt{\frac{\text{Vout}}{\text{Vinmin}} \times \frac{(\text{Vinmin} - \text{Vout})}{\text{Vinmin}}} \tag{18}$$

$$\Delta\text{Vin} = \frac{\text{Ioutmax} \times 0.25}{\text{Cin} \times f\text{sw}} \tag{19}$$

8.2.2.5 Soft Start Capacitor

The soft-start capacitor determines the minimum amount of time it takes for the output voltage to reach its nominal programmed value during power up. This is useful if a load requires a controlled voltage slew rate. This is also used if the output capacitance is very large and would require large amounts of current to quickly charge the capacitor to the output voltage level. The large currents necessary to charge the capacitor may make the TPS54116-Q1 reach the current limit or excessive current draw from the input power supply may cause the input voltage rail to sag. Limiting the output voltage slew rate solves both of these problems.

The soft-start capacitor value can be calculated using 公式 20. For the example circuit, the soft-start time is not too critical since the output capacitor value of 3 x 47 µF does not require much current to charge to 1.5 V. With the higher switching frequency used in this example a faster start-up time improves the start up behavior. Near the beginning of the start up time when the output voltage is low the minimum on-time of the converter is too large to regulate the output causing additional ripple on the output. A faster start-up time will reduce the time the converter spends in this region. The example circuit is designed for a soft-start time of 0.6 ms which requires a 3300 pF capacitor.

$$C_{SS}(\text{nF}) = 5.3 \times t_{SS}(\text{ms}) \tag{20}$$

8.2.2.6 Undervoltage Lock Out Set Point

The Undervoltage Lock Out (UVLO) can be adjusted using an external voltage divider on the ENSW and ENLDO pin of the TPS54116. Each pin can have its own resistor divider if different thresholds are needed for the VTT LDO and the buck converter. If only one threshold is needed only one resistor divider is needed and the pins can be connected in parallel. If connected in parallel the pull up current and hysteresis current should be increased to 3.4 µA and 5.1 µA respectively as shown in the electrical specifications. The UVLO has two thresholds, one for power-up when the input voltage is rising, and one for power-down or brown outs when the input voltage is falling.

For the example design, the supply should turn on and start switching once the input voltage increases above 2.9 V (enabled). After the regulator starts switching, it should continue to do so until the input voltage falls below 2.6 V (UVLO stop). The EN pins are also connected in parallel so the higher pull up current and hysteresis current is used. 公式 2 through 公式 3 can be used to calculate the resistance values necessary. A 45.3 kΩ between PVIN and the EN pins (R1) and a 30.1 kΩ between the EN pins and ground (R2) are used producing a start voltage of 2.85 V and stop voltage of 2.47 V. The 2.47 V stop voltage is below the 2.65 V AVIN UVLO so with this application example the TPS54116-Q1 will turn off due to the AVIN UVLO.

8.2.2.7 Bootstrap Capacitor

A 0.1 µF ceramic capacitor must be connected between the BOOT and SW pins for proper operation. It is recommended to use a ceramic capacitor with X5R or better grade dielectric. The capacitor should have 10 V or higher voltage rating.

8.2.2.8 Power Good Pullup

A 100 kΩ resistor is used to pull up the power good signal to VIN when FB conditions are met.

8.2.2.9 ILIM Resistor

The recommended peak current limit is calculated with 公式 21 using ILpeak from 公式 13. This calculation includes 10% margin for load transients and an additional 1.5 A for the tolerance of the peak current limit. In this application a 100 kΩ resistor is placed from ILIM to AGND to set the peak current limit to its maximum value. For applications requiring a different peak current limit 公式 7 is used to calculate the ILIM resistor.

$$I_{limit} = ILpeak \times 1.1 + 1.5A \tag{21}$$

8.2.2.10 Output Voltage and Feedback Resistors Selection

For the example design, 10.0 kΩ was selected for R7. Using 公式 22, R5 is calculated as 15.0 kΩ which is a standard 1% resistor.

$$R_{FBT} = R_{FBB} \times \left(\frac{V_{OUT}}{V_{REF}} - 1 \right) \tag{22}$$

8.2.2.11 Compensation

There are several methods used to compensate DC - DC regulators. The method presented here is easy to calculate and ignores the effects of the slope compensation that is internal to the device. Because the slope compensation is ignored, the actual cross-over frequency will usually be lower than the cross-over frequency used in the calculations. This method assumes the cross-over frequency is between the modulator pole and the ESR zero and the ESR zero is at least 10 times greater the modulator pole. This is the case when using low ESR output capacitors. Use the WEBENCH software for more accurate loop compensation. These tools include a more comprehensive model of the control loop.

To get started, the modulator pole, fpmod, and the ESR zero, fz1 must be calculated using 公式 23 and 公式 24. For Cout, use a derated value of 154 µF. Use equations 公式 25 and 公式 26, to estimate a starting point for the crossover frequency, fco, to design the compensation. For the example design, fpmod is 2.8 kHz and fzmod is 388 kHz. 公式 25 is the geometric mean of the modulator pole and the esr zero and 公式 26 is the mean of modulator pole and one half the switching frequency or 250 kHz, whichever is larger. For the 2.1 MHz switching frequency application 250 kHz is used so 公式 25 yields 33 kHz and 公式 26 gives 52 kHz. Use the lower value of 公式 25 or 公式 26 for an initial crossover frequency. Next, the compensation components are calculated. A resistor-in-series with a capacitor is used to create a compensating zero. A capacitor in parallel to these two components forms the compensating pole.

$$fp\ mod = \frac{Ioutmax}{2 \times \pi \times Vout \times Cout} \quad (23)$$

$$fz\ mod = \frac{1}{2 \times \pi \times Resr \times Cout} \quad (24)$$

$$f_{co} = \sqrt{f_p mod \times f_z mod} \quad (25)$$

$$f_{co} = \sqrt{f_p mod \times \frac{f_{sw}}{2}} \quad (26)$$

To determine the compensation resistor, R6, use 公式 27. Assume the power stage transconductance, gmps, is 16 A/V. The output voltage, Vo, reference voltage, VREF, and amplifier transconductance, gmea, are 1.5 V, 0.6 V and 260 µA/V, respectively. R6 is calculated to be 19 kΩ and the closest standard value 19.1 kΩ. Use 公式 28 to set the compensation zero to the modulator pole frequency. 公式 28 yields 3020 pF for compensating capacitor C6 and the closest standard value is 3300 pF.

$$R_{COMP} = \left(\frac{2 \times \pi \times f_{CO} \times C_{OUT}}{gm_{PS}} \right) \times \left(\frac{V_{OUT}}{V_{REF} \times gm_{EA}} \right) \quad (27)$$

$$C_{COMP} = \frac{1}{2 \times \pi \times R_{COMP} \times f_{PMOD}} \quad (28)$$

A compensation pole is implemented using an additional capacitor C7 in parallel with the series combination of R6 and C6. This capacitor is recommended to help filter any noise that may couple to the COMP voltage signal. Use the larger value of 公式 29 and 公式 30 to calculate the C7, to set the compensation pole. C7 is calculated to 21 pF or 8 pF and the closest standard value is 22 pF.

$$C_{HF} = \frac{C_{OUT} \times R_{ESR}}{R_{COMP}} \quad (29)$$

$$C_{HF} = \frac{1}{\pi \times R_{COMP} \times f_{SW}} \quad (30)$$

Type III compensation is used by adding the feed forward capacitor (C17) in parallel with the upper feedback resistor. This increases the crossover and adds phase boost above what is normally possible from Type II compensation. It places an additional zero/pole pair. This zero and pole pair is not independent. Once the zero location is chosen, the pole is fixed as well. The zero is placed at the intended crossover frequency by calculating the value of C17 with 公式 31. The calculated value is 216 pF and the closest standard value is 220 pF.

$$C_{FF} = \frac{1}{3 \times \pi \times R_{FBT} \times f_{CO}} \quad (31)$$

The initial compensation based on these calculations is R6 = 19.1 kΩ, C6 = 3300 pF, C7 = 22 pF and C17 = 220 pF. These values yield a stable design but after testing the real circuit these values were changed to optimize performance. The final values used in the schematic are R6 = 20.5 kΩ, C6 = 1800 pF, C7 = 180 pF and C17 = 180 pF.

8.2.2.12 LDOIN Capacitor

Depending on the trace impedance between the LDOIN bulk power supply to the device, a transient increase of source current is supplied mostly by the charge from the LDOIN input capacitor. Use a 10-µF (or greater) and X5R grade (or better) ceramic capacitor to supply this transient charge.

8.2.2.13 VTTREF Capacitor

Add a ceramic capacitor, with a value 0.22 µF and X5R grade (or better), placed close to the VTTREF terminal for stable operation.

8.2.2.14 VTT Capacitor

For stable operation, two 10-µF (or greater) and X5R (or better) grade ceramic capacitor(s) need to be attached close to the VTT terminal. This capacitor is recommended to minimize any additional equivalent series resistance (ESR) and/or equivalent series inductance (ESL) of ground trace between the PGND terminal and the VTT capacitor(s).

8.2.3 Application Curves

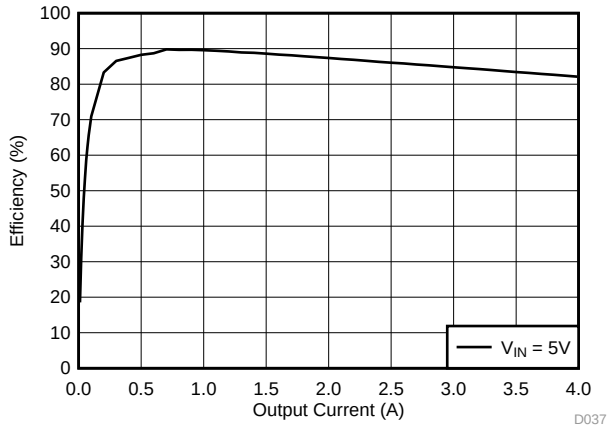


图 49. V_{DD} Output Efficiency

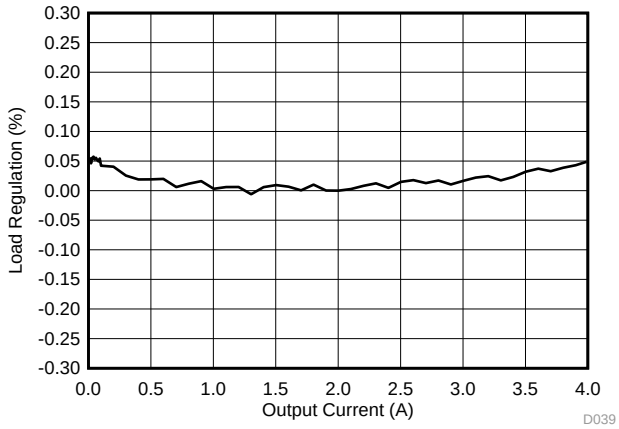


图 50. V_{DD} Output Load Regulation, V_{IN} = 5 V

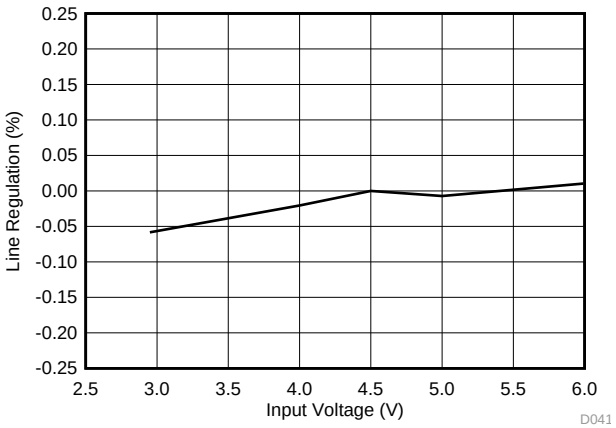


图 51. V_{DD} Output Line Regulation, I_{OUT} = 2 A

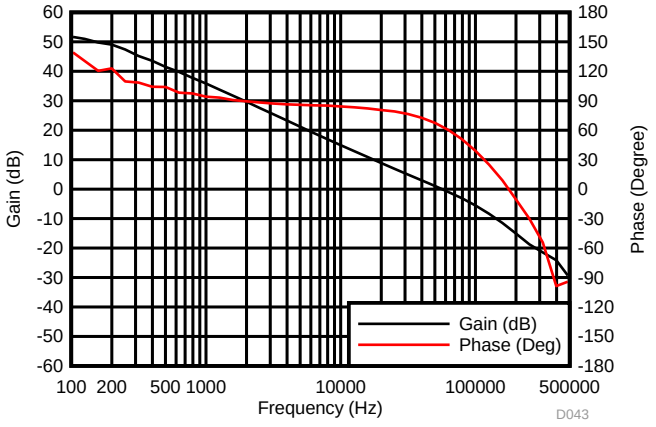


图 52. V_{DD} Output Loop Response

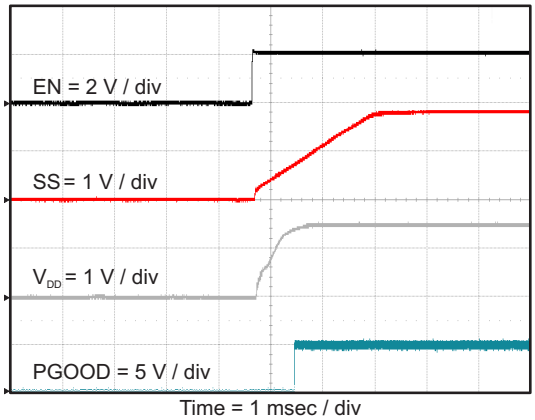


图 53. V_{DD} Start-Up Relative to Enable

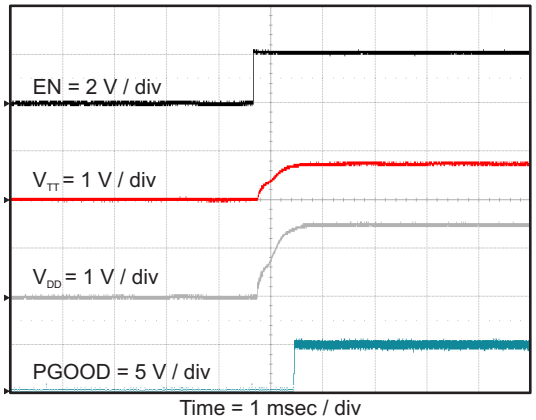


图 54. V_{TT} and V_{DD} Start-Up Relative to Enable

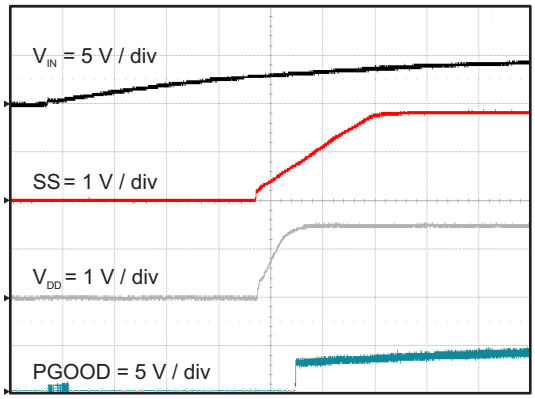


图 55. V_{DD} Start-Up Relative to V_{IN}

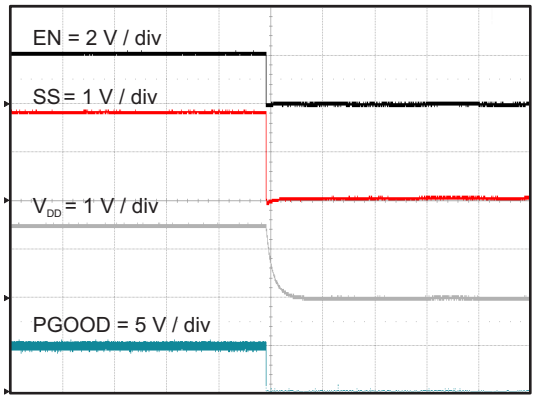


图 56. V_{DD} Shutdown Relative to Enable

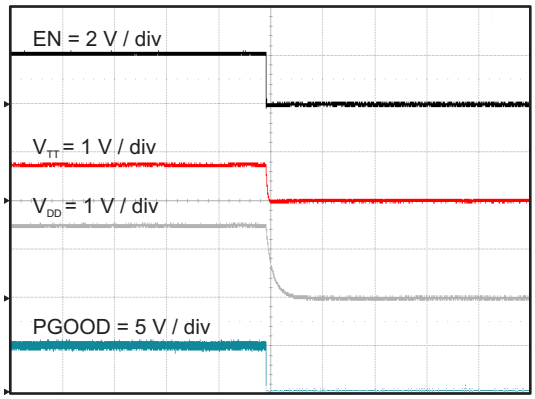


图 57. V_{TT} and V_{DD} Shutdown Relative to Enable

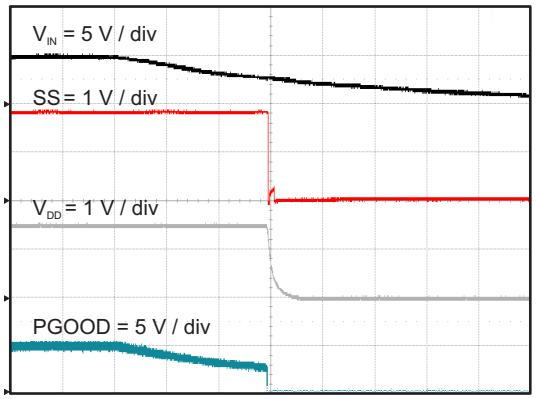


图 58. V_{DD} Shutdown Relative to V_{IN}

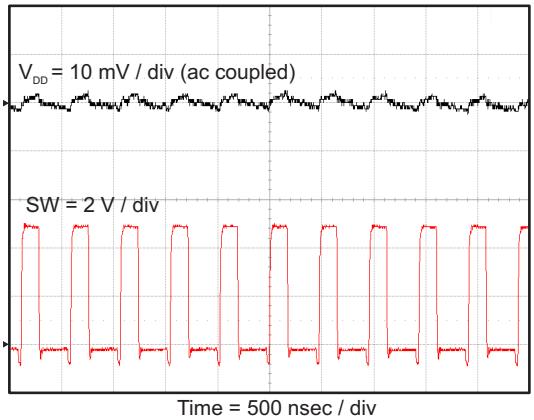


图 59. V_{DD} Output Ripple

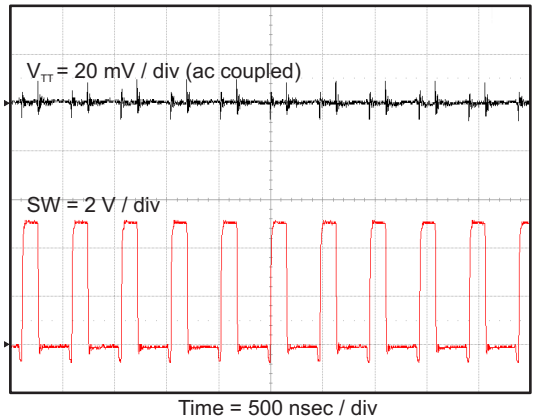


图 60. V_{TT}Output Ripple

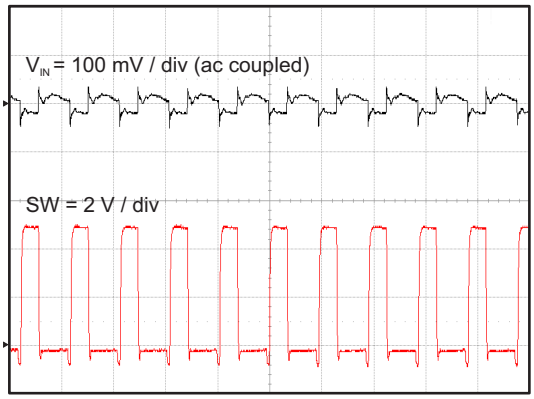


图 61. Input Ripple

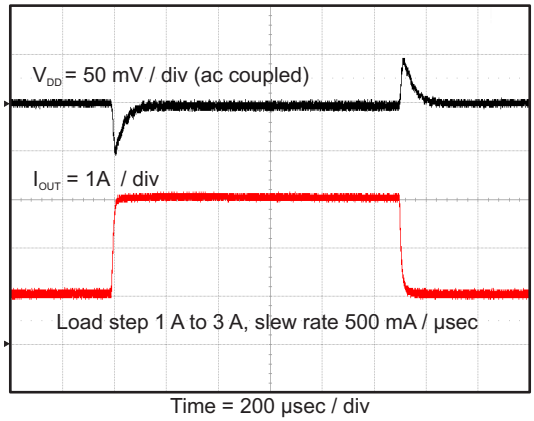


图 62. V_{DD} Output Transient Response

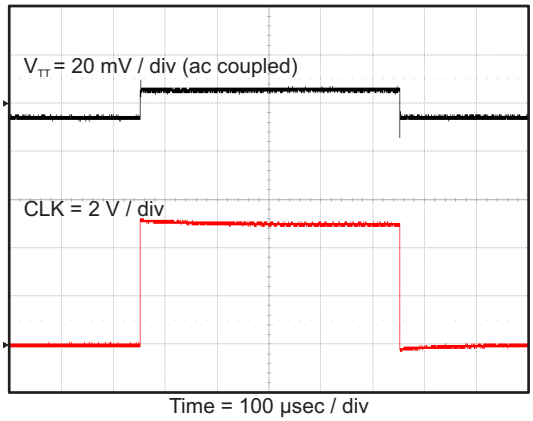


图 63. V_{TT} Output Transient Response

9 Power Supply Recommendations

The TPS54116-Q1 is designed to be powered by a well regulated dc voltage between 2.95 and 6 V. The TPS54116-Q1 is a buck converter so the input supply voltage must be greater than the desired output voltage to regulate the output voltage to the desired value. If the input supply voltage is not high enough the output voltage will begin to drop. Input supply current must be appropriate for the desired output current.

10 Layout

10.1 Layout Guidelines

Layout is a critical portion of good power supply design. There are several signal paths that conduct fast changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power supplies performance. Guidelines are as follows. See 图 64 for a PCB layout example.

- The input bypass capacitor for PVIN to PGND should be placed as close as possible to the TPS54116-Q1 with short and wide connections to minimize parasitic inductance.
- The input bypass capacitor for AVIN should be placed as close as possible to the TPS54116-Q1 with a short return to the AGND pin. This capacitor and pin should also be tied to the input voltage before the PVIN bypass capacitors to limit the switching noise from PVIN.
- The output capacitor for VTT to VTTGND should be placed as close as possible to the TPS54116-Q1 with short and wide connections to minimize parasitic inductance and resistance. Too much parasitic inductance and resistance can affect the stability of the high performance VTT LDO.
- The VTTSNS pin should be connected tothe VTT output capacitors as a seperate trace from the high current VTT power trace. If sensing the voltage at the pont of the load is required, it is recommended to also attach the output capacitors at that point while still minimizing parasitic inductance and resistance.
- The input bypass capacitor for LDOIN to VTTGND should be placed as close as possible to the TPS54116-Q1 with short and wide connections to minimize parasitic inductance. This capacitor is used to supply the transient current to the VTT output.
- The VDDQSNS pin should be routed as a separate trace from the high current VDDQ trace and connect near the point of regulation for VDDQ.
- The top of the FB resistor divider should be routed as a separate trace from the high current VDDQ trace and connect near the the point of regulation for VDDQ.
- The analog control circuits should have a return path to the quiet AGND and not overlap with the noisey PGND. Sensitive pins containing analog control circuits are RT/SYNC, SS/TRK, COMP, FB, ILIM, and VTTREF. It is important to minimize the length of the traces connected to the RT/SYNC, COMP, FB and ILIM pins.
- The PGND pins, AGND and VTTGND pin should be tied directly to the power pad under the IC to provide a low impedance connection between the pins.
- The BOOT capacitor should connect directly between the BOOT and SW pins.
- The SW pin should be routed to the output inductor with a short and wide trace to minimize capacitive coupling.
- The thermal pad should be connected to any internal PCB ground planes using multiple vias directly under the IC. For operation at full rated load, the top side ground area and bottom side ground area along with any additional internal ground planes must provide adequate heat dissipating area. For best thermal performance minimize cuts in the bottom side ground copper.
- Additional vias can be used to connect the top side ground area to the internal planes near the input and output capacitors for the buck converter and VTT LDO.

The additional external components can be placed approximately as shown. It may be possible to obtain acceptable performance with alternate PCB layouts, however this layout has been shown to produce good results and is meant as a guideline.

10.2 Layout Example

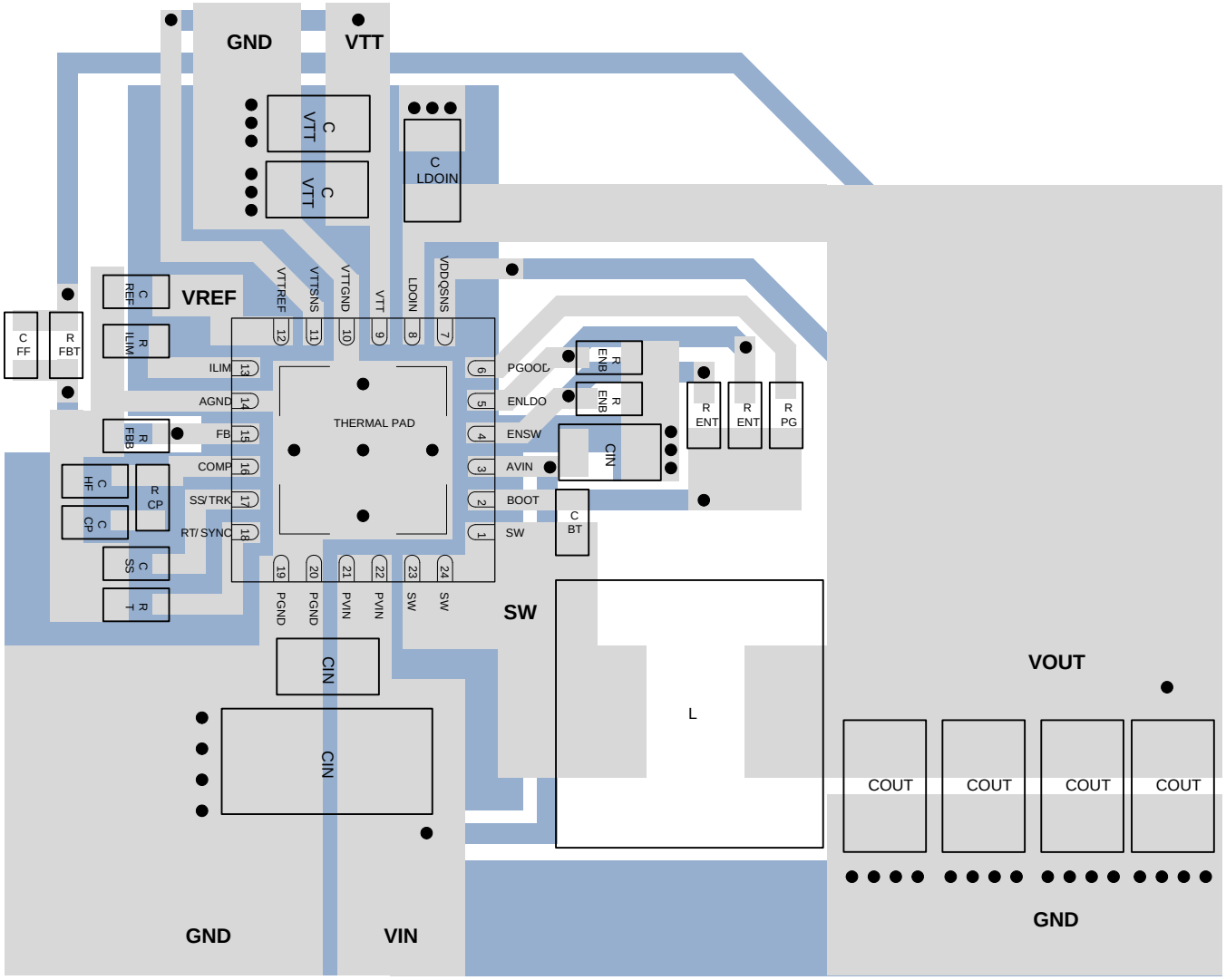


图 64. PCB Layout Example

11 器件和文档支持

11.1 接收文档更新通知

如需接收文档更新通知，请访问 www.ti.com.cn 网站上的器件产品文件夹。点击右上角的*提醒我* (Alert me) 注册后，即可每周定期收到已更改的产品信息。有关更改的详细信息，请查阅已修订文档中包含的修订历史记录。

11.2 社区资源

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 商标

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页中包括机械、封装和可订购信息。这些信息是针对指定器件可提供的最新数据。这些数据会在无通知且不对本文档进行修订的情况下发生改变。欲获得该数据表的浏览器版本，请查阅左侧的导航栏

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS54116QRTWRQ1	ACTIVE	WQFN	RTW	24	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	54116Q A2	Samples
TPS54116QRTWTQ1	ACTIVE	WQFN	RTW	24	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	54116Q A2	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

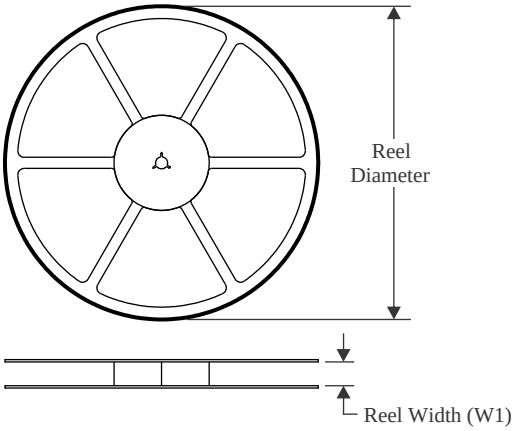
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

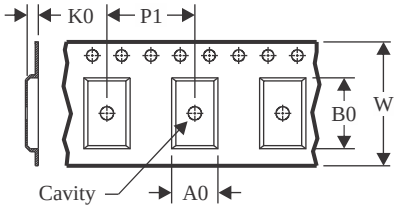
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

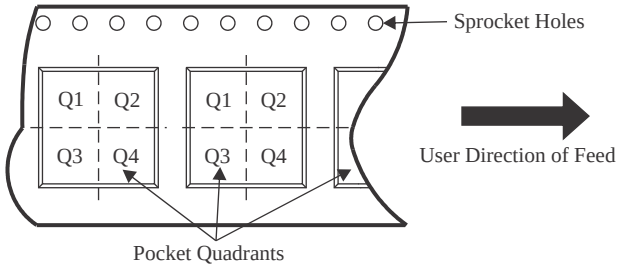


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

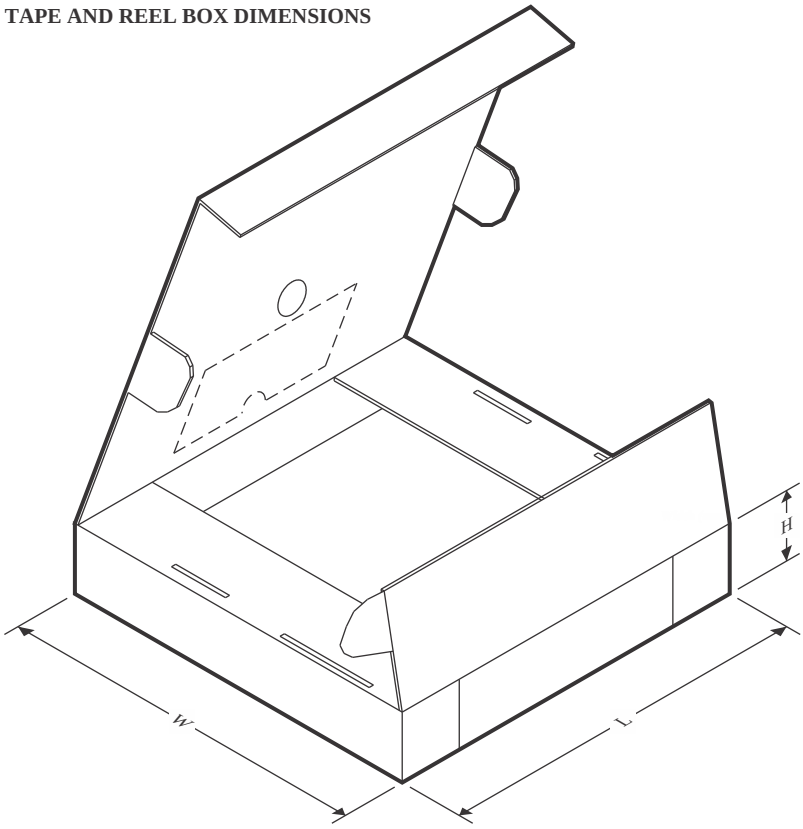
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS54116QRTWRQ1	WQFN	RTW	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
TPS54116QRTWTQ1	WQFN	RTW	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS54116QRTWRQ1	WQFN	RTW	24	3000	346.0	346.0	33.0
TPS54116QRTWTQ1	WQFN	RTW	24	250	210.0	185.0	35.0

重要声明和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 TI 的销售条款或 ti.com 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265