TEXAS INSTRUMENTS
TPS543820E
ZHCSM41A – MAY 2020 – REVISED JUNE 2021

TPS543820E 具有内部补偿高级电流模式控制功能的 TPS543820 4V 至 18V 输入、83668A 同步 SWIFT™ 降压转换器

1 特性

- 固定频率、内部补偿高级电流模式 (ACM) 控制
- 集成式 25mΩ 和 6.5mΩ MOSFET
- 输入电压范围：4V 至 18V
- 输出电压范围：0.5V 至 7V
- 三种可选的 PWM 斜坡选项，可优化控制环路性能
- 五种可选的开关频率：500kHz、750kHz、1MHz、1.5MHz 和 2.2MHz
- 与一个外部时钟同步
- 0.5V，整个温度范围内的电压基准精度为 ±0.5%
- 可选的软启动时间：0.5ms、1ms、2ms 和 4ms
- 单调启动至预偏置输出
- 可选的电流限制，支持 8A 和 6A 运行
- 具有可调节输入欠压锁定功能的使能端
- 电源正常输出监视器
- 输出过压、输出欠压、输入欠压、过流和过热保护
- -55°C 至 150°C 的工作结温范围
- 2.5mm × 3mm 14 引脚 VQFN-HR 封装，间距为 0.5mm

2 应用

- 支持国防、航空航天和医疗应用
  - 额定结温范围为 -55°C 至 +150°C
- 加固型通信
- 铁路运输
- 航电设备和飞机控制

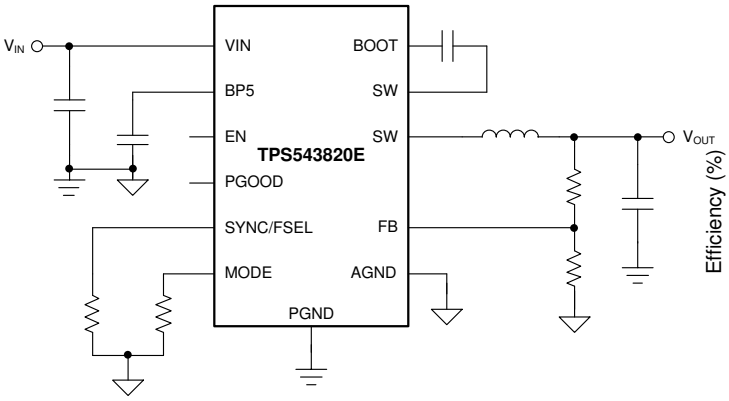
3 说明

TPS543820E 是一款高效的 18V、8A 同步降压转换器，其中采用了内部补偿固定频率高级电流模式控制。该器件能够在以高达 2.2MHz 的开关频率运行时提供高效率。该器件采用 2.5mm × 3mm 小型 HotRod™ VQFN 封装，并且在高频率下具有很高的效率，因此成为需要小解决方案尺寸的设计的理想选择。固定频率控制器可以在 500kHz 至 2.2MHz 范围内运行，并且可以通过 SYNC 引脚与外部时钟同步。其他功能包括高精度电压基准、可选的软启动时间、单调启动至预偏置输出、可选的电流限制、可调 UVLO（通过 EN 引脚实现）以及全套故障保护。

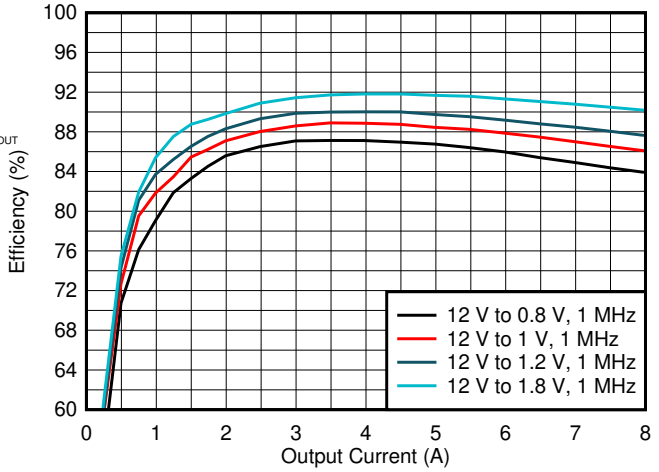
器件信息

器件型号	封装(1)	封装尺寸（标称值）
TPS543820E	VQFN-HR (14)	2.50mm x 3.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



简化版原理图



效率

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4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision * (December 2020) to Revision A (June 2021)	Page
• Changed 10-ns transient to 20-ns transient	4
• Changed VIN to SW, transient 20 ns min value to -6	4
• Changed SW, transient 20 ns min value to -5	4
• Changed max V_{OUT} to 7 V	4
• Added $T_{OFF(min)}$ max value	5
• Added text for considering minimum off-time for fsw selection	18

5 Pin Configuration and Functions

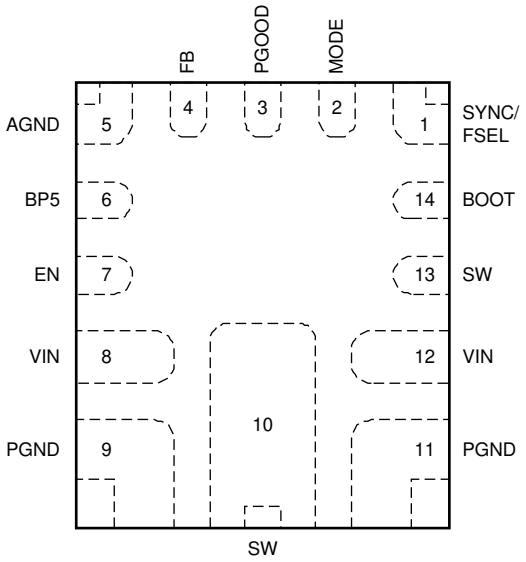


图 5-1. 14-Pin VQFN-HR RPY Package (Top View)

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
SYNC/FSEL	1	I	Frequency select and external clock synchronization. A resistor to ground sets the switching frequency of the device. An external clock can also be applied to this pin to synchronize the switching frequency.
MODE	2	I	A resistor to ground selects the current limit, soft start rate, and PWM ramp amplitude.
PGOOD	3	O	Open-drain power good indicator
FB	4	I	Feedback pin for output voltage regulation. Connect this pin to the midpoint of a resistor divider to set the output voltage.
AGND	5	-	Ground return for internal analog circuits
BP5	6	O	Internal 4.5-V regulator output. Bypass this pin with a 2.2- μ F capacitor to AGND.
EN	7	I	Enable pin. Float to enable, enable/disable with an external signal, or adjust the input undervoltage lockout with a resistor divider.
VIN	8, 12	I	Input power to the power stage. Low impedance bypassing of these pins to PGND is critical. A 10-nF to 100-nF capacitor from each VIN to PGND close to IC is required.
PGND	9, 11	-	Ground return for the power stage. This pin is internally connected to the source of the low-side MOSFET.
SW	10	O	Switch node of the converter. Connect this pin to the output inductor.
SW	13	O	Return path for the internal high-side MOSFET gate driver bootstrap capacitor. Connect a capacitor from BOOT to this pin. The SW pins are connected internally.
BOOT	14	I	Supply for the internal high-side MOSFET gate driver. Connect a capacitor from this pin to SW.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Input voltage	VIN	-0.3	20	V
Input voltage	VIN to SW, DC	-0.3	20	V
Input voltage	VIN to SW, transient 20 ns	-6	25	V
Input voltage	BOOT	-0.3	25	V
Input voltage	BOOT to SW	-0.3	6	V
Input voltage	EN, PGOOD, MODE, SYNC/FSEL, FB	-0.3	6	V
Output voltage	SW, DC	-0.3	20	V
Output voltage	SW, transient 20 ns	-5	22	V
Operating junction temperature, T_J	Operating junction temperature, T_J	-55	150	°C
Storage temperature, T_{stg}		– 55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
$V_{(ESD)}$	Electrostatic discharge	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Input voltage	V_{IN}	4		18	V
Output voltage	V_{OUT}	0.5		7	V
Output current	I_{OUT}			8	A
T_J	Operating junction temperature	-55		150	°C
f_{SYNC}	External clock frequency	400		2600	kHz

6.4 Thermal Information

THERMAL METRIC(1)		TPS543820E		UNIT
		RPY (QFN, JEDEC)	RPY (QFN, TI EVM)	
		14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	58.9	29.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	37.8	Not applicable (2)	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	7.3	Not applicable (2)	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.9	1.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	7.2	13.4	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
(2) Not applicable to an EVM layout.

6.5 Electrical Characteristics

T_J = –55°C to +150°C, V_{VIN} = 4 V - 18 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE						
$I_{Q(VIN)}$	VIN operating non-switching supply current	V_{EN} = 1.3 V, V_{FB} = 550 mV, V_{VIN} = 12 V, 1 MHz		1200	1600	µA
$I_{SD(VIN)}$	VIN shutdown supply current	V_{EN} = 0 V, V_{VIN} = 12 V		15	25	µA
	VIN UVLO rising threshold	VIN rising	3.9	4	4.1	V
	VIN UVLO hysteresis			150		mV
ENABLE AND UVLO						
$V_{EN(rise)}$	EN voltage rising threshold	EN rising, enable switching		1.2	1.25	V
$V_{EN(fall)}$	EN voltage falling threshold	EN falling, disable switching	1.05	1.1		V
$V_{EN(hyst)}$	EN voltage hysteresis			100		mV
	EN pin sourcing current	V_{EN} = 1.1 V	0.4	1.5		µA
	EN pin sourcing current	V_{EN} = 1.3 V		11.6		µA
INTERNAL LDO BP5						
V_{BP5}	Internal LDO BP5 output voltage	V_{VIN} = 12 V		4.5		V
	BP5 dropout voltage	V_{VIN} – V_{BP5}, V_{VIN} = 3.8 V			350	mV
	BP5 short-circuit current limit	V_{VIN} = 12 V		75		mA
REFERENCE VOLTAGE						
V_{FB}	Feedback Voltage	T_J = –55°C to 150°C	497.5	500	502.5	mV
$I_{FB(LKG)}$	Input leakage current into FB pin	V_{FB} = 500 mV, non-switching, V_{VIN} = 12 V, V_{EN} = 0 V		1		nA
SWITCHING FREQUENCY AND OSCILLATOR						
f_{SW}	Switching frequency	R_{MODE} = 24.3 kΩ	450	500	550	kHz
f_{SW}	Switching frequency	R_{MODE} = 17.4 kΩ	675	750	825	kHz
f_{SW}	Switching frequency	R_{MODE} = 11.8 kΩ	900	1000	1100	kHz
f_{SW}	Switching frequency	R_{MODE} = 8.06 kΩ	1350	1500	1650	kHz
f_{SW}	Switching frequency	R_{MODE} = 4.99 kΩ	1980	2200	2420	kHz
SYNCHRONIZATION						
$V_{IH(sync)}$	High-level input voltage		1.8			V
$V_{IL(sync)}$	Low-level input voltage				0.8	V
SOFT-START						
t_{SS1}	Soft-start time	R_{MODE} = 1.78 kΩ		0.5		ms
t_{SS2}	Soft-start time	R_{MODE} = 2.21 kΩ		1		ms
t_{SS3}	Soft-start time	R_{MODE} = 2.74 kΩ		2		ms
t_{SS4}	Soft-start time	R_{MODE} = 3.32 kΩ		4		ms
POWER STAGE						
$R_{DS(on)HS}$	High-side MOSFET on-resistance	T_J = 25°C, V_{VIN} = 12 V, $V_{BOOT-SW}$ = 4.5 V		25		mΩ
$R_{DS(on)LS}$	Low-side MOSFET on-resistance	T_J = 25°C, V_{BP5} = 4.5 V		6.5		mΩ
$V_{BOOT-SW(UV\_r)}$	BOOT-SW UVLO rising threshold	$V_{BOOT-SW}$ rising		3.2		V
$V_{BOOT-SW(UV\_f)}$	BOOT-SW UVLO falling threshold	$V_{BOOT-SW}$ falling		2.8		V
$T_{ON(min)}$	Minimum ON pulse width	I_{OUT} > ½ I_{L_PK-PK}		30	37	ns
$T_{OFF(min)}$	Minimum OFF pulse width (1)			115	140	ns
CURRENT SENSE AND OVERCURRENT PROTECTION						
$I_{OC\_HS\_pk1}$	High-side peak current limit	R_{MODE} = 1.78 kΩ	11.7	12.2	12.7	A
$I_{OC\_HS\_pk2}$	High-side peak current limit	R_{MODE} = 22.1 kΩ	8.6	9	9.6	A
$I_{OC\_LS\_src1}$	Low-side sourcing current limit	R_{MODE} = 1.78 kΩ	9.4	10.4	11.3	A
$I_{OC\_LS\_src2}$	Low-side sourcing current limit	R_{MODE} = 22.1 kΩ	6.2	7.4	8.5	A
$I_{OC\_LS\_snk}$	Low-side sinking current limit	Current into SW pin	2.95			A
OUTPUT OVERVOLTAGE AND UNDERVOLTAGE PROTECTIONS						

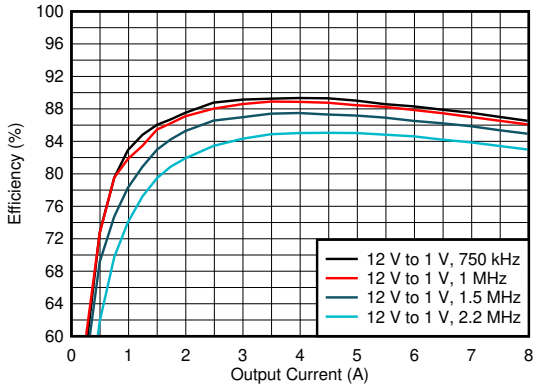
T_J = – 55°C to +150°C, V_{VIN} = 4 V - 18 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OVP}	Overvoltage-protection (OVP) threshold voltage	V_{FB} rising		120		% V_{REF}
V_{UVP}	Undervoltage-protection (UVP) threshold voltage	V_{FB} falling		80		% V_{REF}
POWER GOOD						
	PGOOD threshold	V_{FB} rising (Fault)	113	116	119	% V_{REF}
	PGOOD threshold	V_{FB} falling (Good)	105	108	111	% V_{REF}
	PGOOD threshold	V_{FB} rising (Good)	89	92	95	% V_{REF}
	PGOOD threshold	V_{FB} falling (Fault)	81	84	87	% V_{REF}
$I_{PGOOD(LKG)}$	Leakage current into PGOOD pin when open drain output is high	V_{PGOOD} = 4.7 V			5	µA
$V_{PG(low)}$	PGOOD low-level output voltage	I_{PGOOD} = 2 mA, V_{IN} = 12 V			0.5	V
	Min VIN for valid PGOOD output			0.9	1	V
HICCUP						
	Hiccup time before re-start			7*t_{SS}		ms
OUTPUT DISCHARGE						
R_{Dischg}	Output discharge resistance	V_{VIN} = 12 V, V_{SW} = 0.5 V, power conversion disabled.		100		Ω
THERMAL SHUTDOWN						
T_{SDN}	Thermal shutdown threshold (1)	Temperature rising		165	175	°C
T_{HYST}	Thermal shutdown hysteresis (1)			12		°C

(1) Specified by design. Not production tested.

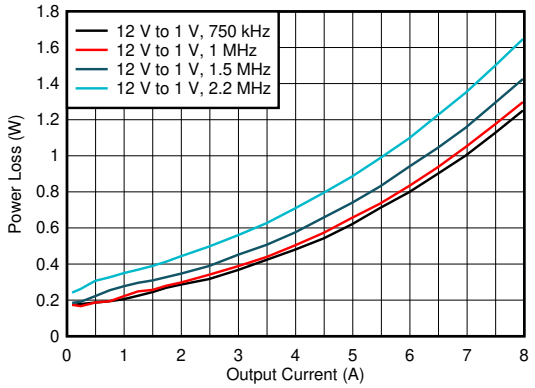
6.6 Typical Characteristics

T_A = 25°C



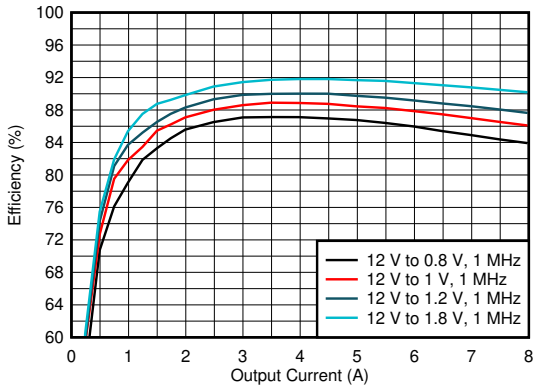
L = 470 nH, 2.5 mΩ typical

图 6-1. Efficiency vs Output Current



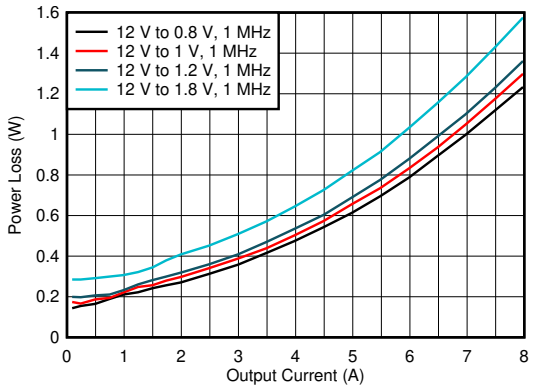
L = 470 nH, 2.5 mΩ typical

图 6-2. Power Loss vs Output Current



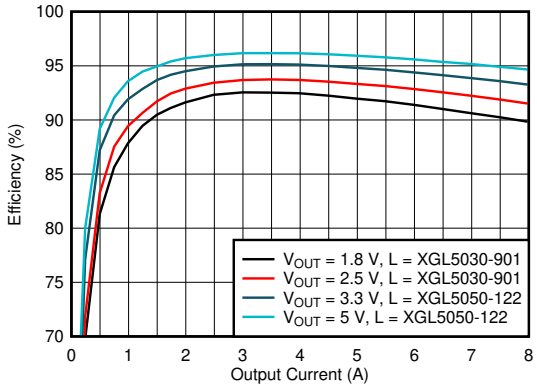
L = 470 nH, 2.5 mΩ typical

图 6-3. Efficiency vs Output Current



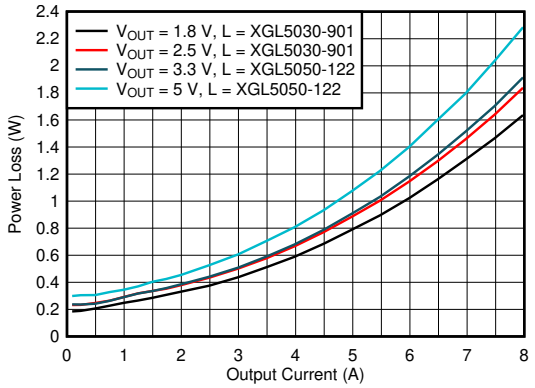
L = 470 nH, 2.5 mΩ typical

图 6-4. Power Loss vs Output Current



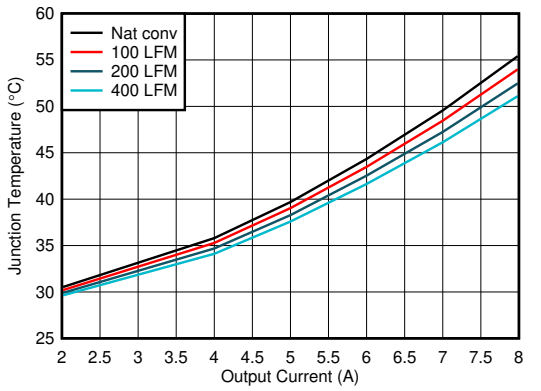
V_{IN} = 12 V f_{SW} = 1.0 MHz

图 6-5. Efficiency vs Output Current – 1.8-V to 5.0-V Output



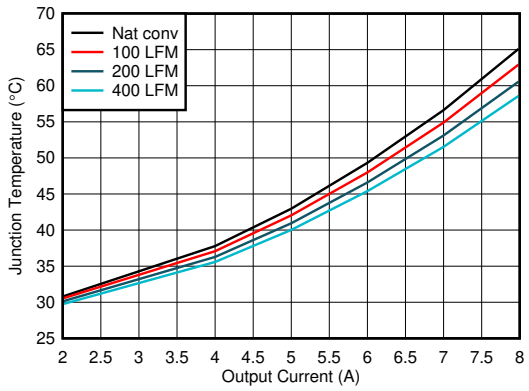
V_{IN} = 12 V f_{SW} = 1.0 MHz

图 6-6. Power Loss vs Output Current – 1.8-V to 5.0-V Output



V_{IN} = 12 V f_{SW} = 1.0 MHz T_A = 25 °C

图 6-7. Junction Temperature vs Output Current – 1-V Output



V_{IN} = 12 V f_{SW} = 1.0 MHz T_A = 25 °C

图 6-8. Junction Temperature vs Output Current – 3.3-V Output

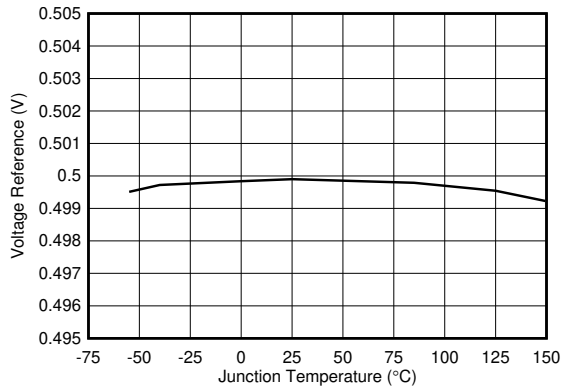
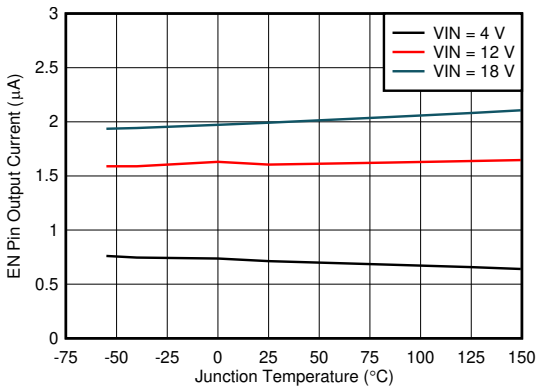
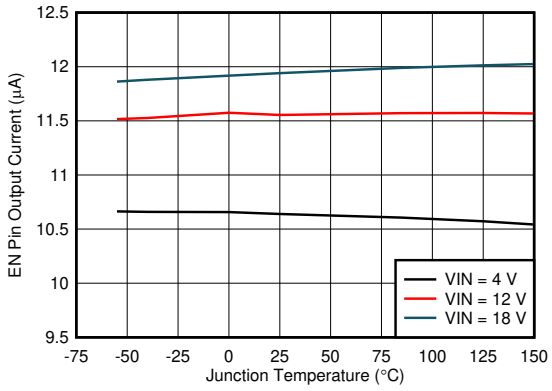


图 6-9. Regulated FB Voltage vs Junction Temperature



V_{EN} = 1.1 V

图 6-10. EN Pin Current vs Junction Temperature



V_{EN} = 1.3 V

图 6-11. EN Pin Current vs Junction Temperature

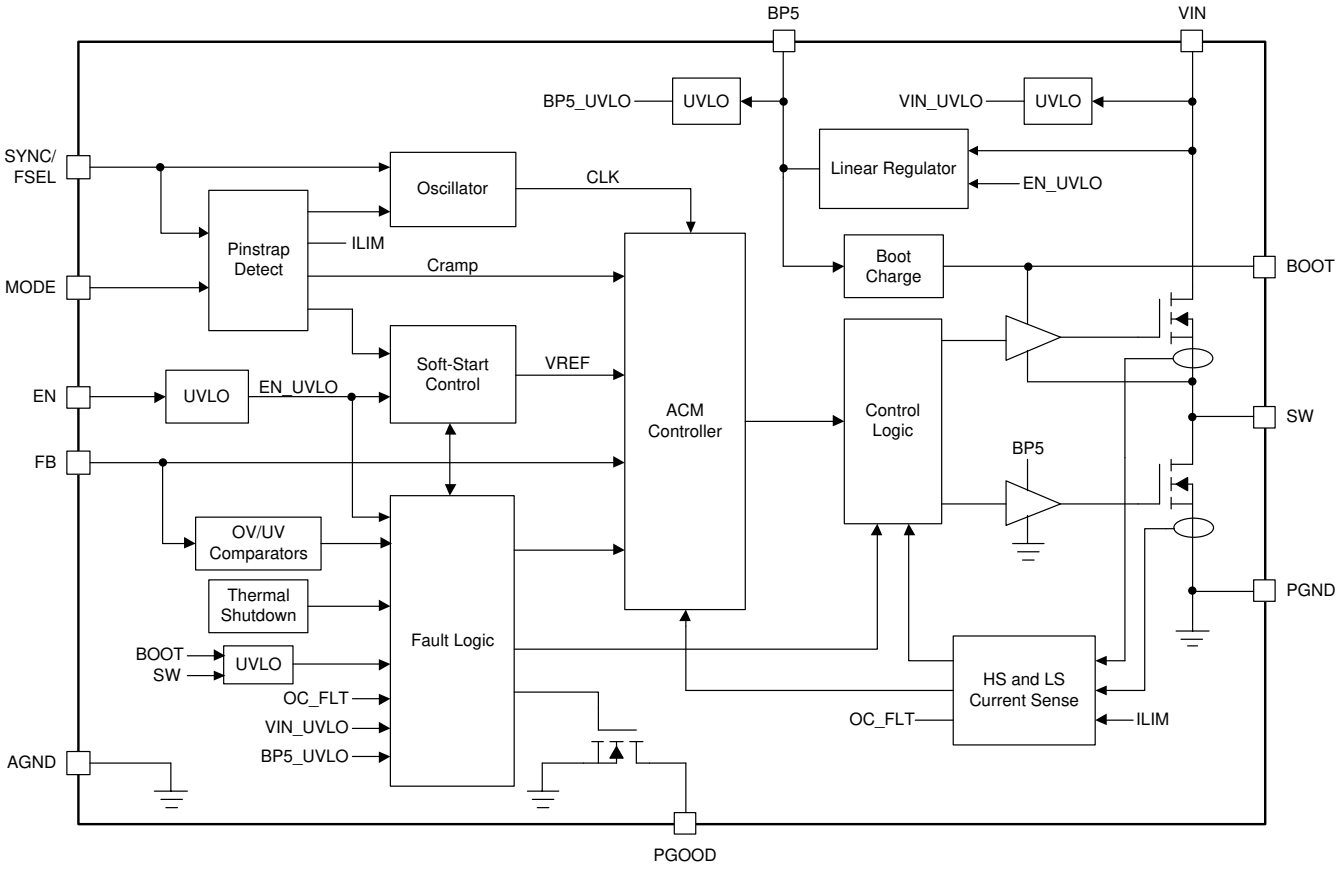
7 Detailed Description

7.1 Overview

The TPS543820E device is a 8-A, high-performance, synchronous buck converter with two integrated N-channel MOSFETs. The TPS543820E has a maximum operating junction temperature of 150°C, making it suitable for high-ambient temperature applications such as wireless infrastructure. The input voltage range is 4 V to 18 V and the output voltage range is 0.5 V to 7 V. The device features a fixed-frequency Advanced Current Mode control with a switching frequency of 500 kHz to 2.2 MHz, allowing for efficiency and size optimization when selecting output filter components. The switching frequency of the device can be synchronized to an external clock applied to the SYNC pin.

Advanced Current Mode (ACM) is an emulated peak current control topology. It supports stable static and transient operation without complex external compensation design. This control architecture includes an internal ramp generation network that emulates inductor current information, enabling the use of low-ESR output capacitors such as multi-layered ceramic capacitors (MLCC). The internal ramp also creates a high signal-to-noise ratio for good noise immunity. The TPS543820E has three ramp options (see 节 *7.3.6* for details) to optimize the internal loop for various inductor and output capacitor combinations with only a single resistor to AGND. The TPS543820E is easy-to-use and allows low external component count with fast load transient response. Fixed-frequency operation also provides ease-of-filter design to overcome EMI noise.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 VIN Pins and VIN UVLO

The VIN pin voltage supplies the internal control circuits of the device and provides the input voltage to the power stage. The input voltage for VIN can range from 4 V to 18 V. The device implements internal UVLO circuitry on the VIN pin. The device is disabled when the VIN pin voltage falls below the internal VIN UVLO

threshold. The internal VIN UVLO threshold has a hysteresis of 150 mV. A voltage divider connected to the EN pin can adjust the input voltage UVLO as appropriate. See 节 7.3.2 for more details.

7.3.2 Enable and Adjustable UVLO

The EN pin provides on/off control of the device. Once the EN pin voltage exceeds its threshold voltage, the device begins its start-up sequence. If the EN pin voltage is pulled below the threshold voltage, the regulator stops switching and enters a low operating current state. The EN pin has an internal pullup current source, Ip, allowing it to be floated to enable the device by default. It is important to ensure that leakage currents of anything connected to the EN pin do not exceed the minimum EN pullup current or the device may not be able to start. If an application requires controlling the EN pin, an open drain or open collector output logic can be interfaced with the pin.

When the EN pin voltage exceeds its threshold voltage and the VIN pin voltage exceeds its VIN UVLO threshold, the device begins its start-up sequence. First, the BP5 LDO is enabled and charges the external BP5 capacitor. Once the voltage on the BP5 pin exceeds its UVLO threshold, the device enters a power-on delay. During the power-on delay, the values of the pinstrap resistors on the MODE pin (see 节 7.3.8) and SYNC/FSEL pin (see 节 7.3.4) are determined and the control loop is initialized. The power-on delay is typically 600 μs. After the power-on delay, soft start begins.

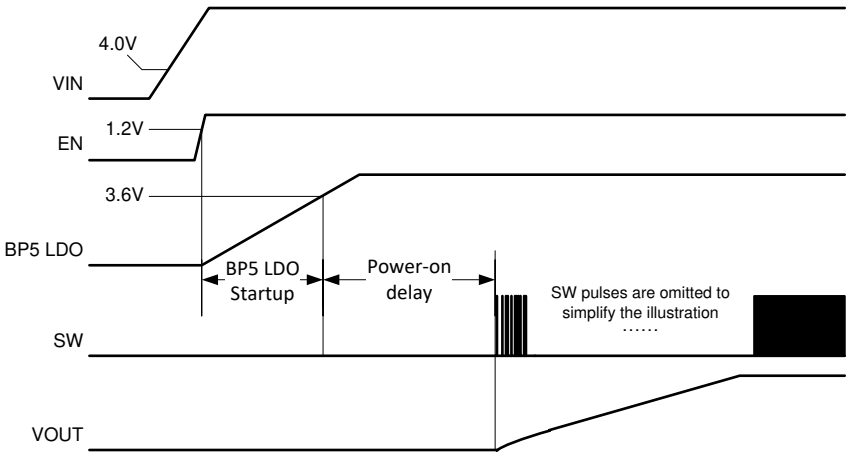


图 7-1. Start-up Sequence

An external resistor divider can be added from VIN to the EN pin for adjustable UVLO and hysteresis as shown in 图 7-2. The EN pin has a small pullup current, Ip, which sets the default state of the pin to enable when no external components are connected. The pullup current is also used to control the voltage hysteresis for the UVLO function since it increases by Ih once the EN pin crosses the enable threshold. The UVLO thresholds can be calculated using 方程式 1 and 方程式 2. When using the adjustable UVLO function, 500 mV or greater hysteresis is recommended. For applications with very slow input voltage slew rate, a capacitor can be placed from the EN pin to ground to filter any glitches on the input voltage.

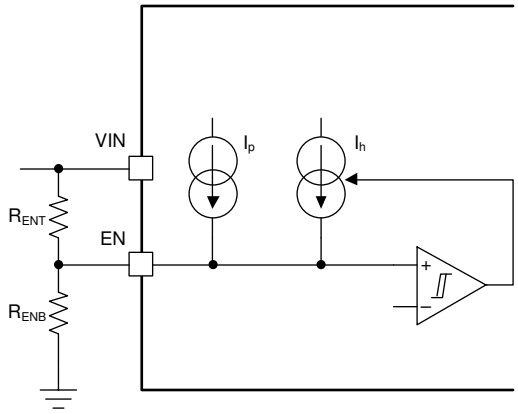


图 7-2. Adjustable UVLO Using EN

$$R_{ENT} = \frac{V_{START} \times \left(\frac{V_{ENFALLING}}{V_{ENRISING}} \right) - V_{STOP}}{I_p \times \left(1 - \frac{V_{ENFALLING}}{V_{ENRISING}} \right) + I_h} \quad (1)$$

$$R_{ENB} = \frac{R_{ENT} \times V_{ENFALLING}}{V_{STOP} - V_{ENFALLING} + R_{ENT} \times \left(I_p + I_h \right)} \quad (2)$$

7.3.3 Adjusting the Output Voltage

The output voltage is programmed with a resistor divider from the output (V_{OUT}) to the FB pin shown in 图 7-3. It is recommended to use 1% tolerance or better divider resistors. Starting with a fixed value for the bottom resistor, typically 10 kΩ, use 方程式 3 to calculate the top resistor in the divider.

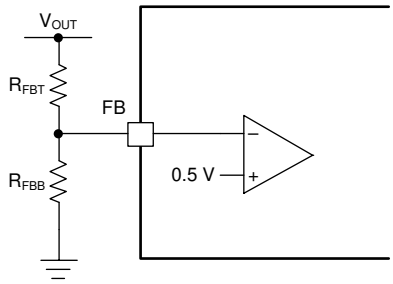


图 7-3. FB Resistor Divider

$$R_{FBT} = R_{FBB} \times \left(\frac{V_{OUT}}{V_{REF}} - 1 \right) \quad (3)$$

7.3.4 Switching Frequency Selection

The switching frequency of the device can be selected by connecting a resistor (R_{FSEL}) between the SYNC/FSEL pin and AGND. The frequency options and their corresponding programming resistors are listed in 表 7-1. It is required to use a 1% tolerance resistor or better.

表 7-1. Switching Frequency Selection

R_{FSEL} ALLOWED NOMINAL RANGE (1%) (kΩ)	RECOMMENDED E96 STANDARD VALUE (1%) (kΩ)	RECOMMENDED E12 STANDARD VALUE (1%) (kΩ)	Fsw (kHz)
⩾24.0	24.3	27	500
17.4-18.0	17.4	18	750
11.8-12.1	11.8	12	1000
8.06-8.25	8.06	8.2	1500
⩽5.11	4.99	4.7	2200

7.3.5 Switching Frequency Synchronization to an External Clock

The device can be synchronized to an external clock by applying a square wave clock signal to the SYNC/FSEL pin with a duty cycle from 20% to 80%. The clock can either be applied before the device starts up or during operation. If the clock is to be applied before the device starts, a resistor between SYNC/FSEL and AGND is not needed. If the clock is to be applied after the device starts, then the clock frequency should be within ±20% of the frequency set by the SYNC/FSEL resistor. When the clock is applied after the device starts, the device will begin synchronizing to this clock after counting four consectutive switching cycles with a clock pulse present. This is shown in 图 7-4.

7.3.5.1 Internal PWM Oscillator Frequency

When the external clock is present, the device synchronizes the switching frequency to the clock. Any time the external clock is not present, the device will default to the internal PWM oscillator frequency.

If the device starts up before an external clock signal is applied, then the internal PWM oscillator frequency is set by the R_{FSEL} resistor according to 表 7-1. The device switches at this frequency until the external clock is applied or anytime the external clock is not present.

If the external clock is applied before the device starts up, then the R_{FSEL} resistor is not needed. The device will determine the internal clock frequency by decoding the external clock frequency. 表 7-2 shows the decoding of the internal PWM oscillator frequency based on the external clock frequency.

表 7-2. Internal Oscillator Frequency Decode

EXTERNAL SYNC CLOCK FREQUENCY (kHz)	DECODED INTERNAL PWM OSCILLATOR FREQUENCY (kHz)
400 - 600	500
600 - 857	750
857 - 1200	1000
1200 - 1810	1500
1810 - 2640	2200

The thresholds for the external SYNC clock frequency ranges have approximately a ±5% tolerance. If the external clock frequency is to be within that tolerance range, it is possible for the internal PWM oscillator frequency to be decoded as either the frequency above or below that threshold. Since the internal frequency is what is used in case of the loss of the synchronization clock, it is recommended that the output LC filter and ramp selection are chosen to be stable for either frequency. 表 7-3 shows the tolerance range of the decode thresholds. If the external clock is to be within any of these ranges, it is recommended to ensure converter stability for both possible internal PWM oscillator frequencies.

表 7-3. Frequency Decode Thresholds

MINIMUM (kHz)	TYPICAL (kHz)	MAXIMUM (kHz)
570	600	630
814	857	900
1140	1200	1260
1736	1810	1884

7.3.5.2 Loss of Synchronization

If at any time during operation, there is a loss of synchronization, the device will default to the internal PWM oscillator frequency until the synchronization clock returns. Once the clock is no longer present, the device will switch at 70% of the internal clock frequency for four consecutive cycles. After four consecutive cycles without clock pulses, the device will operate at the normal internal PWM oscillator frequency. This is demonstrated in 图 7-4.

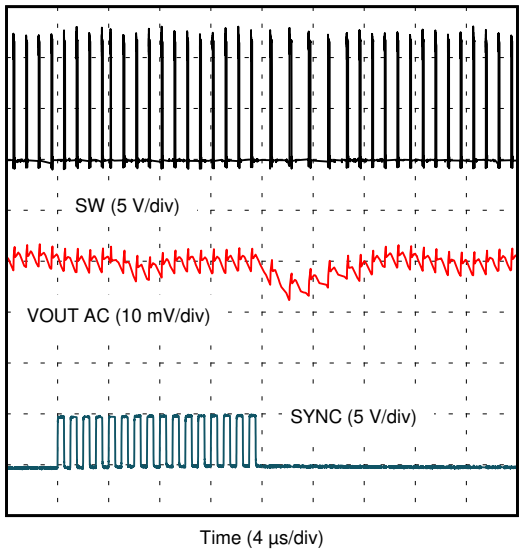


图 7-4. Clock Synchronization Transitions

7.3.5.3 Interfacing the SYNC/FSEL Pin

If an application requires synchronizing to a SYNC clock but the clock is unavailable before the device is enabled, a high impedance buffer is recommended to ensure proper detection of the R_{FSEL} value. 图 7-5 shows the recommended implementation. The leakage current into the buffer output must be less than 5 µA to ensure proper detection of the R_{FSEL} value. Power the buffer from the BP5 output of the device to ensure its VCC voltage is available and the buffers output is high impedance before the device tries to detect the R_{FSEL} value. When powering the buffer from the BP5 pin, the external load on the BP5 pin must be less than 2 mA.

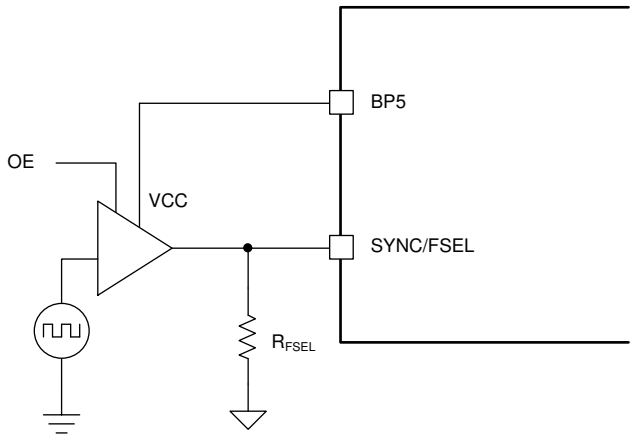


图 7-5. Interfacing the SYNC/FSEL Pin with a Buffer

7.3.6 Ramp Amplitude Selection

The TPS543820E uses V_{IN}, duty cycle, and low-side FET current information to generate an internal ramp. The ramp amplitude is determined by an internal ramp generation capacitor, C_{RAMP}. Three different values for C_{RAMP}

can be selected with a resistor to AGND on the MODE pin (see 节 7.3.8). The capacitor options are 1 pF, 2 pF, and 4 pF. A larger ramp capacitor results in a smaller ramp amplitude, which results in a higher control loop bandwidth. 图 7-6 and 图 7-7 show how the loop changes with each ramp setting for the schematic in 节 8.2.3.

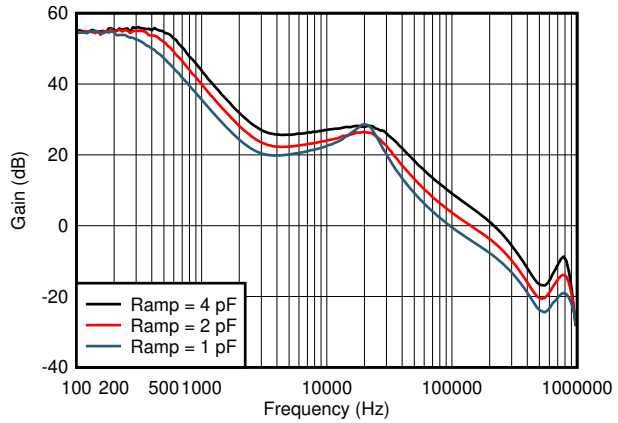


图 7-6. Loop Gain vs Ramp Settings

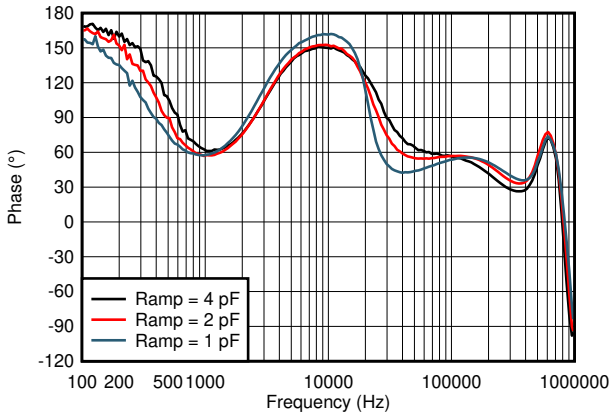


图 7-7. Loop Phase vs Ramp Settings

7.3.7 Soft Start and Prebiased Output Start-up

During start-up, the device softly ramps the reference voltage to reduce inrush currents. There are four options for the soft-start time, which is the time it takes for the reference to ramp to 0.5 V: 0.5 ms, 1 ms, 2 ms, and 4 ms. The soft-start time is selected with a resistor to AGND on the MODE pin (see 节 7.3.8).

The device prevents current from being discharged from the output during start-up when a prebiased output condition exists. It does this by operating in discontinuous conduction mode (DCM) during the first 16 cycles to prevent the device from sinking current. This ensures the output voltage will be smooth and monotonic during soft start.

7.3.8 Mode Pin

The ramp amplitude, soft-start time, and current limit settings are programmed with a single resistor, R_{MODE}, between MODE and AGND. 表 7-4 lists the resistor values for the available options. It is required to use a 1% tolerance resistor or better. See 节 7.3.10 for the corresponding current limit thresholds for the "High" and "Low" settings.

表 7-4. MODE Pin Selection

R_{MODE} (kΩ)	CURRENT LIMITS	C_{RAMP} (pF)	SOFT-START TIME (ms)
1.78	High	1	0.5
2.21	High	1	1
2.74	High	1	2
3.32	High	1	4
4.02	High	2	0.5
4.87	High	2	1
5.9	High	2	2
7.32	High	2	4
9.09	High	4	0.5
11.3	High	4	1
14.3	High	4	2
18.2	High	4	4
22.1	Low	1	0.5
26.7	Low	1	1
33.2	Low	1	2

表 7-4. MODE Pin Selection (continued)

R_{MODE} (kΩ)	CURRENT LIMITS	C_{RAMP} (pF)	SOFT-START TIME (ms)
40.2	Low	1	4
49.9	Low	2	0.5
60.4	Low	2	1
76.8	Low	2	2
102	Low	2	4
137	Low	4	0.5
174	Low	4	1
243	Low	4	2
412	Low	4	4

7.3.9 Power Good (PGOOD)

The PGOOD pin is an open-drain output requiring an external pullup resistor to output a high signal. Once the FB pin is between 92% and 108% of the internal voltage reference, soft start is complete, and after a 256-µs deglitch time, the PGOOD pin is de-asserted and the pin floats. A pullup resistor between the values of 10 kΩ and 100 kΩ to a voltage source that is 5.5 V or less is recommended. PGOOD is in a defined state once the VIN input voltage is greater than 1 V but with reduced current sinking capability. When the FB is lower than 84% or greater than 116% of the nominal internal reference voltage, after a 8-µs deglitch time, the PGOOD pin is pulled low. PGOOD is immediately pulled low if VIN falls below its UVLO, the EN pin is pulled low or the device enters thermal shutdown.

7.3.10 Current Protection

The protects against overcurrent events by cycle-by-cycle current limiting both the high-side MOSFET and low-side MOSFET. In an extended overcurrent condition, the device will enter hiccup. Different protections are active during positive inductor current and negative inductor current conditions.

7.3.10.1 Positive Inductor Current Protection

The current is sensed in the high-side MOSFET while it is conducting after a short blanking time to allow noise to settle. Whenever the high-side overcurrent threshold is exceeded, the high-side MOSFET is immediately turned off and the low-side MOSFET is turned on. The high-side MOSFET does not turn back on until the current falls below the low-side MOSFET overcurrent threshold. This effectively limits the peak current in the case of a short circuit condition. If a high-side overcurrent is detected for 15 consecutive cycles, the device enters hiccup.

The current is also sensed in the low-side MOSFET while it is conducting after a short blanking time to allow noise to settle. If the low-side overcurrent threshold is exceeded when the next incoming PWM signal is received from the controller, the device skips processing that PWM pulse. The device does not turn the high-side MOSFET on again until the low-side overcurrent threshold is no longer exceeded. If the low-side overcurrent threshold remains exceeded for 15 consecutive cycles, the device enters hiccup. There are two separate counters for the high-side and low-side overcurrent events. If the off-time is too short, the low-side overcurrent may not trip. The low-side overcurrent will, however, begin tripping after the high-side peak overcurrent limit is hit as hitting the peak current limit shortens the on-time and lengthens the off-time.

Both the high-side and low-side positive overcurrent thresholds are programmable using the MODE pin. Two sets of thresholds are available ("High" and "Low"), which are summarized in 表 7-5. The values for these thresholds are obtained using open-loop measurements with a DC current in order to accurately specify the values. In real applications, the inductor current will ramp and the ramp rate will be a function of the voltage across the inductor (V_{IN} - V_{OUT}) as well as the inductance value. This ramp rate combined with delays in the current sense circuitry can result in slightly different values than specified. The current at which the high-side overcurrent limit takes effect can be slightly higher than specified, and the current at which the low-side overcurrent limit takes effect can be slightly lower than specified.

表 7-5. Overcurrent Thresholds

MODE PIN CURRENT LIMIT SETTING	HIGH-SIDE OVERCURRENT TYPICAL VALUE (A)	LOW-SIDE OVERCURRENT TYPICAL VALUE (A)
High	12.2	10.4
Low	9.0	7.4

7.3.10.2 Negative Inductor Current Protection

Negative current is sensed in the low-side MOSFET while it is conducting after a short blanking time to allow noise to settle. Whenever the low-side negative overcurrent threshold is exceeded, the low-side MOSFET is immediately turned off. The next high-side MOSFET turnon is determined by the clock and PWM comparator. The negative overcurrent threshold minimum value is 2.95 A. Similar to the positive inductor current protections, the actual value of the inductor current when the current sense comparators trip will be a function of the current ramp rate. As a result the current at which the negative inductor current limit takes effect can be slightly more negative than specified.

7.3.11 Output Overvoltage and Undervoltage Protection

The device incorporates both output overvoltage and undervoltage protection. If an overvoltage is detected, the device tries to discharge the output voltage to a safe level before attempting to restart. When the overvoltage threshold is exceeded, the low-side MOSFET is turned on until the low-side negative overcurrent threshold is reached. At this point, the high-side MOSFET is turned on until the inductor current reaches zero. Then, the low-side MOSFET is turned back on until the low-side negative overcurrent threshold is reached. This process repeats until the output voltage falls back into the PGOOD window. Once this happens, the device restarts and goes through a soft start cycle. The device does not wait the hiccup time before restarting.

When an undervoltage condition is detected, the device will enter hiccup where it waits seven soft-start cycles before restarting. Undervoltage protection is enabled after soft start is complete.

7.3.12 Overtemperature Protection

When the die temperature exceeds 165°C, the device turns off. Once the die temperatures falls below the hysteresis level, typically 12°C, the device restarts. While waiting for the temperature to fall below the hysteresis level, the device does not switch or attempt to hiccup to restart. Once the temperature falls below this level, the device restarts without going through hiccup.

7.3.13 Output Voltage Discharge

When the device is enabled, but the high-side FET and low-side FET are disabled due to a fault condition, the output voltage discharge mode is enabled. This mode turns on the discharge FET from SW to PGND to discharge the output voltage. The discharge FET is turned off when the converter is ready to resume switching, either after the fault clears or after the wait time before hiccup is over.

The output voltage discharge mode is activated by any of below fault events:

1. High-side or low-side positive overcurrent
2. Thermal shutdown
3. Output voltage undervoltage
4. VIN UVLO

7.4 Device Functional Modes

7.4.1 Forced Continuous-Conduction Mode

The TPS543820E operates in forced continuous-conduction mode (FCCM) throughout normal operation.

7.4.2 Discontinuous Conduction Mode during Soft Start

During soft start, the converter operates in discontinuous conduction mode (DCM) during the first 16 PWM cycles. During this time, a zero-cross detect comparator is used to turn off the low-side MOSFET when the current reaches zero amps. This prevents the discharge of any pre-biased conditions on the output. After 16 cycles of DCM, the converter enters FCCM mode.

8 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

The TPS543820E is a synchronous buck regulator designed for 4-V to 18-V input and 8-A load. This procedure illustrates the design of a high-frequency switching regulator using ceramic output capacitors.

8.2 Typical Applications

8.2.1 1.0-V Output, 1-MHz Application

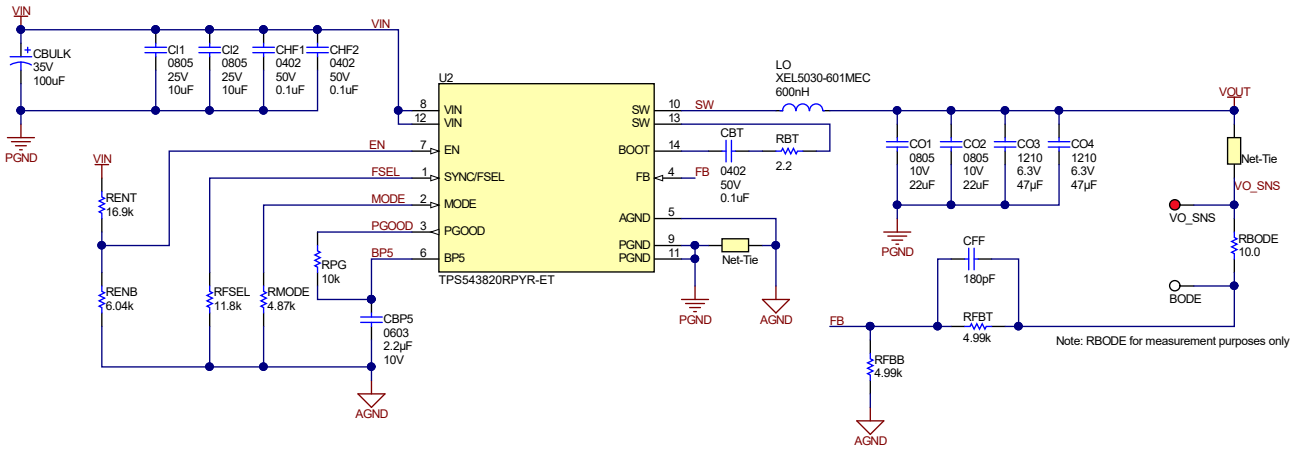


图 8-1. 12-V Input, 1.0-V Output, 1-MHz Schematic

8.2.1.1 Design Requirements

For this design example, use the parameters shown in 表 8-1.

表 8-1. Design Parameters

PARAMETER	EXAMPLE VALUE
Input voltage range (V_{IN})	4.5 to 13.2 V, 12 V nominal
Output voltage (V_{OUT})	1.0 V
Output current rating (I_{OUT})	8 A
Switching frequency (f_{SW})	1000 kHz
Steady state output ripple voltage	10 mV
Output current load step	3 A
Transient response	± 30 mV (± 3%)

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Switching Frequency

The first step is to decide on a switching frequency. The TPS543820E can operate at five different frequencies from 500 kHz to 2.2 MHz. The f_{SW} is set by the resistor value from the FSEL pin to ground. Typically the highest switching frequency possible is desired because it produces the smallest solution size. A high switching frequency allows for smaller inductors and output capacitors compared to a power supply that switches at a lower frequency. The main tradeoff made with selecting a higher switching frequency is extra switching power loss, which hurts the efficiency of the regulator.

The maximum switching frequency for a given application can be limited by the minimum on-time of the regulator. The maximum f_{SW} can be estimated with 方程式 4. Using the maximum minimum on-time of 40 ns and 13.2-V maximum input voltage for this application, the maximum switching frequency is 1890 kHz. The selected switching frequency must also consider the tolerance of the switching frequency. A switching frequency of 1000 kHz was selected for a good balance of solution size and efficiency. To set the frequency to 1000 kHz, the selected FSEL resistor is 11.8 kΩ per 表 7-1.

$$f_{SW}(max) = \frac{1}{t_{on\,min}} \times \frac{V_{OUT}}{V_{IN}(max)} \tag{4}$$

图 8-2 shows the maximum recommended input voltage versus output voltage for each FSEL frequency. This graph uses a minimum on-time of 45 ns and includes the 10% tolerance of the switching frequency. A minimum on-time of 45 ns is used in this graph to provide margin to the minimum controllable on-time to ensure pulses are not skipped at no load. At light loads, the dead-time between the low-side MOSFET turning off and high-side MOSFET turning on contributes to the minimum SW node pulse-width.

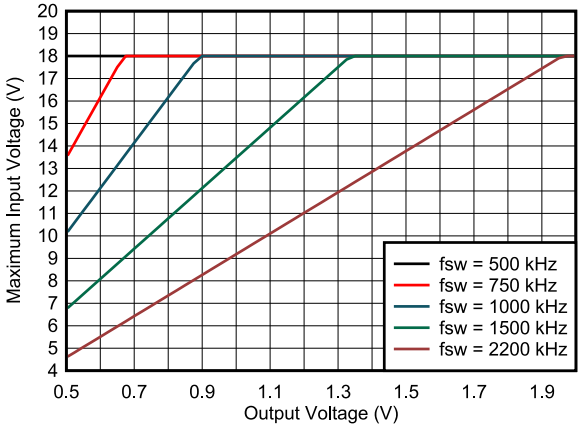


图 8-2. Maximum Input Voltage vs Output Voltage

In high output voltage applications, the minimum off-time must also be considered when selecting the switching frequency. When hitting the minimum off-time limits, the operating duty cycle will max out and the output voltage will begin to drop with the input voltage. 方程式 5 calculates the maximum switching frequency to avoid this limit. This equation requires the DC resistance of the inductor, R_{DCR}, selected in the following step. A preliminary estimate of 10 mΩ can be used but this should be recalculated based on the specifications of the inductor selected. If operating near the maximum f_{SW} limited by the minimum off-time, the increase in resistance at higher temperature must be considered.

$$f_{SW}(max) = \frac{V_{IN}(min) - V_{OUT} - I_{OUT}(max) \times \left(R_{DCR} + R_{DS(ON)\_HS}\right)}{t_{OFF\_MIN}(max) \times \left(V_{IN}(min) - I_{OUT}(max) \times \left(R_{DS(ON)\_HS} - R_{DS(ON)\_LS}\right)\right)} \tag{5}$$

8.2.1.2.2 Output Inductor Selection

To calculate the value of the output inductor, use 方程式 6. K_{IND} is a ratio that represents the amount of inductor ripple current relative to the maximum output current. The inductor ripple current is filtered by the output capacitor. Therefore, choosing high inductor ripple currents impacts the selection of the output capacitor since the output capacitor must have a ripple current rating equal to or greater than the inductor ripple current. Choosing small inductor ripple currents can degrade the transient response performance. The inductor ripple, K_{IND}, is normally from 0.1 to 0.4 for the majority of applications giving a peak to peak ripple current range of 0.8 A to 3.2 A. The recommended minimum target Iripple is 0.6 A or larger.

For this design example, K_{IND} = 0.2 is used and the inductor value is calculated to be 0.58 µH. An inductor with an inductance of 0.6 µH is selected. It is important that the RMS (Root Mean Square) current and saturation current ratings of the inductor not be exceeded. The RMS and peak inductor current can be found from 方程式 8 and 方程式 9. For this design, the RMS inductor current is 8 A, and the peak inductor current is 8.8 A. The chosen inductor is a XEL5030-601. It has a saturation current rating of 22 A, an RMS current rating of 21.4 A, and a typical DC series resistance of 4.44 mΩ.

The peak current through the inductor is the inductor ripple current plus the output current. During power up, faults, or transient load conditions, the inductor current can increase above the calculated peak inductor current level calculated in 方程式 9. In transient conditions, the inductor current can increase up to the switch current limit of the device. For this reason, the most conservative approach is to specify the current ratings of the inductor based on the switch current limit rather than the steady-state peak inductor current.

$$L1 = \frac{Vinmax - Vout}{Io \times Kind} \times \frac{Vout}{Vinmax \times fsw} \tag{6}$$

$$Iripple = \frac{Vinmax - Vout}{L1} \times \frac{Vout}{Vinmax \times fsw} \tag{7}$$

$$ILrms = \sqrt{Io^2 + \frac{1}{12} \times \left(\frac{Vo \times (Vinmax - Vo)}{Vinmax \times L1 \times fsw}\right)^2} \tag{8}$$

$$ILpeak = Iout + \frac{Iripple}{2} \tag{9}$$

表 8-2 shows recommended E6 standard inductor values for other common output voltages with a 1-MHz f_{SW}. Using an inductance outside this recommended range typically works but the performance can be affected and should be evaluated. The recommended value is calculated for a nominal input voltage of 12 V. The minimum values are calculated with the maximum input voltage of 18 V. The maximum values are calculated with with an input voltage of 5-V for all but the 5-V output. For the 5-V output, an 8-V input is used.

表 8-2. Recommended Inductor Values

OUTPUT VOLTAGE (V)	SWITCHING FREQUENCY (kHz)	MINIMUM INDUCTANCE (µH)	RECOMMENDED INDUCTANCE FOR 8 A (µH)	RECOMMENDED INDUCTANCE FOR 6 A (µH)	MAXIMUM INDUCTANCE (µH)
1	1000	0.33	0.47	0.47	1
1.8		0.47	0.68	1	1.5
3.3		0.68	1	1.5	1.5
5		1	1.5	1.5	2.2

8.2.1.2.3 Output Capacitor

There are two primary considerations for selecting the value of the output capacitor: the output voltage ripple and how the regulator responds to a large change in load current. The output capacitance needs to be selected based on the more stringent of these criteria.

The desired response to a large change in the load current is the first criteria and is typically the most stringent. A regulator does not respond immediately to a large, fast increase or decrease in load current. The output capacitor supplies or absorbs charge until the regulator responds to the load step. The control loop needs to sense the change in the output voltage then adjust the peak switch current in response to the change in load. The minimum output capacitance is selected based on an estimate of the loop bandwidth. Typically the loop bandwidth is near f_{SW} / 10. 方程式 10 estimates the minimum output capacitance necessary, where ΔI_{OUT} is the change in output current and ΔV_{OUT} is the allowable change in the output voltage.

For this example, the transient load response is specified as a 3% change in V_{OUT} for a load step of 3 A. Therefore, ΔI_{OUT} is 3 A and ΔV_{OUT} is 30 mV. Using this target gives a minimum capacitance of 159 µF. This value does not take the ESR of the output capacitor into account in the output voltage change. For ceramic capacitors, the effect of the ESR can be small enough to be ignored. Aluminum electrolytic and tantalum capacitors have higher ESR that must be considered for load step response.

$$C_{OUT} > \frac{\Delta I_{OUT}}{\Delta V_{OUT}} \times \frac{1}{2\pi \times \frac{f_{SW}}{10}} \tag{10}$$

In addition to the loop bandwidth, it is possible for the inductor current slew rate to limit how quickly the regulator responds to the load step. For low duty cycle applications, the time it takes for the inductor current to ramp down after a load step down can be the limiting factor. 方程式 11 estimates the minimum output capacitance necessary to limit the change in the output voltage after a load step down. Using the 0.6-µH inductance selected gives a minimum capacitance of 90 µF.

$$C_{OUT} > \frac{L_{OUT} \times \Delta I_{OUT}^2}{2 \times \Delta V_{OUT} \times V_{OUT}} \tag{11}$$

方程式 12 calculates the minimum output capacitance needed to meet the output voltage ripple specification. In this case, the target maximum steady state output voltage ripple is 10 mV. Under this requirement, 方程式 12 yields 19 µF.

$$Co > \frac{1}{8 \times fsw} \times \frac{1}{\frac{Voripple}{Iripple}} \tag{12}$$

where

- ΔI_{OUT} is the change in output current
- ΔV_{OUT} is the allowable change in the output voltage

- *f*sw is the regulators switching frequency
- Voripple is the maximum allowable steady state output voltage ripple
- Iripple is the inductor ripple current

Lastly, if an application does not have a strict load transient response or output ripple requirement, a minimum amount of capacitance is still required to ensure the control loop is stable with the lowest gain ramp setting on the MODE pin. 方程式 13 estimates the minimum capacitance needed for loop stability. This equation sets the minimum amount of capacitance by keeping the LC frequency relative to the switching frequency at a minimum value. See 图 8-3 for the limit versus output voltage with the lowest gain ramp setting of 1 pF. With a 1-V output, the minimum ratio is 35 and with this ratio, 方程式 13 gives a minimum capacitance of 52 µF.

$$C_{OUT} > \left(\frac{Ratio}{2\pi \times f_{SW}}\right)^2 \times \frac{1}{L_{OUT}} \tag{13}$$

方程式 14 calculates the maximum combined ESR the output capacitors can have to meet the output voltage ripple specification and this shows the ESR should be less than 6 mΩ. In this case, ceramic capacitors are used and the combined ESR of the ceramic capacitors in parallel is much less than is needed to meet the ripple. Capacitors also have limits to the amount of ripple current they can handle without producing excess heat and failing. An output capacitor that can support the inductor ripple current must be specified. The capacitor data sheet specifies the RMS value of the maximum ripple current. 方程式 15 can be used to calculate the RMS ripple current the output capacitor needs to support. For this application, 方程式 15 yields 445 mA and ceramic capacitors typically have a ripple current rating much higher than this.

$$Resr < \frac{Voripple}{Iripple} \tag{14}$$

$$Icorms = \frac{Vout \times (Vinmax - Vout)}{\sqrt{12} \times Vinmax \times L1 \times fsw} \tag{15}$$

Select X5R and X7R ceramic dielectrics or equivalent for power regulator capacitors since they have a high capacitance-to-volume ratio and are fairly stable over temperature. The output capacitor must also be selected with the DC bias and AC voltage derating taken into account. The derated capacitance value of a ceramic capacitor due to DC voltage bias and AC RMS voltage is usually found on the capacitor manufacturer's website. For this application example, two 22-µF, 10-V, X7S, 0805 and two 47-µF, 6.3-V, X7R, 1210 ceramic capacitors each with 2 mΩ of ESR are used. The two 22-µF capacitors are used since they have a higher resonance frequency and can help reduce the output ripple caused by parasitic inductance. With the four parallel capacitors, the estimated effective output capacitance after derating using the capacitor manufacturer's website is 142 µF. There is almost no DC bias derating at 1 V. This design was able to use less than the calculated minimum because the loop crossover frequency was above the f_{SW} / 10 estimate as shown in the Load Transient graph in the *Application Curves*.

8.2.1.2.4 Input Capacitor

Input decoupling ceramic capacitors type X5R, X7R, or similar from VIN to PGND that are placed as close as possible to the IC are required. A total of at least 10 µF of capacitance is required and some applications can require a bulk capacitance. At least 1 µF of bypass capacitance is recommended as close as possible to each VIN pin to minimize the input voltage ripple. A 0.1-µF to 1-µF capacitor must be placed as close as possible to both VIN pins 8 and 12 on the same side of the board of the device to provide high frequency bypass to reduce the high frequency overshoot and undershoot on VIN and SW pins. The voltage rating of the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple current rating greater than the maximum RMS input current. The RMS input current can be calculated using 方程式 16.

For this example design, a ceramic capacitor with at least a 16-V voltage rating is required to support the maximum input voltage. Two 10-µF, 0805, X7S, 25-V and two 0.1-µF, 0402, X7R 50-V capacitors in parallel have been selected to be placed on both sides of the IC near both VIN pins to PGND pins. Based on the capacitor manufacturer's website, the total ceramic input capacitance derates to 5.4 µF at the nominal input voltage of 12 V. A 100-µF bulk capacitance is also used to bypass long leads when connected a lab bench top power supply.

The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using 方程式 17. The maximum input ripple occurs when operating nearest to 50% duty cycle. Using the nominal design example values of Ioutmax = 8 A, C_{IN} = 5.4 µF, and f_{SW} = 1000 kHz, the input voltage ripple with the 12 V nominal input is 113 mV and the RMS input ripple current with the 4.5 V minimum input is 3.3 A.

$$Icirms = Iout \times \sqrt{\frac{Vout}{Vinmin} \times \frac{(Vinmin - Vout)}{Vinmin}} \tag{16}$$

$$\Delta Vin = \frac{Ioutmax \times \left(1 - \frac{Vout}{Vin}\right) \times \frac{Vout}{Vin}}{Cin \times f_{SW}} \tag{17}$$

8.2.1.2.5 Adjustable Undervoltage Lockout

The undervoltage lockout (UVLO) is adjusted using the external voltage divider network of R_{ENT} and R_{ENB}. The UVLO has two thresholds: one for power up when the input voltage is rising and one for power down or brownouts when the input voltage is falling. For the example design, the supply is set to turn on and start switching once the input voltage increases above 4.5 V (UVLO start or enable). After the regulator starts switching, it continues to do so until the input voltage falls below 3.95 V (UVLO stop or disable). In this example, these start and stop voltages set by the EN resistor divider were selected to have more hysteresis than the internally fixed VIN UVLO.

方程式 1 and 方程式 2 can be used to calculate the values for the upper and lower resistor values. For these equations to work, V_{START} must be 1.1 × V_{STOP} due to the EN pin's voltage hysteresis. For the voltages specified, the standard resistor value used for R_{ENT} is 16.9 kΩ and for R_{ENB} is 6.04 kΩ.

8.2.1.2.6 Output Voltage Resistors Selection

The output voltage is set with a resistor divider created by R_{FBT} and R_{FBB} from the output node to the FB pin. It is recommended to use 1% tolerance or better resistors. For this example design, 4.99 kΩ was selected for R_{FBB}. Using 方程式 18, R_{FBT} is calculated as 4.99 kΩ. This is a standard 1% resistor.

$$R_{FBT} = R_{FBB} \times \left(\frac{V_{OUT}}{V_{REF}} - 1 \right) \tag{18}$$

If the PCB layout does not use the recommended AGND to PGND connection in 节 *10.1*, noise on the feedback pin can degrade the output voltage regulation at max load. Use a smaller R_{FBB} of 1.00 kΩ minimizes the impact of this noise.

8.2.1.2.7 Bootstrap Capacitor Selection

A 0.1-µF ceramic capacitor must be connected between the BOOT and SW pins for proper operation. The capacitor must be rated for at least 10-V to minimize DC bias derating.

A resistor must be added in series with the BOOT capacitor to slow down the turnon of the high-side MOSFET and rising edge overshoot on the SW pin for applications with input voltage greater than 13.5 V. This comes with the trade off of more power loss and lower efficiency. As a best prectice, include a 0-Ω placeholder in all prototype designs in case parasitic inductance in the PCB layout results in more voltage overshoot at the SW pin than is normal. This helps keep the voltage within the ratings of the device and reduces the high frequency noise on the SW node. The recommended BOOT resistor value to decrease the SW pin overshoot is 2.2 Ω.

8.2.1.2.8 BP5 Capacitor Selection

A 2.2-µF ceramic capacitor must be connected between the BP5 pin and AGND for proper operation. The capacitor must be rated for at least 10 V to minimize DC bias derating.

8.2.1.2.9 PGOOD Pullup Resistor

A 10-kΩ resistor is used to pull up the power good signal when FB conditions are met. The pullup voltage source must be less than the 6-V absolute maximum of the PGOOD pin.

8.2.1.2.10 Current Limit Selection

The MODE pin is used to select between two current limit settings. Select the current limit setting whose minimum is greater than at least 1.1 times the maximum steady state peak current. This is to provide margin for component tolerance and load transients. For this design, the minimum current limit should be greater than 9.64 A so the high current limit setting is selected.

8.2.1.2.11 Soft-Start Time Selection

The MODE pin is used to select between four different soft-start times. This is useful if a load has specific timing requirements for the output voltage of the regulator. A longer soft-start time is also useful if the output capacitance is very large and would require large amounts of current to quickly charge the output capacitors to the output voltage level. The large currents necessary to charge the capacitor can reach the current limit or cause the input voltage rail to sag due excessive current draw from the input power supply. Limiting the output voltage slew rate solves both of these problems. The example design has the soft-start time set to 1.0 ms. With this soft-start time the current required to charge the output capacitors to the nominal output voltage is only 0.14 A.

8.2.1.2.12 Ramp Selection and Control Loop Stability

The MODE pin is used to select between three different ramp settings. The most optimal ramp setting depends on V_{OUT}, f_{SW}, L_{OUT}, and C_{OUT}. To get started, calculate LC double pole frequency using 方程式 19. The ratio between f_{SW} and f_{LC} should then be calculated. Based on this ratio and the output voltage, the recommended ramp setting should be selected using 图 8-3. With a 1-V output, the 1-pF ramp is recommended for ratios between approximately 35 and 58, the 2-pF ramp is recommended for ratios between approximately 58 and 86, and the 4-pF ramp is recommended for ratios greater than approximately 86. In general, it is best to use the largest ramp capacitor the design will support. Increasing the ramp capacitor improves transient response but can reduce stability margin or increase on-time jitter.

For this design, f_{LC} is 17.5 kHz and the ratio is 57 which is on the border of the 1-pF and 2-pF ramp settings. Through bench evaluation, it was found that the design had sufficient stability margin with the 2-pF ramp so this setting was selected for the best transient response. The recommended ramp settings given by 图 8-3 include margin to account for potential component tolerances and variations across operating conditions so it is possible to use a higher ramp setting as shown in this example.

$$f_{LC} = \frac{1}{2 \times \pi \times \sqrt{L_{OUT} \times C_{OUT}}} \tag{19}$$

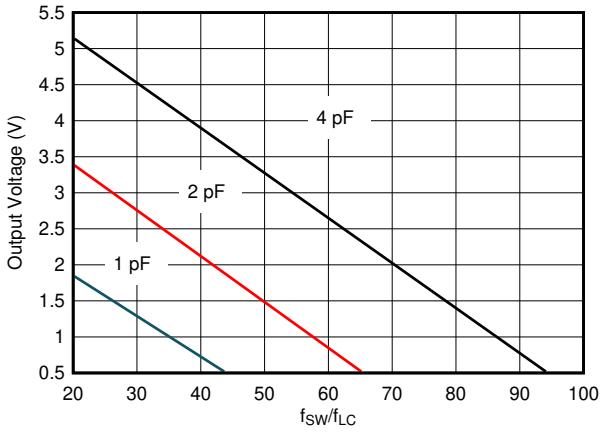


图 8-3. Recommended Ramp Settings

Use a feedforward capacitor (C_{FF}) in parallel with the upper feedback resistor (R_{FBT}) to add a zero into the control loop to provide phase boost. Include a placeholder for this capacitor as the zero it provides can be required to meet phase margin requirements. This capacitor also adds a pole at a higher frequency than the zero. The pole and zero frequency are not independent so as a result, once the zero location is chosen, the pole is fixed as well. The zero is placed at 1/4 the f_{SW} by calculating the value of C_{FF} with 方程式 20. The calculated value is 128 pF — round this down to the closest standard value of 120 pF.

Using bench measurements of the AC response, the feedforward capacitor for this example design was increased to 180 pF to improve the transient response.

$$C_{FF} = \frac{1}{\pi \times R_{FBT} \times \frac{f_{SW}}{2}} \tag{20}$$

It is possible to use larger feedforward capacitors to further improve the transient response but take care to ensure there is a minimum of -9-dB gain margin in all operating conditions. The feedforward capacitor injects noise on the output into the FB pin. This added noise can result in increased on-time jitter at the switching node. Too little gain margin can cause a repeated wide and narrow pulse behavior. Adding a 100-Ω resistor in series with the feedforward capacitor can help reduce the impact of noise on the FB pin in case of non-ideal PCB layout. The value of this resistor must be kept small as larger values bring the feedforward pole and zero closer together degrading the phase boost the feedforward capacitor provides.

When using higher ESR output capacitors, such as polymer or tantalum, their ESR zero (f_{ESR}) should be accounted for. The ESR zero can be calculated using 方程式 21. If the ESR zero frequency is less than the estimated bandwidth of 1/10th the f_{SW}, it can affect the gain margin and phase margin. A series R-C from the FB pin to ground can be used to add a pole into the control loop if necessary. All ceramic capacitors are used in this design so the effect of the ESR zero is ignored.

$$f_{ESR} = \frac{1}{2 \times \pi \times C_{OUT} \times R_{ESR}} \tag{21}$$

8.2.1.2.13 MODE Pin

The MODE resistor is set to 4.87 kΩ to select the high current limit setting, 1.0-ms soft-start and the 2 pF ramp. See 表 7-4 for the full list of the MODE pin settings.

8.2.1.3 Application Curves

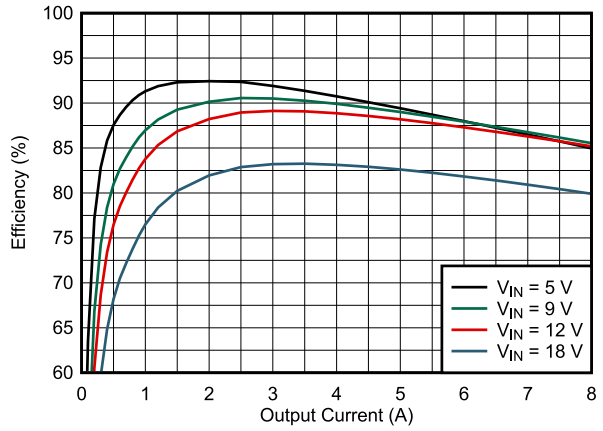


图 8-4. Efficiency

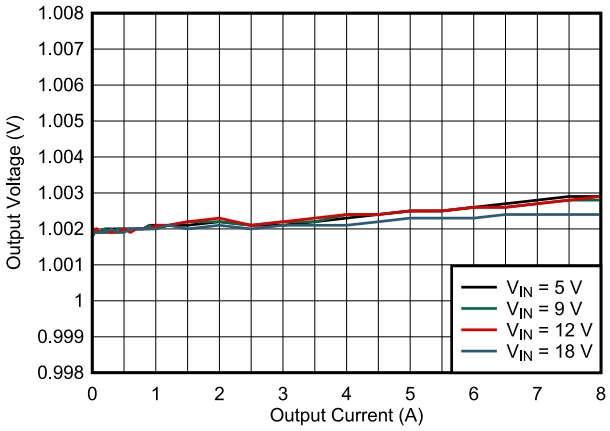


图 8-5. Load Regulation

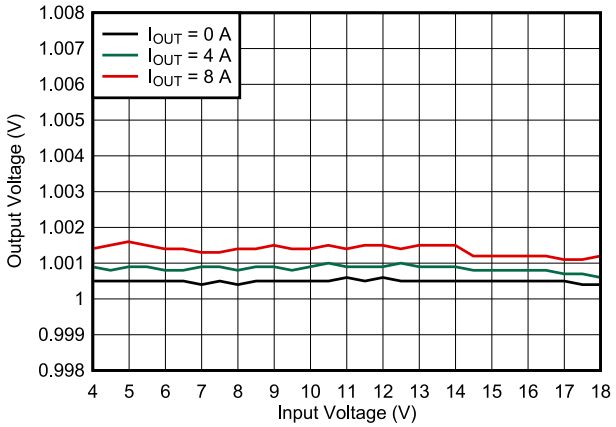
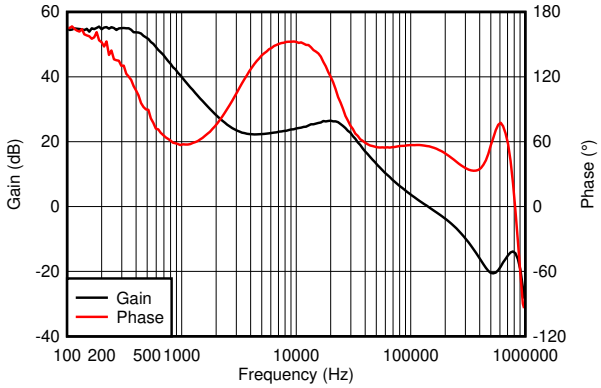
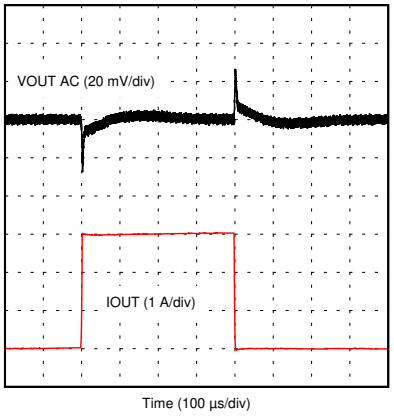


图 8-6. Line Regulation



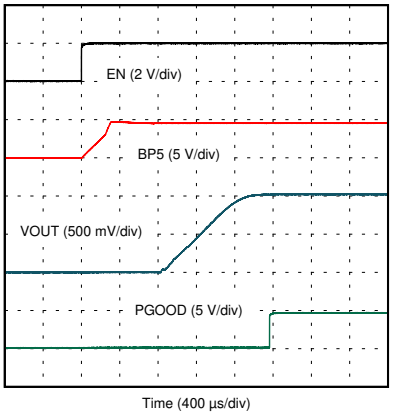
VIN = 12 V ROUT = 0.3 Ω

图 8-7. Bode Plot



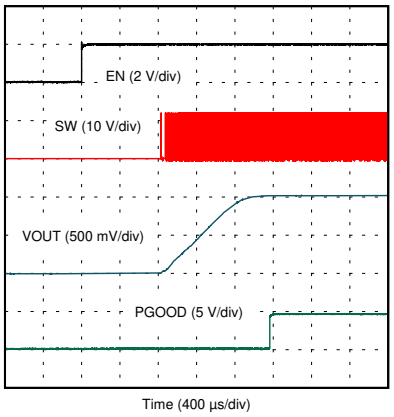
VIN = 12 V IOUT(DC) = 1.5 A ISTEP = 3 A at 1A/µs

图 8-8. Load Transient



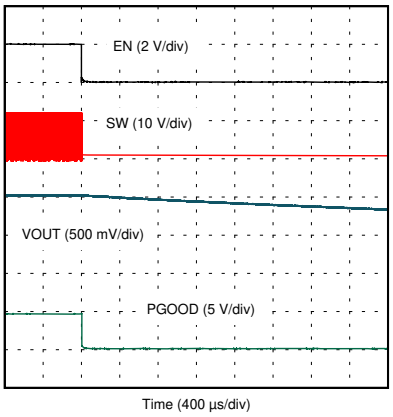
VIN = 12 V IOUT = 0 A

图 8-9. EN Start-up – Measuring BP5



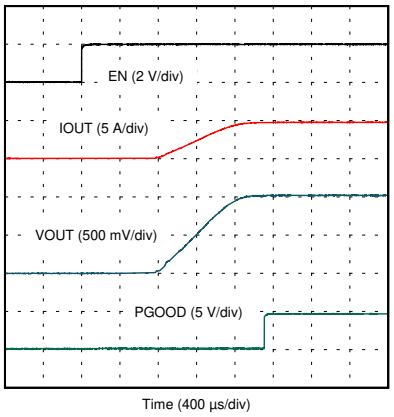
V_{IN} = 12 V I_{OUT} = 0 A

图 8-10. EN Startup – Measuring SW



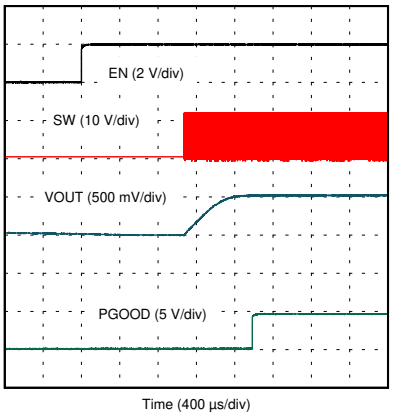
V_{IN} = 12 V I_{OUT} = 0 A

图 8-11. EN Shutdown



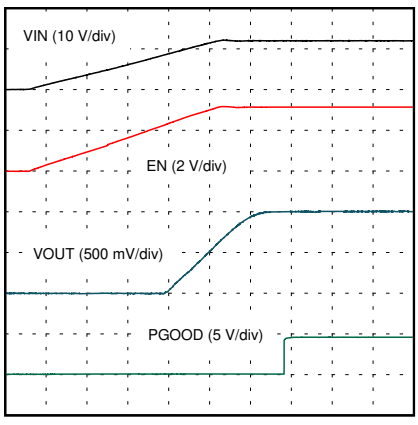
V_{IN} = 12 V R_{OUT} = 0.2 Ω

图 8-12. EN Start-up – With Load



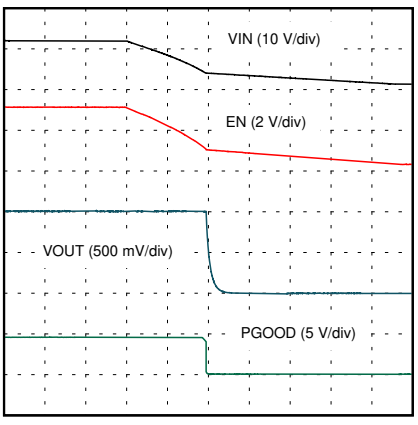
V_{IN} = 12 V I_{OUT} = 0 A

图 8-13. EN Start-up – 0.5-V Prebias



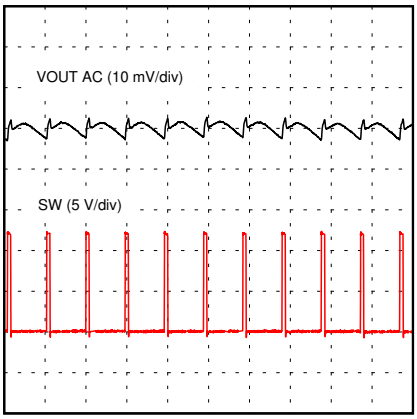
R_{OUT} = 0.3 Ω

图 8-14. VIN Start-up



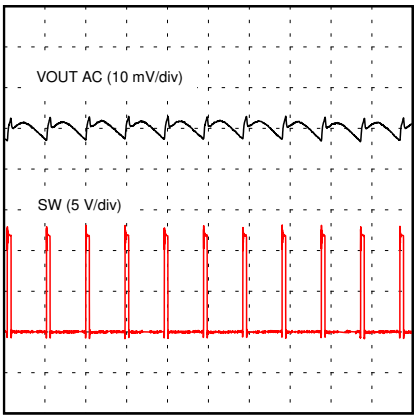
R_{OUT} = 0.3 Ω

图 8-15. VIN Shutdown



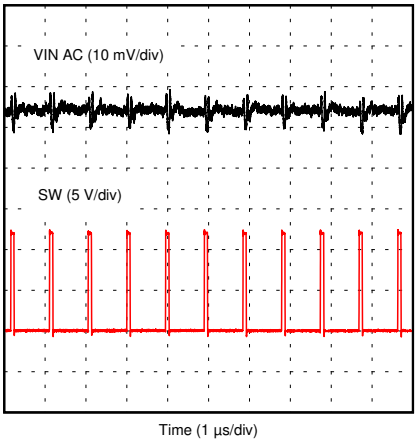
V_{IN} = 12 V I_{OUT} = 0 A

图 8-16. Output Ripple – No Load



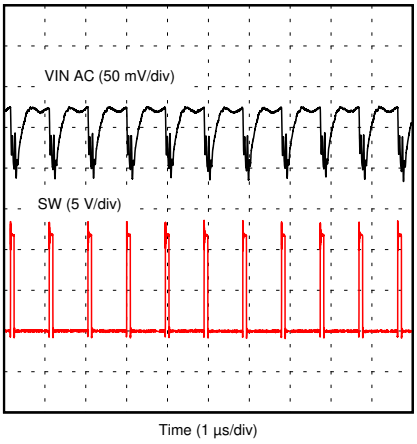
V_{IN} = 12 V I_{OUT} = 6 A

图 8-17. Output Ripple – 6-A Load



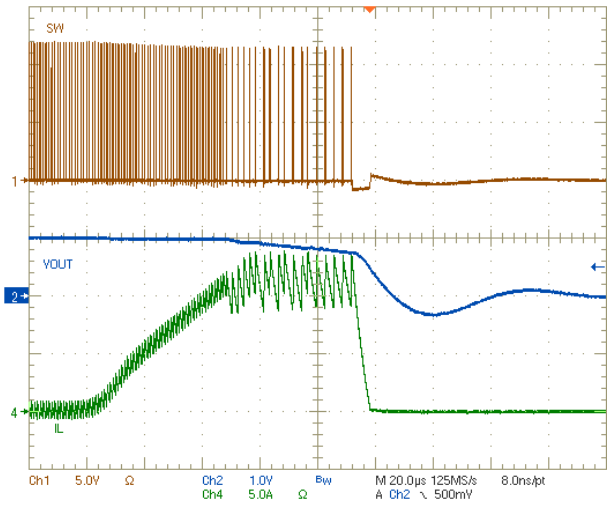
V_{IN} = 12 V I_{OUT} = 0 A

图 8-18. Input Ripple – No Load



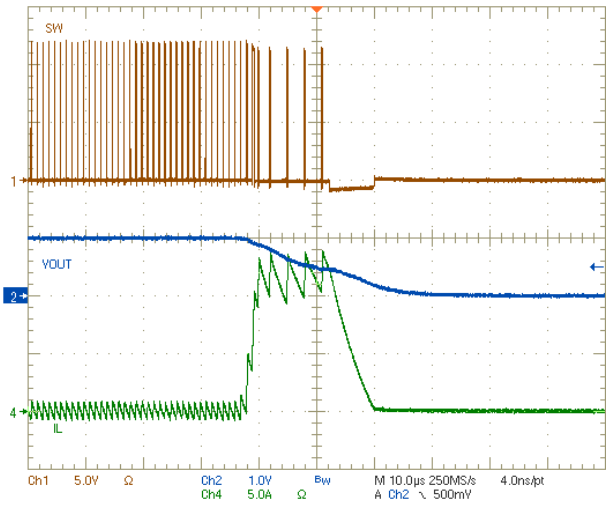
V_{IN} = 12 V I_{OUT} = 6 A

图 8-19. Input Ripple – 6-A Load



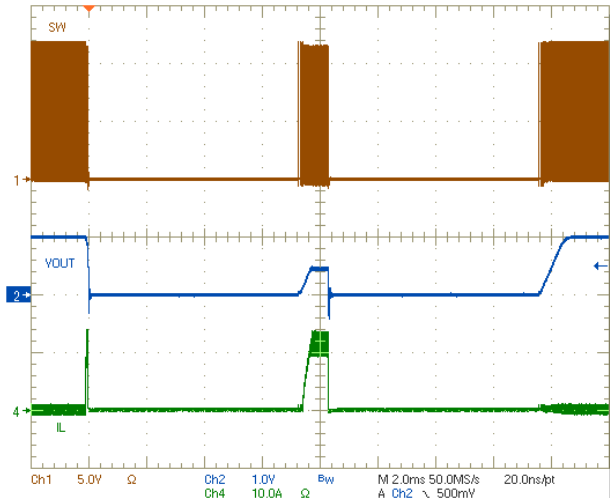
V_{IN} = 12 V

图 8-20. Overcurrent Protection – Overload



V_{IN} = 12 V

图 8-21. Overcurrent Protection – Short



V_{IN} = 12 V

图 8-22. Overcurrent Protection – Hiccup and Recover

8.2.2 1.0-V Output, 1.5-MHz Application

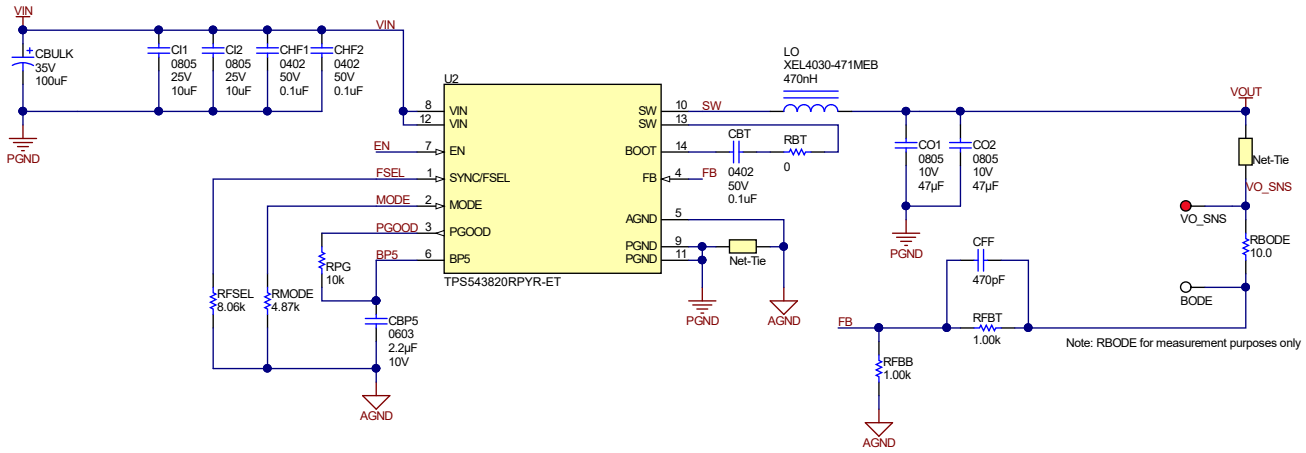


图 8-23. 12-V Input, 1.0-V Output, 1.5-MHz Schematic

8.2.2.1 Design Requirements

表 8-3. Design Parameters

PARAMETER	EXAMPLE VALUE
Input voltage range (V_{IN})	4 to 13.2 V, 12 V nominal
Output voltage (V_{OUT})	1.0 V
Output current rating (I_{OUT})	8 A
Switching frequency (f_{SW})	1500 kHz
Steady state output ripple voltage	10 mV
Output current load step	3 A
Transient response	± 30 mV (± 3%)

8.2.2.2 Detailed Design Procedure

Follow the design procedure in 节 *8.2.1.2* for selecting the external components in this example application.

8.2.2.3 Application Curves

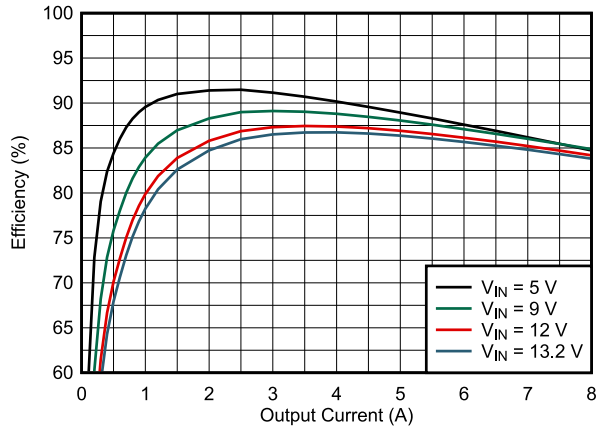
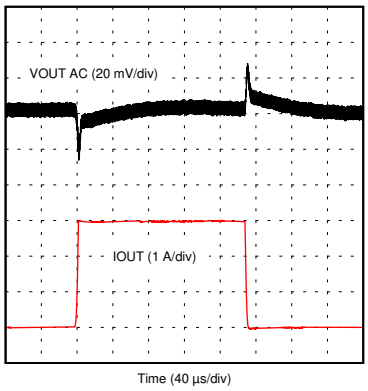


图 8-24. Efficiency



V_{IN} = 12 V $I_{OUT(DC)}$ = 1.5 A I_{STEP} = 3 A at 1A/µs

图 8-25. Load Transient

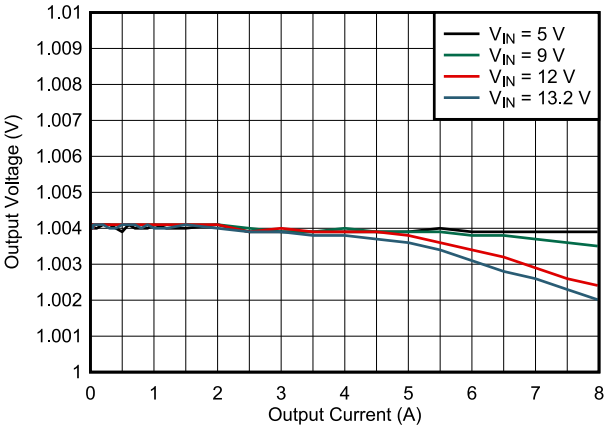
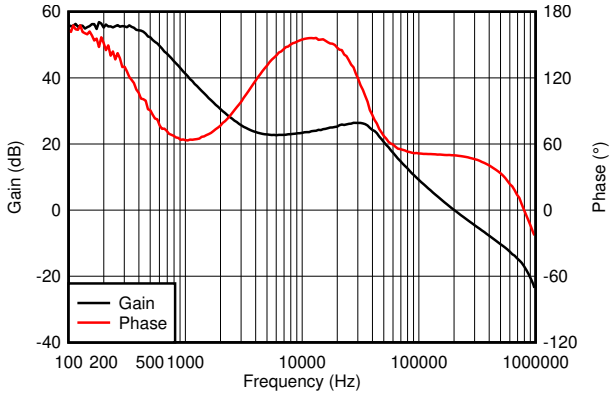
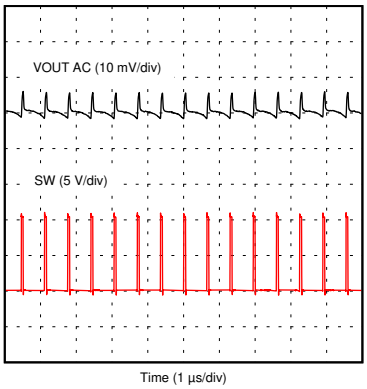


图 8-26. Load Regulation



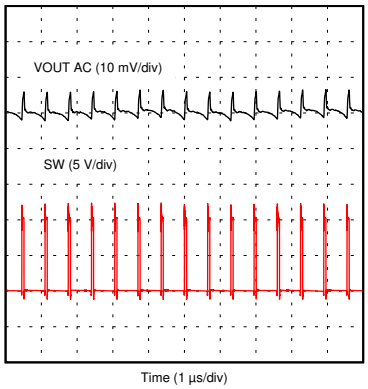
V_{IN} = 12 V R_{OUT} = 0.3 Ω

图 8-27. Bode Plot



V_{IN} = 12 V I_{OUT} = 0 A

图 8-28. Output Ripple – No Load



V_{IN} = 12 V I_{OUT} = 6 A

图 8-29. Output Ripple – 6-A Load

8.2.3 3.3-V Output, 1.0-MHz Application

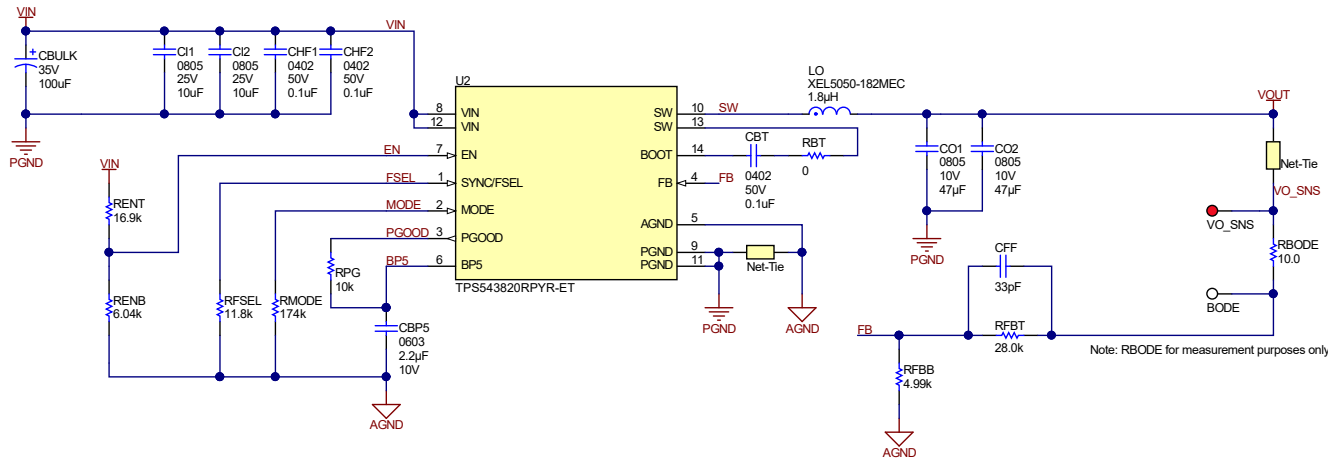


图 8-30. 12-V Input, 3.3-V Output, 1.0-MHz Schematic

8.2.3.1 Design Requirements

For this design example, use the parameters shown in 表 8-4.

表 8-4. Design Parameters

PARAMETER	EXAMPLE VALUE
Input voltage range (V_{IN})	4 to 13.2 V, 12 V nominal
Output voltage (V_{OUT})	3.3 V
Output current rating (I_{OUT})	6 A
Switching frequency (f_{SW})	1000 kHz
Steady state output ripple voltage	10 mV
Output current load step	3 A
Transient response	± 99 mV (± 3%)

8.2.3.2 Detailed Design Procedure

Follow the design procedure in 节 8.2.1.2 for selecting the external components in this example application.

8.2.3.3 Application Curves

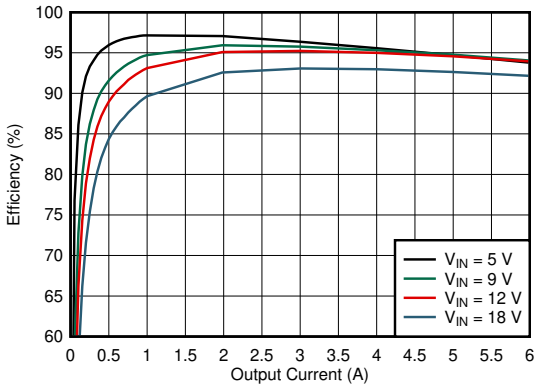
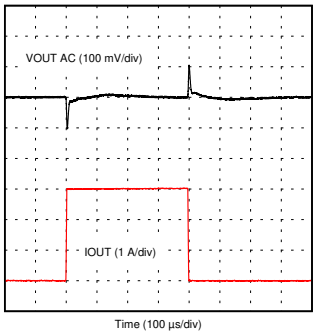


图 8-31. Efficiency



V_{IN} = 12 V $I_{OUT(DC)}$ = 1.5 A I_{STEP} = 3 A at 1A/µs

图 8-32. Load Transient

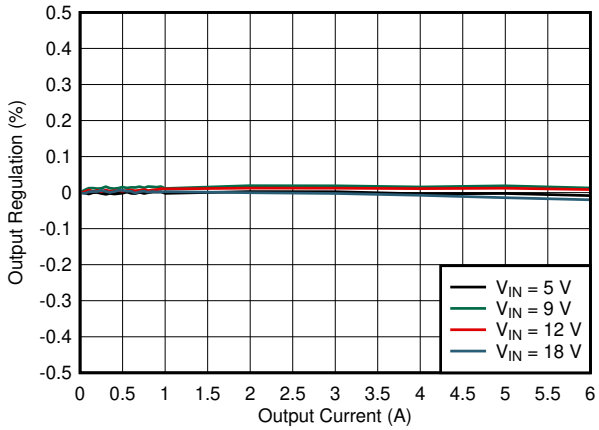
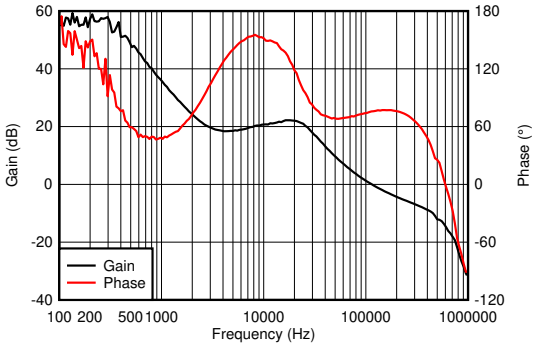
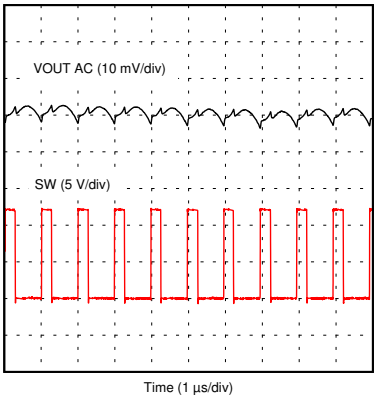


图 8-33. Load Regulation



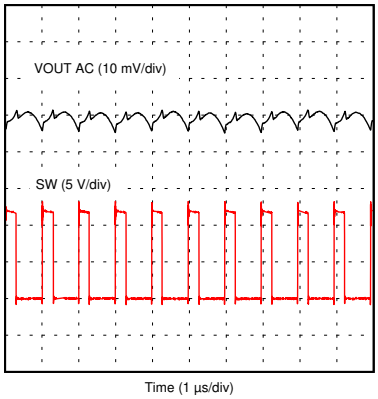
V_{IN} = 12 V R_{OUT} = 1.1 Ω

图 8-34. Bode Plot



V_{IN} = 12 V I_{OUT} = 0 A

图 8-35. Output Ripple – No Load



V_{IN} = 12 V I_{OUT} = 6 A

图 8-36. Output Ripple – 6-A Load

9 Power Supply Recommendations

The TPS543820E is designed to operate from an input voltage supply range between 4 V and 18 V. This supply voltage must be well regulated. Proper bypassing of the input supply is critical for proper electrical performance, as is the PCB layout and the grounding scheme. A minimum of 4 µF (after derating) ceramic capacitance, type X5R or better, must be placed near the device. TI recommends splitting the ceramic input capacitance equally between the VIN and PGND pins on each side of the device resulting in at least 2 µF of ceramic capacitance on each side of the device.

10 Layout

10.1 Layout Guidelines

Layout is a critical portion of good power supply design. See 图 10-1 for a PCB layout example. Key guidelines to follow for the layout are:

- VIN, PGND, and SW traces must be as wide as possible to reduce trace impedance and improve heat dissipation.
- Place a 10-nF to 100-nF capacitor from each VIN to PGND pin and place them as close as possible to the device on the same side of the PCB. Place the remaining ceramic input capacitance next to these high frequency bypass capacitors. The remaining input capacitance can be placed on the other side of the board but use as many vias as possible to minimize impedance between the capacitors and the pins of the IC.
- Use multiple vias near the PGND pins and use the layer directly below the device to connect them together. This helps to minimize noise and can help heat dissipation.
- Use vias near both VIN pins and provide a low impedance connection between them through an internal layer.
- Place the inductor as close as possible to the device to minimize the length of the SW node routing.
- Place the BOOT-SW capacitor as close as possible to the BOOT and SW pins.
- Place the BP5 capacitor as close as possible to the BP5 and AGND pins.
- Place the bottom resistor in the FB divider as close as possible to the FB and AGND pins of the IC. Also keep the upper feedback resistor and the feedforward capacitor near the IC. Connect the FB divider to the output voltage at the desired point of regulation.
- Use multiple vias in the AGND island to connect it back to internal PGND layers. Do not place these vias between the BP5 capacitor and the AGND pin. These vias will conduct switching currents between the BP5 capacitor and PGND. Placing the vias near the AGND pin can add noise to the FB divider.
- Return the FSEL and MODE resistors to a quiet AGND island.

10.2 Layout Example

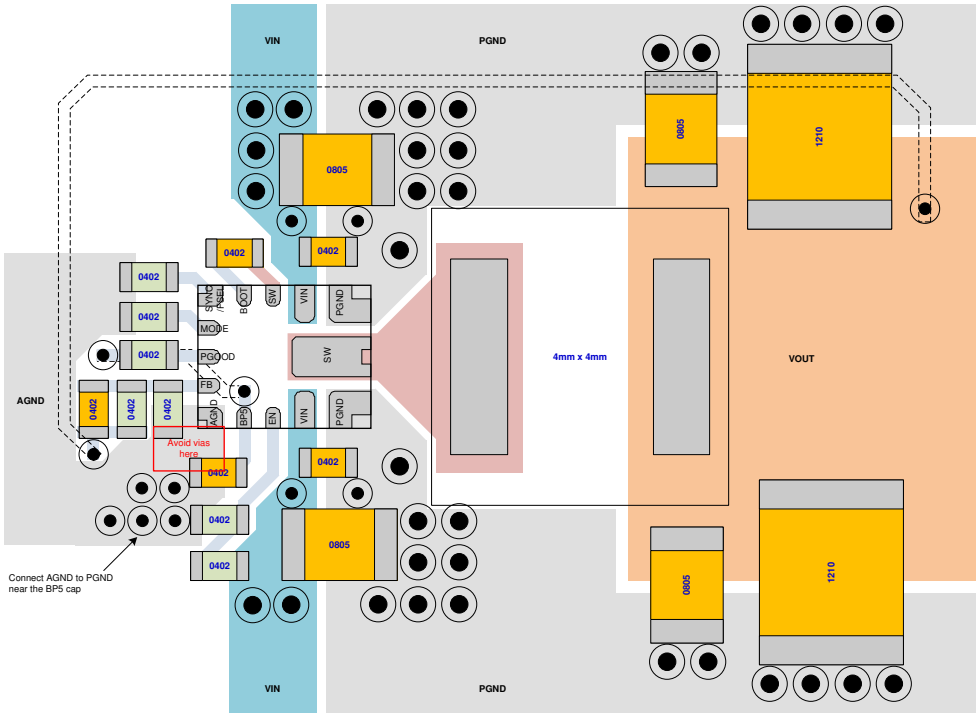


图 10-1. Example PCB Layout

10.2.1 Thermal Performance

Test Conditions: f_{SW} = 1 MHz, Vin = 12 V, Vout = 1 V, Iout = 8 A, Inductor = 600 nH (4.44 mΩ typ), Ambient temperature = 25°C

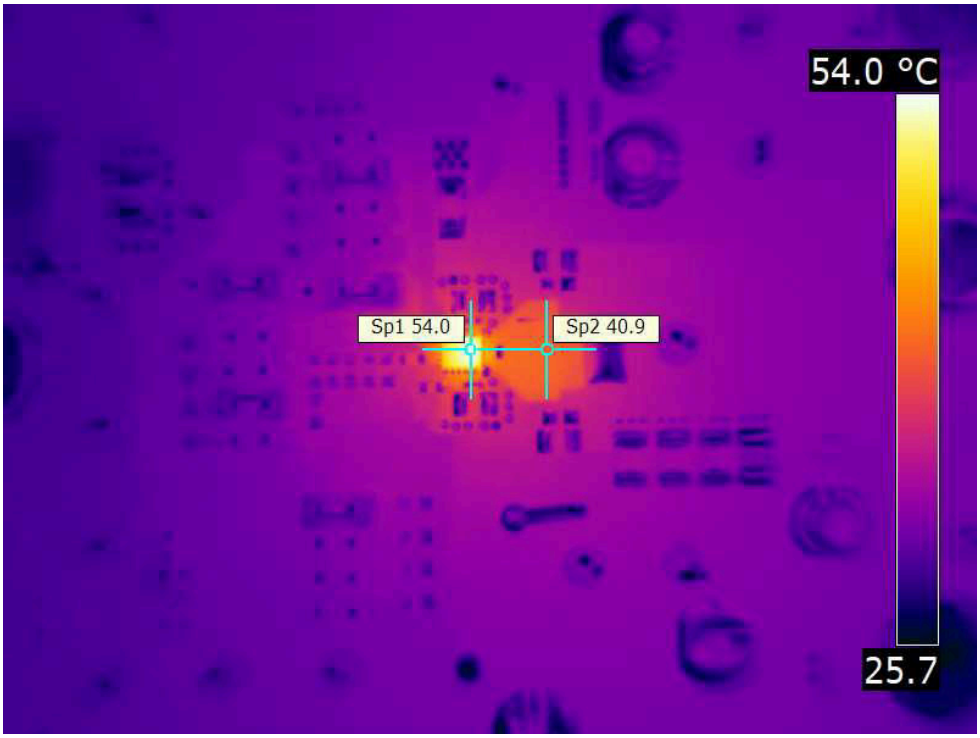


图 10-2. Thermal Image at 25°C Ambient

11 Device and Documentation Support

11.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.2 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

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静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.5 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS543820RPYR-ET	ACTIVE	VQFN-HR	RPY	14	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-55 to 150	3820ET	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

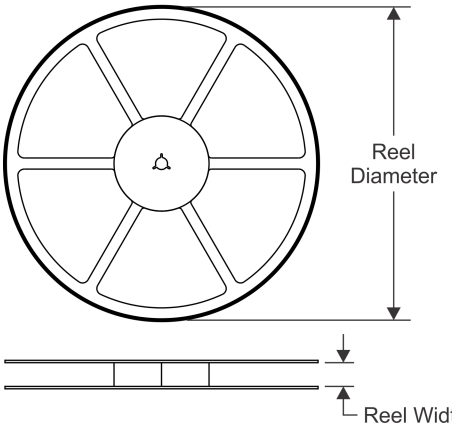
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

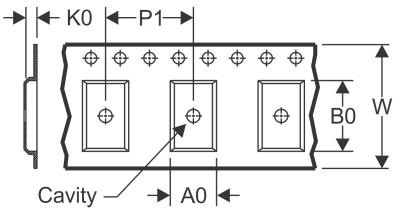
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

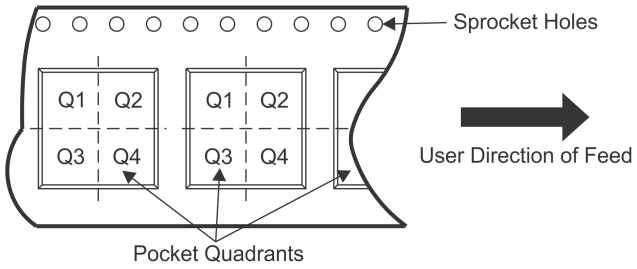


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

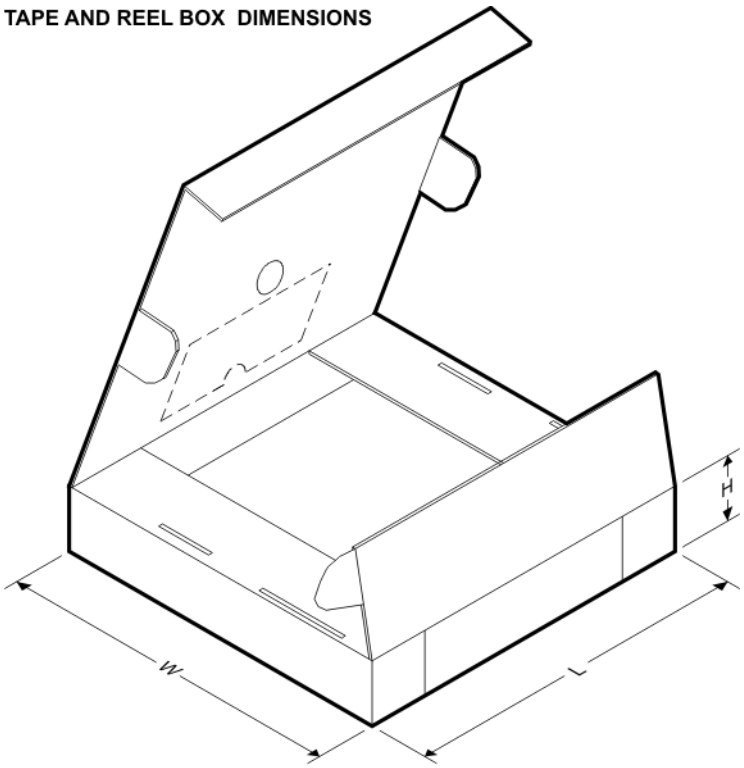
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS543820RPYR-ET	VQFN-HR	RPY	14	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

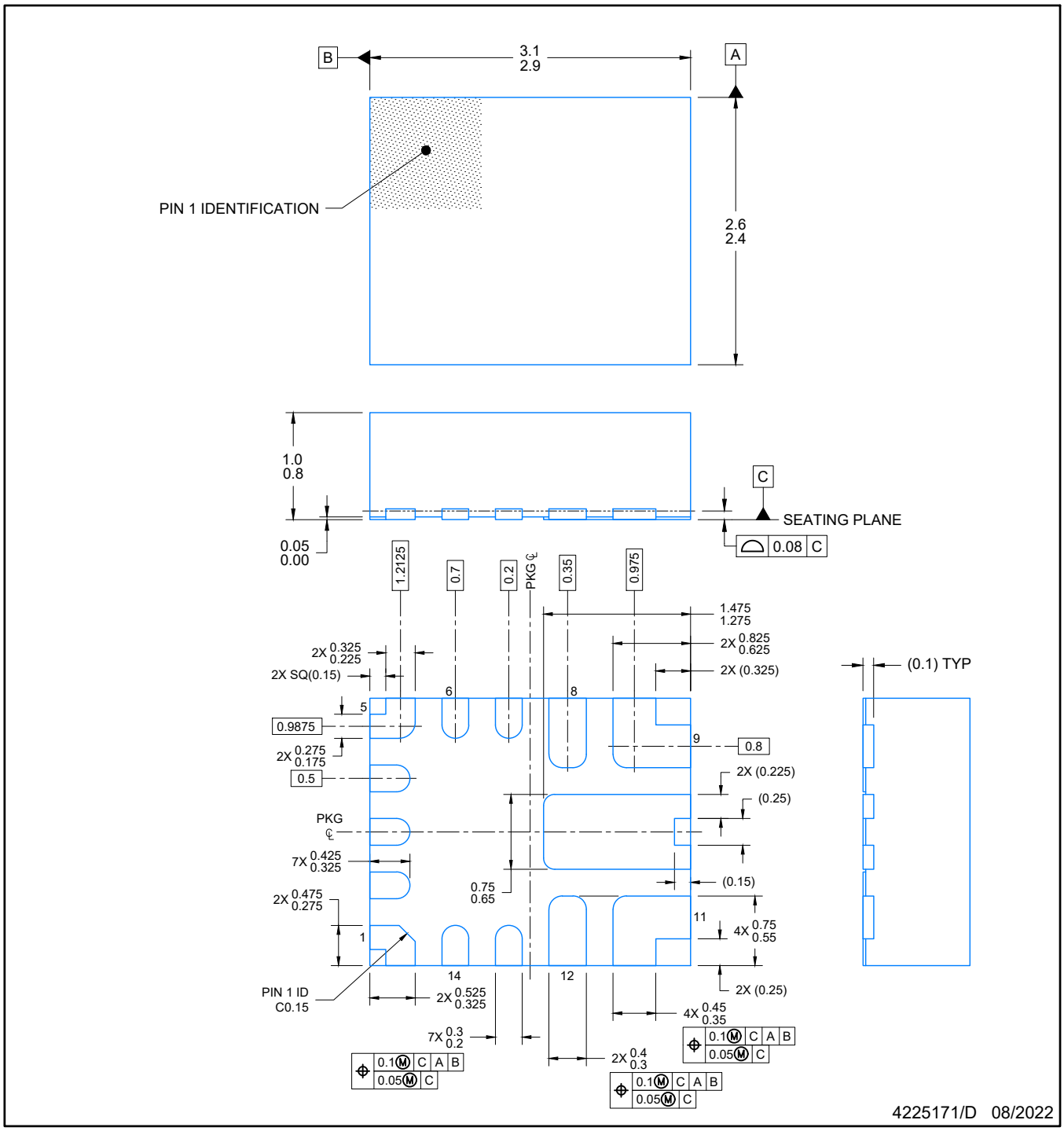
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS543820RPYR-ET	VQFN-HR	RPY	14	3000	210.0	185.0	35.0

PACKAGE OUTLINE

RPY0014A

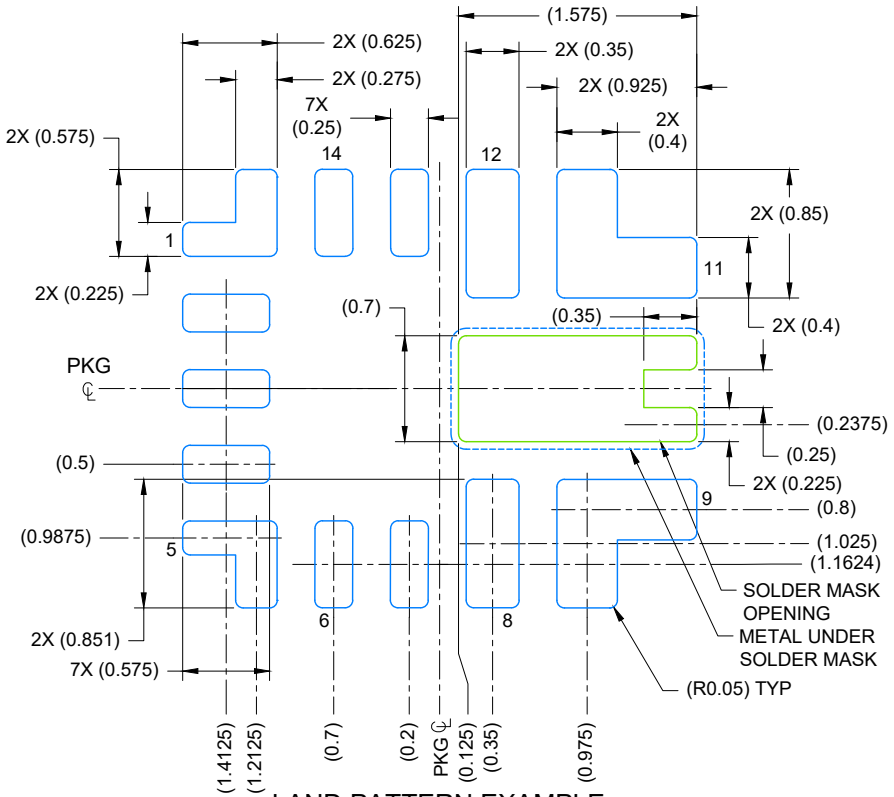
VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK-NO LEAD



NOTES:

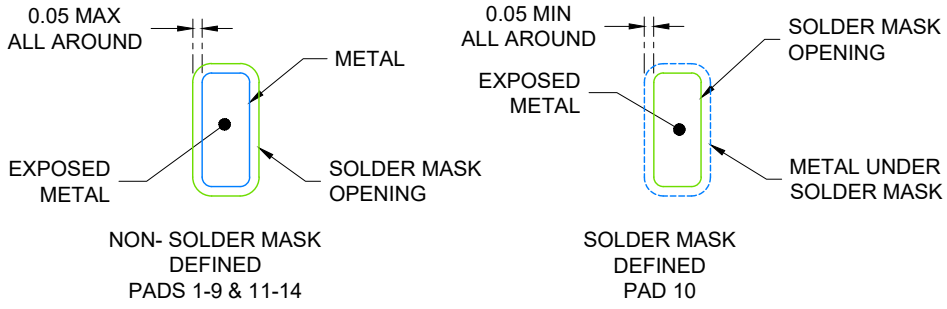
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE

EXPOSED METAL SHOWN

SCALE: 20X



SOLDER MASK DETAILS

NOT TO SCALE

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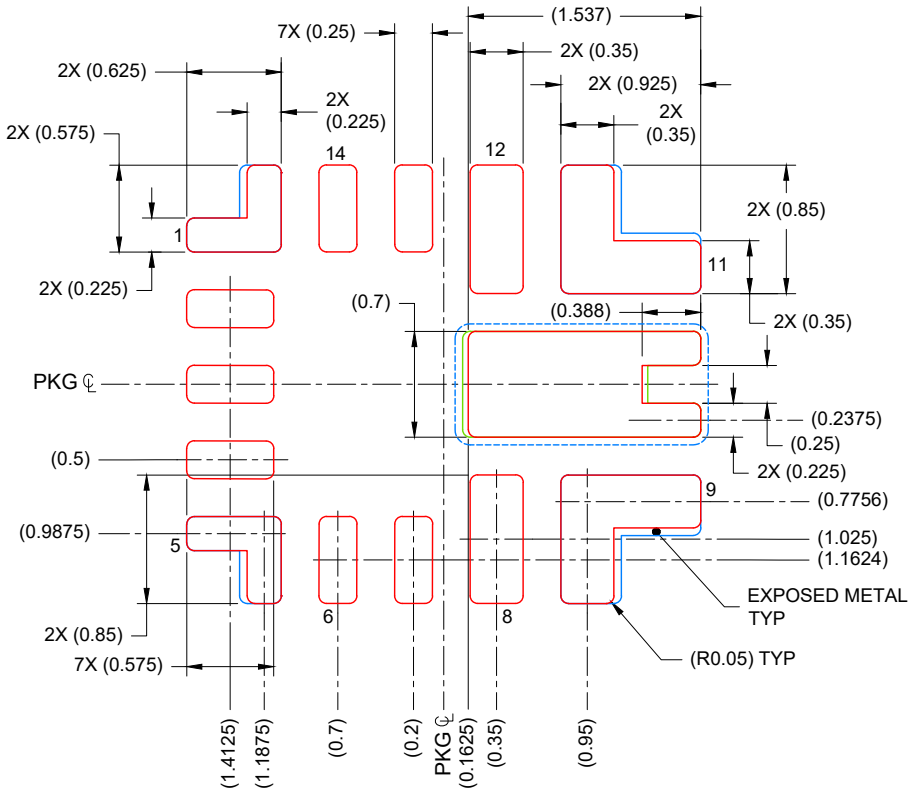
NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

SOLDER PASTE COVERAGE:
PIN 1 & 5: 93%; PIN 9 &11: 91%; PIN 10: 96%
SCALE: 20X

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NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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