TPS54719 2.95V 至 6V 输入、7A 同步降压转换器

1 特性

- 两个可在 7A 负载下获得高效率的 30mΩ（典型值）MOSFET
- 200kHz 至 2MHz 开关频率
- 在温度范围内提供 0.6V±1.5% 的电压基准
- 可调慢起动/时序/时序控制
- 欠压 (UV) 和过压 (OV) 电源正常输出
- 低运行和关断静态电流
- 安全启动至预偏置输出电压
- 逐周期电流限制、过热和频率折返保护
- –40°C 至 140°C 的工作结温范围
- 热增强型 3mm x 3mm 16 引脚 QFN 封装

2 应用

- 低电压、高密度电源系统
- 针对高性能 DSP、FPGA、ASIC 和微处理器的负载点调节
- 宽带、网络和光纤通信基础设施

3 说明

TPS54719 器件一款全功能 6V、7A 同步降压电流模式转换器，具有两个集成的 MOSFET。

TPS54719 集成了 MOSFET、通过实施电流模式控制来减少外部组件数量、通过启用高达 2MHz 的开关频率来减小电感器尺寸，并借助小型 3mm × 3mm 热增强型 QFN 封装尽量减小 IC 封装尺寸，从而实现小型设计。

TPS54719 可在温度范围内为多种负载提供一个电压基准 (VREF) 精度达 ±1.5% 的准确调节。

通过集成的 30mΩ MOSFET 和典型值为 455μA 的电源电流，效率得到最大限度提升。通过使用使能引脚进入关断模式，关断电流可减少至 1μA。

欠压锁定在内部设定为 2.4 V，但可通过使能引脚上的电阻器网络来设定阈值，使之提高。输出电压启动斜升由慢启动引脚控制。一个开漏电源正常信号表示输出处于其标称电压值的 93% 至 108% 之内。

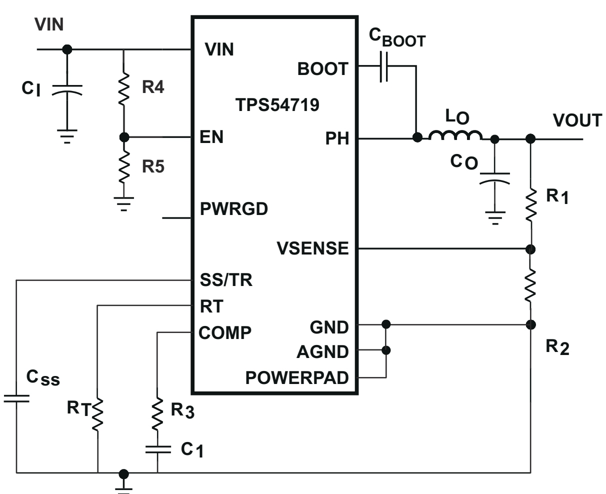
频率折返和热关断功能在过流情况下保护器件不受损坏。

www.ti.com/webench 上的 WEBENCH™ 软件工具支持 TPS54719。

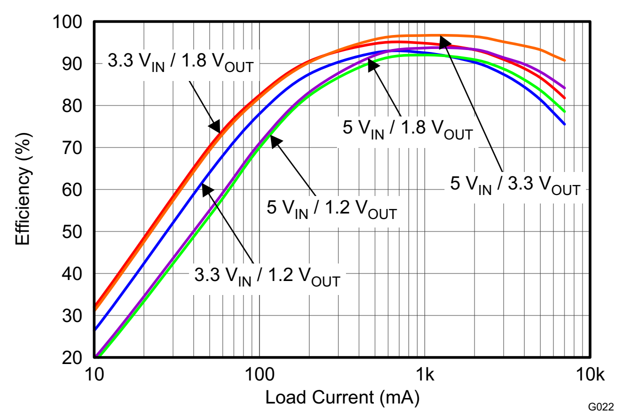
器件信息

器件型号	封装(1)	封装尺寸（标称值）
TPS54719	四方扁平无引线 (QFN) (16)	3.00mm × 3.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



简化版原理图



效率与输出电流间的关系

Table of Contents

4 Revision History

Changes from Revision B (February 2016) to Revision C (September 2021)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式	1
• Added I/O column to 表 5-1	3

Changes from Revision A (July 2014) to Revision B (February 2016)	Page
• 从数据表标题删除了 SWIFT™	1
• Moved Storage temperature to the *节 6.1*	4
• Changed *Handling Ratings* to *节 6.2*	4

5 Pin Configuration and Functions

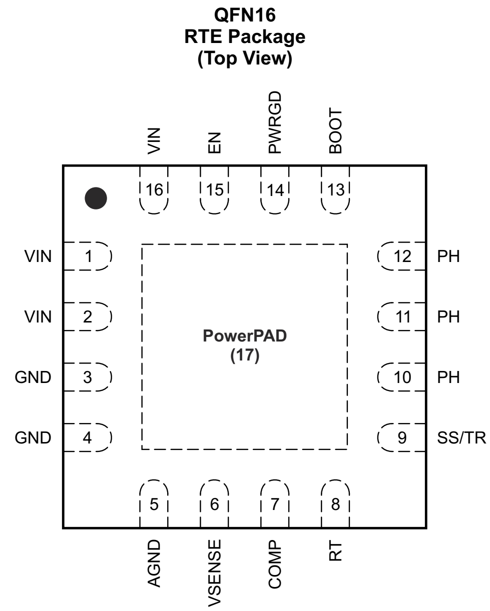


图 5-1. 16-Pin RTE QFN Package (Top View)

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
AGND	5		Analog Ground should be electrically connected to GND close to the device.
BOOT	13	I	A bootstrap capacitor is required between BOOT and PH. If the voltage on this capacitor is below the minimum required by the BOOT UVLO, the output is forced to switch off until the capacitor is refreshed.
COMP	7	O	Error amplifier output and input to the output switch current comparator. Connect frequency compensation components to this pin.
EN	15	I	Enable pin, internal pullup current source. Pull below 1.18 V to disable. Float to enable. Can be used to set the on/off threshold (adjust UVLO) with two additional resistors.
GND	3, 4		Power Ground. This pin should be electrically connected directly to the power pad under the IC.
PH	10, 11, 12	O	The source of the internal high-side power MOSFET and drain of the internal low-side (synchronous) rectifier MOSFET.
PWRGD	14	O	An open-drain output. Asserts low if output voltage is low due to thermal shutdown, overcurrent, overvoltage/undervoltage, or EN shut down.
RT	8	I	Resistor timing
SS/TR	9	I/O	Slow start. An external capacitor connected to this pin sets the output voltage rise time. This pin can also be used for tracking.
Thermal Pad	17		GND pin should be connected to the exposed power pad for proper operation. This thermal pad should be connected to any internal PCB ground plane using multiple vias for good thermal performance.
VIN	1, 2, 16	I	Input supply voltage: 2.95 V to 6 V
VSENSE	6	I	Inverting node of the transconductance (gm) error amplifier

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) [(1)]

		MIN	MAX	UNIT
Input voltage	VIN	–0.3	7	V
	EN	–0.3	7	
	BOOT		PH + 8	
	VSENSE	–0.3	3	
	COMP	–0.3	3	
	PWRGD	–0.3	7	
	SS/TR	–0.3	3	
	RT	–0.3	6	
Output voltage	BOOT-PH		8	V
	PH	–0.6	7	
	PH 10 ns Transient	–2	7	
Source current	EN		100	µA
	RT		100	
Sink current	COMP		100	µA
	PWRGD		10	mA
	SS/TR		100	µA
Operating Junction temperature, T_j		–40	140	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins[(1)]	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins[(2)]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VIN	Supply voltage	2.95		6	V
Input voltage	EN	0		6	V
	PWRGD	0		6	
	SS/RT	0		2.7	
	RT	0		5.5	
T_A	Operating free-air temperature	–40		85	°C

6.4 Thermal Information

THERMAL METRIC [1]		TPS54719 RTE (16 PINS)	UNITS
$R_{\theta JA}$	Junction-to-ambient thermal resistance (standard board)	49.1	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance (custom board)[2]	37.0	
ψ_{JT}	Junction-to-top characterization parameter	0.7	
ψ_{JB}	Junction-to-board characterization parameter	21.8	
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	50.7	
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	7.5	
$R_{\theta JB}$	Junction-to-board thermal resistance	21.8	

(1) Power rating at a specific ambient temperature T_A should be determined with a junction temperature of 140°C. This is the point where distortion starts to substantially increase. See power dissipation estimate in the application section of this data sheet for more information.
(2) Test boards conditions:
  a. 2 inches x 2 inches, 4 layers, thickness: 0.062 inch
  b. 2 oz. copper traces located on the top of the PCB
  c. 2 oz. copper ground planes on the 2 internal layers and bottom layer
  d. 4 thermal vias (10mil) located under the device package

6.5 Electrical Characteristics

T_J = –40°C to 140°C, V_{IN} = 2.95 to 6 V (unless otherwise noted)

DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VIN PIN)					
Operating input voltage		2.95		6	V
Internal undervoltage lockout threshold	Rising V_{IN}		2.4	2.8	V
Internal UVLO hysteresis			0.2		V
Shutdown supply current	EN = 0 V, 2.95 V ≤ VIN ≤ 6 V		1	5	μA
Quiescent current – I_q	V_{SENSE} = 620 mV, RT = 84 kΩ		455	550	μA
ENABLE AND UVLO (EN PIN)					
Enable threshold	Rising	1.16	1.25	1.37	V
	Falling		1.18		
Input current	Enable threshold + 50 mV		-3.6		μA
	Enable threshold – 50 mV		-0.7		
VOLTAGE REFERENCE (VSENSE PIN)					
Voltage reference	2.95 V ≤ V_{IN} ≤ 6 V, –40°C < T_J < 140°C	0.591	0.600	0.609	V
	25°C	0.594	0.600	0.606	
MOSFET					
High-side switch resistance	BOOT-PH = 5 V; T_J = 25°C		26	60	mΩ
	BOOT-PH = 2.95 V; T_J = 25°C		35	70	
Low-side switch resistance	V_{IN} = 5 V; T_J = 25°C		26	60	mΩ
	V_{IN} = 2.95 V; T_J = 25°C		35	70	
ERROR AMPLIFIER					
Input current			50		nA
Error amplifier transconductance (gm)	–2 μA < $I_{(COMP)}$ < 2 μA, $V_{(COMP)}$ = 1 V		250		μmhos
Error amplifier transconductance (gm) during slow start	–2 μA < $I_{(COMP)}$ < 2 μA, $V_{(COMP)}$ = 0.9 V, Vsense = 0.3 V		85		μmhos
Error amplifier source/sink	$V_{(COMP)}$ = 1 V, 100 mV overdrive		±20		μA
COMP to Iswitch gm			25		A/V

T_J = –40°C to 140°C, V_{IN} = 2.95 to 6 V (unless otherwise noted)

DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT LIMIT					
Current limit threshold		8.5	10.5		A
Low-side reverse current limit		–1.5	–2.7		A
THERMAL SHUTDOWN					
Thermalshutdown		150	155		°C
Hysteresis			7.5		°C
TIMING RESISTOR (RT PIN)					
Switching frequency range using RT mode		200		2000	kHz
Switching frequency	RT = 84 kΩ	400	490	600	kHz
BOOT (BOOT PIN)					
BOOT charge resistance	V_{IN} = 5 V		15		Ω
BOOT-PH UVLO	V_{IN} = 2.95 V		2.1	2.75	V
SLOW START / TRACKING (SS/TR PIN)					
Charge current	$V_{(SS)}$ = 0.3 V		2.4		μA
SS/TR to VSENSE matching	V_{SSTR} = 0.3 V		73	115	mV
SS to reference crossover	98% nominal		0.87		V
SS discharge current (overload)	VSENSE = 0 V, V_{SS} = 0.3 V		70		μA
SS discharge voltage (overload)	VSENSE = 0 V		80		mV
SS discharge current (UVLO, EN, thermal fault)	VIN = 5 V, $V_{(SS)}$ = 0.5 V		1.2		mA
POWER GOOD (PWRGD PIN)					
VSENSE threshold	VSENSE rising (Good)		93		% Vref
	VSENSE rising (Fault)		110		% Vref
Hysteresis	VSENSE falling		2		% Vref
Output high leakage	VSENSE = VREF, $V_{(PWRGD)}$ = 5.5 V		100		nA
On resistance	VIN = 5 V, T_J = 25°C		78		Ω
Minimum VIN for valid output	$V_{(PWRGD)}$ < 0.5 V at 100 μA			0.8	V

6.6 Timing Requirements

DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
PH (PH PIN)					
Minimum on time	Measured at 50% points on PH, VIN = 5 V, IOUT = 500 mA		100		ns
Minimum on time	Measured at 50% points on PH, VIN = 5 V, IOUT = 7 A		64		ns
Minimum off time	Prior to skipping off pulses, BOOT-PH = 2.95 V, I_{OUT} = 4 A		0		ns
Rise/fall time	V_{IN} = 5 V		1.5		V/ns
Dead time	Prior to skipping off pulses. BOOT-PH = 2.95 V, I_{OUT} = 4 A		70		ns

6.7 Typical Characteristics

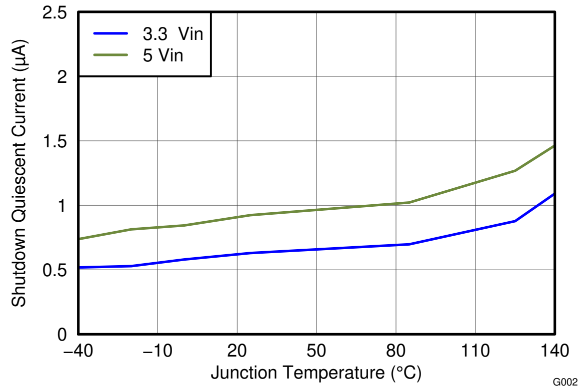


图 6-1. Shutdown Supply Current vs Temperature

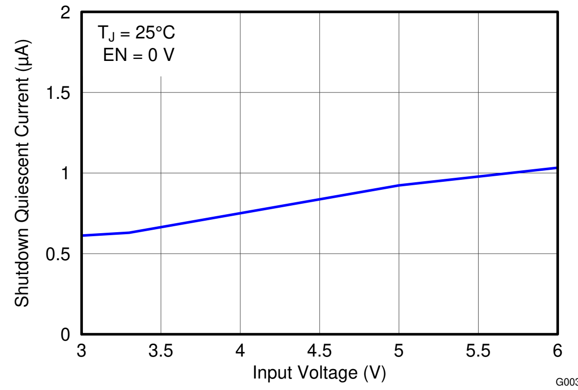


图 6-2. Shutdown Supply Current vs Voltage

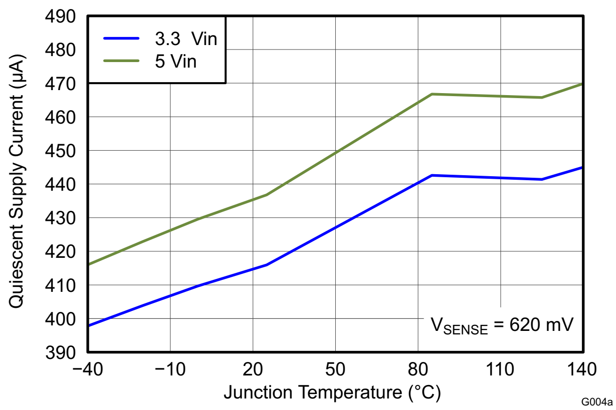


图 6-3. V_{IN} Supply Current vs Temperature

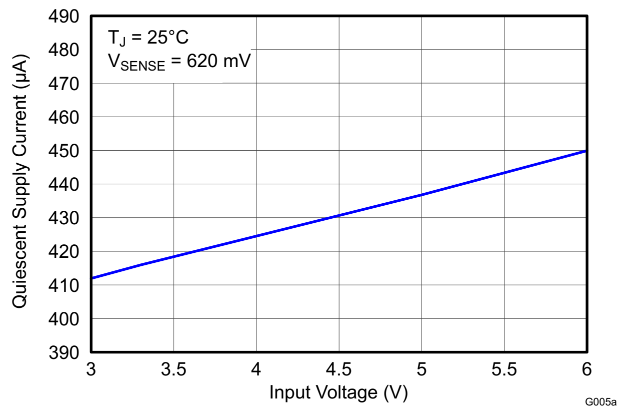


图 6-4. V_{IN} Supply Current vs Voltage

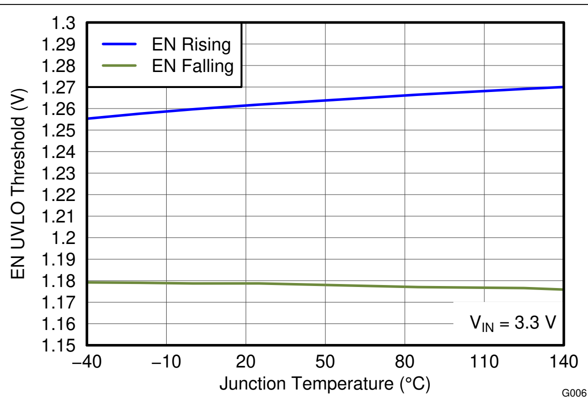


图 6-5. UVLO Threshold vs Temperature

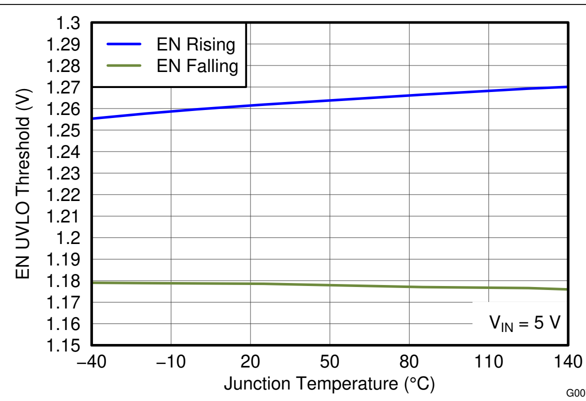


图 6-6. UVLO Threshold vs Temperature

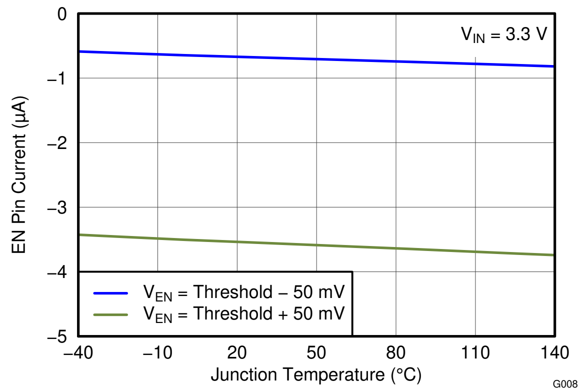


图 6-7. EN Pin Current vs Temperature

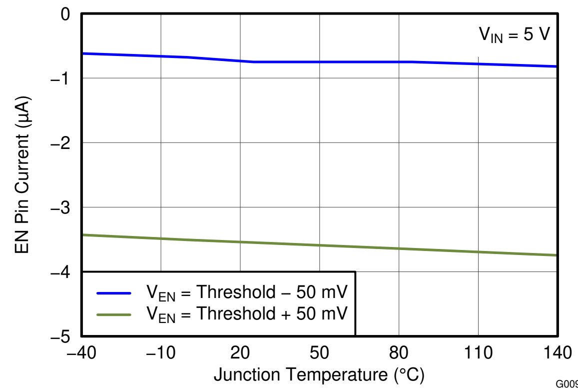


图 6-8. EN Pin Current vs Temperature

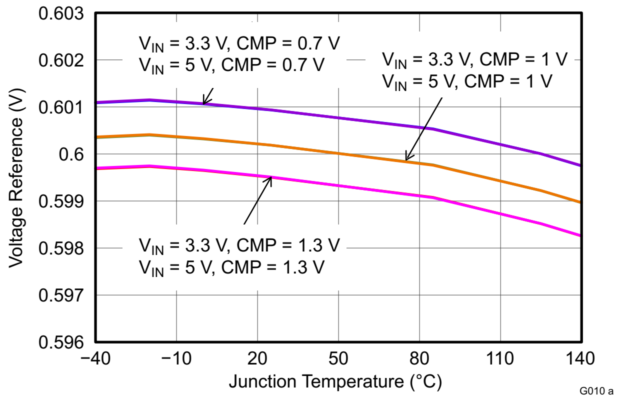


图 6-9. Voltage Reference vs Temperature

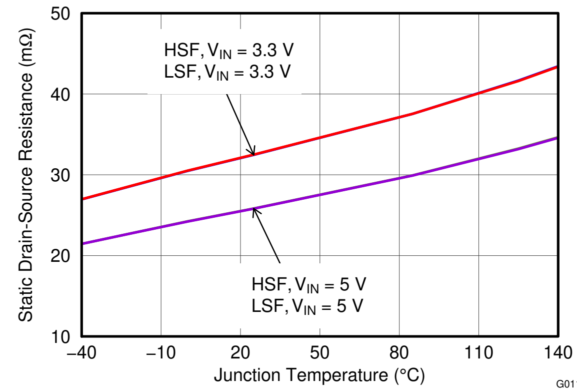


图 6-10. Rdson vs Temperature

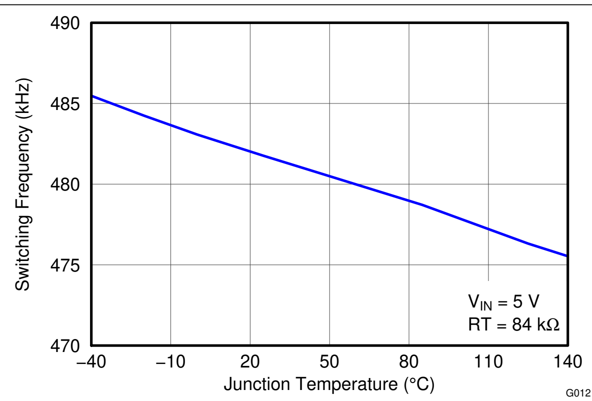


图 6-11. Switching Frequency vs Temperature

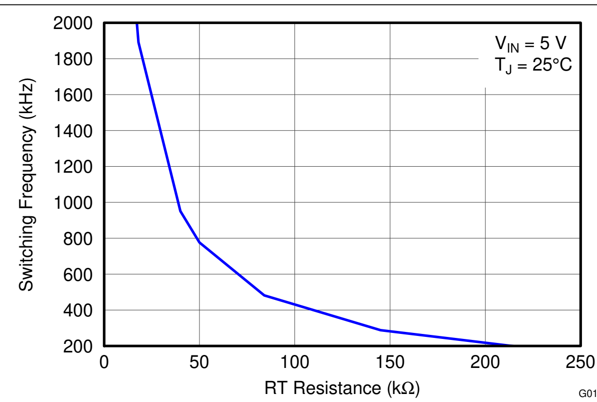


图 6-12. Switching Frequency vs RT Resistance

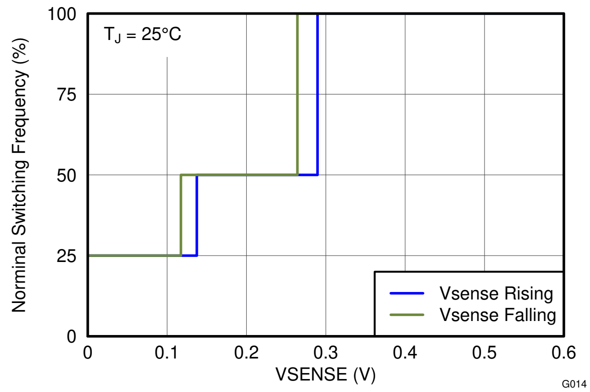


图 6-13. Switching Frequency vs Vsense

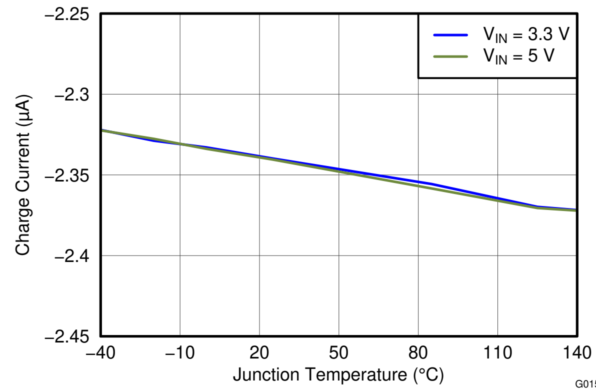


图 6-14. SS Charge Current vs Temperature

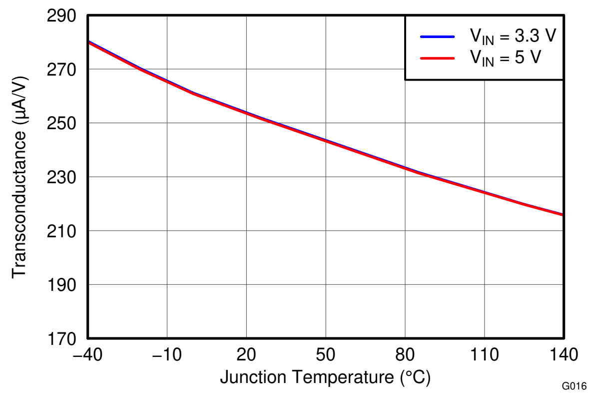


图 6-15. Transconductance vs Temperature

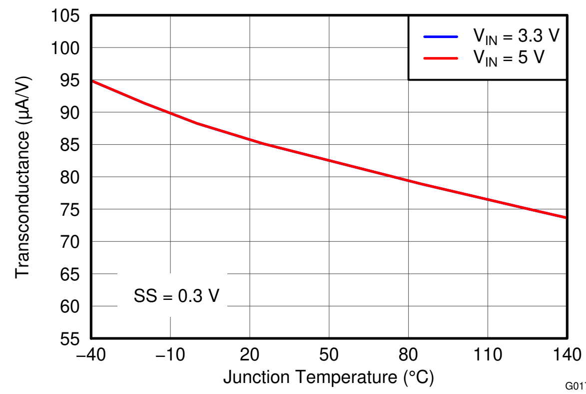


图 6-16. Transconductance (Slow Start) vs Temperature

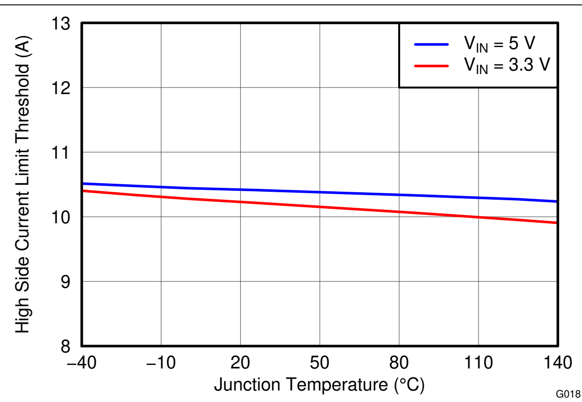


图 6-17. High-Side FET Current Limit vs Temperature

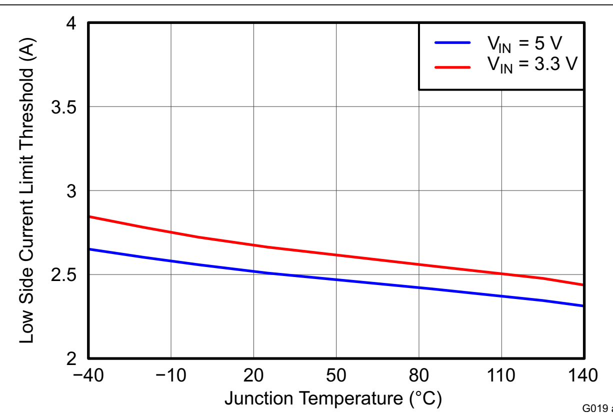


图 6-18. Low-Side FET Current Limit vs Temperature

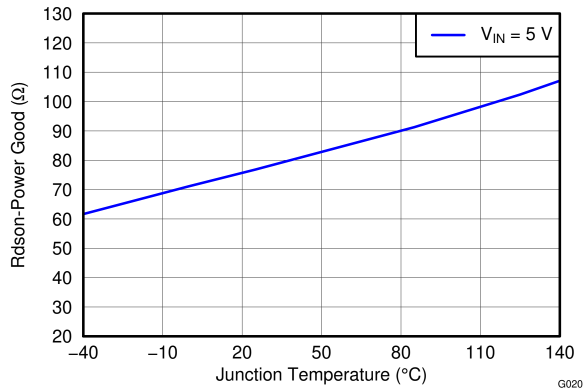


图 6-19. PWRGD Rdson vs Temperature

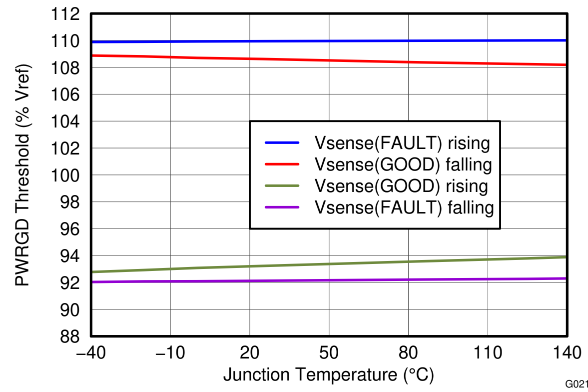


图 6-20. PWRGD Threshold vs Temperature

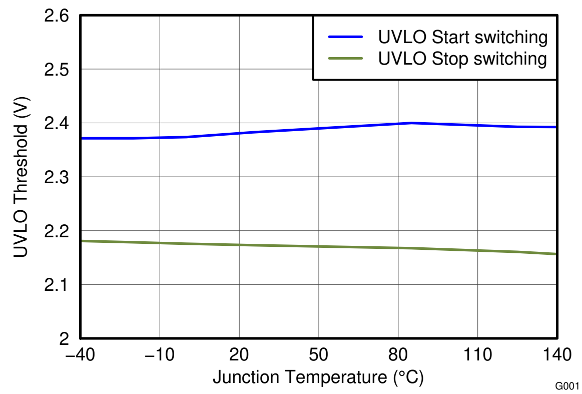


图 6-21. UVLO Threshold vs Temperature

7 Detailed Description

7.1 Overview

The TPS54719 is a 6-V, 7-A, synchronous step-down (buck) converter with two integrated n-channel MOSFETs. To improve performance during line and load transients, the device implements a constant frequency, peak current mode control, which reduces output capacitance and simplifies external frequency compensation design. The wide switching frequency of 200 kHz to 2000 kHz allows for efficiency and size optimization when selecting the output filter components. The switching frequency is adjusted using a resistor to ground on the RT pin.

The TPS54719 has a typical default start-up voltage of 2.4 V. The EN pin has an internal pullup current source that can be used to adjust the input voltage undervoltage lockout (UVLO) with two external resistors. In addition, the pullup current provides a default condition when the EN pin is floating for the device to operate. The total operating current for the TPS54719 is 455 µA when not switching and under no load. When the device is disabled, the supply current is less than 5 µA.

The integrated 30-mΩ MOSFETs allow for high efficiency power supply designs with continuous output currents up to 7 amperes.

The TPS54719 reduces the external component count by integrating the boot recharge diode. The bias voltage for the integrated high-side MOSFET is supplied by a capacitor on the BOOT to PH pin. The boot capacitor voltage is monitored by an UVLO circuit and turns off the high-side MOSFET when the voltage falls below a preset threshold. This BOOT circuit allows the TPS54719 to operate approaching 100%. The output voltage can be stepped down to as low as the 0.6-V reference.

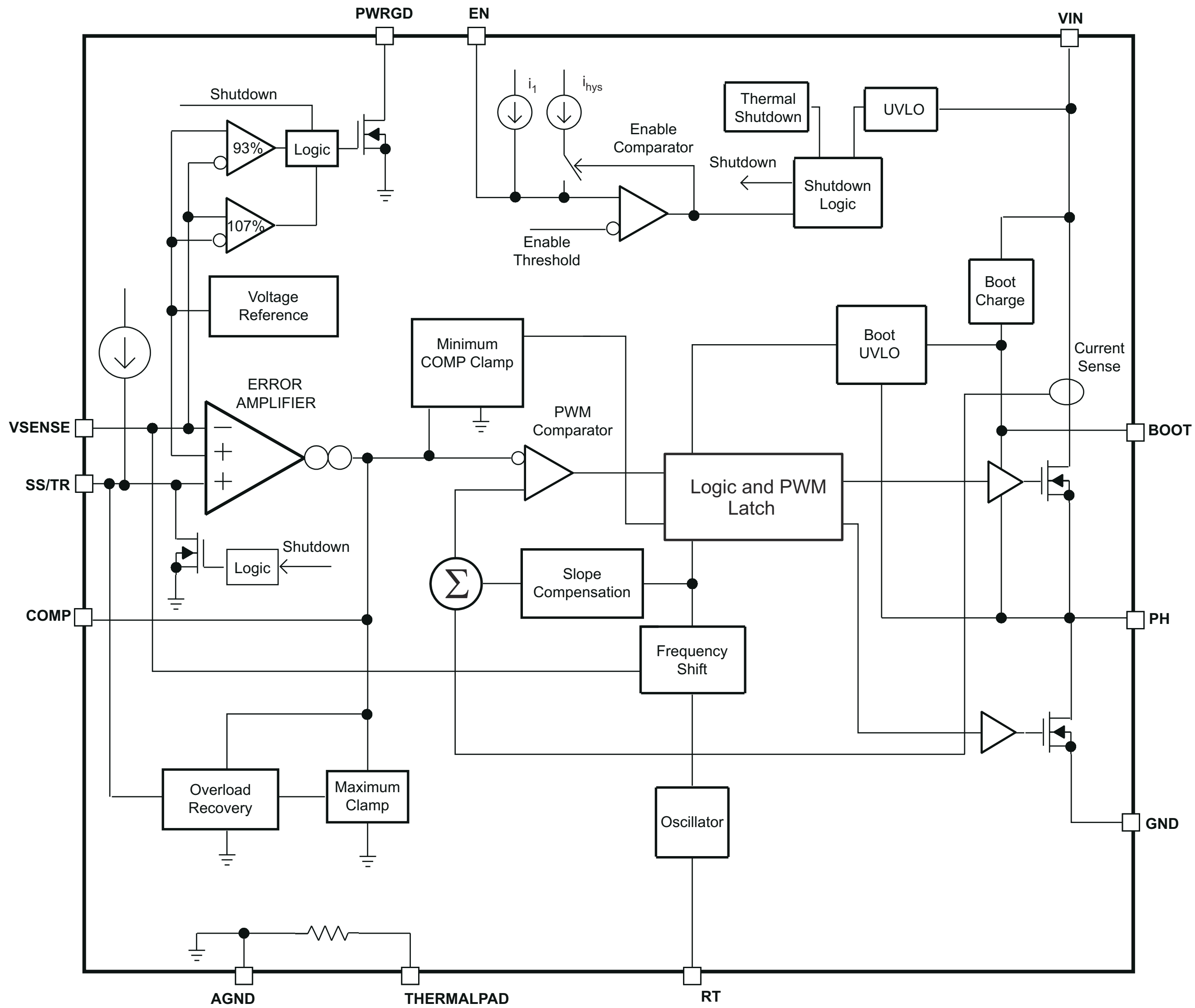
The TPS54719 has a power-good comparator (PWRGD) with 2% hysteresis.

The TPS54719 minimizes excessive output overvoltage transients by taking advantage of the overvoltage power-good comparator. When the regulated output voltage is greater than 110% of the nominal voltage, the overvoltage comparator is activated, and the high-side MOSFET is turned off and masked from turning on until the output voltage is lower than 108%.

The SS/TR pin is used to minimize inrush currents or provide power supply sequencing during power up. A small value capacitor should be coupled to the pin for slow start. The SS/TR pin is discharged before the output power up to make sure there is a repeatable restart after an over-temperature fault, UVLO fault, or disabled condition.

The use of a frequency foldback circuit reduces the switching frequency during start-up and overcurrent fault conditions to help limit the inductor current.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Fixed Frequency PWM Control

The TPS54719 uses an adjustable fixed frequency, peak current mode control. The output voltage is compared through external resistors on the VSENSE pin to an internal voltage reference by an error amplifier, which drives the COMP pin. An internal oscillator initiates the turn on of the high-side power switch. The error amplifier output is compared to the high-side power switch current. When the power switch current reaches the COMP voltage level, the high-side power switch is turned off and the low-side power switch is turned on. The COMP pin voltage increases and decreases as the output current increases and decreases. The device implements a current limit by clamping the COMP pin voltage to a maximum level and also implements a minimum clamp for improved transient response performance.

7.3.2 Slope Compensation And Output Current

The TPS54719 adds a compensating ramp to the switch current signal. This slope compensation prevents subharmonic oscillations as duty cycle increases. The available peak inductor current remains constant over the full duty cycle range.

7.3.3 Bootstrap Voltage (Boot) And Low Dropout Operation

The TPS54719 has an integrated boot regulator and requires a small ceramic capacitor between the BOOT and PH pin to provide the gate drive voltage for the high-side MOSFET. The value of the ceramic capacitor should be 0.1 μF. A ceramic capacitor with an X7R or X5R grade dielectric with a voltage rating of 10 V or higher is recommended because of the stable characteristics over temperature and voltage.

To improve dropout, the TPS54719 is designed to operate at 100% duty cycle as long as the BOOT to PH pin voltage is greater than 2.1 V, typically. The high-side MOSFET is turned off using an UVLO circuit, allowing for the low-side MOSFET to conduct when the voltage from BOOT to PH drops below 2.1 V. Since the supply current sourced from the BOOT pin is very low, the high-side MOSFET can remain on for more switching cycles than are required to refresh the capacitor, thus the effective duty cycle of the switching regulator is very high.

7.3.4 Error Amplifier

The TPS54719 has a transconductance amplifier. The error amplifier compares the VSENSE voltage to the lower of the SS/TR pin voltage or the internal 0.6-V voltage reference. The transconductance of the error amplifier is 250 μA/V during normal operation. When the voltage of VSENSE pin is below 0.6 V and the device is regulating using the SS/TR voltage, the gm is 85 μA/V. The frequency compensation components are placed between the COMP pin and ground.

7.3.5 Voltage Reference

The voltage reference system produces a precise ±1.5% voltage reference over temperature by scaling the output of a temperature stable bandgap circuit. The bandgap and scaling circuits produce 0.6 V at the non-inverting input of the error amplifier.

7.3.6 Adjusting The Output Voltage

The output voltage is set with a resistor divider from the output node to the VSENSE pin. It is recommended to use divider resistors with 1% tolerance or better. Start with a 100 kΩ for the R1 resistor and use the 方程式 1 to calculate R2. To improve efficiency at very light loads consider using larger value resistors. If the values are too high the regulator is more susceptible to noise and voltage errors from the VSENSE input current are noticeable.

$$R2 = R1 \times \left(\frac{0.6\ \text{V}}{V_O - 0.6\ \text{V}} \right) \tag{1}$$

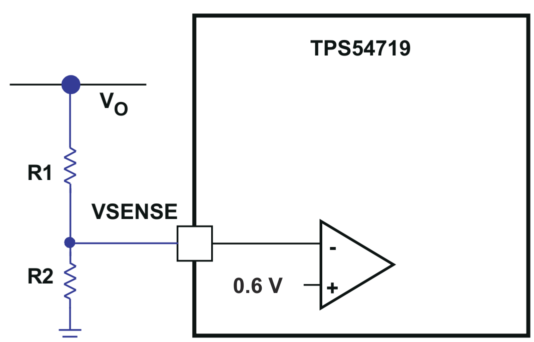


图 7-1. Voltage Divider Circuit

7.3.7 Enable and Adjusting Undervoltage Lockout

The TPS54719 is disabled when the VIN pin voltage falls below 2.2 V. If an application requires a higher undervoltage lockout (UVLO), use the EN pin as shown in 图 7-2 to adjust the input voltage UVLO by using two external resistors. It is recommended to use the enable resistors to set the UVLO falling threshold (V_{STOP}) above 2.7 V. The rising threshold (V_{START}) should be set to provide enough hysteresis to allow for any input supply variations. The EN pin has an internal pullup current source that provides the default condition of the TPS54719 operating when the EN pin floats. Once the EN pin voltage exceeds 1.25 V, an additional 2.9 μA of hysteresis is added. When the EN pin is pulled below 1.18 V, the 2.9 μA is removed. This additional current facilitates input voltage hysteresis.

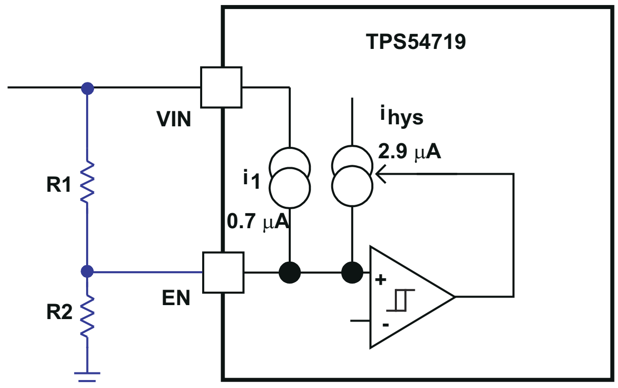


图 7-2. Adjustable Undervoltage Lockout

$$R1 = \frac{V_{START}\left(\frac{V_{ENFALLING}}{V_{ENRISING}}\right) - V_{STOP}}{I_P\left(1 - \frac{V_{ENFALLING}}{V_{ENRISING}}\right) + I_h} \quad (2)$$

$$R2 = \frac{R1 \times V_{ENFALLING}}{V_{STOP} - V_{ENFALLING} + R1(I_P + I_h)} \quad (3)$$

where:

- I_h = 2.9 μA
- I_P = 0.7 μA
- $V_{ENRISING}$ = 1.25 V
- $V_{ENFALLING}$ = 1.18 V

7.3.8 Slow Start/Tracking Pin

The TPS54719 regulates to the lower of the SS/TR pin and the internal reference voltage. A capacitor on the SS/TR pin to ground implements a slow start time. The TPS54719 has an internal pullup current source of 2.4 μA, which charges the external slow-start capacitor. 方程式 4 calculates the required slow-start capacitor value.

$$Css(nF) = \frac{Tss(mS) \times Iss(\mu A)}{Vref(V)} \quad (4)$$

where:

- Tss is the desired slow-start time in ms
- Iss is the internal slow start charging current of 2.4 μA
- Vref is the internal voltage reference of 0.6 V

If during normal operation, VIN goes below the UVLO, the EN pin pulled below 1.18 V, or a thermal shutdown event occurs, the TPS54719 stops switching and the SS/TR is discharged to 0 volts before reinitiating a power-up sequence.

7.3.9 Sequencing

Many of the common power supply sequencing methods can be implemented using the SS/TR, EN, and PWRGD pins. The sequential method can be implemented using an open-drain or collector output of a power on reset pin of another device. 图 7-3 shows the sequential method. The power good is coupled to the EN pin on the TPS54719, which enables the second power supply once the primary supply reaches regulation.

Ratio-metric start-up can be accomplished by connecting the SS/TR pins together. The regulator outputs ramp up and reach regulation at the same time. When calculating the slow start time, the pullup current source must be doubled in 方程式 4. The ratio metric method is illustrated in 图 7-5.

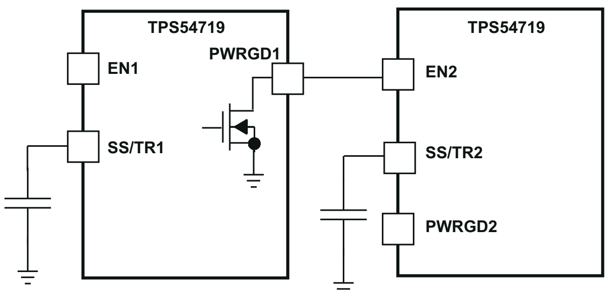


图 7-3. Sequential Start-Up Sequence

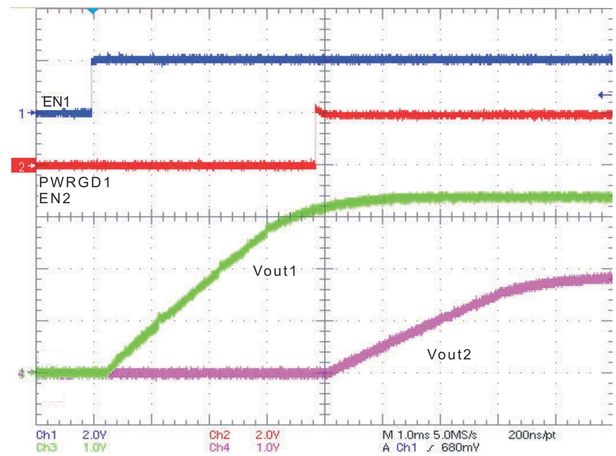


图 7-4. Sequential Start-Up Using EN And PWRGD

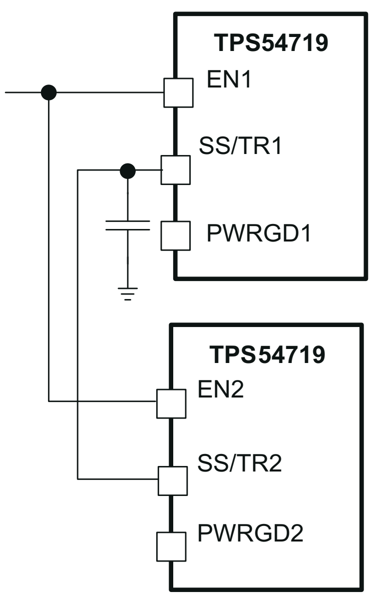


图 7-5. Schematic For Ratio-Metric Start-Up Sequence

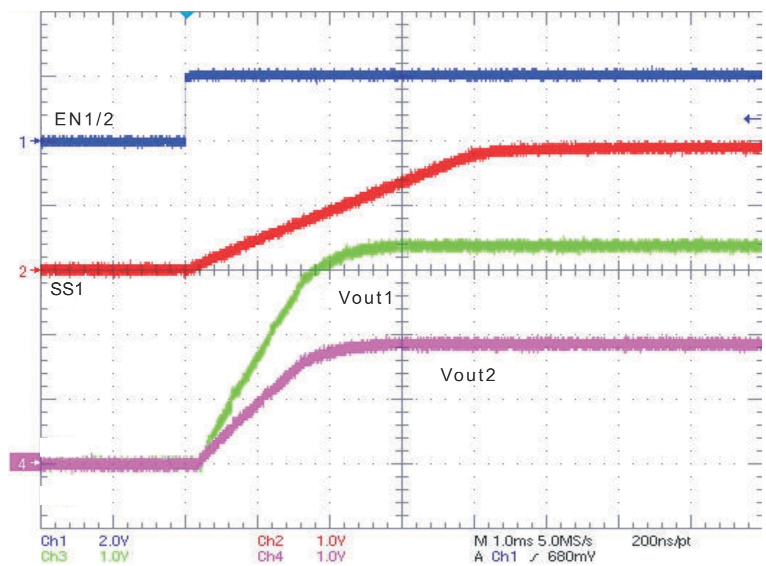


图 7-6. Ratio-Metric Start-Up With V_{OUT1} Leading V_{OUT2}

Ratio-metric and simultaneous power supply sequencing can be implemented by connecting the resistor network of R1 and R2 shown in 图 7-5 to the output of the power supply that needs to be tracked or another voltage reference source. Using 方程式 5 and 方程式 6, the tracking resistors can be calculated to initiate the V_{OUT2} slightly before, after, or at the same time as V_{OUT1}. 方程式 7 is the voltage difference between V_{OUT1} and V_{OUT2}. The ΔV variable is zero volts for simultaneous sequencing. To minimize the effect of the inherent SS/TR to VSENSE offset (Vssoffset) in the slow start circuit and the offset created by the pullup current source (Iss) and tracking resistors, the Vssoffset and Iss are included as variables in the equations. To design a ratio-metric start-up in which the V_{OUT2} voltage is slightly greater than the V_{OUT1} voltage when V_{OUT2} reaches regulation, use a negative number in 方程式 5 through 方程式 7 for ΔV. 方程式 7 will result in a positive number for applications where the V_{OUT2} is slightly lower than V_{OUT1} when V_{OUT2} regulation is achieved. As the SS/TR voltage becomes more than 85% of the nominal reference voltage, the Vssoffset becomes larger as the slow start circuits gradually handoff the regulation reference to the internal voltage reference. The SS/TR pin voltage needs to be greater than 0.87 V for a complete handoff to the internal voltage reference as shown in 图 7-6.

$$R1 = \frac{Vout2 + \Delta V}{Vref} \times \frac{Vssoffset}{Iss} \tag{5}$$

$$R2 = \frac{Vref \times R1}{Vout2 + \Delta V - Vref} \tag{6}$$

$$\Delta V = Vout1 - Vout2 \tag{7}$$

where:

- V_{OUT2} is the regulated output of IC2
- V_{OUT1} is the output of IC1 at the moment IC2 just reaches its regulation

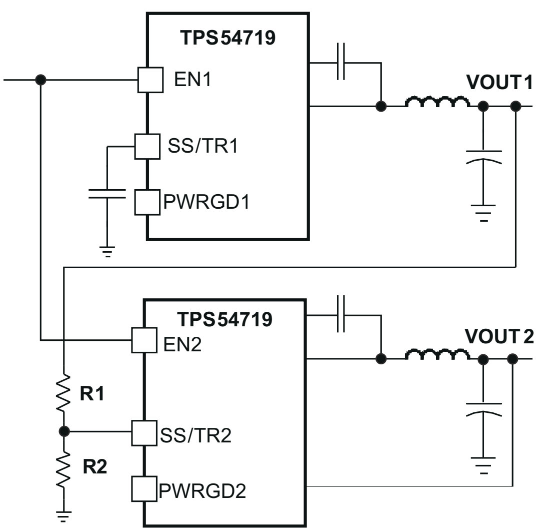


图 7-7. Schematic For Ratio-Metric Start-Up Sequence

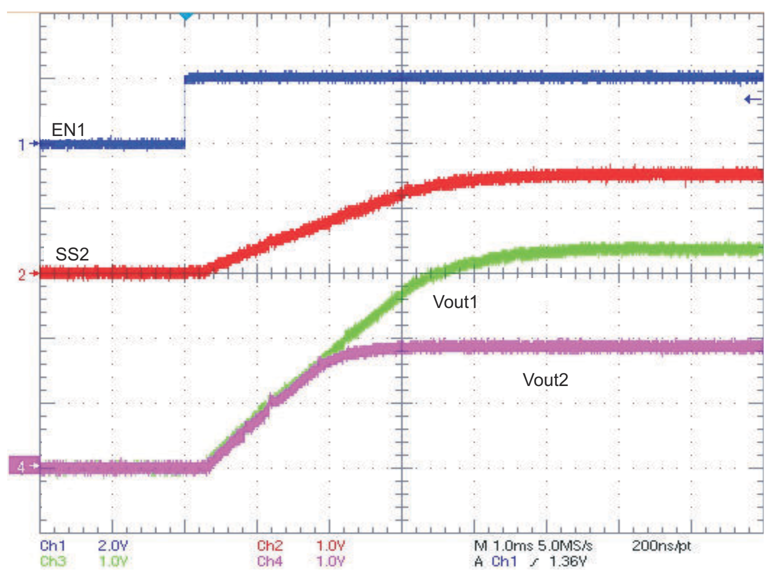


图 7-8. Ratio-Metric Start-Up Using Coupled SS/TR Pins

7.4 Device Functional Modes

7.4.1 Constant Switching Frequency And Timing Resistor (RT Pin)

The switching frequency of the TPS54719 is adjustable over a wide range from 200 kHz to 2000 kHz by placing a maximum of 218 kΩ and minimum of 16.9 kΩ, respectively, on the RT pin. An internal amplifier holds this pin at a fixed voltage when using an external resistor to ground to set the switching frequency. The RT is typically 0.5 V. To determine the timing resistance for a given switching frequency, use the curve in 图 6-12 or 方程式 8.

$$RT\,(k\Omega) = 84145 \times F_{SW}\,(kHz)^{-1.121} \tag{8}$$

$$Fsw(kHz) = 24517 \times RT(k\Omega)^{-0.89} \quad (9)$$

To reduce the solution size, one would typically set the switching frequency as high as possible, but tradeoffs of the efficiency, maximum input voltage, and minimum controllable on time should be considered.

The minimum controllable on time is typically 64 ns at full current load and 100 ns at no load, and limits the maximum operating input voltage or output voltage.

7.4.2 Overcurrent Protection

The TPS54719 implements a cycle-by-cycle current limit. During each switching cycle, the high-side switch current is compared to the voltage on the COMP pin. When the instantaneous switch current intersects the COMP voltage, the high-side switch is turned off. During overcurrent conditions that pull the output voltage low, the error amplifier responds by driving the COMP pin high, increasing the switch current. The error amplifier output is clamped internally. This clamp functions as a switch current limit.

7.4.3 Frequency Shift

To operate at high switching frequencies and provide protection during overcurrent conditions, the TPS54719 implements a frequency shift. If frequency shift was not implemented, during an overcurrent condition, the low-side MOSFET may not be turned off long enough to reduce the current in the inductor, causing a current runaway. With frequency shift, during an overcurrent condition, the switching frequency is reduced from 100%, then 50%, then 25% as the voltage decreases from 0.6 to 0 volts on VSENSE pin to allow the low-side MOSFET to be off long enough to decrease the current in the inductor. During start-up, the switching frequency increases as the voltage on VSENSE increases from 0 to 0.6 volts. See 图 6-13 for details.

7.4.4 Reverse Overcurrent Protection

The TPS54719 implements low-side current protection by detecting the voltage across the low-side MOSFET. When the converter sinks current through its low-side FET, the control circuit turns off the low-side MOSFET if the reverse current is more than 2.7 A. By implementing this additional protection scheme, the converter is able to protect itself from excessive current during power cycling and start-up into pre-biased outputs.

7.4.5 Power Good (PWRGD Pin)

The PWRGD pin output is an open-drain MOSFET. The output is pulled low when the VSENSE voltage enters the fault condition by falling below 91% or rising above 110% of the nominal internal reference voltage. There is a 2% hysteresis on the threshold voltage, so when the VSENSE voltage rises to the good condition above 93% or falls below 108% of the internal voltage reference the PWRGD output MOSFET is turned off. It is recommended to use a pullup resistor between the values of 1 kΩ and 100 kΩ to a voltage source that is 6 V or less. The PWRGD is in a valid state once the VIN input voltage is greater than 0.8 V, typically.

7.4.6 Overvoltage Transient Protection

The TPS54719 incorporates an overvoltage transient protection (OVTP) circuit to minimize voltage overshoot when recovering from output fault conditions or strong unload transients. The OVTP feature minimizes the output overshoot by implementing a circuit to compare the VSENSE pin voltage to the OVTP threshold, which is 110% of the internal voltage reference. If the VSENSE pin voltage is greater than the OVTP threshold, the high-side MOSFET is disabled, preventing current from flowing to the output and minimizing output overshoot. When the VSENSE voltage drops lower than the OVTP threshold, which is 108% of the internal voltage reference, the high-side MOSFET is allowed to turn on the next clock cycle.

7.4.7 Thermal Shutdown

The device implements an internal thermal shutdown to protect itself if the junction temperature exceeds 155°C. The thermal shutdown forces the device to stop switching when the junction temperature exceeds the thermal trip threshold. Once the die temperature decreases below 147.5°C, the device reinitiates the power-up sequence by discharging the SS/TR pin to 0 volts. The thermal shutdown hysteresis is 7.5°C.

7.4.8 Small Signal Model For Loop Response

图 7-9 shows an equivalent model for the TPS54719 control loop, which can be modeled in a circuit simulation program to check frequency response and dynamic load response. The error amplifier is a transconductance amplifier with a gm of 250 µA/V. The error amplifier can be modeled using an ideal voltage controlled current source. The resistor Ro and capacitor Co model the open loop gain and frequency response of the amplifier. The 1-mV AC voltage source between the nodes a and b effectively breaks the control loop for the frequency response measurements. Plotting a/c shows the small signal response of the frequency compensation. Plotting a/b shows the small signal response of the overall loop. The dynamic loop response can be checked by replacing the R_L with a current source with the appropriate load step amplitude and step rate in a time domain analysis.

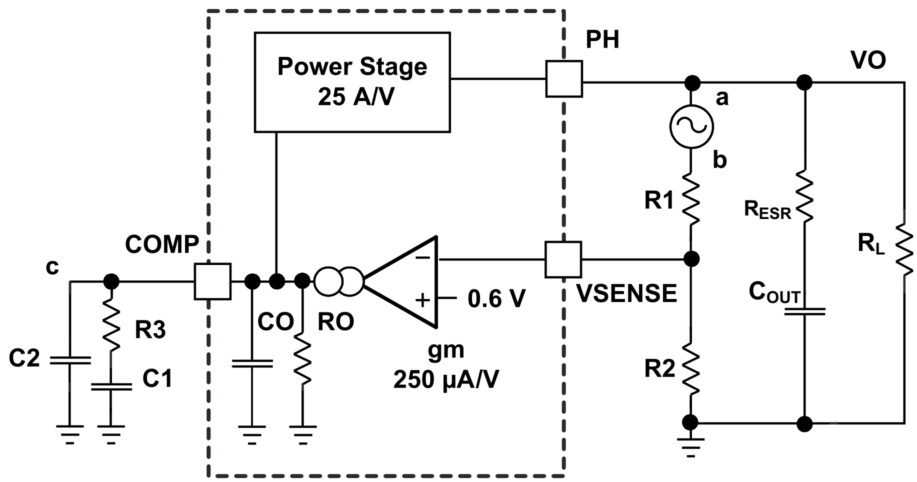


图 7-9. Small Signal Model For Loop Response

7.4.9 Simple Small Signal Model For Peak Current Mode Control

图 7-9 is a simple small signal model that can be used to understand how to design the frequency compensation. The TPS54719 power stage can be approximated to a voltage controlled current source (duty cycle modulator) supplying current to the output capacitor and load resistor. The control to output transfer function is shown in 方程式 10 and consists of a dc gain, one dominant pole, and one ESR zero. The quotient of the change in switch current and the change in COMP pin voltage (node c in 图 7-9) is the power stage transconductance. The gm for the TPS54719 is 25 A/V. The low frequency gain of the power stage frequency response is the product of the transconductance and the load resistance as shown in 方程式 11. As the load current increases and decreases, the low frequency gain decreases and increases, respectively. This variation with load can seem problematic at first glance, but the dominant pole moves with load current [see 方程式 12]. The combined effect is highlighted by the dashed line in the right half of 图 7-10. As the load current decreases, the gain increases and the pole frequency lowers, keeping the 0-dB crossover frequency the same for the varying load conditions which makes it easier to design the frequency compensation.

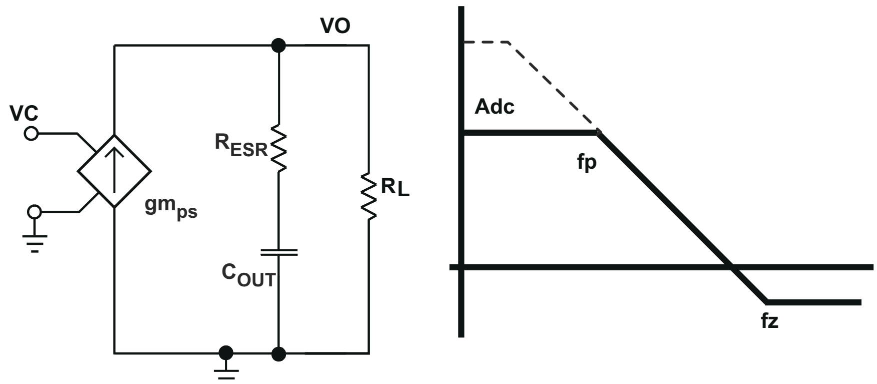


图 7-10. Simple Small Signal Model And Frequency Response For Peak Current Mode Control

$$\frac{vo}{vc} = Adc \times \frac{\left(1+\frac{s}{2\pi \times fz}\right)}{\left(1+\frac{s}{2\pi \times fp}\right)} \tag{10}$$

$$Adc = gm_{ps} \times R_L \tag{11}$$

$$fp = \frac{1}{C_{OUT} \times R_L \times 2\pi} \tag{12}$$

$$fz = \frac{1}{C_{OUT} \times R_{ESR} \times 2\pi} \tag{13}$$

7.4.10 Small Signal Model For Frequency Compensation

The TPS54719 uses a transconductance amplifier for the error amplifier and readily supports two of the commonly used frequency compensation circuits. The compensation circuits are shown in 图 7-11. The Type 2 circuits are most likely implemented in high bandwidth power supply designs using low-ESR output capacitors. In Type 2A, one additional high frequency pole is added to attenuate high frequency noise.

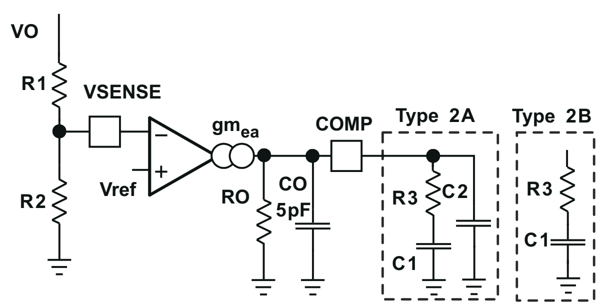


图 7-11. Types Of Frequency Compensation

The design guidelines for TPS54719 loop compensation are as follows:

1. The modulator pole, fpmod, and the esr zero, fz1, must be calculated using 方程式 14 and 方程式 15. Derating the output capacitor (C_{OUT}) can be needed if the output voltage is a high percentage of the capacitor rating. Use the capacitor manufacturer information to derate the capacitor value. Use 方程式 16 and 方程式 17 to estimate a starting point for the crossover frequency, fc. 方程式 16 is the geometric mean

of the modulator pole and the esr zero and 方程式 17 is the mean of modulator pole and the switching frequency. Use the lower value of 方程式 16 or 方程式 17 as the maximum crossover frequency.

$$fp\ mod = \frac{Ioutmax}{2\pi \times Vout \times Cout} \quad (14)$$

$$fz\ mod = \frac{1}{2\pi \times Resr \times Cout} \quad (15)$$

$$f_C = \sqrt{fp\ mod \times fz\ mod} \quad (16)$$

$$f_C = \sqrt{fp\ mod \times \frac{fsw}{2}} \quad (17)$$

2. R3 can be determined by

$$R3 = \frac{2\pi \times fc \times Vo \times C_{OUT}}{gm_{ea} \times Vref \times gm_{ps}} \quad (18)$$

where:

- gm_{ea} is the amplifier gain (250 μA/V)
- gm_{ps} is the power stage gain (25 A/V)

3. Place a compensation zero at the dominant pole $fp = \frac{1}{C_{OUT} \times R_L \times 2\pi}$. C1 can be determined by

$$C1 = \frac{R_L \times C_{OUT}}{R3} \quad (19)$$

4. C2 is optional. It can be used to cancel the zero from the ESR of Co.

$$C2 = \frac{Resr \times C_{OUT}}{R3} \quad (20)$$

8 Application and Implementation

备注

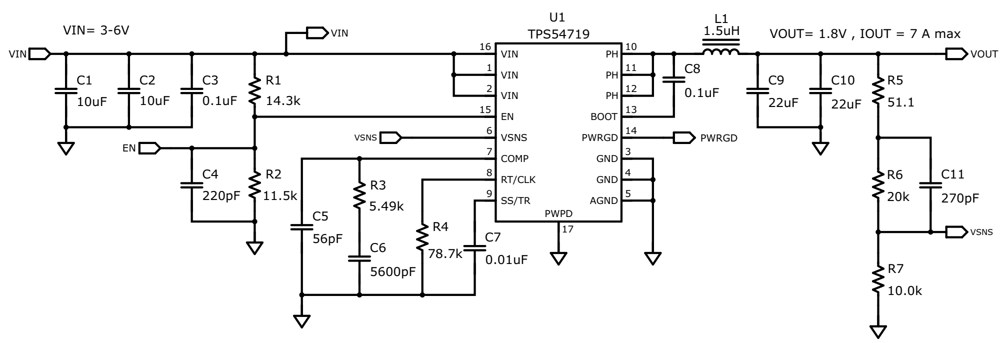
以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

This example details the design of a high frequency switching regulator design using ceramic output capacitors. This design is available as the PWR037-002 evaluation module (EVM). A few parameters must be known in order to start the design process. These parameters are typically determined on the system level.

8.2 Typical Application

8.2.1 High Frequency, 1.8-V Output Power Supply Design With Adjusted UVLO



8.2.2 Design Requirements

For this example, start with the following known parameters:

DESIGN PARAMETER	VALUE
Output Voltage	1.8 V
Transient Response 1.75 to 5.25 A load step	∆ Vout = 6 %
Maximum Output Current	7 A
Input Voltage	3 V - 6 V
Output Voltage Ripple	< 30 mV p-p
Start Input Voltage (rising VIN)	2.9 V
Stop Input Voltage (falling VIN)	2.66 V
Switching Frequency (Fsw)	500 kHz

8.2.3 Detailed Design Procedure

8.2.3.1 Selecting The Switching Frequency

The first step is to decide on a switching frequency for the regulator. Typically, the user wants to choose the highest switching frequency possible since this produces the smallest solution size. The high switching frequency allows for lower valued inductors and smaller output capacitors compared to a power supply that switches at a lower frequency. However, the highest switching frequency causes extra switching losses, which hurt the performance of the converter. The converter is capable of running from 200 kHz to 2 MHz. Unless a small solution size is an ultimate goal, a moderate switching frequency of 500 kHz is selected to achieve both a small solution size and a high efficiency operation. Using 方程式 8, R4 is calculated to be 77.8 kΩ. A standard 1% 78.7-kΩ value was chosen in the design.

8.2.3.2 Output Inductor Selection

The inductor selected works for the entire TPS54719 input voltage range. To calculate the value of the output inductor, use 方程式 21. K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum output current. The inductor ripple current is filtered by the output capacitor. Therefore, choosing high inductor ripple currents impacts the selection of the output capacitor since the output capacitor must have a ripple current rating equal to or greater than the inductor ripple current. In general, the inductor ripple value is at the discretion of the designer; however, K_{IND} is normally from 0.1 to 0.3 for the majority of applications.

For this design example, use K_{IND} = 0.3 and the minimum inductor value is calculated to be 1.2 µH. For this design, a larger standard value of 1.5 µH was chosen. For the output filter inductor, it is important that the RMS current and saturation current ratings not be exceeded. The RMS and peak inductor current can be found from 方程式 23 and 方程式 24.

For this design, the RMS inductor current is 7.017 A and the peak inductor current is 7.84 A. The chosen inductor is a Würth 744311150 1.5 µH. It has a saturation current rating of 14 A (30% inductance loss) and an RMS current rating of 11 A (40 °C temperature rise). The series resistance is 6.6 mΩ typical.

The current flowing through the inductor is the inductor ripple current plus the output current. During power up, faults, or transient load conditions, the inductor current can increase above the calculated peak inductor current level calculated above. In transient conditions, the inductor current can increase up to the switch current limit of the device. For this reason, the most conservative approach is to specify an inductor with a saturation current rating equal to or greater than the switch current limit rather than the peak inductor current.

$$L1 = \frac{Vinmax - Vout}{Io \times Kind} \times \frac{Vout}{Vinmax \times fsw} \tag{21}$$

$$Iripple = \frac{Vinmax - Vout}{L1} \times \frac{Vout}{Vinmax \times fsw} \tag{22}$$

$$ILrms = \sqrt{Io^2 + \frac{1}{12} \times \left(\frac{Vo \times (Vinmax - Vo)}{Vinmax \times L1 \times fsw}\right)^2} \tag{23}$$

$$ILpeak = Iout + \frac{Iripple}{2} \tag{24}$$

8.2.3.3 Output Capacitor

There are three primary considerations for selecting the value of the output capacitor. The output capacitor determines the modulator pole, the output voltage ripple, and how the regulator responds to a large change in load current. The output capacitance needs to be selected based on the more stringent of these three criteria.

The desired response to a large change in the load current is the first criteria. The output capacitor needs to supply the load with current when the regulator can not. This situation would occur if there are desired hold-up times for the regulator where the output capacitor must hold the output voltage above a certain level for a specified amount of time after the input power is removed. The regulator is temporarily not able to supply sufficient output current if there is a large, fast increase in the current needs of the load, such as transitioning from no load to a full load. The regulator response to the load step change is limited by the control loop bandwidth, F_{CO}. The output capacitor must be sized to supply the extra current without excessive output voltage drop until the control loop can respond to the load change. 方程式 25 shows the minimum output capacitance necessary for an instantaneous load step change. Practical circuits will have a slew rate limited load step and will typically require less capacitance.

For this example, the transient load response is specified as a 6% change in Vout for a load step from 1.75 A (25%) to 5.25 A (75%), and ΔVout = 0.06 × 1.8 = 108 mV. For a load step slew rate of 30 mA / µsec, 2 × 22 µF is sufficient to meet the voltage drop requirement. The ESR of the output capacitor is ignored as the ESR of ceramic capacitors is small.

方程式 26 calculates the minimum output capacitance needed to meet the output voltage ripple specification. In this case, the maximum output voltage ripple is 30 mV. Under this requirement, 方程式 26 yields 14 µF.

$$Co > \frac{\Delta I_{OUT}}{F_{CO} \times \Delta V_{OUT}} \tag{25}$$

$$Co > \frac{1}{8 \times fsw} \times \frac{1}{\frac{Voripple}{Iripple}} \tag{26}$$

where:

- ∆ Iout is the change in output current
- Fsw is the regulators switching frequency
- ∆ Vout is the allowable change in the output voltage
- Vripple is the maximum allowable output voltage ripple
- Iripple is the inductor ripple current

方程式 27 calculates the maximum ESR an output capacitor can have to meet the output voltage ripple specification. 方程式 27 indicates the ESR should be less than 28.6 mΩ. In this case, the ESR of the ceramic capacitor is much less than 17.9 mΩ.

Additional capacitance de-ratings for aging, temperature and DC bias should be factored in which increases this minimum value. For this example, two 22-µF 10-V X5R ceramic capacitors with 3 mΩ of ESR are used.

Capacitors generally have limits to the amount of ripple current they can handle without failing or producing excess heat. An output capacitor that can support the inductor ripple current must be specified. Some capacitor data sheets specify the RMS (Root Mean Square) value of the maximum ripple current. 方程式 28 can be used to calculate the RMS ripple current the output capacitor needs to support. For this application, 方程式 28 yields 485 mA.

$$Resr < \frac{Voripple}{Iripple} \tag{27}$$

$$Icorms = \frac{Vout \times (Vinmax - Vout)}{\sqrt{12} \times Vinmax \times L1 \times fsw} \tag{28}$$

8.2.3.4 Input Capacitor

The TPS54719 requires a high quality ceramic, type X5R or X7R, input decoupling capacitor of at least 10 µF of effective capacitance and in some applications a bulk capacitance. The effective capacitance includes any DC bias effects. The voltage rating of the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple current rating greater than the maximum input current ripple of the TPS54719. The input ripple current can be calculated using 方程式 29.

The value of a ceramic capacitor varies significantly over temperature and the amount of DC bias applied to the capacitor. The capacitance variations due to temperature can be minimized by selecting a dielectric material that is stable over temperature. X5R and X7R ceramic dielectrics are usually selected for power regulator capacitors because they have a high capacitance to volume ratio and are fairly stable over temperature. The output capacitor must also be selected with the DC bias taken into account. The capacitance value of a capacitor decreases as the DC bias across a capacitor increases.

For this example design, ceramic capacitors with at least a 10-V voltage rating are required to support the maximum input voltage. For this example, two 10-µF and one 0.1-µF, 10-V capacitors in parallel have been selected. The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using 方程式 30. Using the design example values, Ioutmax = 7 A, Cin = 20 µF, and Fsw = 500 kHz, yields an input voltage ripple of 174 mV and a rms input ripple current of 3.43 A.

$$Icirms = Iout \times \sqrt{\frac{Vout}{Vinmin} \times \frac{(Vinmin - Vout)}{Vinmin}} \tag{29}$$

$$\Delta Vin = \frac{Ioutmax \times 0.25}{Cin \times fsw} \tag{30}$$

8.2.3.5 Slow-Start Capacitor

The slow-start capacitor determines the minimum amount of time it takes for the output voltage to reach its nominal programmed value during power up. This is useful if a load requires a controlled voltage slew rate. This is also used if the output capacitance is very large and would require large amounts of current to quickly charge the capacitor to the output voltage level. The large currents necessary to charge the capacitor can make the TPS54719 reach the current limit or excessive current draw from the input power supply can cause the input voltage rail to sag. Limiting the output voltage slew rate solves both of these problems.

The slow-start capacitor value can be calculated using 方程式 4. For the example circuit, the slow-start time is not too critical since the output capacitor value is 2 × 22 µF, which does not require much current to charge to 1.8 V. The example circuit has the slow start time set to an arbitrary value of 2.5 ms, which requires a 10-nF capacitor. In TPS54719, Iss is 2.4 µA and Vref is 0.6 V.

8.2.3.6 Bootstrap Capacitor Selection

A 0.1-µF ceramic capacitor must be connected between the BOOT to PH pin for proper operation. It is recommended to use a ceramic capacitor with X5R or better grade dielectric. The capacitor should have 10-V or higher voltage rating.

8.2.3.7 Undervoltage Lockout Set Point

The Undervoltage Lockout (UVLO) can be adjusted using an external voltage divider on the EN pin of the TPS54719. The UVLO has two thresholds: one for power up when the input voltage is rising and one for power down or brown outs when the input voltage is falling. For the example design, the supply should turn on and start switching once the input voltage increases above 2.794 V (V_{START}). After the regulator starts switching, it should continue to do so until the input voltage falls below 2.595 V (V_{STOP}).

The programmable UVLO and enable voltages are set using a resistor divider between Vin and ground to the EN pin. 方程式 2 and 方程式 3 can be used to calculate the resistance values necessary. From 方程式 2 and 方程式 3, a 14.3 kΩ between VIN and EN and a 11.5 kΩ between EN and ground are required to produce the 2.794 and 2.595 volt start and stop voltages.

8.2.3.8 Output Voltage And Feedback Resistors Selection

For the example design, 20.0 kΩ was selected for R6. Using 方程式 31, R7 is calculated as 10.0 kΩ.

$$R7 = \frac{Vref}{Vo - Vref} R6 \tag{31}$$

Due to the internal design of the TPS54719, there is a minimum output voltage limit for any given input voltage. The output voltage can never be lower than the internal voltage reference of 0.6 V. Above 0.6 V, the output voltage may be limited by the minimum controllable on time. The minimum output voltage in this case is given by 方程式 32.

$$V_{OUT(MIN)} = V_{IN}\left(\frac{t_{ON}}{t_S}\right) - I_{OUT}\left(R_{DS} + R_L\right) - \left(0.7V - \left(I_{OUT} \times R_{DS}\right)\right)\frac{t_{DEAD}}{t_S} \tag{32}$$

where:

- $V_{OUT(MIN)}$ = minimum achievable output voltage
- t_{ON} = minimum controllable on time (64 ns - 100 nsec typical)
- t_S = 1/f_{SW} (switching frequency)
- t_{DEAD} = dead time (70 nsec typical)
- V_{IN} = maximum input voltage
- R_{DS} = minimum high side MOSFET on resistance (26 - 35 mΩ)
- I_{OUT} = minimum load current
- R_L = series resistance of output inductor

There is also a maximum achievable output voltage which is limited by the minimum off time. The maximum output voltage is given by 方程式 33

$$V_{OUT(MAX)} = V_{IN}\left(1-\frac{t_{OFF}}{t_S}\right)-I_{OUT}\left(R_{DS}+R_L\right)-\left(V_{IN}+0.7V-\left(I_{OUT}\times R_{DS}\right)\right)\frac{t_{DEAD}}{t_S} \tag{33}$$

where:

- $V_{OUT(MAX)}$ = maximum achievable output voltage
- t_S = 1/f_{SW} (switching frequency)
- t_{OFF} = minimum off time (0 nsec typical)
- t_{DEAD} = dead time (70 nsec typical)
- V_{IN} = minimum input voltage
- I_{OUT} = maximum load current
- R_{DS} = maximum high side MOSFET on resistance (60 - 70 mΩ)
- R_L = series resistance of output inductor

8.2.3.9 Compensation

There are several possible methods to design closed loop compensation for dc/dc converters. For the ideal current mode control, the design equations can be easily simplified. The power stage gain is constant at low frequencies, and rolls off at -20 dB/decade above the modulator pole frequency. The power stage phase is 0 degrees at low frequencies and starts to fall one decade below the modulator pole frequency reaching a minimum of -90 degrees one decade above the modulator pole frequency. The modulator pole is a simple pole shown in 方程式 34.

$$fp\ \mathrm{mod} = \frac{\mathrm{Ioutmax}}{2\pi \times \mathrm{Vout} \times \mathrm{Cout}} \tag{34}$$

For the TPS54719, most circuits will have relatively high amounts of slope compensation. As more slope compensation is applied, the power stage characteristics will deviate from the ideal approximations. The phase loss of the power stage will now approach -180 degrees, making compensation more difficult. The power stage transfer function can be solved but it is a tedious hand calculation that does not lend itself to simple approximations. It is best to use Pspice or TINA-TI to accurately model the power stage gain and phase so that a reliable compensation circuit can be designed. That is the technique used in this design procedure. Using the pspice model of (insert link here). Apply the values calculated previously to the output filter components of L1, C9 and C10. Set Rload to the appropriate value. For this design, L1 = 1.5 µH. C9 and C10 are set to 22 µF each, and the ESR is set to 3 mΩ. The Rload resistor is 1.8 V / 3.5 A = 514 mΩ for one half rated load. Now the power stage characteristic can be plotted as shown in 图 8-1.

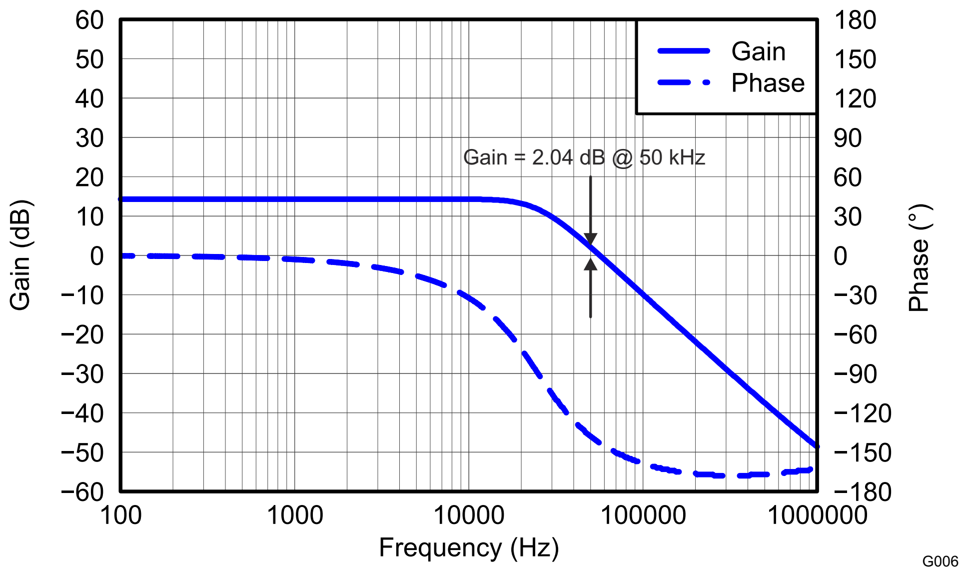


图 8-1. Power Stage Gain And Phase Characteristics

For this design, the intended crossover frequency is 50 kHz. From the power stage gain and phase plots, the gain at 50 kHz is 2.04 dB and the phase is about – 135 degrees. For 60 degrees of phase margin, additional phase boost from a feedforward capacitor in parallel with the upper resistor of the voltage set point divider will be required. R3 sets the gain of the compensated error amplifier to be equal and opposite the power stage gain at crossover. The required value of R3 can be calculated from 方程式 35.

$$R3 = \frac{10^{\frac{-G_{PWRSTG}}{20}}}{gm_{EA}} \cdot \sqrt{\frac{V_{out}}{V_{REF}}} \tag{35}$$

To maximize phase gain, the compensator zero is placed one decade below the crossover frequency of 50 kHz. The required value for C6 is given by 方程式 36.

$$C6 = \frac{1}{2 \cdot \pi \cdot R3 \cdot \frac{F_{CO}}{10}} \tag{36}$$

To maximize phase gain the high frequency pole is placed one decade above the crossover frequency of 50 kHz. The pole can also be useful to offset the ESR of aluminum electrolytic output capacitors. The value for C5 can be calculated from 方程式 37.

$$C5 = \frac{1}{2 \cdot \pi \cdot R3 \cdot F_P} \tag{37}$$

For maximum phase boost, the pole frequency F_P will typically be one decade above the intended crossover frequency F_{CO}.

The feedforward capacitor, C11, is used to increase the phase boost at crossover above what is normally available from Type II compensation. It places an additional zero/pole pair located at 方程式 38 and 方程式 39.

$$F_Z = \frac{1}{2 \cdot \pi \cdot C11 \cdot R6} \tag{38}$$

$$F_P = \frac{1}{2 \cdot \pi \cdot C11 \cdot R6 \parallel R7} \quad (39)$$

This zero and pole pair is not independent. Once the zero location is chosen, the pole is fixed as well. For optimum performance, the zero and pole should be located symmetrically about the intended crossover frequency. The required value for C10 can calculated from 方程式 40.

$$C11 = \frac{1}{2 \cdot \pi \cdot R6 \cdot F_{CO} \cdot \sqrt{\frac{V_{REF}}{V_{OUT}}}} \quad (40)$$

For this design the calculated values for the compensation components are R3 = 5.49 kΩ, C6 = 5600 pF, C5 = 56 pF, and C11 = 270 pF.

8.2.4 Application Curves

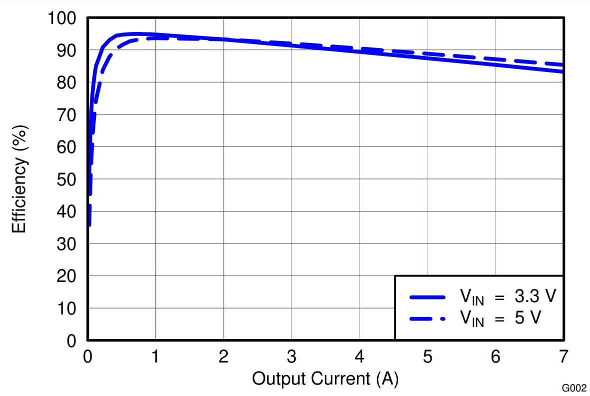


图 8-2. Efficiency vs Load Current

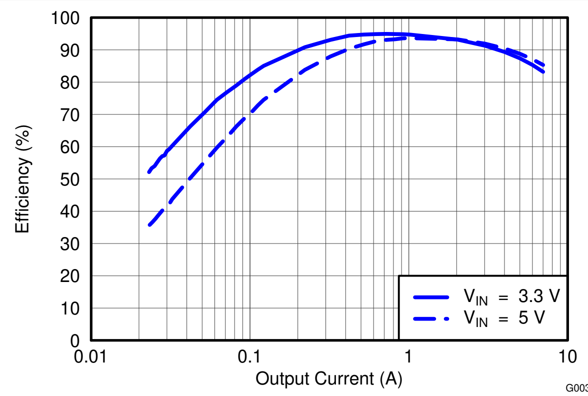


图 8-3. Efficiency vs Load Current

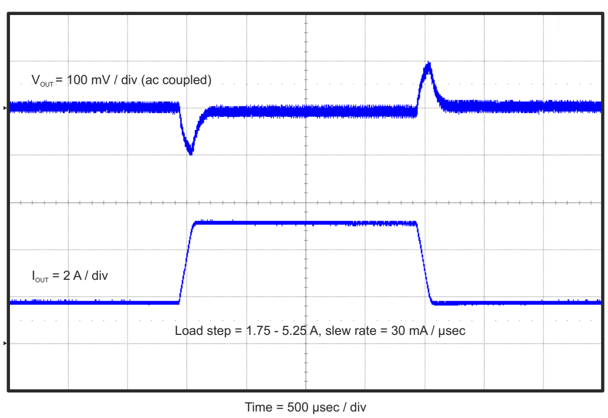


图 8-4. Transient Response, 3.5 A Step

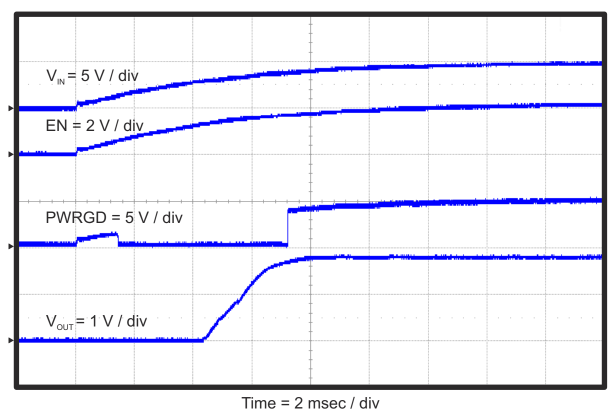


图 8-5. Power Up Relative To VIN

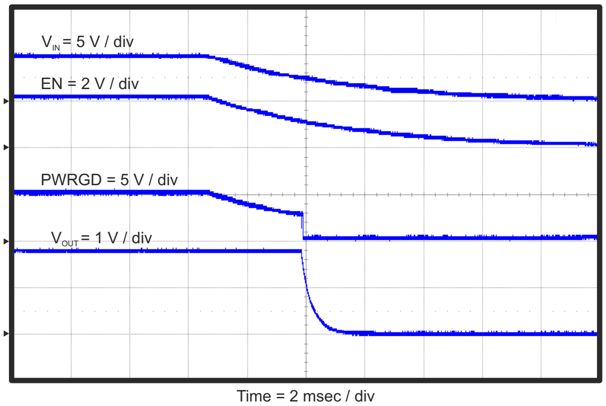


图 8-6. Power Down Relative To VIN

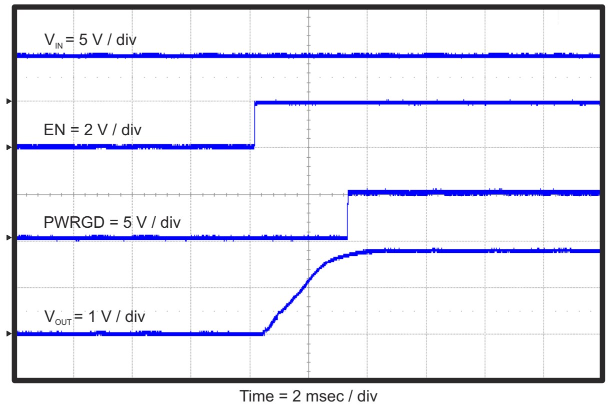


图 8-7. Power Up Relative To EN

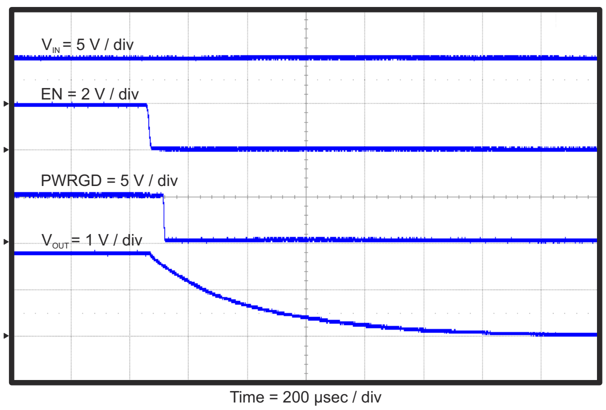


图 8-8. Power Down Relative To EN

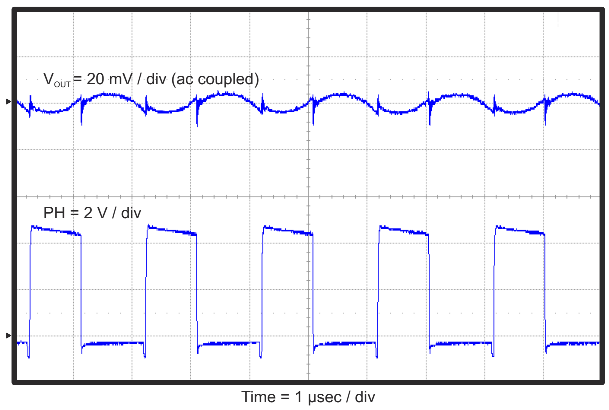


图 8-9. Output Ripple, I_{OUT} = 7 A

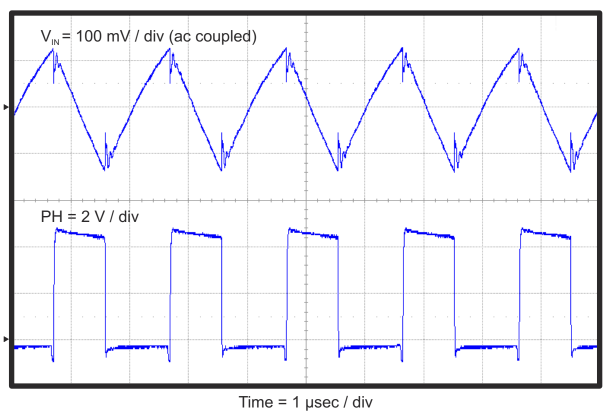


图 8-10. Input Ripple, I_{OUT} = 7 A

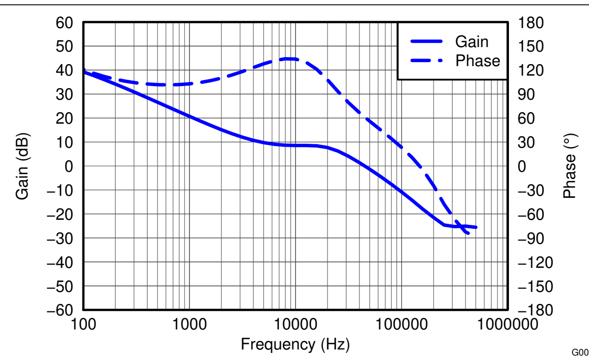


图 8-11. Closed Loop Response, V_{IN} = 5 V, I_{OUT} = 3.5 A

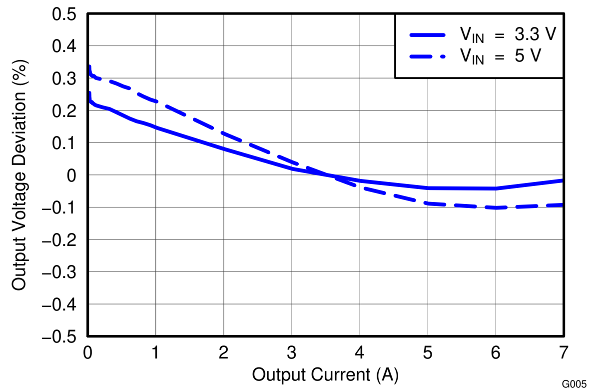
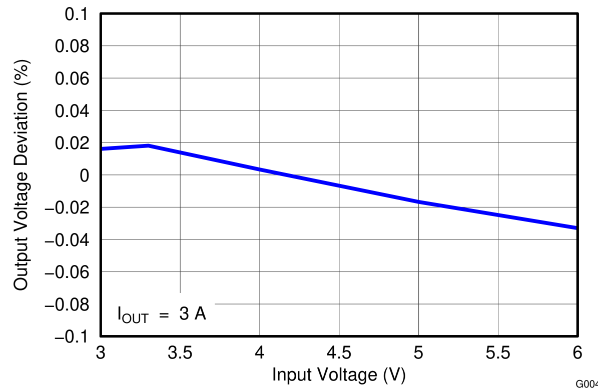


图 8-12. Output Voltage Regulation vs Load Current



I_{OUT} = 3 A

图 8-13. Output Voltage Regulation vs Input Voltage

9 Power Supply Recommendations

The input voltage for VIN pin should be well controlled to avoid exceeding the maximum voltage rating of 7 V; otherwise, the device can have risk of damage.

10 Layout

10.1 Layout Guidelines

Layout is a critical portion of good power supply design. There are several signal paths that conduct fast changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power supplies performance. Care should be taken to minimize the loop area formed by the bypass capacitor connections and the VIN pins. See 图 10-1 for a PCB layout example. The GND pins and AGND pin should be tied directly to the power pad under the IC. The power pad should be connected to any internal PCB ground planes using multiple vias directly under the IC. Additional vias can be used to connect the top side ground area to the internal planes near the input and output capacitors. For operation at full rated load, the top side ground area along with any additional internal ground planes must provide adequate heat dissipating area.

Locate the input bypass capacitor as close to the IC as possible. The PH pin should be routed to the output inductor. Since the PH connection is the switching node, the output inductor should be located very close to the PH pins, and the area of the PCB conductor minimized to prevent excessive capacitive coupling. The boot capacitor must also be located close to the device. The sensitive analog ground connections for the feedback voltage divider, compensation components, slow start capacitor and frequency set resistor should be connected to a separate analog ground trace as shown. The RT pin is particularly sensitive to noise so the RT resistor should be located as close as possible to the IC and routed with minimal lengths of trace. The additional external components can be placed approximately as shown. It may be possible to obtain acceptable performance with alternate PCB layouts, however this layout has been shown to produce good results and is meant as a guideline.

10.2 Layout Example

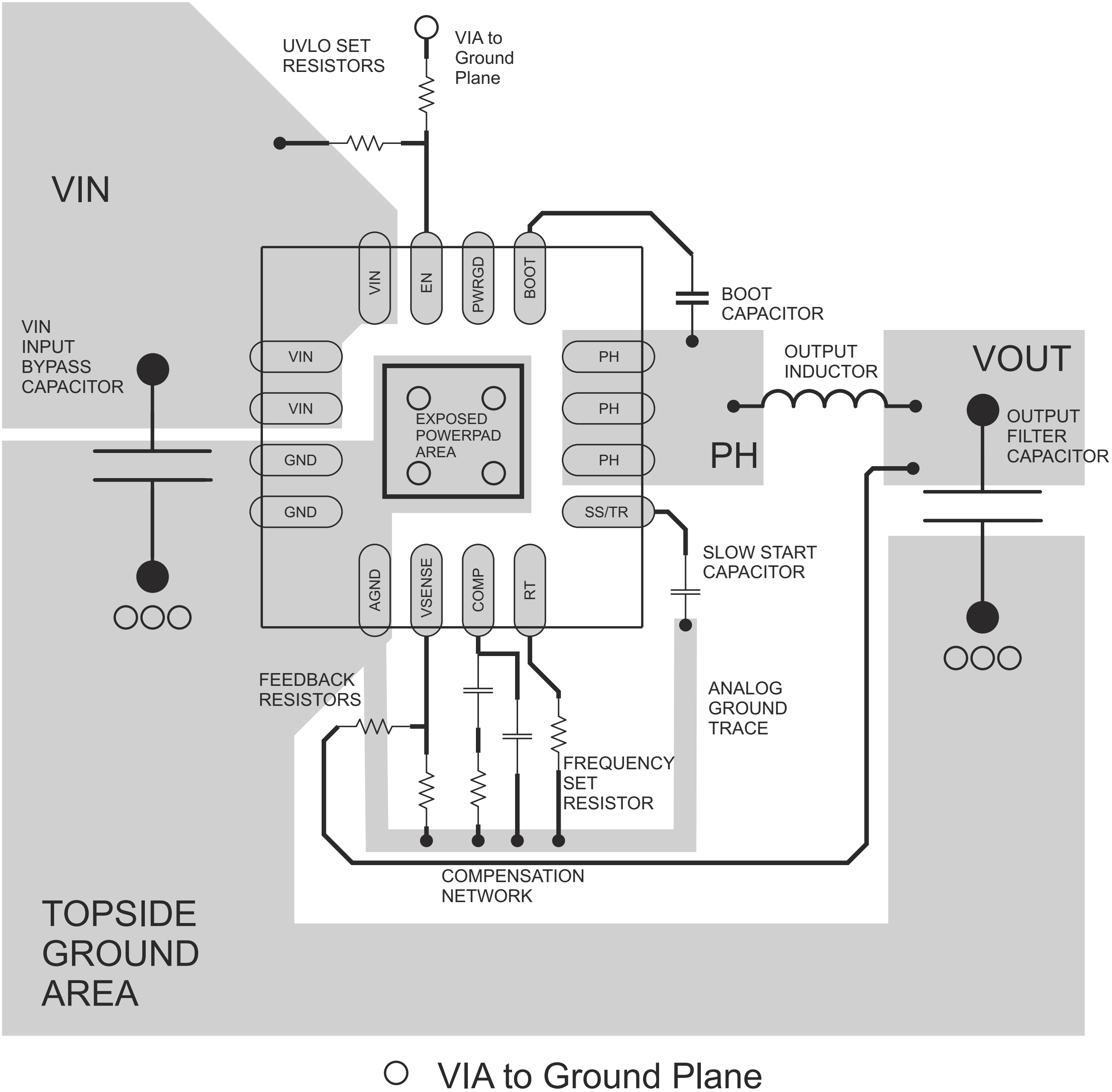


图 10-1. PCB Layout Example

10.2.1 Power Dissipation Estimate

The following formulas show how to estimate the IC power dissipation under continuous conduction mode (CCM) operation. The power dissipation of the IC (Ptot) includes the following:

- Conduction loss (Pcon)
- Dead time loss (Pd)
- Switching loss (Psw)
- Gate drive loss (Pgd)
- Supply current loss (Pq)

$Pcon = Io^2 \times Rdson\_temp$

$Pd = f sw \times Iout \times 0.7 \times 70 \times 10^{-9}$

$Psw = 0.5 \times Vin \times Io \times f sw \times 9 \times 10^{-9}$

$Pgd = 2 \times Vin \times 6 \times 10^{-9} \times f sw$

$Pq = 455 \times 10^{-6} \times Vin$

where:

- IOUT is the output current (A)
- Rdson is the on-resistance of the high-side MOSFET (Ω)
- VIN is the input voltage (V)
- $f$sw is the switching frequency (Hz)

So

Ptot = Pcon + Pd + Psw + Pgd + Pq

For given TA,

TJ = TA + Rth × Ptot

For given TJMAX = 140°C

TAmax = TJMAX – Rth × Ptot

where:

- Ptot is the total device power dissipation (W)
- TA is the ambient temperature (°C)
- TJ is the junction temperature (°C)
- Rth is the thermal resistance of the package (°C/W)
- TJMAX is maximum junction temperature (°C)
- TAMAX is maximum ambient temperature (°C)

There are additional power losses in the regulator circuit due to the inductor AC and DC losses and trace resistance that impact the overall efficiency of the regulator.

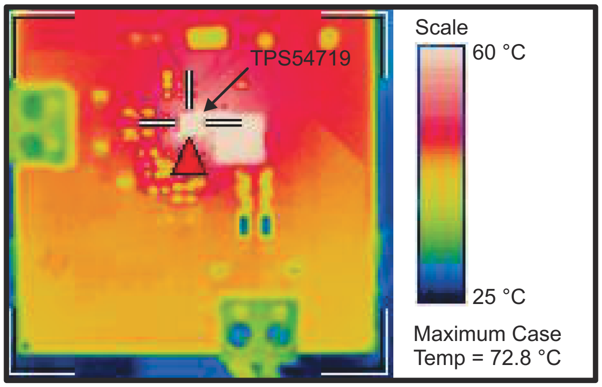


图 10-2. Thermal Image, I_{OUT} = 7 A

11 Device and Documentation Support

11.1 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击 *订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.2 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

11.3 Trademarks

WEBENCH™ and TI E2E™ are trademarks of Texas Instruments.
所有商标均为其各自所有者的财产。

11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

重要声明和免责声明

TI 提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他安全、安保或其他要求。这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 TI 的销售条款 (https:www.ti.com/legal/termsofsale.html) 或 ti.com 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS54719RTER	ACTIVE	WQFN	RTE	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 140	54719	Samples
TPS54719RTET	ACTIVE	WQFN	RTE	16	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 140	54719	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

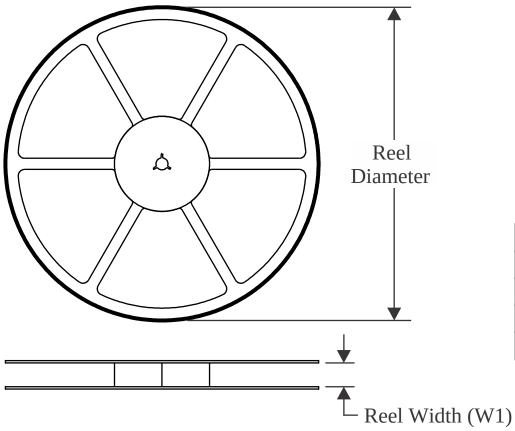
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

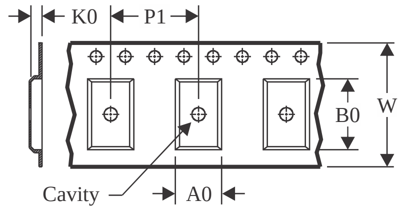
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

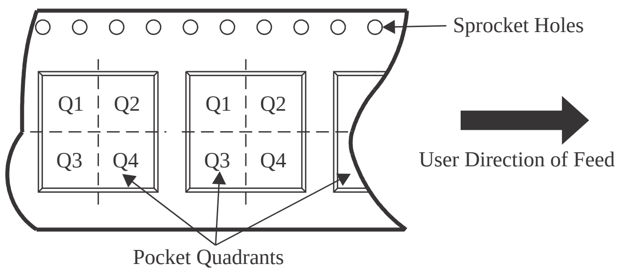


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

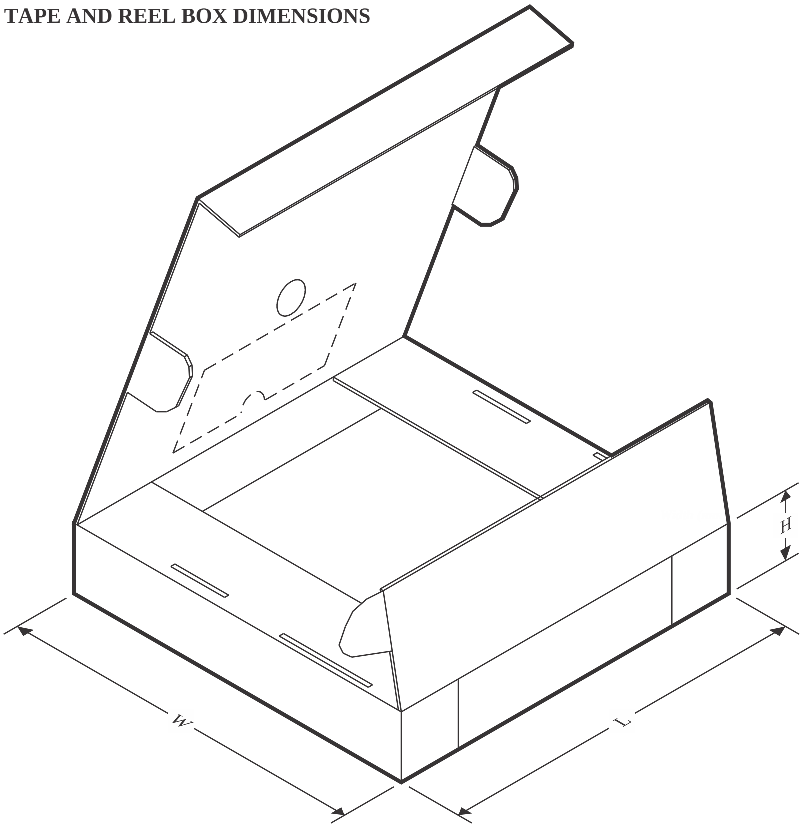
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS54719RTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS54719RTET	WQFN	RTE	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS54719RTER	WQFN	RTE	16	3000	346.0	346.0	33.0
TPS54719RTET	WQFN	RTE	16	250	182.0	182.0	20.0

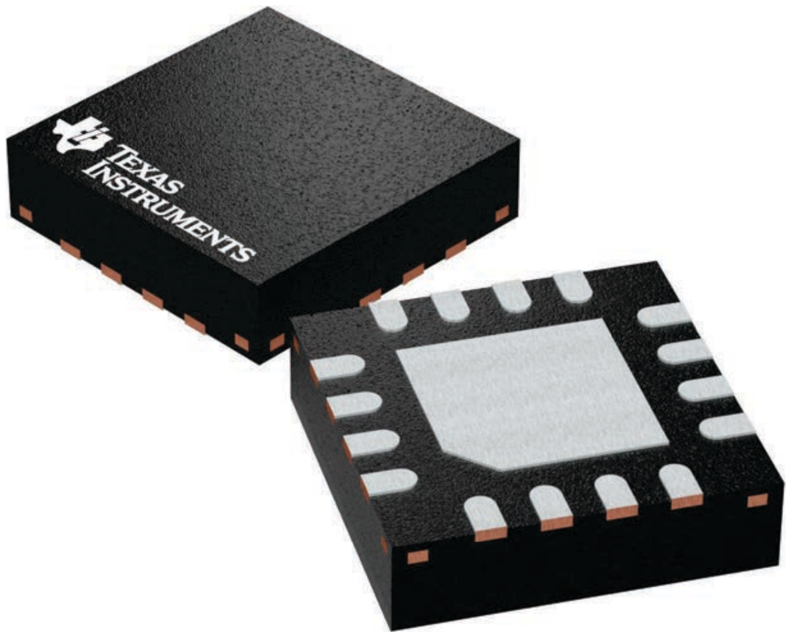
RTE 16

WQFN - 0.8 mm max height

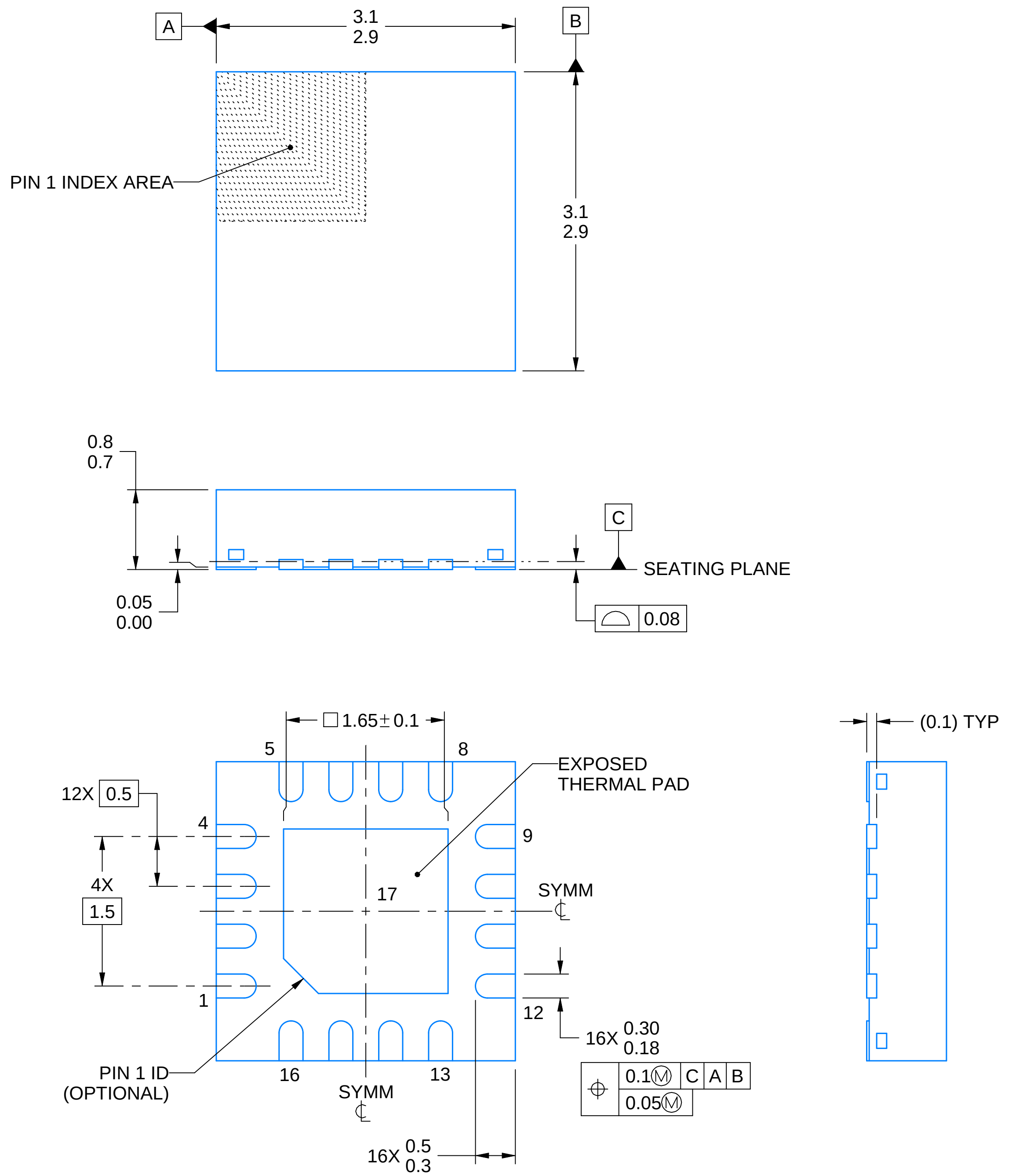
3 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



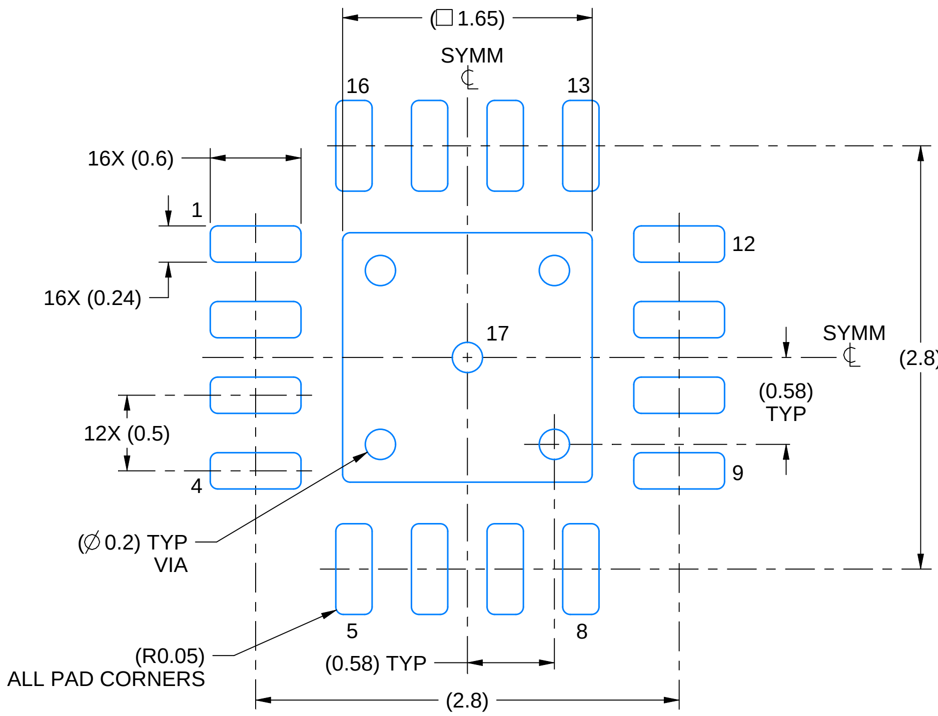
4225944/A



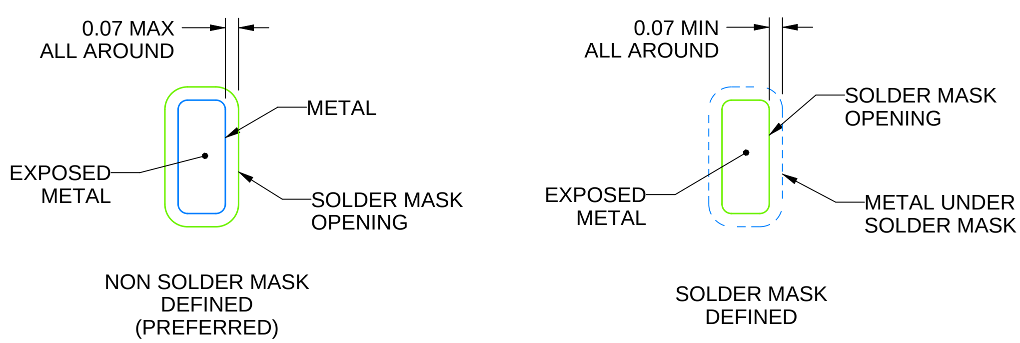
4219119/A 03/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

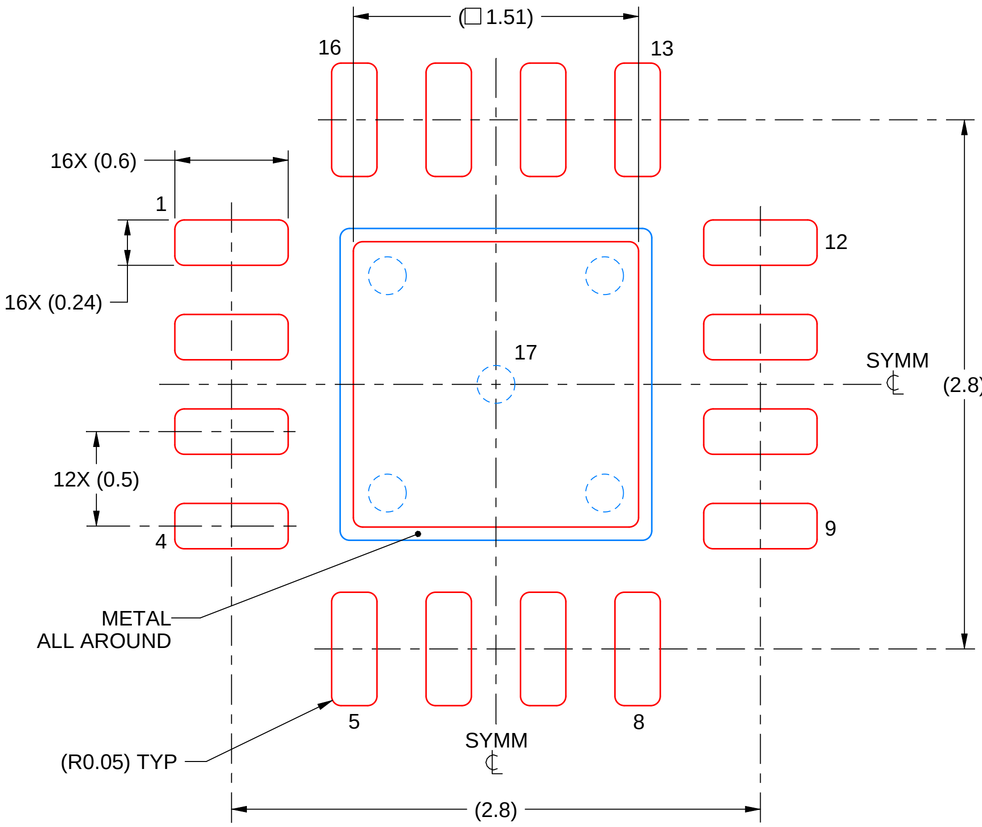


SOLDER MASK DETAILS

4219119/A 03/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
84% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4219119/A 03/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要声明和免责声明

TI“按原样”提供技术和可靠性数据（包括数据表）、设计资源（包括参考设计）、应用或其他设计建议、网络工具、安全信息和其他资源，不保证没有瑕疵且不做出任何明示或暗示的担保，包括但不限于对适销性、某特定用途方面的适用性或不侵犯任何第三方知识产权的暗示担保。

这些资源可供使用 TI 产品进行设计的熟练开发人员使用。您将自行承担以下全部责任：(1) 针对您的应用选择合适的 TI 产品，(2) 设计、验证并测试您的应用，(3) 确保您的应用满足相应标准以及任何其他功能安全、信息安全、监管或其他要求。

这些资源如有变更，恕不另行通知。TI 授权您仅可将这些资源用于研发本资源所述的 TI 产品的应用。严禁对这些资源进行其他复制或展示。您无权使用任何其他 TI 知识产权或任何第三方知识产权。您应全额赔偿因在这些资源的使用中对 TI 及其代表造成的任何索赔、损害、成本、损失和债务，TI 对此概不负责。

TI 提供的产品受 TI 的销售条款或 ti.com 上其他适用条款/TI 产品随附的其他适用条款的约束。TI 提供这些资源并不会扩展或以其他方式更改 TI 针对 TI 产品发布的适用的担保或担保免责声明。

TI 反对并拒绝您可能提出的任何其他或不同的条款。

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265