具有 5.5μA 静态电流的低输入电压，0.7V 升压转换器

查询样品: TPS61222-EP

特性

- 在典型工作条件下效率高达 **95%**
- **5.5μA** 静态电流
- 在输入电压为 **0.7V** 时启动进入负载
- 运行输入电压范围为 **0.7V** 至 **5.5V**
- 停机期间具有导通功能
- 最小开关电流为 **200mA**
- 保护特性：
  - 输出过压
  - 过热
  - 输入欠压闭锁
- 固定输出电压版本
- 小型 **6** 引脚 **SC-70** 封装

应用范围

- 电池供电型应用
  - **1** 至 **3** 节碱性电池、镍镉电池 **(NiCd)** 或者镍氢电池 **(NiMH)**
  - **1** 节锂离子或者锂离子一次性电池
- 太阳能或者燃料供电类应用
- 消费类及便携式医疗产品
- 个人护理产品
- 白色或者状态发光二极管 **(LED)**
- 智能电话

支持国防、航空航天、和医疗应用

- 受控基线
- 一个组装和测试场所
- 一个制造场所
- 支持军用（**-55°C** 至 **125°C**）温度范围 (1)
- 延长的产品生命周期
- 延长的产品变更通知
- 产品可追溯性

(1) 可定制工作温度范围

说明

TLV61222 为通过单节、双节、或者三节碱性，NiCd 或者 NiMH，或单节锂离子或者锂聚合物电池供电的产品提供电源解决方案。 可实现的输出电流取决于输入输出电压比。 升压转换器建立在采用同步整流的磁滞控制器拓扑基础之上，能够以最少的静态电流实现最高的效率。 可通过一个外部电阻分压器对此可调版本的输出电压进行设定，或者可将此电压内部设定为一个固定值。 此转换器可由一个特定的使能引脚关闭。 关闭时，电池消耗降至最低。 该器件采用 2mm x 2mm 6 引脚 SC-70 封装 (DCK) 以支持最小电路布局尺寸。

English Data Sheet: SLVSBI2

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

AVAILABLE DEVICE OPTIONS(1)

T_J	PACKAGE MARKING	PACKAGE(2)	PART NUMBER	VID NUMBER
–55°C to 125°C	SHL	6-Pin SC-70	TPS61222MDCKTEP	V62/12603-01XE

(1) Contact the factory to check availability of other fixed output voltage versions.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

			UNIT
V_{IN}	Input voltage range on VIN, L, VOUT, EN, FB	–0.3 to 7.5	V
T_J	Operating junction temperature range	–55 to 145	°C
T_{stg}	Storage temperature range	–65 to 150	°C
ESD	Human Body Model (HBM)(2)	2	kV
	Machine Model (MM)(2)	200	V
	Charged Device Model (CDM)(2)	1.5	kV

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) ESD testing is performed according to the respective JESD22 JEDEC standard.

THERMAL INFORMATION

THERMAL METRIC(1)		TPS61222	UNITS
		DCK	
		6 PINS	
$θ_{JA}$	Junction-to-ambient thermal resistance(2)	231.2	°C/W
$θ_{JCtop}$	Junction-to-case (top) thermal resistance(3)	61.8	
$θ_{JB}$	Junction-to-board thermal resistance(4)	78.8	
$ψ_{JT}$	Junction-to-top characterization parameter(5)	2.2	
$ψ_{JB}$	Junction-to-board characterization parameter(6)	78	
$θ_{JCbot}$	Junction-to-case (bottom) thermal resistance(7)	N/A	

(1) 有关传统和新的热 度量的更多信息，请参阅*IC 封装热度量*应用报告， SPRA953。
(2) 在 JESD51-2a 描述的环境中，按照 JESD51-7 的指定，在一个 JEDEC 标准高 K 电路板上进行仿真，从而获得自然 对流条件下的结至环境热阻。
(3) 通过在封装顶部模拟一个冷板测试来获得结至芯片外壳（顶部）的热阻。 不存在特定的 JEDEC 标准测试，但 可在 ANSI SEMI 标准 G30-88 中能找到内容接近的说明。
(4) 按照 JESD51-8 中的说明，通过 在配有用于控制 PCB 温度的环形冷板夹具的环境中进行仿真，以获得结板热阻。
(5) 结至顶部特征参数， $ψ_{JT}$，估算真实系统中器件的结温，并使用 JESD51-2a（第 6 章和第 7 章）中 描述的程序从仿真数据中 提取出该参数以便获得 $θ_{JA}$。
(6) 结至电路板特征参数， $ψ_{JB}$，估算真实系统中器件的结温，并使用 JESD51-2a（第 6 章和第 7 章）中 描述的程序从仿真数据中 提取出该参数以便获得 $θ_{JA}$ 。
(7) 通过在外露（电源）焊盘上进行冷板测试仿真来获得 结至芯片外壳（底部）热阻。 不存在特定的 JEDEC 标准 测试，但可在 ANSI SEMI 标准 G30-88 中能找到内容接近的说明。

RECOMMENDED OPERATING CONDITIONS

		MIN	NOM	MAX	UNIT
V_{IN}	Supply voltage at VIN	0.7		5.5	V
T_J	Operating free air temperature range	–55		125	°C

ELECTRICAL CHARACTERISTICS

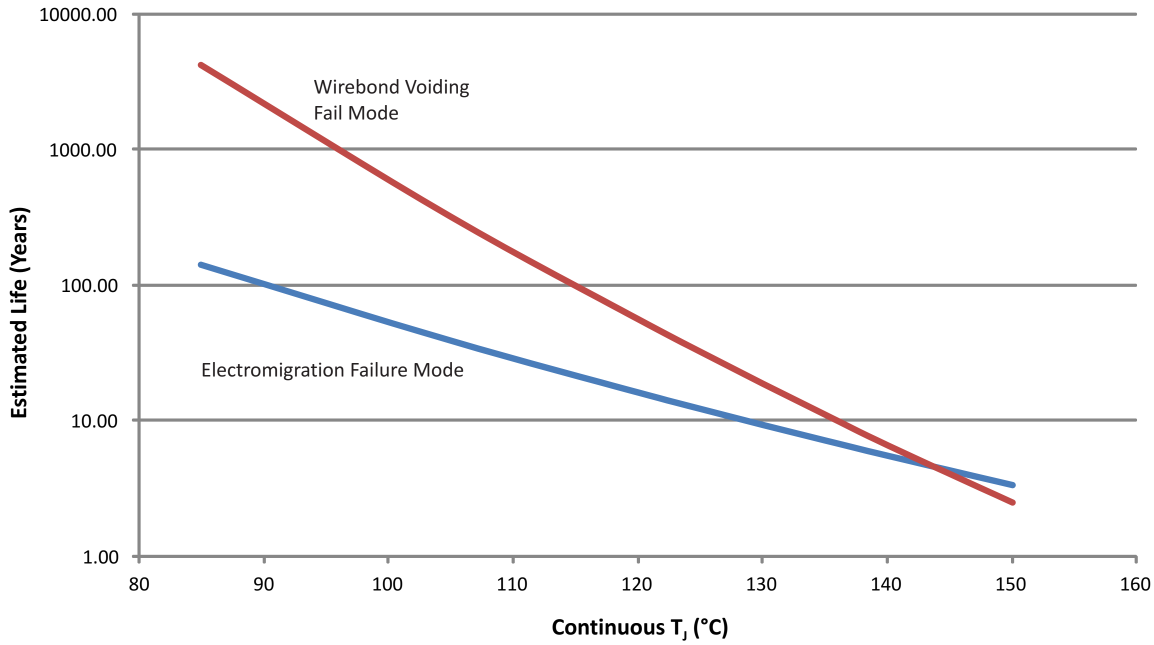
T_J = −55°C to 125°C, T_J = T_A and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

DC/DC STAGE

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range			0.7		5.5	V
V_{IN}	Minimum input voltage at startup		R_{Load} ≥ 150 Ω			0.7	V
V_{OUT}	Output voltage (5 V)		V_{IN} < V_{OUT}	4.8	5	5.19	V
I_{LH}	Inductor current ripple				200		mA
I_{SW}	Switch current limit		V_{OUT} = 5 V, V_{IN} = 1.2 V	200	400		mA
R_{DSon_HSD}	Rectifying switch on resistance		V_{OUT} = 5 V		700		mΩ
R_{DSon_LSD}	Main switch on resistance		V_{OUT} = 5 V		550		mΩ
	Line regulation		V_{IN} < V_{OUT}		0.5		%
	Load regulation		V_{IN} < V_{OUT}		0.5		%
I_Q	Quiescent current	V_{IN}	I_O = 0 mA, V_{EN} = V_{IN} = 1.2 V, V_{OUT} = 5 V		0.5	1.4	μA
		V_{OUT}			5	8.5	μA
I_{SD}	Shutdown current	V_{IN}	V_{EN} = 0 V, V_{IN} = 1.2 V, V_{OUT} ≥ V_{IN}		0.2	0.96	μA
I_{LKG_L}	Leakage current into L		V_{EN} = 0 V, V_{IN} = 1.2 V, V_L = 1.2 V, V_{OUT} ≥ V_{IN}		0.01	0.3	μA
I_{EN}	EN input current		Clamped on GND or V_{IN} (V_{IN} < 1.5 V)		0.005	0.13	μA

CONTROL STAGE

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IL}	EN input low voltage	V_{IN} ≤ 1.5 V			0.15 × V_{IN}	V
V_{IH}	EN input high voltage	V_{IN} ≤ 1.5 V	0.8 × V_{IN}			V
V_{IL}	EN input low voltage	5 V > V_{IN} > 1.5 V			0.34	V
V_{IH}	EN input high voltage	5 V > V_{IN} > 1.5 V	1.28			V
V_{UVLO}	Undervoltage lockout threshold for turn off	V_{IN} decreasing		0.5	0.72	V
	Overvoltage protection threshold		5.5		7.5	V
	Overtemperature protection			140		°C
	Overtemperature hysteresis			20		°C



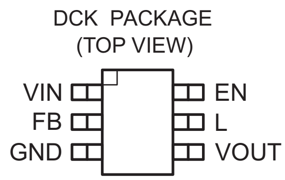
(1) See data sheet for absolute maximum and minimum recommended operating conditions.

(2) Silicon operating life design goal is 10 years at 105°C junction temperature (does not include package interconnect life).

(3) Enhanced plastic product disclaimer applies.

Figure 1. TPS61222-EP Operating Life Derating Chart

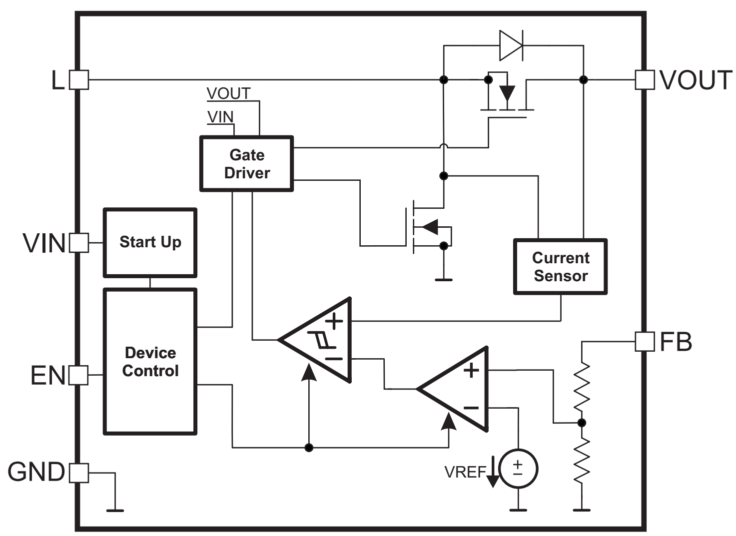
PIN ASSIGNMENTS



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
EN	6	I	Enable input (1: enabled, 0: disabled). Must be actively tied high or low.
FB	2	I	Voltage feedback of adjustable version. Must be connected to V_{OUT} at fixed output voltage versions.
GND	3		Control / logic and power ground
L	5	I	Connection for Inductor
VIN	1	I	Boost converter input voltage
VOUT	4	O	Boost converter output voltage

FUNCTIONAL BLOCK DIAGRAM



PARAMETER MEASUREMENT INFORMATION

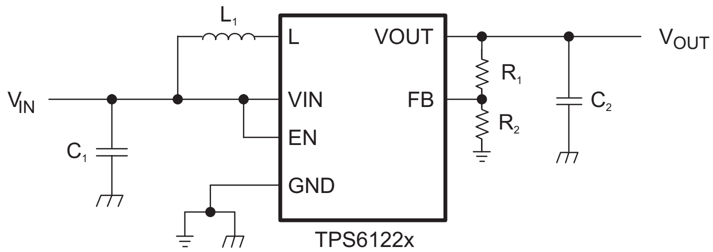


Table 1. List of Components[1]

COMPONENT REFERENCE	PART NUMBER	MANUFACTURER	VALUE
C_1	GRM188R60J106ME84D	Murata	10 μF, 6.3V. X5R Ceramic
C_2	GRM188R60J106ME84D	Murata	10 μF, 6.3V. X5R Ceramic
L_1	EPL3015-472MLB	Coilcraft	4.7 μH
R_1, R_2			adjustable version: Values depending on the programmed output voltage
			fixed version: R_1= 0 Ω, R_2 not used

(1) Design was tested using these components at 25°C ambient temperature.

TYPICAL CHARACTERISTICS

Table of Graphs

		FIGURE
Maximum Output Current	vs Input Voltage	Figure 2
Efficiency	vs Output Current, V_{IN} = [0.7 V; 1.2 V; 2.4V; 3.6 V; 4.2 V]	Figure 3
	vs Input Voltage, I_{OUT} = [100 uA; 1 mA; 10 mA; 50 mA]	Figure 4
Input Current	at No Output Load, Device Enabled	Figure 5
Output Voltage	vs Output Current, V_{IN} = [0.7 V; 1.2 V; 2.4 V; 3.6 V]	Figure 6
Waveforms	Load Transient Response, V_{IN} = 2.4 V, I_{OUT} = 14 mA to 126 mA	Figure 7
	Line Transient Response, V_{IN} = 2.8 V to 3.6 V, R_{LOAD} = 100 Ω	Figure 8

MAXIMUM OUTPUT CURRENT vs INPUT VOLTAGE

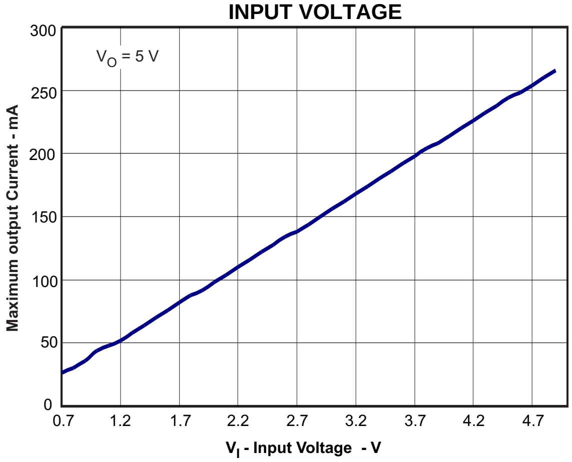


Figure 2.

EFFICIENCY vs OUTPUT CURRENT AND INPUT VOLTAGE

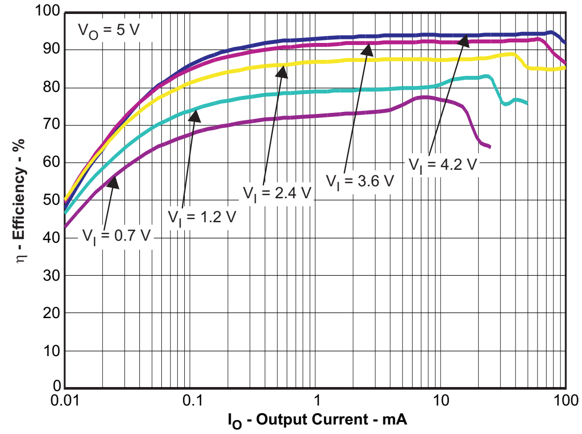


Figure 3.

EFFICIENCY vs INPUT VOLTAGE AND OUTPUT CURRENT

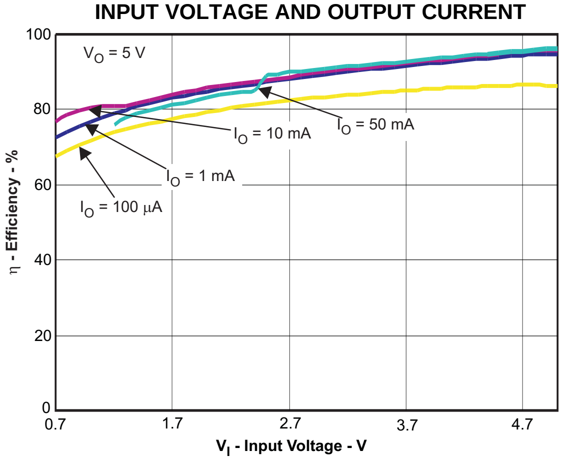


Figure 4.

NO LOAD INPUT CURRENT vs INPUT VOLTAGE, DEVICE ENABLED

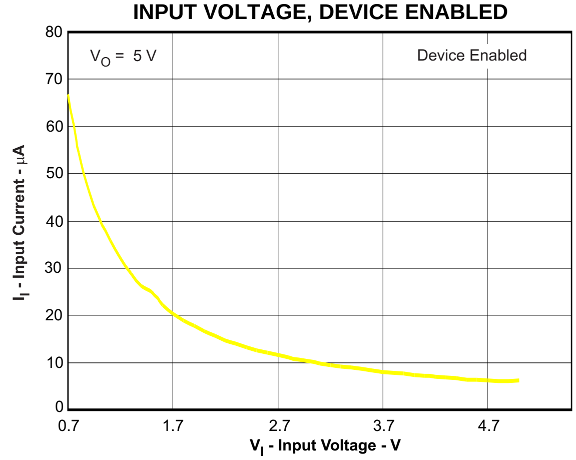


Figure 5.

OUTPUT VOLTAGE
vs
OUTPUT CURRENT AND INPUT VOLTAGE

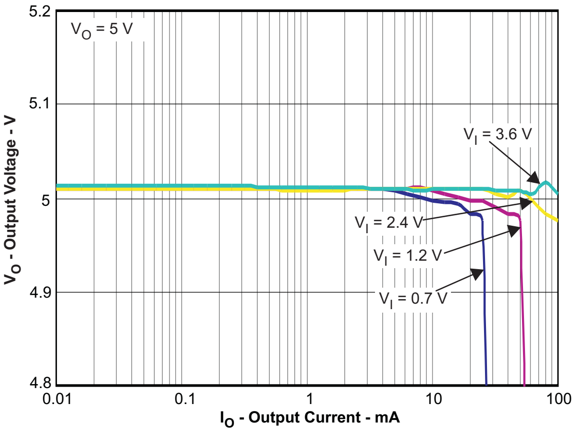


Figure 6.

LOAD TRANSIENT RESPONSE

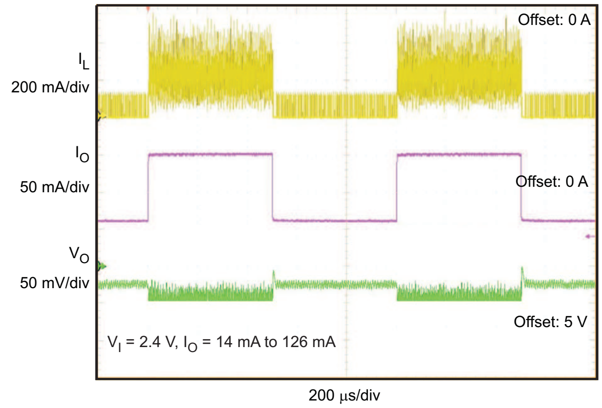


Figure 7.

LINE TRANSIENT RESPONSE

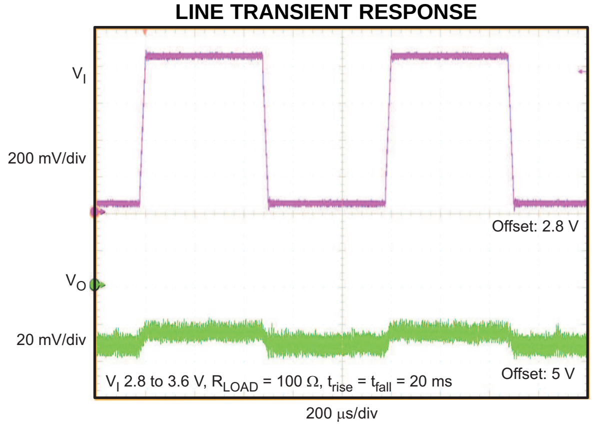


Figure 8.

DETAILED DESCRIPTION

OPERATION

The TPS61222 is a high performance, high efficient switching boost converter. To achieve high efficiency the power stage is realized as a synchronous boost topology. For the power switching two actively controlled low R_{DSon} power MOSFETs are implemented.

CONTROLLER CIRCUIT

The device is controlled by a hysteretic current mode controller. This controller regulates the output voltage by keeping the inductor ripple current constant in the range of 200 mA and adjusting the offset of this inductor current depending on the output load. In case the required average input current is lower than the average inductor current defined by this constant ripple the inductor current gets discontinuous to keep the efficiency high at low load conditions.

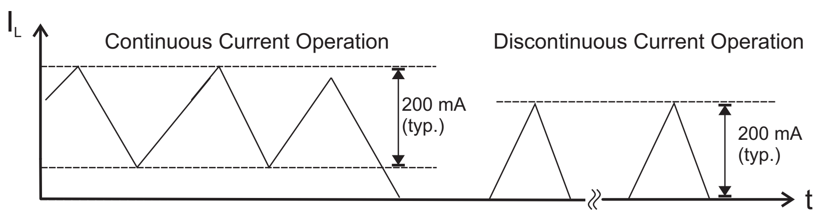


Figure 9. Hysteretic Current Operation

The output voltage V_{OUT} is monitored via the feedback network which is connected to the voltage error amplifier. To regulate the output voltage, the voltage error amplifier compares this feedback voltage to the internal voltage reference and adjusts the required offset of the inductor current accordingly. At fixed output voltage versions an internal feedback network is used to program the output voltage, at adjustable versions an external resistor divider needs to be connected.

The self oscillating hysteretic current mode architecture is inherently stable and allows fast response to load variations. It also allows using inductors and capacitors over a wide value range.

Device Enable and Shutdown Mode

The device is enabled when EN is set high and shut down when EN is low. During shutdown, the converter stops switching and all internal control circuitry is turned off. In this case the input voltage is connected to the output through the back-gate diode of the rectifying MOSFET. This means that there always will be voltage at the output which can be as high as the input voltage or lower depending on the load.

Startup

After the EN pin is tied high, the device starts to operate. In case the input voltage is not high enough to supply the control circuit properly a startup oscillator starts to operate the switches. During this phase the switching frequency is controlled by the oscillator and the maximum switch current is limited. As soon as the device has built up the output voltage to about 1.8V, high enough for supplying the control circuit, the device switches to its normal hysteretic current mode operation. The startup time depends on input voltage and load current.

Operation at Output Overload

If in normal boost operation the inductor current reaches the internal switch current limit threshold the main switch is turned off to stop further increase of the input current.

In this case the output voltage will decrease since the device can not provide sufficient power to maintain the set output voltage.

If the output voltage drops below the input voltage the backgate diode of the rectifying switch gets forward biased and current starts flow through it. This diode cannot be turned off, so the current finally is only limited by the remaining DC resistances. As soon as the overload condition is removed, the converter resumes providing the set output voltage.

Undervoltage Lockout

An implemented undervoltage lockout function stops the operation of the converter if the input voltage drops below the typical undervoltage lockout threshold. This function is implemented in order to prevent malfunctioning of the converter.

Overvoltage Protection

If, for any reason, the output voltage is not fed back properly to the input of the voltage amplifier, control of the output voltage will not work anymore. Therefore an overvoltage protection is implemented to avoid the output voltage exceeding critical values for the device and possibly for the system it is supplying. For this protection the TPS61222 output voltage is also monitored internally. In case it reaches the internally programmed threshold of 6.5 V typically the voltage amplifier regulates the output voltage to this value.

If the TPS61222 is used to drive LEDs, this feature protects the circuit if the LED fails.

Overtemperature Protection

The device has a built-in temperature sensor which monitors the internal IC junction temperature. If the temperature exceeds the programmed threshold (see electrical characteristics table), the device stops operating. As soon as the IC temperature has decreased below the programmed threshold, it starts operating again. To prevent unstable operation close to the region of overtemperature threshold, a built-in hysteresis is implemented.

APPLICATION INFORMATION

DESIGN PROCEDURE

The TPS61222 DC/DC converter is intended for systems powered by a single cell battery to up to three Alkaline, NiCd or NiMH cells with a typical terminal voltage between 0.7 V and 5.5 V. It can also be used in systems powered by one-cell Li-Ion or Li-Polymer batteries with a typical voltage between 2.5 V and 4.2 V. Additionally, any other voltage source with a typical output voltage between 0.7 V and 5.5 V can be used with the TPS61222.

Programming the Output Voltage

Output voltage

The output voltage is set by a resistor divider internally. The FB pin is used to sense the output voltage. To configure the fixed output devices properly, the FB pin needs to be connected directly to VOUT as shown in Figure 10.

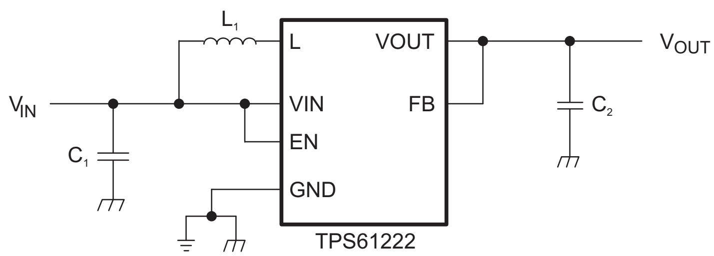


Figure 10. Typical Application Circuit

Inductor Selection

To make sure that the TPS61222 can operate, a suitable inductor must be connected between pin VIN and pin L. Inductor values of 4.7 µH show good performance over the whole input and output voltage range .

Choosing other inductance values affects the switching frequency *f* proportional to 1/L as shown in Equation 1.

$$L = \frac{1}{f \times 200\ mA} \times \frac{V_{IN} \times (V_{OUT} - V_{IN})}{V_{OUT}} \tag{1}$$

Choosing inductor values higher than 4.7 µH can improve efficiency due to reduced switching frequency and therefore with reduced switching losses. Using inductor values below 2.2 µH is not recommended.

Having selected an inductance value, the peak current for the inductor in steady state operation can be calculated. Equation 2 gives the peak current estimate.

$$I_{L,MAX} = \begin{cases} \frac{V_{OUT} \times I_{OUT}}{0.8 \times V_{IN}} + 100\ mA; & \text{continous current operation} \\ 200\ mA; & \text{discontinuous current operation} \end{cases} \tag{2}$$

For selecting the inductor this would be the suitable value for the current rating. It also needs to be taken into account that load transients and error conditions may cause higher inductor currents.

Equation 3 provides an easy way to estimate whether the device will work in continuous or discontinuous operation depending on the operating points. As long as the inequation is true, continuous operation is typically established. If the inequation becomes false, discontinous operation is typically established.

$$\frac{V_{OUT} \times I_{OUT}}{V_{IN}} > 0.8 \times 100\ mA \tag{3}$$

The following inductor series from different suppliers have been used with TPS61222 converters:

Table 2. List of Inductors(1)

VENDOR	INDUCTOR SERIES
Coilcraft	EPL3015
	EPL2010
Murata	LQH3NP
Tajo Yuden	NR3015
Wurth Elektronik	WE-TPC Typ S

(1) Design was tested using these components at 25°C ambient temperature.

Capacitor Selection

Input Capacitor

At least a 10-µF input capacitor is recommended to improve transient behavior of the regulator and EMI behavior of the total power supply circuit. A ceramic capacitor placed as close as possible to the VIN and GND pins of the IC is recommended.

Output Capacitor

For the output capacitor C_2 , it is recommended to use small ceramic capacitors placed as close as possible to the VOUT and GND pins of the IC. If, for any reason, the application requires the use of large capacitors which can not be placed close to the IC, the use of a small ceramic capacitor with an capacitance value of around 2.2µF in parallel to the large one is recommended. This small capacitor should be placed as close as possible to the VOUT and GND pins of the IC.

A minimum capacitance value of 4.7 µF should be used, 10 µF are recommended. If the inductor value exceeds 4.7 µH, the value of the output capacitance value needs to be half the inductance value or higher for stability reasons, see Equation 4.

$$C_2 \geq \frac{L}{2} \times \frac{\mu F}{\mu H} \tag{4}$$

The TPS61222 is not sensitive to the ESR in terms of stability. Using low ESR capacitors, such as ceramic capacitors, is recommended anyway to minimize output voltage ripple. If heavy load changes are expected, the output capacitor value should be increased to avoid output voltage drops during fast load transients.

Layout Considerations

As for all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator could show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current path and for the power ground paths. The input and output capacitor, as well as the inductor should be placed as close as possible to the IC.

The feedback divider should be placed as close as possible to the control ground pin of the IC. To lay out the ground, it is recommended to use short traces as well, separated from the power ground traces. This avoids ground shift problems, which can occur due to superimposition of power ground current and control ground current. Assure that the ground traces are connected close to the device GND pin.

THERMAL INFORMATION

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below.

- Improving the power-dissipation capability of the PCB design
- Improving the thermal coupling of the component to the PCB
- Introducing airflow in the system

For more details on how to use the thermal parameters in the dissipation ratings table please check the Thermal Characteristics Application Note (SZZA017) and the IC Package Thermal Metrics Application Note (SPRA953).

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS61222MDCKTEP	ACTIVE	SC70	DCK	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 145	SHL	Samples
V62/12603-01XE	ACTIVE	SC70	DCK	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 145	SHL	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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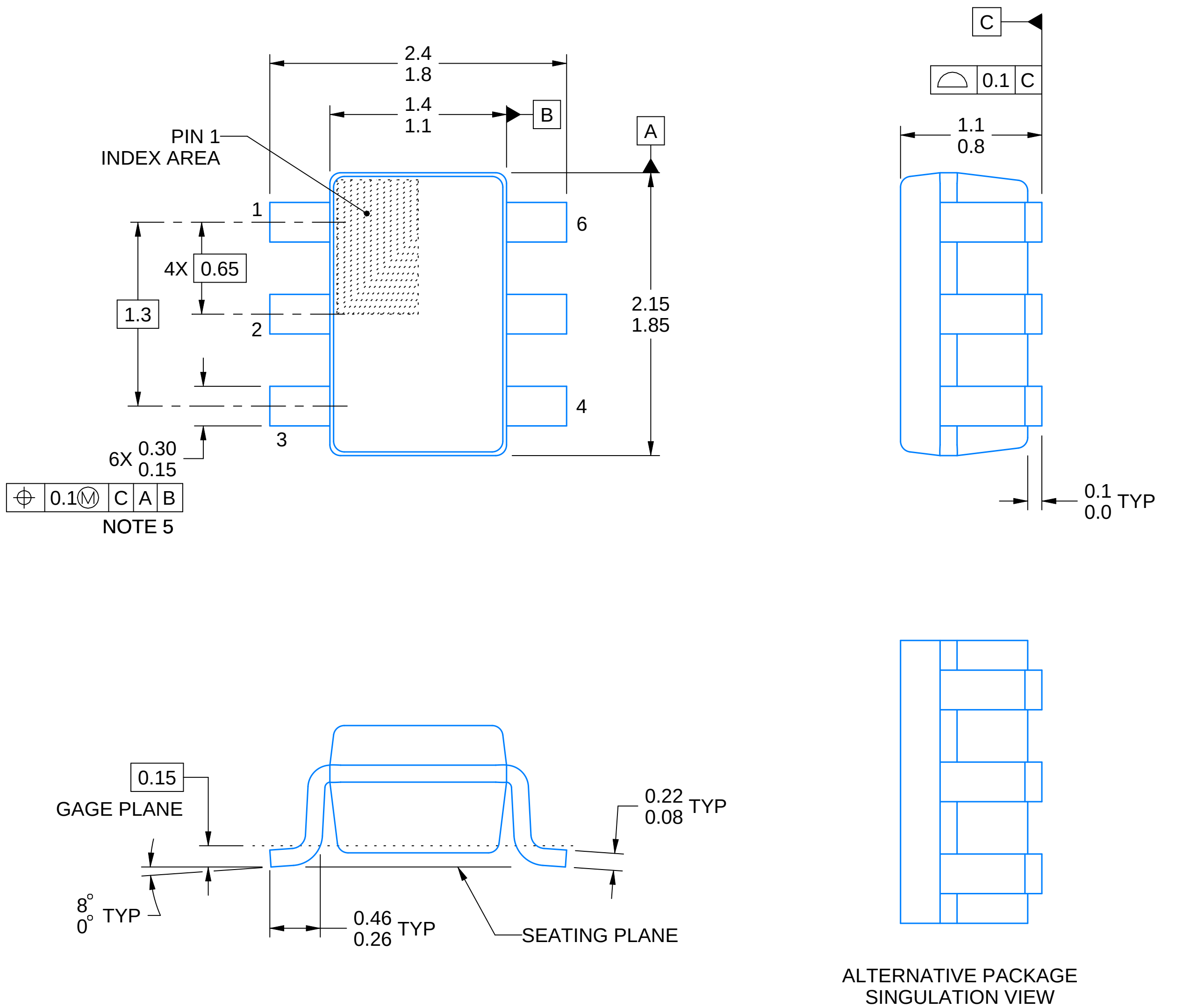
OTHER QUALIFIED VERSIONS OF TPS61222-EP :

- Catalog : TPS61222

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product



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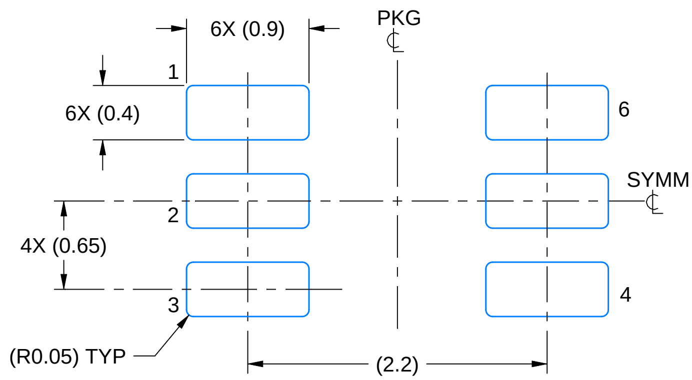
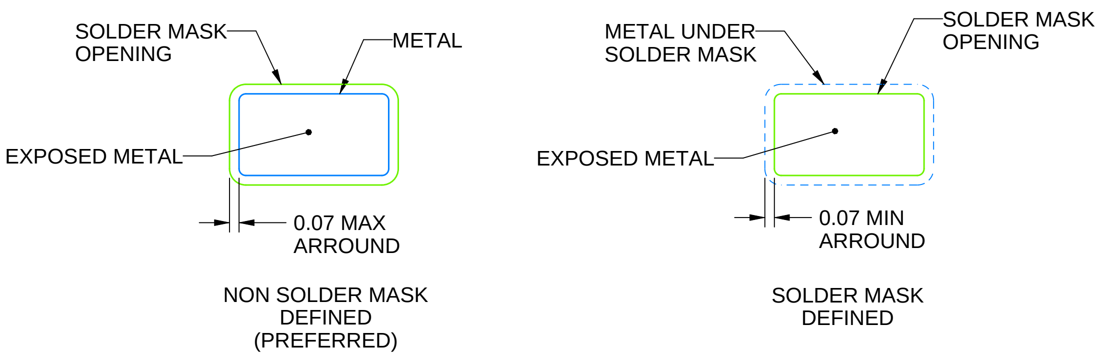
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
4. Falls within JEDEC MO-203 variation AB.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X



SOLDER MASK DETAILS

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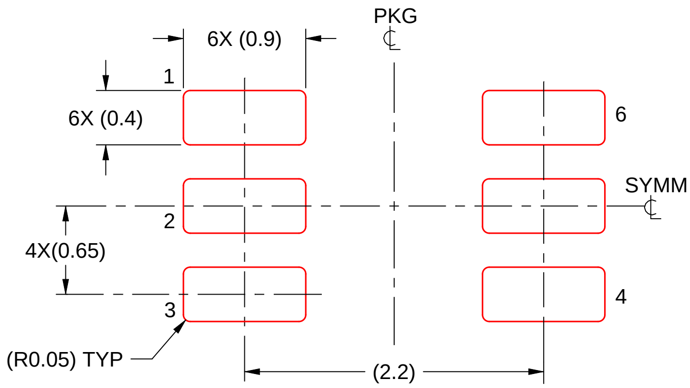
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.