TPS65200 Li+ Battery Charger With WLED Driver and Current Shunt Monitor

1 Features

- Battery Switching Charger, WLED Driver, and Current Shunt Monitor in a Single Package
- Battery Charger
  - Charges Faster Than Linear Chargers
  - High-Accuracy Voltage and Current Regulation
    - Input Current Regulation Accuracy: ±5% (100 mA, 500 mA)
    - Charge Voltage Regulation Accuracy: ±0.5% (25°C) ±1% (0 - 125°C)
    - Charge Current Regulation Accuracy: ±5%
  - Bad Adaptor Detection and Rejection
  - Safety Limit Register for Maximum Charge Voltage and Current Limiting
  - High-Efficiency Mini-USB/AC Battery Charger for Single-Cell Li-Ion and Li-Polymer Battery Packs
  - Built-In Input Current Sensing and Limiting
  - Integrated Power FETs for Up to 1.25-A Charge Rate
  - Programmable Charge Parameters through I^2C Interface (Up to 400 Kbps):
    - Input Current
    - Fast-Charge/Termination Current
    - Charge Voltage (3.5 V - 4.44 V)
    - Safety Timer
    - Termination Enable
  - Synchronous Fixed-Frequency PWM Controller Operating at 3 MHz With 0% to 99.5% Duty Cycle
  - Safety Timer With Reset Control
  - Reverse Leakage Protection Prevents Battery Drainage
  - Thermal Regulation and Protection
  - Input/Output Overvoltage Protection
  - Automatic Charging
  - Boost Mode Operation for USB OTG
    - Input Voltage Range (VSYS): 2.5 V to 4.5 V
    - Output Voltage for VBUS: 5 V
- WLED Driver
  - 35-V Open LED Protection for Up to 8 LEDs
  - 200-mV Reference Voltage With ±2% Accuracy
  - Built-In Soft Start for WLED Boost
  - Up to 90% Efficiency
- Current Shunt Monitor
  - Fixed Gain of 25 V/V
  - Input Referred Offset Voltage Less Than ±40 µV Typical Enables Use of Shunt Resistors as Low as 20 mΩ
  - Buffered Reference Voltage
- Package
  - 36-Ball, 0.4-mm Pitch DSBGA Package

2 Applications

- Mobile Phones and Smart Phones
- MP3 Players
- Portable Navigation Devices
- Handheld Devices

3 Description

The TPS65200 device integrates a high-efficiency, USB-friendly switched-mode charger with OTG support for single-cell Li-ion and Li-polymer batteries, D+D- detection, a 50-mA fixed-voltage LDO, a high-efficiency WLED boost converter, and high-accuracy current-shunt monitor into a single chip.

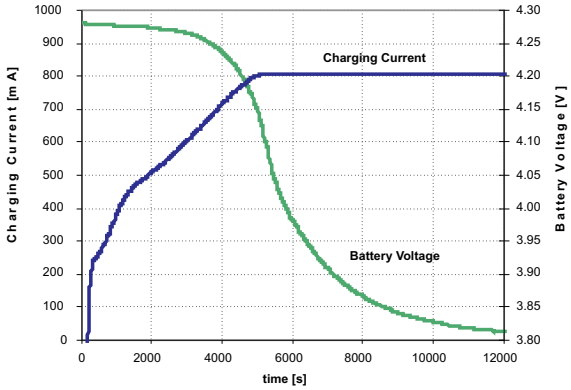
The TPS65200 comes in a tiny, 2.8-mm × 2.6-mm, 36-pin, 0.4-mm pitch die size ball grid array (DSBGA).

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS65200	DSBGA (36)	2.60 mm × 2.90 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Charging Curve



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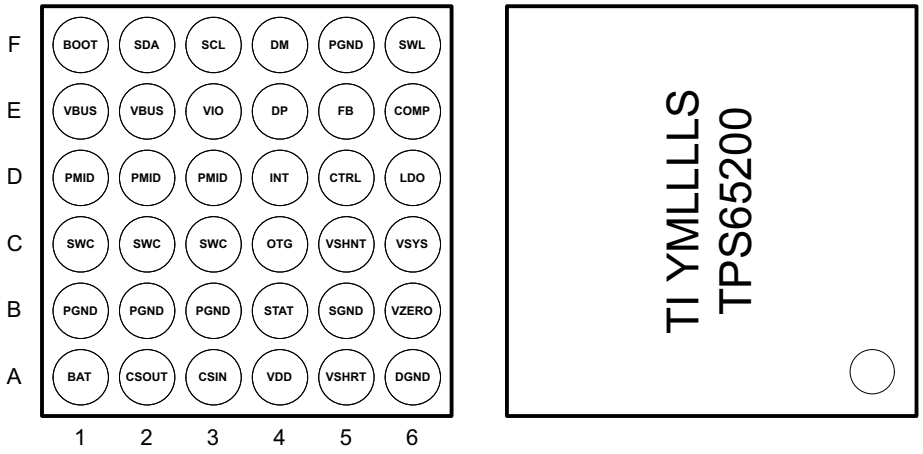
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (April 2010) to Revision A	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section	1

5 Pin Configuration and Functions

YFF Package
36-Pin DSBGA
Bottom View, Top View



TI = TI LETTERS
YM = YEAR / MONTH DATE CODE
LLLL = LOT TRACE CODE
S = ASSEMBLY SITE CODE

O = Pin A1 (Filled Solid)

Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
A1	BAT	O	Output of the linear charger and battery voltage sense. Connect the battery from this pin to ground.
A2	CSOUT	I	Charge current-sense input. Battery current is sensed through the voltage drop across an external sense resistor. A 0.1-µF ceramic capacitor to PGND is required.
A3	CSIN	I	Charge current-sense input. Battery current is sensed through the voltage drop across an external sense resistor. A 0.1-µF ceramic capacitor to PGND is required.
A4	VDD	O	Internal supply for battery charger. Connect a 1-mF ceramic capacitor from this output to PGND. External load on VDD is not recommended.
A5	VSHRT	I	The voltage on this pin defines the battery voltage for transitioning from linear charge (pre-charge) to fast charge. A 10-µA current source is internally connected to this pin. Connect a resistor from this pin to ground to setup VSHORT reference. If the pin is left floating or tied to VDD an internal VSHORT reference of 2.1 V is used.
A6	DGND		Digital ground
B1	PGND		Power ground
B2			
B3			
B4	STAT	O	Charge status pin. Pulled low when charge in progress. Open drain for other conditions. This pin can also be controlled through I^2C register. STAT can be used to drive a LED or communicate with a host processor.
B5	SGND		Signal ground
B6	VZERO	I	This pin sets the zero-current output voltage level of the current shunt monitor.
C1	SWC	O	Internal switch to inductor connection (charger)
C2			
C3			
C4	OTG	I	Boost control pin. Boost mode is turned on whenever this pin is active. Polarity is user defined through I^2C register. The pin is disabled by default and can be enabled through I^2C register bit.
C5	VSHNT	O	Output of current shunt monitor. For positive currents (into battery) VSHNT > VZERO. For negative currents (out of the battery) VSHNT < VZERO.
C6	VSYS	I	Input supply for WLED driver and current shunt monitor
D1	PMID	O	Connection point between reverse blocking MOSFET and high-side switching MOSFET. Bypass it with a minimum of 1-µF capacitor from PMID to PGND. No other circuits are recommended to connect at PMID pin.
D2			
D3			
D4	INT	O	Interrupt pin (open-drain). This pin is pulled low to signal to the main processor that a fault has occurred.

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NO.	NAME		
D5	CTRL	I	Control pin of the LED boost regulator. It is a multi-functional pin which can be used for enable control and PWM dimming.
D6	LDO	O	LDO output. LDO is regulated to 4.9 V and drives 60-mA of current. Bypass LDO to GND with at least a 1-µF ceramic capacitor. LDO is enabled when VBUS is above the VBUS UVLO threshold.
E1	VBUS	I/O	Charger input voltage. Bypass it with a 1-µF ceramic capacitor from VBUS to PGND. It also provides power to the load in boost mode.
E2			
E3	VIO	I	I/O reference voltage. A VIO level above 0.6 V disables automatic D+/D- detection.
E4	DP	I	USB port D+ input connection
E5	FB	I	Feedback pin for current. Connect the sense resistor from FB to GND.
E6	COMP	O	Output of the transconductance error amplifier. Connect an external capacitor to this pin to compensate the regulator.
F1	BOOT	O	Boot-strapped capacitor for the high-side MOSFET gate driver. Connect a 10-nF ceramic capacitor (voltage rating above 10 V) from BOOST pin to SWC pin.
F2	SDA	I/O	I^2C interface data
F3	SCL	I	I^2C interface clock
F4	DM	I	USB port D- input connection
F5	PGND		Power ground
F6	SWL	I	This is the switching node of the LED driver. Connect the inductor from the supply to the SWL pin. This pin is also used to sense the output voltage for open LED protection.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)(2)

			MIN	MAX	UNIT
	Supply voltage (with respect to PGND)	VBUS	–2	20	V
	Input/Output voltage (with respect to PGND)	SDA, SCL, DM, DP, SWL, VZERO, VSHRT, CSIN, CSOUT, CSOT, LDO, INT, OTG, VSYS, VSHNT, VDD, VIO, BAT, CTRL	–0.3	7	V
		PMID, STAT	–0.3	20	
		VDD		6.5	
		SWC, BOOT	–0.7	20	
		FB,COMP	–0.3	3	
		SWL	–0.3	44	
	Voltage difference between CSIN and CSOUT inputs (VCSIN -VCSOUT)			± 7	V
	Output current (average)	SWC		1.5	A
	Output current (continuous)	LDO		100	mA
T_A	Operating ambient temperature		–40	85	°C
T_J	Max operating junction temperature			150	°C
T_C	Max operating case temperature			150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VBUS	Supply voltage	4		6	V
SWL	Output voltage	VBAT		39	V

6.4 Thermal Information

THERMAL METRIC(1)		TPS65200 YFF (DSBGA) 36 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	54.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	0.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	8.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	8.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

VBAT = 3.6 V ±5%, T_J = 27ºC (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
INPUT CURRENTS							
$I_{DISCHARGE}$	Battery discharge current in high Impedance mode (CSIN, CSOUT,SWC, SWL, BAT, VSYS pins)	0°C < TJ < 85°C, V_{BAT} = 4.2 V	Charger Hi-Z mode WLED disabled Shunt monitor disabled		2	10	µA
			Charger Hi-Z mode WLED enabled, no load Shunt monitor disabled			1800	
			Charger HiZ mode WLED disabled Shunt monitor enabled			60	
I_{VBUS}	VBUS supply current	V_{BUS} > $V_{BUS(min)}$	Charger PWM ON		10000		µA
			Charger PWM OFF			5000	
		0°C < T_J < 85°C, HZ_MODE = 1				15	
I_{VBUS_LEAK}	Leakage current from battery to VBUS pin	0°C < T_J < 85°C, V_{BAT} = 4.2 V HiZ mode				5	µA
VOLTAGE REGULATION							
V_{OREG}	Output charge voltage	Operating in voltage regulation, programmable		3.5		4.44	V
	Voltage regulation accuracy	T_A = 25°C		–0.5%		0.5%	
		Full temperature range		–1%		1%	

Electrical Characteristics (continued)

VBAT = 3.6 V ±5%, T_J = 27ºC (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
CURRENT REGULATION -FAST CHARGE						
$I_{OCHARGE}$	Output charge current	$V_{SHRT} \le V_{CSOUT} < V_{OREG}$, V_{BUS} > 5 V, R_{SNS} = 20 mΩ, LOW_CHG = 0, Programmable	550		1250	mA
		$V_{LOWV} \le V_{CSOUT} < V_{OREG}$, V_{BUS} > 5 V, R_{SNS} = 20 mΩ, LOW_CHG = 1		150	200	
CHARGE TERMINATION DETECTION						
I_{TERM}	Termination charge current	$V_{CSOUT} > V_{OREG-VRCH}$, V_{BUS} > 5 V, R_{SNS} = 20 mΩ, Programmable	50		400	mA
	Deglitch time for charge termination	Both rising and falling, 2-mV overdrive, t_{RISE}, t_{FALL} = 100 ns		30		ms
CHARGE CURRENT ACCURACY						
$V_{OS, CHRGR}$	Offset voltage, sense voltage amplifier Charge current accuracy = $V_{OS}/(I_{SET}xR_{SNS})$	T_A = 0°C to 85°C	–1		1	mV
BAD ADAPTOR DETECTION						
$V_{IN(MIN)}$	Input voltage lower limit	Bad adaptor detection, V_{BUS} falling	3.6	3.8	4	V
	Deglitch time for V_{BUS} rising above $V_{IN(MIN)}$	Rising voltage, 2-mV over drive, t_{RISE} = 100 ns		30		ms
	Hysteresis for $V_{IN(MIN)}$	V_{BUS} rising	100		200	mV
I_{ADET}	Current source to GND	During bad adaptor detection	20	30	40	mA
T_{INT}	Detection interval	Input power source detection		2		s
INPUT BASED DYNAMIC POWER MANAGEMENT						
V_{IN_LOW}	The threshold when input based DPM loop kicks in	Charge mode, programmable	4.2		4.76	V
	DPM loop kick-in threshold tolerance		–2%		2%	
INPUT CURRENT LIMITING						
I_{IN_LIMIT}	Input current limiting threshold	I_{IN_LIMIT} = 100 mA	88	93	98	mA
		I_{IN_LIMIT} = 500 mA	450	475	500	
		I_{IN_LIMIT} = 975 mA	875	925	975	
VDD REGULATOR						
V_{DD}	Internal bias regulator voltage	$V_{BUS} > V_{IN(min)}$ or $V_{SYS} > V_{BATMIN}$, I_{VDD} = 1 mA, C_{VDD} = 1 µF	2		6.5	V
	VDD output short current limit			30		mA
	Voltage from BST pin to SWC pin	During charge or boost operation			6.5	V
BATTERY RECHARGE THRESHOLD						
V_{RCH}	Recharge threshold voltage	Below V_{OREG}	100	130	160	mV
	Deglitch time	V_{CSOUT} decreasing below threshold, t_{FALL} = 100 ns, 10-mV overdrive		130		ms
STAT OUTPUT						
$V_{OL(STAT)}$	Low-level output saturation voltage	I_O = 10 mA, sink current			0.4	V
	High-level leakage current	Voltage on STAT pin is 5 V			1	µA
REVERSE PROTECTION COMPARATOR						
V_{REV}	Reverse protection threshold, $V_{BUS-VCSOUT}$	2.3 V ≤ V_{CSOUT} ≤ V_{OREG}, V_{BUS} falling	0	40	100	mV
$V_{REV-EXIT}$	Reverse protection exit hysteresis	2.3 V ≤ V_{CSOUT} ≤ V_{OREG}	140	200	260	mV
	Deglitch time for V_{BUS} rising above V_{REV} + V_{REV_EXIT}	Rising voltage		30		ms

Electrical Characteristics (continued)

VBAT = 3.6 V ±5%, T_J = 27ºC (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VBUS UVLO						
V_{UVLO}	IC active threshold voltage	V_{BUS} rising	3.05	3.3	3.55	V
V_{UVLO_HYS}	IC active hysteresis	V_{BUS} falling from above V_{UVLO}	120	150		mV
PWM						
f_{PWM}	PWM frequency, charger			3		MHz
R_{DSON}	Internal top reverse blocking MOSFET on-resistance	I_{IN_LIMIT} = 500 mA, Measured from VBUS to PMID		180		mΩ
	Internal top N-channel Switching MOSFET on-resistance	Measured from PMID to SWC		120		
	Internal bottom N-channel MOSFET on-resistance	Measured from SW to PGND		150		
D_{MAX}	Maximum duty cycle			99.5%		
D_{MIN}	Minimum duty cycle		0%			
	Synchronous mode to nonsynchronous mode transition current threshold(1)	Low-side MOSFET cycle-by-cycle current sensing		100		mA
BOOST MODE OPERATION FOR VBUS (OPA_MODE=1, HZ_MODE=0)						
V_{BUS_B}	Boost output voltage (to pin VBUS)	2.5 V < V_{BUS} < 4.5 V; Including line and load regulation over full temp range	4.75	5	5.25	V
I_{BO}	Maximum output current for boost	V_{BUS_B} = 5 V, 2.5 V < V_{BUS} < 4.5 V	200			mA
I_{BLIMIT}	Cycle by cycle current limit for boost	V_{BUS_B} = 5 V, 2.5 V < V_{SYS} < 4.5 V		1		A
V_{BUSOVP}	Overvoltage protection threshold for boost (VBUS pin)	Threshold over V_{BUS} to turn off converter during boost	5.8	6	6.2	V
	VBUSOVP hysteresis	V_{BUS} falling from above V_{BUSOVP}		200		mV
V_{BATMAX}	Maximum battery voltage for boost	V_{SYS} rising edge during boost	4.75	4.9	5.05	V
	VBATMAX hysteresis	V_{SYS} falling from above V_{BATMAX}		200		mV
V_{BATMIN}	Minimum battery voltage for boost (VSYS pin)	During boosting		2.5		V
		Before boost starts		2.9	3.05	
	Boost output resistance at high impedance mode (From VBUS to PGND)	HZ_MODE = 1	500			kΩ
CHARGER PROTECTION						
V_{OVP-IN_USB}	Input V_{BUSOVP} threshold voltage	Threshold over V_{BUS} to turn off converter during charge	6.3	6.5	6.7	V
	$V_{OVP\_IN\_USB}$ hysteresis	V_{BUS} falling from above V_{OVP_IN}		140		mV
V_{OVP}	Battery OVP threshold voltage	V_{CSOUT} threshold over V_{OREG} to turn off charger during charge (% V_{OREG})	110%	117%	121%	
	V_{OVP} hysteresis	Lower limit for V_{CSOUT} falling from > V_{OVP} (% V_{OREG})		11%		
I_{LIMIT}	Cycle-by-cycle current limit for charge	Charge mode operation	1.8	2.4	3	A
V_{SHORT}	Trickle to fast charge threshold	V_{CSOUT} rising, VSHRT connected to VDD	2	2.1	2.2	V
		Resistor connected from VSHRT to GND	1.8		V_{BUS} – 0.7	V
	Internal current source connected to V_{SHRT} pin		9.4	10	10.6	µA
	V_{SHORT} hysteresis	V_{CSOUT} falling from above VSHORT		100		mV
	Enable threshold for internal V_{SHORT} reference	percentage of VDD		90%		

(1) Bottom N-channel MOSFET always turns on for approximately 60 ns and then turns off if current is too low.

Electrical Characteristics (continued)

VBAT = 3.6 V ±5%, T_J = 27ºC (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{SHORT}	Trickle charge charging current	$V_{CSOUT} \le V_{SHORT}$	20	30	40	mA
T_{CF}	Thermal regulation threshold	Charge current begins to taper down		120		°C
T_{32S}	Time constant for the 32-second timer	32 second mode		32		s
WLED VOLTAGE AND CURRENT CONTROL						
V_{REF}	Voltage feedback regulation voltage		198	203	208	mV
V_{REF_PWM}	Voltage feedback regulation voltage under brightness control	V_{FB}[4:0] = 01110 (V_{FB} = 25%)	47	50	53	mV
		V_{FB}[4:0] = 01110 (V_{FB} = 10%)	17	20	23	
f_{CTRL}	PWM dimming frequency		1		100	kHz
$t_{CNTRL, MIN}$	Minimum on-time for PWM dimming pulse		2.2			µs
I_{FB}	Voltage feedback input bias current	V_{FB} = 200 mV			1	µA
f_{PWM}	PWM frequency, WLED boost			600		kHz
D_{max}	Maximum duty cycle	V_{FB} = 100 mV	90%	93%		
t_{min_on}	Minimum 0N pulse width			40		ns
L	Inductor		10		22	µH
C_{OUT}	Output capacitor		0.47		10	µF
WLED POWER SWIITCH						
$R_{DS(on)}$	N-channel MOSFET on-resistance	V_{SYS} = 3.6 V		300	600	mΩ
I_{LN_NFET}	N-channel leakage current	V_{SWL} = 30 V, T_A = 25°C			1	µA
WLED PROTECTION						
V_{UVLO}	Under Voltage Lock Out (VSYS pin)	V_{SYS} falling		2.2	2.5	V
	UVLO hysteresis			70		mV
V_{OVP}	Overvoltage Protection threshold		35	37	39	V
I_{LIM}	N-Channel MOSFET current limit	D = D_{max}	560	700	840	mA
I_{LIM_Start}	Startup current limit	D = D_{max}		400		mA
t_{HALF_LIM}	Time step for half current limit			5		ms
t_{REF}	V_{REF} filter time constant			180		µs
t_{step}	V_{REF} ramp up time			213		µs
CURRENT SHUNT MONITOR						
V_{CM}	Common-mode input range	V_{CSIN} = V_{CSOUT}	–0.3		7	V
CMR	Common-mode rejection	V_{CSIN} = 2.7 V to 5 V, V_{CSIN} – V_{CSOUT} = 0 mV	100			dB
$V_{OS, CSM}$	Offset-voltage, referred to input	T_A = 0°C to 60°C	–75		75	µV
		T_A = -20°C to 85°C	–85		85	
G	Gain			25		V/V
	Gain error		–1%		1%	
V_{SHNT}	Swing to positive power supply rail (V_{SYS})	V_{SYS} - V_{SHNT}	100			mV
	Swing to GND	V_{SHNT} - V_{GND}	100			
GBW	Bandwidth	C_{LOAD} = 10 pF		9		kHz
I_{VZERO}	VZERO bias current	T_A = -20°C to 85°C			10	nA
V_{ZERO}	Swing to positive power supply rail (V_{SYS})	V_{SYS} – V_{ZERO}	1.5			V
	Swing to GND	V_{ZERO} - V_{GND}	0.7			
V_{UVLO}	Undervoltage lockout (VSYS pin)	V_{SYS} falling		2.2	2.5	V
	UVLO hysteresis			70		mV

Electrical Characteristics (continued)

VBAT = 3.6 V ±5%, T_J = 27ºC (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LDO						
V_{LDO}	LDO Output Voltage	VIN = 5.5V	4.8	4.9	5	V
	PSRR	f = 100 Hz, CLDO = 1.0 µF		60		dB
I_{LDO}	Maximum LDO Output Current		60			mA
V_{DO}	Dropout Voltage	VIN = 4.5 V, ILDO = 50 mA		100	250	mV
D+/D- DETECTION						
V_{DP_SCR}	D+ voltage source		0.5	0.6	0.7	V
	D+ voltage source output current		250			µA
I_{DM_SINK}	D- current sink		50	100	150	µA
C_I	Input capacitance	DM pin, switch open		4.5	5	pF
		DP pin, switch open		4.5	5	
I_I	Input leakage	DM pin, switch open	–1		1	µA
		DP pin, switch open	–1		1	
V_{DP_LOW}	DP low comparator threshold		0.8			V
V_{DM_HIGH}	DM high comparator threshold		0.8			V
V_{DM_LOW}	DM low comparator threshold				475	mV
LOGIC LEVELS AND TIMING CHARTERISTICS (SCL, SDA, CTRL, INT)						
V_{OL}	Output low threshold level	I_O = 3 mA, sink current (SDA, INT)			0.4	V
	Input low threshold level				0.4	
	Input high threshold level		1.2			
$I_{(bias)}$	Input bias current (SCL, SDA, INT)	V_{IO} = 1.8 V			1	µA
f_{SCL}	SCL clock frequency				400	kHz
R_{CTRL}	CTRL pulldown resistor		400	800	1600	kΩ
t_{OFF}	CTRL pulse width to shutdown	CTRL high to low	2.5			ms
	7-bit slave address			1101 010		
OSCILLATOR						
f_{OSC}	Oscillator frequency			3		MHz
	Frequency accuracy	T_A = –40°C to 85°C	–10%		10%	
THERMAL SHUTDOWN						
T_{SHTDWN}	Thermal trip point			165		°C
	Thermal hysteresis			10		

6.6 Data Transmission Timing

V_{BAT} = 3.6 ±5%, T_A = 25 ºC, C_L = 100 pF (unless otherwise noted)

			MIN	NOM	MAX	UNIT
$f_{(SCL)}$	Serial clock frequency	Standard mode			100	KHz
		Fast mode			400	
$t_{(BUF)}$	Bus free time between stop and start condition	SCL = 100 kHz	4.7			µs
		SCL = 400 kHz	1.3			
$t_{(SP)}$	Tolerable spike width on bus	SCL = 100 kHz			50	ns
		SCL = 400 kHz				
t_{LOW}	SCL low time	SCL = 100 kHz	4.7			µs
		SCL = 400 kHz	1.3			
t_{HIGH}	SCL high time	SCL = 100 kHz	4			µs
		SCL = 400 kHz	0.6			
$t_{S(DAT)}$	SDA → SCL setup time	SCL = 100 kHz	250			ns
		SCL = 400 kHz	100			
$t_{S(STA)}$	Start condition setup time	SCL = 100 kHz	4.7			µs
		SCL = 400 kHz	0.6			
$t_{S(STO)}$	Stop condition setup time	SCL = 100 kHz	4			µs
		SCL = 400 kHz	0.6			
$t_{H(DAT)}$	SDA → SCL hold time	SCL = 100 kHz	0		3.45	µs
		SCL = 400 kHz	0		0.9	
$t_{H(STA)}$	Start condition hold time	SCL = 100 kHz	4			µs
		SCL = 400 kHz	0.6			
$t_{r(SCL)}$	Rise time of SCL Signal	SCL = 100 kHz			1000	ns
		SCL = 400 kHz			300	
$t_{f(SCL)}$	Fall time of SCL Signal	SCL = 100 kHz			300	ns
		SCL = 400 kHz			300	
$t_{r(SDA)}$	Rise time of SDA Signal	SCL = 100 kHz			1000	ns
		SCL = 400 kHz			300	
$t_{f(SDA)}$	Fall time of SDA Signal	SCL = 100 KHz			300	ns
		SCL = 400 kHz			300	

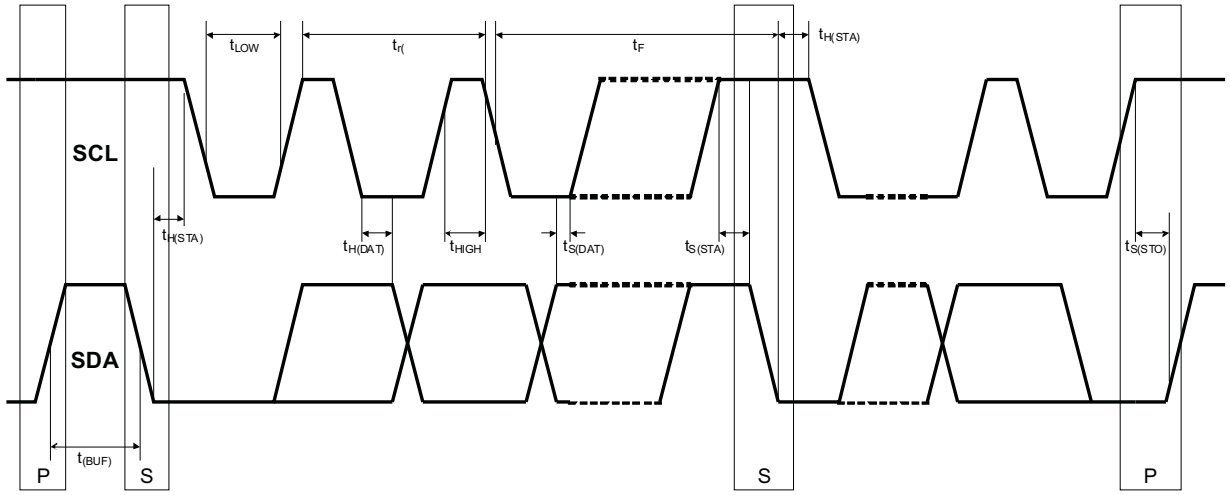
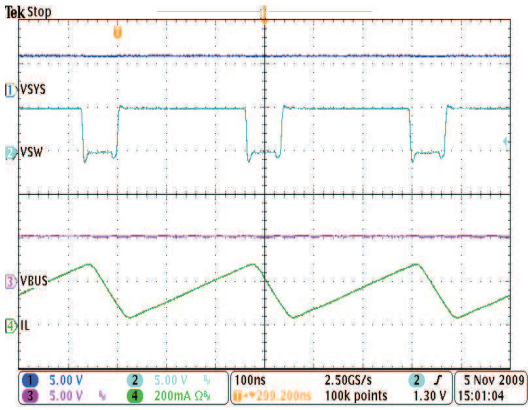


Figure 1. I²C Data Transmission Timing

6.7 Typical Characteristics

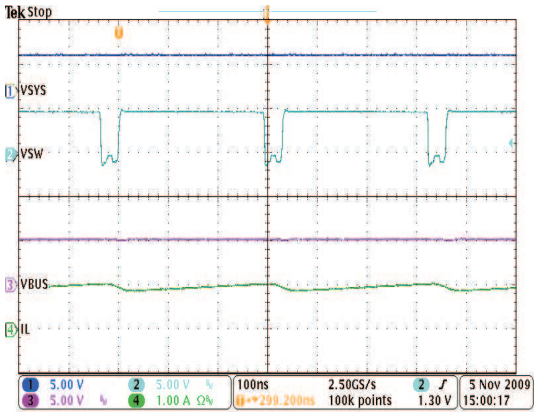
T_A = 25°C, unless otherwise specified.

6.7.1 Switching Charger



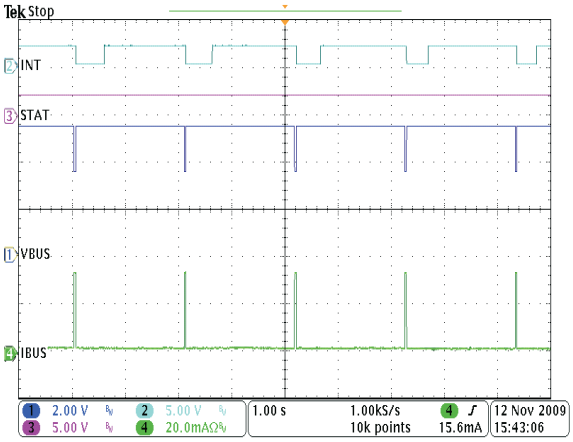
V_{BUS} = 5 V I_{CHARGE} = 150 mA

Figure 2. PWM Charge Operation



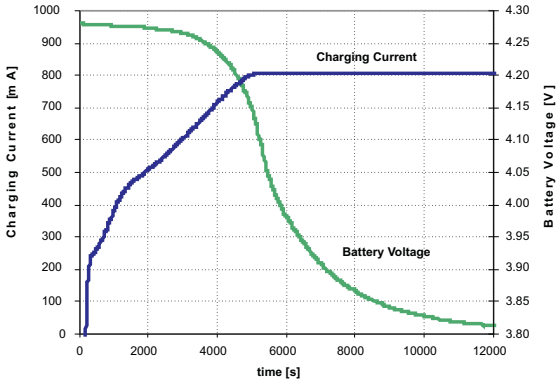
V_{BUS} = 5 V I_{CHARGE} = 150 mA

Figure 3. PWM Charge Operation



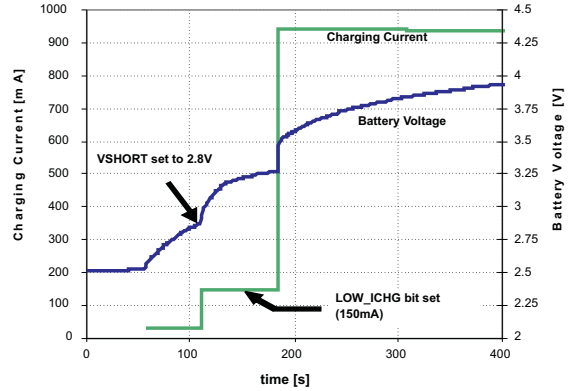
V_{BUS} = 5.5 V R_{IN} = 60 Ω V_{BAT} = 3 V (#165)

Figure 4. Bad Adaptor Detection



1500 mAh Li-ion 5.55 Whr I_{CHARGE} = 950 mA
I_{IN_limit} = 975 mA

Figure 5. Charging Curve



I_{CHARGE} = 950 mA I_{IN_limit} = 975 mA V_{SHORT} = 2.8 V

Figure 6. Precharge Curve

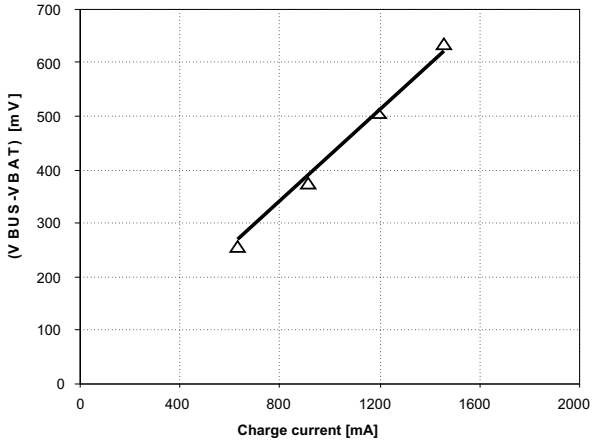
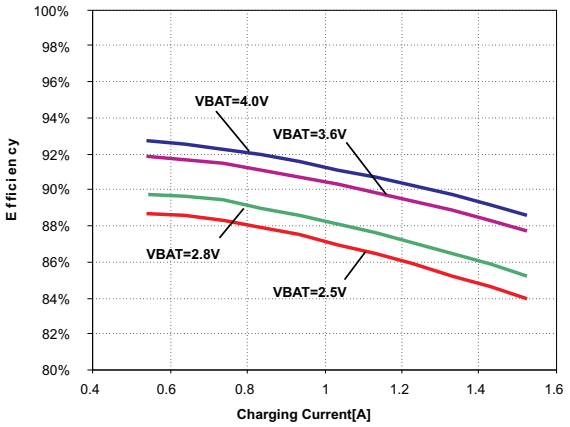


Figure 7. Effective Dropout Voltage

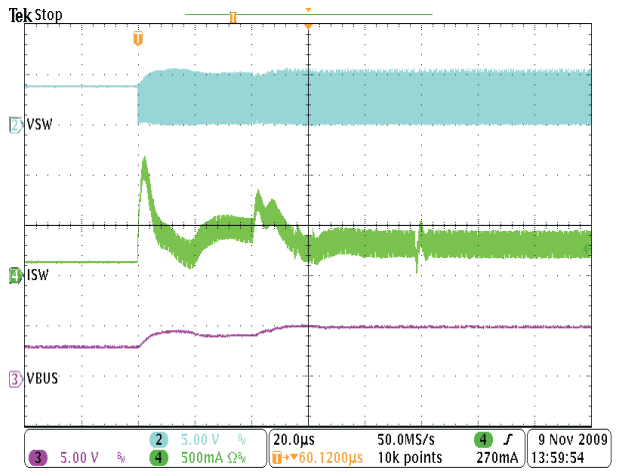
Switching Charger (continued)



V_{BUS} = 5.5 V

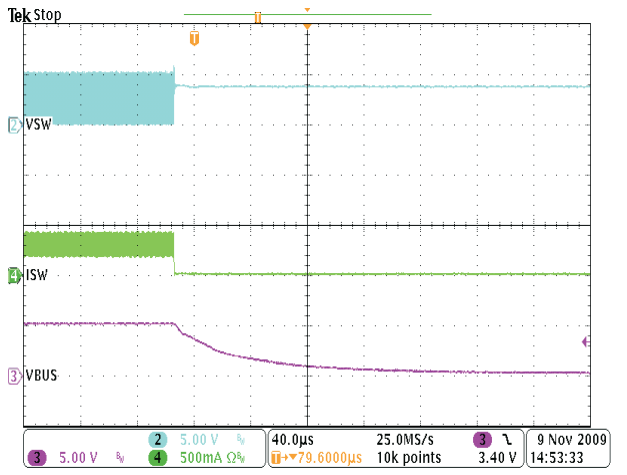
Figure 8. Charger Efficiency

6.7.2 OTG Boost



V_{BAT} = 3.8 V I_{LOAD} = 200 mA

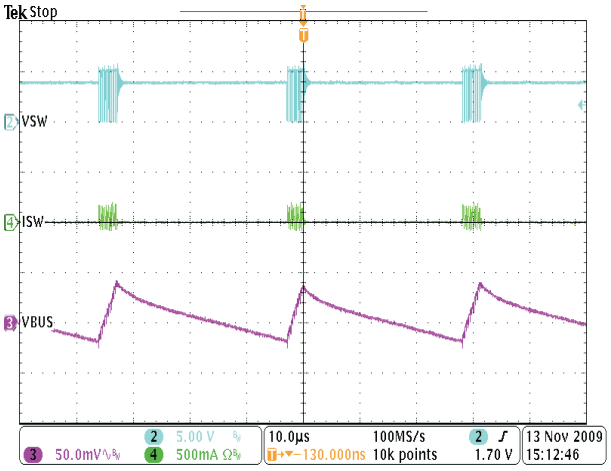
Figure 9. Start Up



V_{BAT} = 3.8 V I_{LOAD} = 200 mA

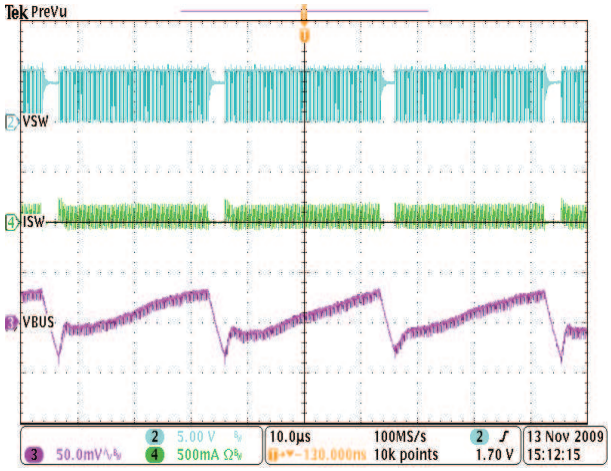
Figure 10. Shutdown

OTG Boost (continued)



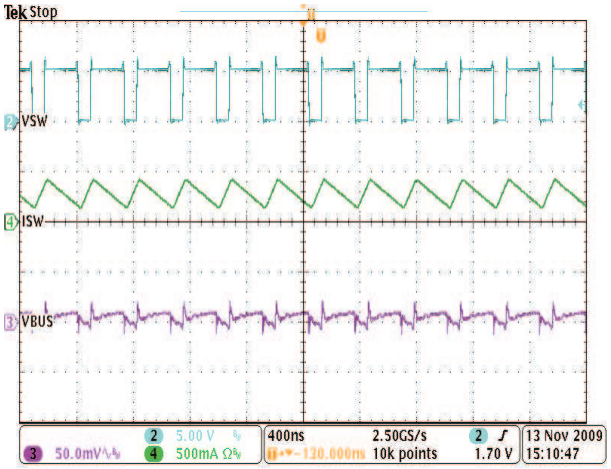
V_{BAT} = 3.8 V I_{LOAD} = 1 mA

Figure 11. PWM Boost Operation



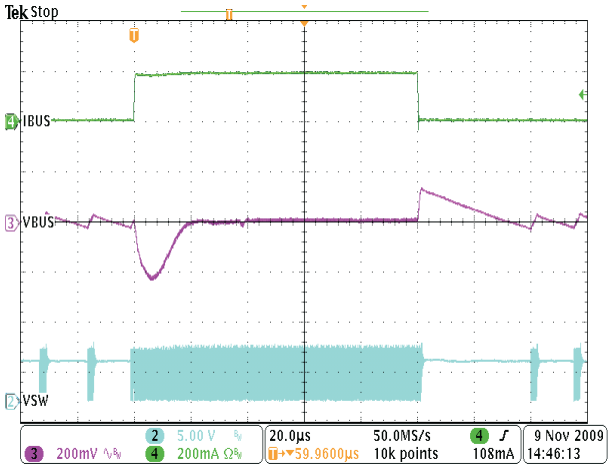
V_{BAT} = 3.8 V I_{LOAD} = 30 mA

Figure 12. PWM Boost Operation



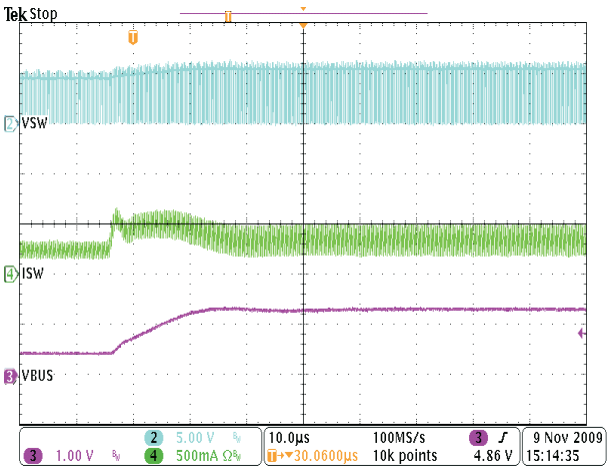
V_{BAT} = 3.8 V I_{LOAD} = 200 mA

Figure 13. PWM Boost Operation



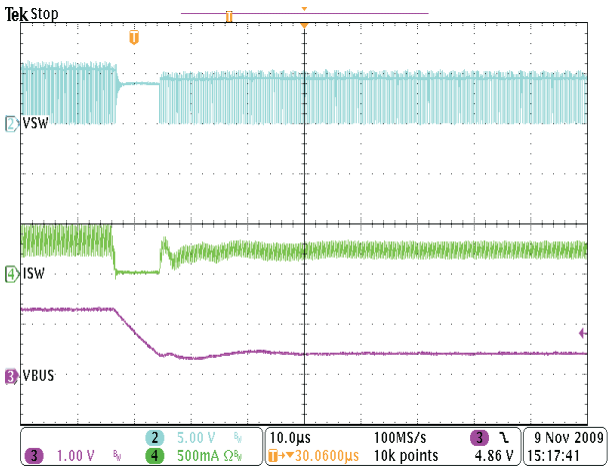
V_{BAT} = 3.8 V I_{LOAD} = 5 mA - 200 mA

Figure 14. Transient Response



V_{BAT} = 3.8 V I_{LOAD} = 200 mA

Figure 15. I²C Controlled Voltage Step



V_{BAT} = 3.8 V I_{LOAD} = 200 mA

Figure 16. I²C Controlled Voltage Step

6.7.3 LDO

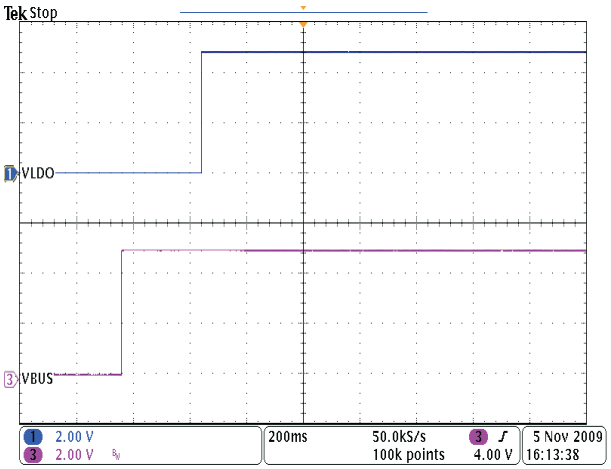


Figure 17. Turnon Delay

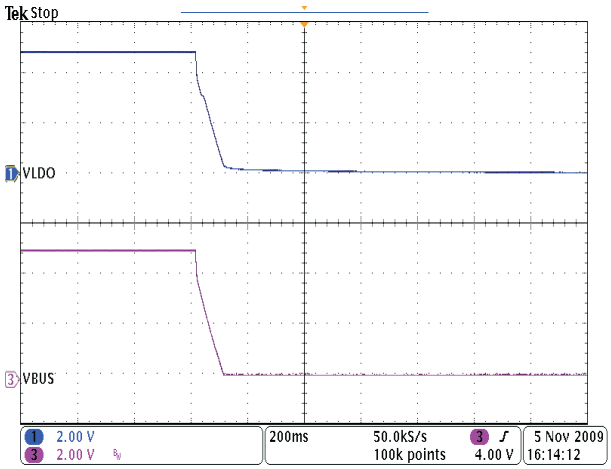
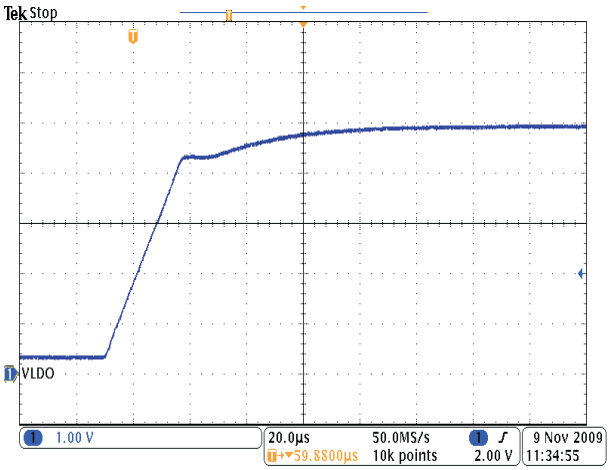
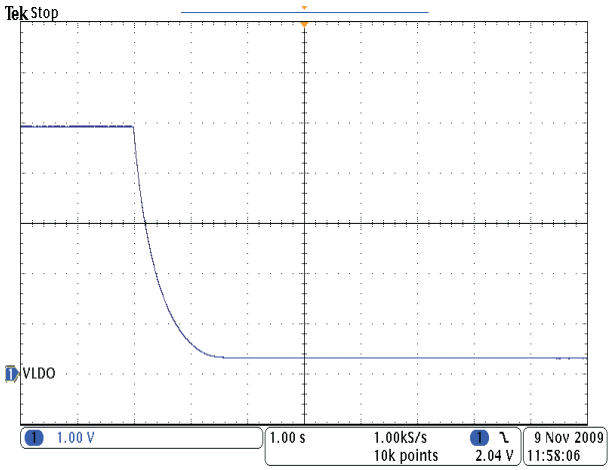


Figure 18. Turnoff Delay



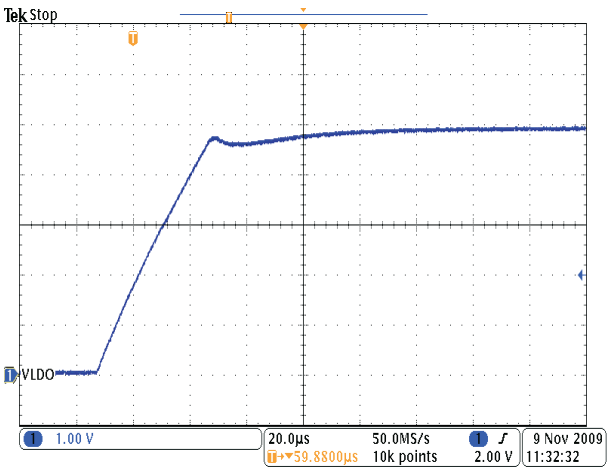
Charger = ON at 950 mA V_{BUS} = 5.5 V

Figure 19. Start-Up



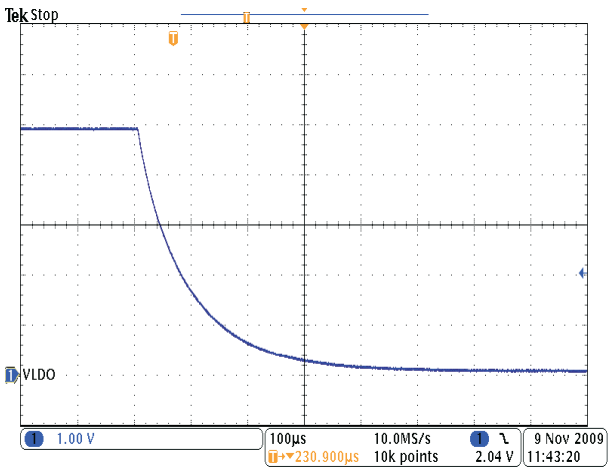
Charger = ON at 950 mA V_{BUS} = 5.5 V

Figure 20. Shutdown



50 mA Load, Charger = ON at 950 mA V_{BUS} = 5.5 V

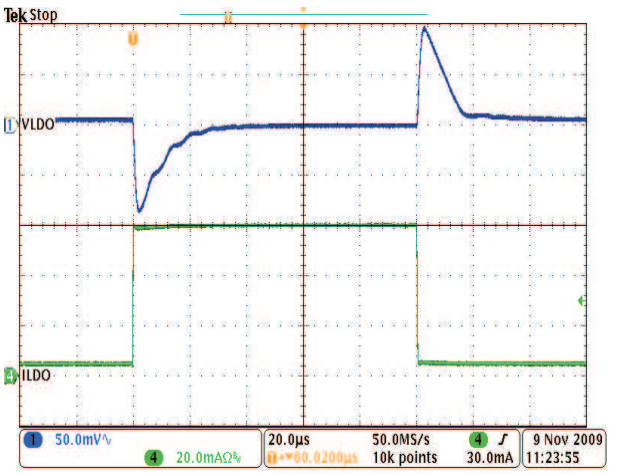
Figure 21. Start-Up



50 mA Load, Charger = ON at 950 mA V_{BUS} = 5.5 V

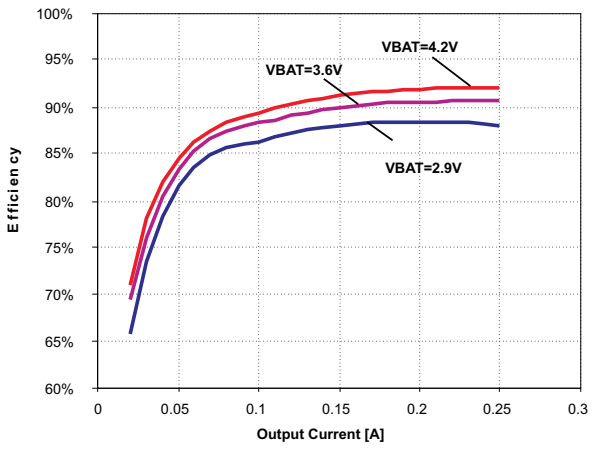
Figure 22. Shutdown

LDO (continued)



Charger OFF I_{LOAD} = 5 mA to 50 mA V_{BUS} = 5.5 V

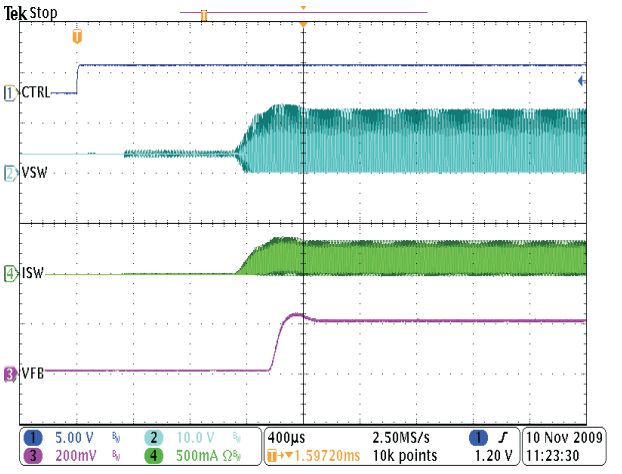
Figure 23. Transient Response



V_{BUS} = 5.5 V

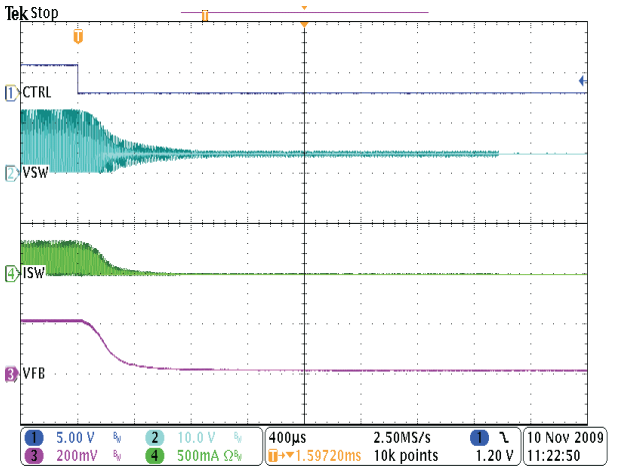
Figure 24. OTG Boost Efficiency

6.7.4 WLED Boost



V_{BAT} = 3.8 V V_{FB} = 200 mV 7 LEDs

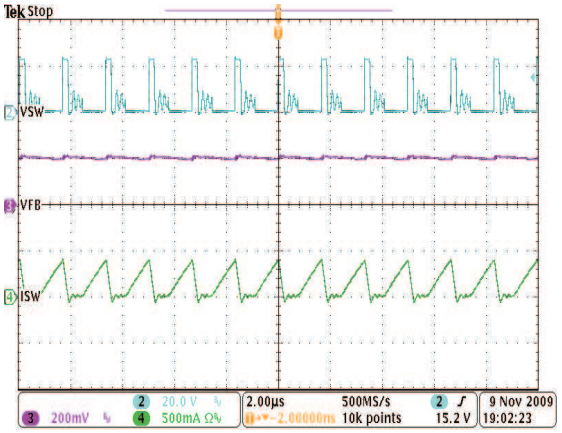
Figure 25. Start-Up



V_{BAT} = 3.8 V V_{FB} = 200 mV 7 LEDs

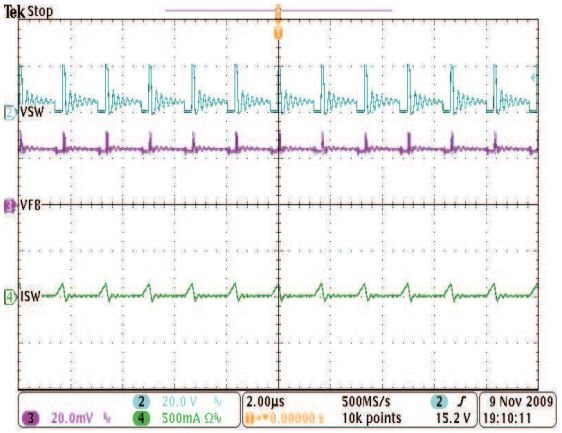
Figure 26. Shutdown

WLED Boost (continued)



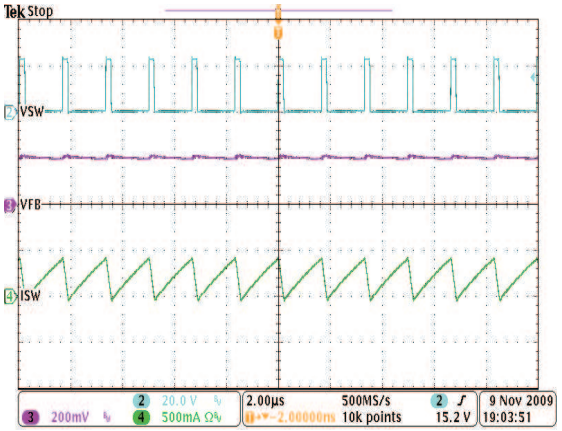
V_{BAT} = 4.2 V V_{FB} = 200 mV 7 LEDs

Figure 27. PWM Operation



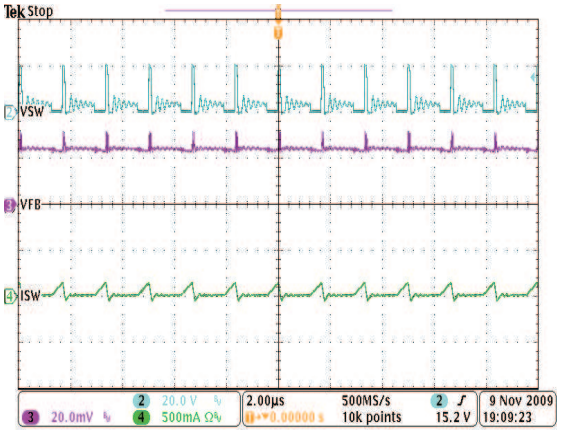
V_{BAT} = 4.2 V V_{FB} = 20 mV 7 LEDs

Figure 28. PWM Operation



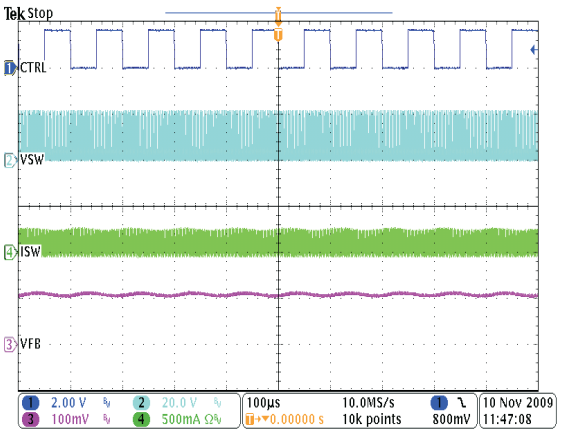
V_{BAT} = 3 V V_{FB} = 200 mV 7 LEDs

Figure 29. PWM Operation



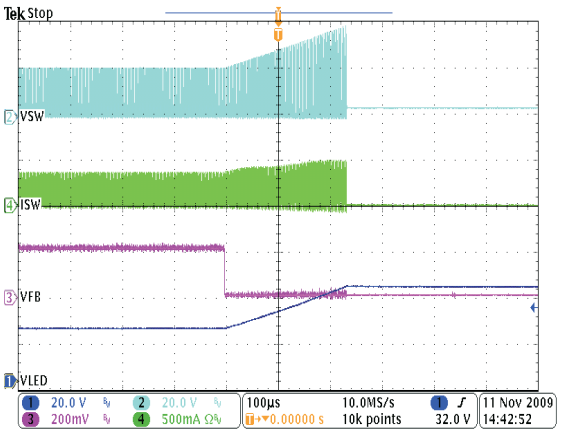
V_{BAT} = 3 V V_{FB} = 20 mV 7 LEDs

Figure 30. PWM Operation



50% Duty Cycle 7 LEDs V_{BAT} = 3.8 V V_{FB} = 200 mV

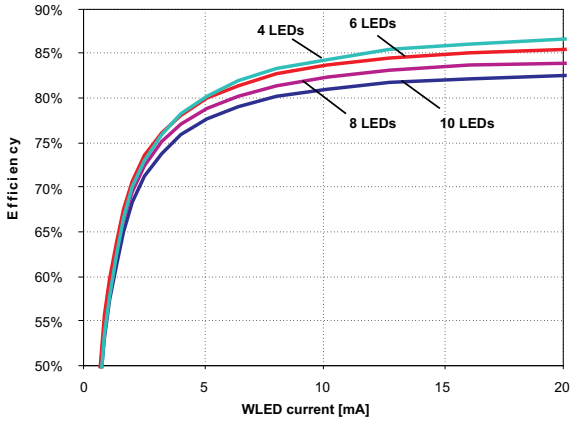
Figure 31. PWM Dimming



V_{BAT} = 3.8 V V_{FB} = 200 mV 7 LEDs (#162)

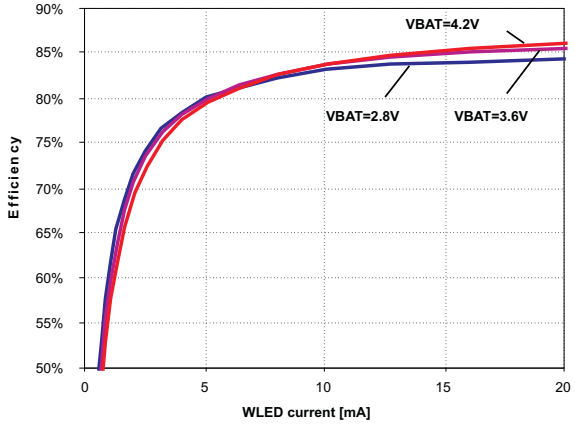
Figure 32. Open LED Protection

WLED Boost (continued)



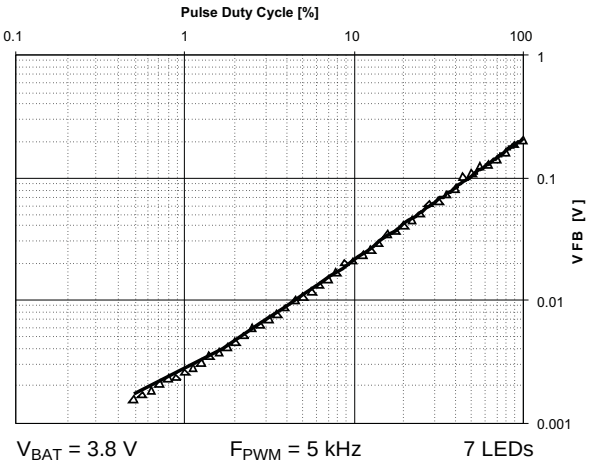
V_{BAT} = 3.3 V

Figure 33. Efficiency



6 LEDs

Figure 34. Efficiency



V_{BAT} = 3.8 V F_{PWM} = 5 kHz 7 LEDs

Figure 35. WLED Dimming Linearity

7 Detailed Description

7.1 Overview

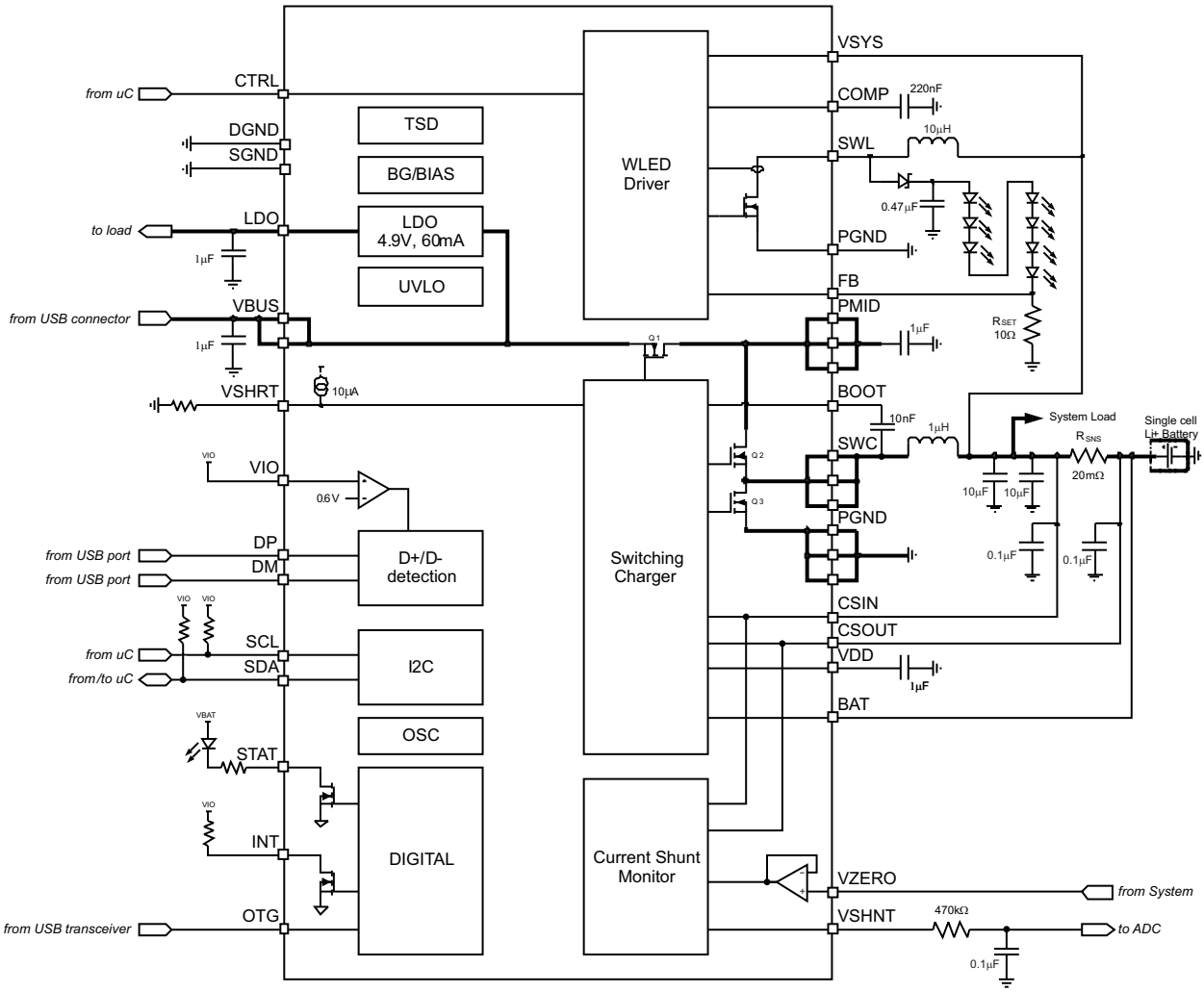
The TPS65200 charger features a synchronous 3-MHz PWM controller with integrated power MOSFETs, input current sensing and regulation, input-voltage dynamic power management, high-accuracy charge current and voltage regulation, and charge termination. The charger charges the battery in three phases: low-current precharge, constant current fast-charge, and constant voltage trickle-charge. The input current is automatically limited to the value set by the host. The charger can be configured to terminate charge based on user-selectable minimum current level and to automatically restart the charge cycle if the battery voltage falls below the recharge threshold. A safety timer with reset control provides a safety backup for I^2C interface. The charger automatically enters sleep mode or high impedance mode when the input supply is removed. The charge status is reported to the host using the I^2C interface and STAT pin. The D+D- detection circuit allows automatic detection of a USB wall-charger. If a wall-charger is detected the input current limit is automatically increased from 500 mA to 975 mA.

In OTG mode the PWM controller boosts the battery voltage to 5 V and provides up to 200-mA of current to the USB output. At very light loads the boost operates in burst mode to optimize efficiency. OTG mode can be enabled either through I^2C interface or GPIO control.

The TPS65200 also provides a WLED boost converter with integrated 40-V switch FET, that drives up to 10 WLEDs in series. The boost converter runs at 600-kHz fixed switching frequency to reduce output ripple, improve conversion efficiency, and allows for the use of small external components. The default WLED current is set with a sense resistor, and the feedback voltage is regulated to 200 mV, as shown in the typical application. For brightness dimming, the feedback voltage can be changed through the I^2C interface or by application of a PWM signal to the CTRL pin. In the latter case the feedback voltage is regulated down proportional to the PWM duty cycle (analog dimming) rather than pulsing the LED current to avoid audible noise on the output capacitor. For maximum protection, the device features integrated open LED protection that disables the TPS65200 to prevent the output from exceeding the absolute maximum ratings during open LED conditions.

A fixed-gain, high-accuracy current shunt monitor senses the voltage drop across an external, 20-mΩ sense resistor and provides an analog output voltage that is proportional to the charge/discharge current of the battery. The sense voltage is amplified by a factor of 25 and offset by V_{ZERO}, an externally provided reference voltage. V_{ZERO} is internally buffered to avoid loading of the reference source.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Global State Diagram

During normal operation, TPS65200 is either in STANDBY mode or ACTIVE mode, depending on user inputs. In STANDBY mode, most functions are turned off to conserve power, but the IC can still be accessed through I^2C bus and the current shunt monitor can be turned on and off. The bias system and main oscillator are turned off in STANDBY mode.

The device enters ACTIVE mode whenever VBUS is asserted or the WLED driver is turned on. In ACTIVE mode, the main oscillator and reference system are turned on. The device remains in ACTIVE mode as long as VBUS remains high, the WLED driver is enabled or both conditions exist.

Feature Description (continued)

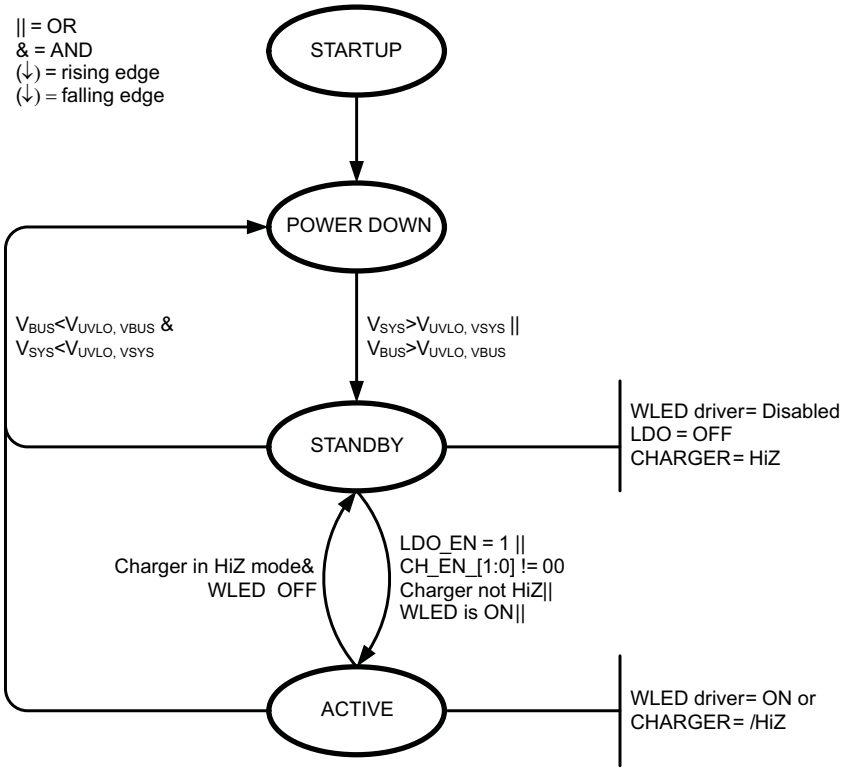


Figure 36. Global State Diagram

7.3.2 LED Driver Operation

The TPS65200 offers a high-efficiency, high-output voltage boost converter designed for driving up to 10 white LED in series. The serial LED connection provides even illumination by sourcing the same output current through all LEDs, eliminating the need for expensive factory calibration. The device integrates 40-V/0.7-A switch FET and operates in pulse width modulation (PWM) with 600-kHz fixed switching frequency. For operation, see *Functional Block Diagram*.

The LED driver can be enabled either through the CTRL pin or the WLED_EN bit in the CONTROL register. The CTRL input is edge sensitive and should be pulled low at power-up. The CTRL pin allows PWM dimming of the LEDs whereas the WLED_EN bit offers simple ON/OFF control only. The WLED_EN bit has priority over the CTRL pin and when set to 1, the CTRL pin is ignored. If WLED_EN is set to 0 and the CTRL pin is low for > 2.5 ms, the WLED driver is shut down.

The feedback loop regulates the FB pin voltage to the reference set by the VFB[4:0] bits in the WLED register with a default setting of 200 mV. If any fault occurs during normal operation the driver is disabled, WLED_EN bit is reset to 0 and the driver is put into FAULT state until the CTRL pin has been low for > 2.5 ms. The state diagram for the WLED driver is shown in Figure 37.

Feature Description (continued)

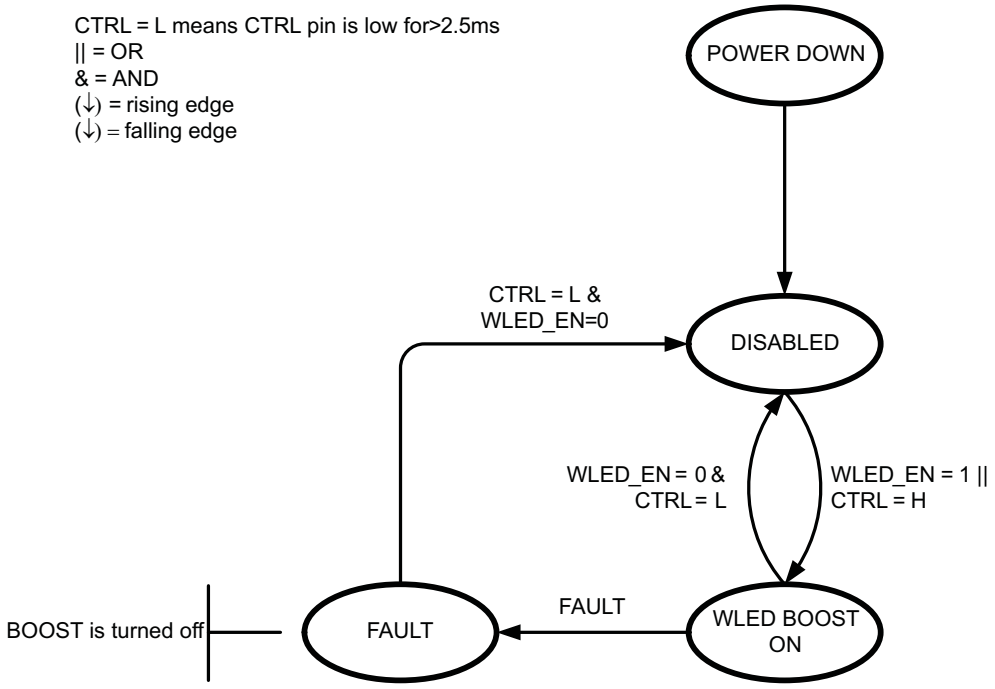


Figure 37. State Diagram for WLED Driver

7.3.2.1 Undervoltage Lockout

An undervoltage lockout circuit prevents operation of the WLED driver at input voltages (CSOUT pin) below 2.2 V. When the input voltage is below the under voltage threshold, the driver is shutdown and the internal switch FET is turned off. If the input voltage rises by 70 mV above the undervoltage lockout hysteresis, the WLED driver restarts. An internal thermal shutdown turns off the device when the typical junction temperature of 165°C is exceeded. The device is released from shutdown automatically when the junction temperature decreases by 10°C.

7.3.2.2 Shutdown

To minimize current consumption, the WLED driver is shutdown when the WLED_EN bit is low and the CTRL pin is pulled low for more than 2.5 ms. Although the internal FET does not switch in shutdown, there is still a DC current path between the input and the LEDs through the inductor and Schottky diode. The minimum forward voltage of the LED array must exceed the maximum input voltage to ensure that the LEDs remain off in shutdown. However, in the typical application with two or more LEDs, the forward voltage is large enough to reverse bias the Schottky and keep leakage current low.

7.3.2.3 Soft-Start Circuit

Soft-start circuitry is integrated into the WLED driver to avoid a high inrush current during start-up. After the device is enabled, the voltage at FB pin ramps up to the reference voltage in 32 steps, each step takes 213 µs. This ensures that the output voltage rises slowly to reduce the input current. Additionally, for the first 5 ms after the COMP voltage ramps, the current limit of the switch is set to half of the normal current limit specification. During this period, the input current is kept below 400 mA (typical).

7.3.2.4 Open LED Protection

Open LED protection circuitry prevents IC damage as the result of white LED disconnection. The TPS65200 monitors the voltage at the SWL pin during each switching cycle. The circuitry turns off the switch FET and shuts down the WLED driver as soon as the SWL voltage exceeds the V_{OVP} threshold for eight clock cycles. As a result, the output voltage falls to the level of the input supply. The WLED driver remains in shutdown mode until it is enabled by toggling the CTRL pin or the WLED_EN bit of the CTRL register.

Feature Description (continued)

7.3.2.5 Current Program

The FB voltage is regulated to a low 200-mV reference voltage. The LED current is programmed externally using a current-sense resistor in series with the LED string. The value of the RSET is calculated using Equation 1.

$$I_{LED} = \frac{V_{FB}}{R_{SET}}$$

where

- I_{LED} = output current of LEDs
- V_{FB} = regulated voltage of FB
- R_{SET} = current sense resistor (1)

The output current tolerance depends on the FB accuracy and the current sensor resistor accuracy.

7.3.2.6 Brightness Dimming

The TPS65200 offers two methods of LED brightness dimming. When the CTRL pin is constantly high, the FB voltage is regulated to the value set in the WLED register which ranges from 0 mV to 200 mV and is divided into 32 steps. For applications requiring higher dimming resolution, a PWM signal can be applied to the CTRL pin to reduce this regulation voltage and dim LED brightness. The relationship between the duty cycle and FB voltage is given by Equation 2.

$$V_{FB} = duty\ cycle \bullet VFB[4:0]$$

where

- Duty = duty cycle of the PWM signal
- VFB[4:0] = internal reference voltage, default = 200 mV (2)

The IC chops up the internal reference voltage at the duty cycle of the PWM signal and filters it by an internal low pass filter. The output of the filter is connected to the error amplifier as the reference voltage for the FB pin regulation. Therefore, although a PWM signal is used for brightness dimming, only the WLED DC current is modulated, which is often referred to as analog dimming. This eliminates the audible noise which often occurs when the LED current is pulsed in replica of the frequency and duty cycle of PWM control. The regulation voltage itself is independent of the PWM logic voltage level which often has large variations.

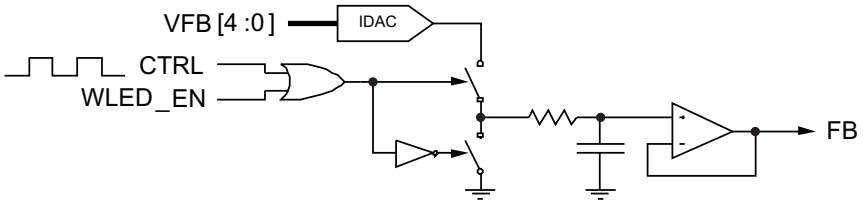


Figure 38. WLED Analog Dimming Circuit

7.3.2.7 Inductor Overcurrent Protection

The overcurrent limit in the boost converter limits the maximum input current and thus maximum input power for a given input voltage. Maximum output power is less than maximum input power due to power conversion losses. Therefore, the current limit setting, input voltage, output voltage and efficiency can all change maximum current output. The current limit clamps the peak inductor current and the maximum DC output current equals the current limit minus half of the peak-peak current ripple. The ripple current is a function of switching frequency, inductor value and duty cycle. Equation 3 through Equation 5 are used to determine the maximum output current.

$$D = 1 - \frac{V_{IN}}{V_{OUT}}$$

Feature Description (continued)

where

- D = duty cycle of the boost converter
- V_{IN} = Input voltage
- V_{OUT} = Output voltage of the boost converter. It is equal to the sum of VFB and the voltage drop across LEDs.

(3)

$$I_{PP} = \frac{V_{IN} \bullet D}{L \bullet f_S}$$

where

- I_{PP} = inductor peak to peak ripple
- L = inductor value
- f_s = switching frequency

(4)

$$I_{OUT(MAX)} = \frac{V_{IN} \bullet \left(I_{LIM} - \frac{I_{PP}}{2} \right) \bullet \eta}{V_{OUT}}$$

where

- $I_{OUT(MAX)}$ = maximum output current of the boost converter
- I_{LIM} = overcurrent limit
- η = efficiency

(5)

For instance, for V_{IN} = 3 V, 7 LEDs output equivalent to V_{OUT} of 23 V, an inductor value of 22 µH, a current limit of 700 mA, and an efficiency of 85%, the maximum output current is ~65 mA.

7.3.3 HV LDO

TPS65200 provides a 4.9-V LDO that is powered off the VBUS input. The LDO is enabled whenever V_{VBUS} > V_{UVLO} (3.3 V) and disabled when V_{VBUS} > V_{OVP-IN_USB} (6.5 V). LDO output voltage follows VBUS for V_{VBUS} < 4.9 V and is regulated to 4.9 V when V_{VBUS} > 4.9 V. In any case output current is limited to 100 mA. The LDO can also be disabled by the host by setting the LDO_EN bit of the CONTROL register to 0. An operational flow chart of the LDO enable is shown in Figure 39.

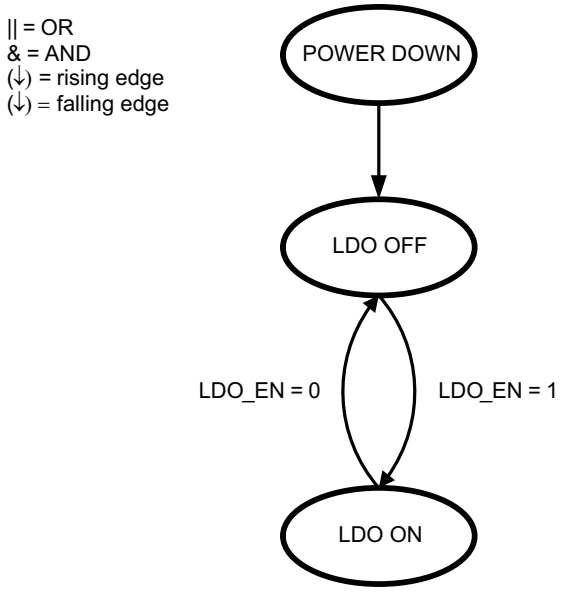


Figure 39. State Diagram for the HV LDO

Feature Description (continued)

7.3.4 Interrupt Pin

The interrupt pin is used to signal any fault condition to the host processor. Whenever a fault occurs in the IC, the corresponding fault bit is set in the INT1, INT2, or INT3 register, and the open-drain output is pulled low. The INT pin is released (returns to HiZ state) if any of the INT1, INT2, INT3 registers is accessed by the host, but fault bits are cleared only by reading the INTx register containing the bit. However, if a failure persists, the corresponding interrupt bit remains set but no new interrupt is issued. The TSD bit (thermal shutdown) is auto cleared which means that the bit is reset to 0 automatically after the chip has cooled down below the thermal shutdown release threshold.

The MASK1, MASK2, and MASK3 registers are used to mask certain events or group of events from generating interrupts. The MASKx settings affect the INT pin only and have no impact on protection and monitor circuits themselves.

7.3.5 Current Shunt Monitor

TPS65230 offers an integrated high-precision current shunt monitor to measure battery charging and discharging currents. The inputs of a low-offset amplifier are connected across an external low-value shunt resistor. This shunt voltage is gained up by a factor of 25 and added to a reference voltage connected to the VZERO terminal.

$V_{SHUNT} > V_{ZERO}$ for currents flowing into the battery and $V_{SHUNT} < V_{ZERO}$ for currents flowing out of the battery. The reference voltage is buffered by a low-offset, high impedance input buffer.

$$V_{SHUNT} = 25 \bullet (V_{CSIN} - V_{CSOUT}) + V_{ZERO} + V_{OFFSET} \quad (6)$$

where

- V_{SHUNT} is the output voltage of the current shunt monitor
- V_{CSIN} is the charger side of the shunt resistor
- V_{CSOUT} is the battery side of the shunt resistor
- V_{ZERO} is the 0-current reference voltage
- V_{OFFSET} is the offset of the differential amplifier

The offset of the differential amplifier introduces a measurement error of ±40 µV input referred, equivalent to ±2 mA assuming a 20-mΩ shunt resistor which can be calibrated out by the system.

The shunt monitor is disabled by default and can be enabled by the host by setting the SMON_EN bit in the CONTROL register to 1.

7.4 Device Functional Modes

7.4.1 Charge Mode Operation

For current limited power source, such as a USB host or hub, the high efficiency converter is critical in fully utilizing the input power capacity and quickly charging the battery. Due to the high efficiency in a wide range of the input voltage and battery voltage, the switching mode charger is a good choice for high speed charging with less power loss and better thermal management.

The TPS65200 is a highly-integrated synchronous switched-mode charger with reverse boost function for USB OTG support, featuring integrated MOSFETs and small external components, targeted at extremely space-limited portable applications powered by 1-cell Li-ion or Li-polymer battery pack.

Device Functional Modes (continued)

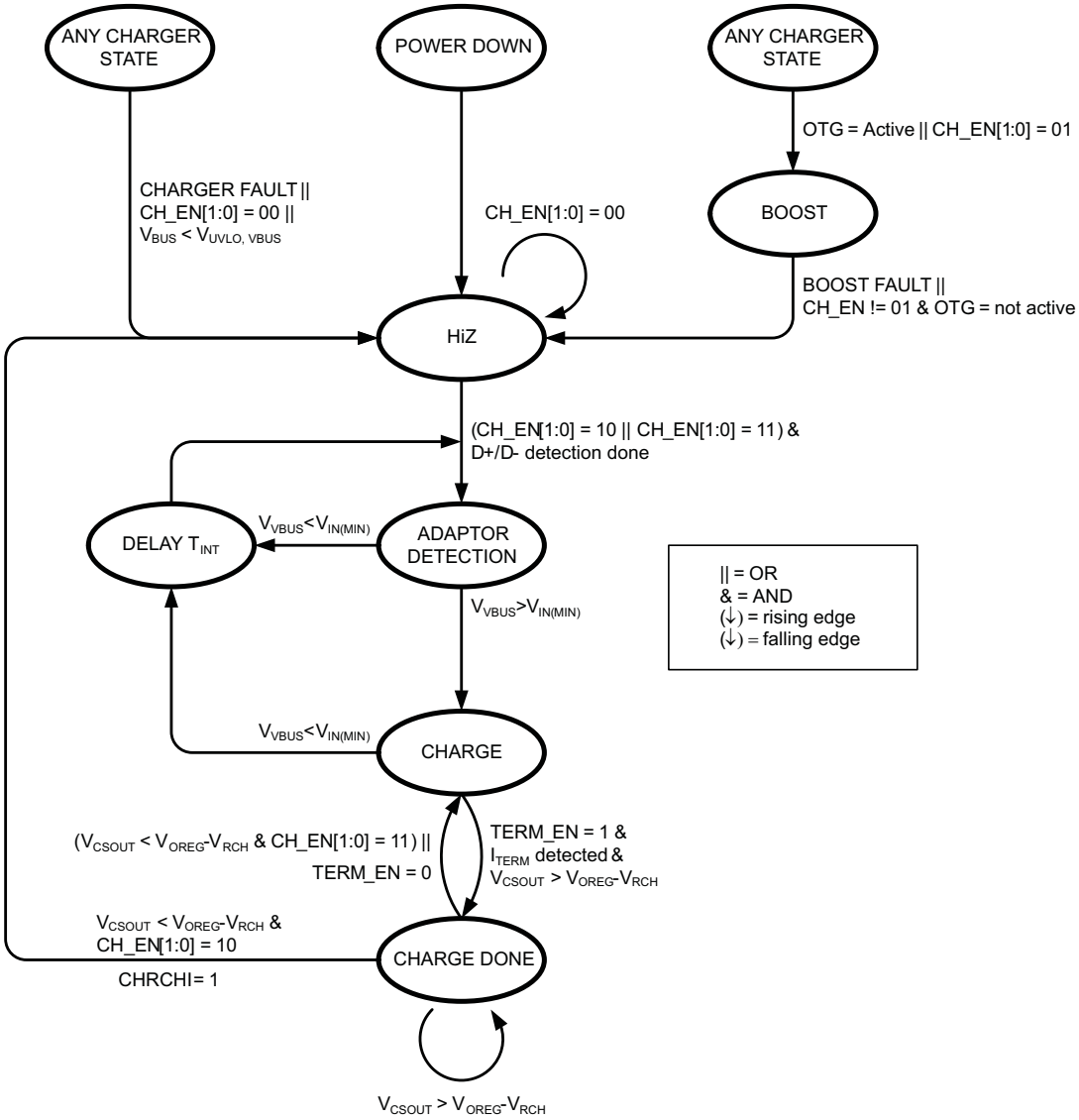


Figure 40. State Diagram of USB Charger Circuit

The TPS65200 has three operation modes: charge mode, boost mode, and high impedance mode. In charge mode, the TPS65200 supports a precision Li-ion or Li-polymer charging system for single-cell applications. In boost mode, TPS65200 will boost the battery voltage to VBUS for powering attached OTG devices. In high impedance mode, the TPS65200 charger stops charging or boosting and operates in a mode with very low current from VBUS or battery, to effectively reduce the power consumption when the portable device is in standby mode. Through carefully designed internal control circuits, TPS65200 achieves smooth transition between different operation modes.

The global state diagram of the charger is shown in Figure 40 and the detailed charging algorithm in Figure 41. HiZ mode is the default state of the charger where Q1, charger PWM and boost operation is turned off. If any fault occurs during charging, the CH_EN[1:0] bits in the CONTROL register are reset to 00b (OFF), fault bits are set in the INT2 register, an interrupt is issued on the INT pin, and HiZ mode is entered. Charging is re-initiated by either host control or automatically if VBUS is power cycled.

Device Functional Modes (continued)

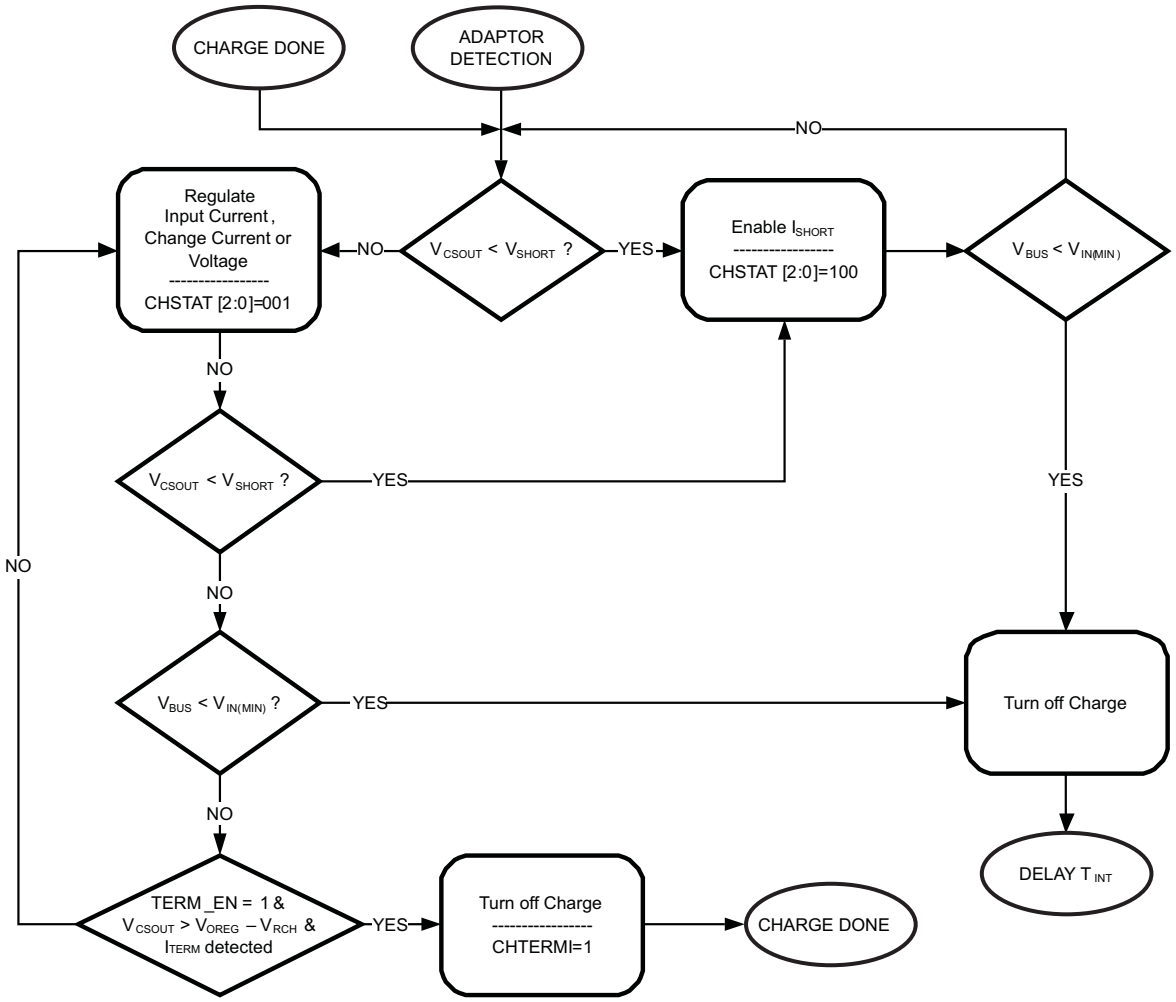


Figure 41. Detailed Charging Flow Chart

7.4.1.1 Input Current Limiting and D+/D- Detection

By default the VBUS input current limit is set to 500 mA. When VBUS is asserted the TPS65200 performs a charger source identification to determine if it is connected to a USB port or dedicated charger. This detection is performed 200 ms after VBUS is asserted to ensure the USB plug has been fully inserted before identification is performed. If a dedicated charger is detected the input current limit is increased to 975 mA, otherwise the current limit remains at 500 mA, unless changed by the user.

Automatic detection is performed only if VIO is below 0.6 V to avoid interfering with the USB transceiver which may also perform D+/D- detection when the system is running normally. However, D+/D- can be initiated at any time by the host by setting the DPDM_EN bit in the CONTROL register to 1. After detection is complete the DPDM_EN bit is automatically reset to 0 and the detection circuitry is disconnected from the DP DM pins to avoid interference with USB data transfer.

The input current limit can also be set through the I^2C interface to 100 mA, 500 mA, 975 mA, or no limit by writing to the CONFIG_B register. The effective current limit will be the higher of the D+D- detection result and the IIN_LIMIT[1:0] setting in CONFIG_A register. Whenever VBUS drops below the UVLO threshold IIN_LIMIT[1:0] is reset to 100-mA setting to avoid excessive current draw from an unknown USB port.

Once the input current reaches the input current limiting threshold, the charge current is reduced to keep the input current from exceeding the programmed threshold. The host can choose to ignore the D+D- detection result by setting the LMTSEL bit of the CONFIG_A register to 1.

Device Functional Modes (continued)

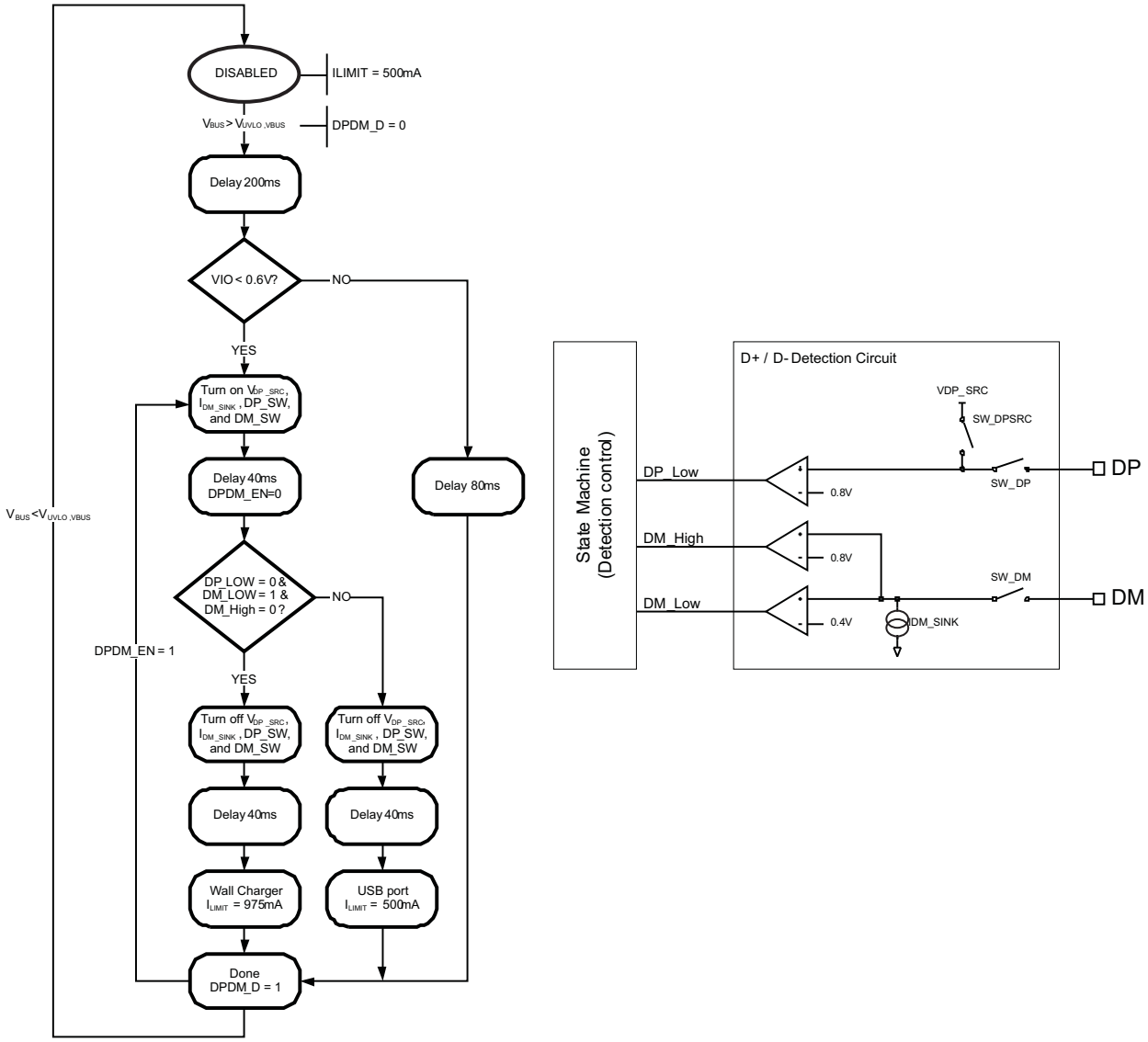


Figure 42. Adaptor Identification Algorithm and Block Diagram

7.4.1.2 Bad Adaptor Detection/Rejection (CHBADI)

At the beginning of the charge cycle, the IC will perform the bad adaptor detection by applying a current sink to VBUS. If V_{VBUS} is higher than $V_{IN(MIN)}$ for 30 ms, the adaptor is good and the charge process will begin. However, if V_{VBUS} drops below $V_{IN(MIN)}$, a bad adaptor is detected. Then, the IC will disable the current sink, issue an interrupt and set the CHBADI interrupt in the INT2 register. After a delay of TINT (2s), the IC will repeat the adaptor detection process, as shown in Figure 44.

If the battery voltage is high (> 3.8 V), it is possible that the input voltage drops below the battery voltage during adaptor rejection test. In this case, the reverse protection will kick-in and disable the charger. Also note that the 30-mA current sink is turned on for 30 ms only. If the input capacitance is > 500 µF (not recommended), the adaptor may be accepted although it is not capable of providing 30-mA of current. In these cases, the VDPPM loop will limit the charging current to maintain the input voltage.

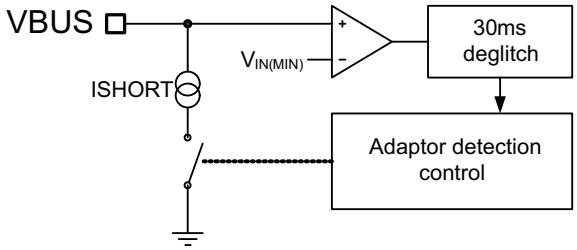


Figure 43. Bad Adaptor Detection Circuit

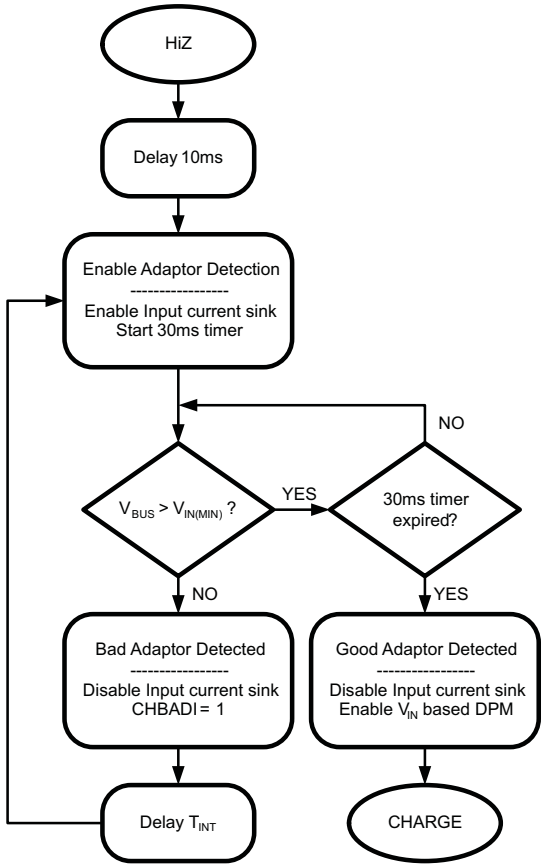


Figure 44. Bad Adaptor Detection Flow-Chart

7.4.1.3 Input Current Limiting at Start-Up

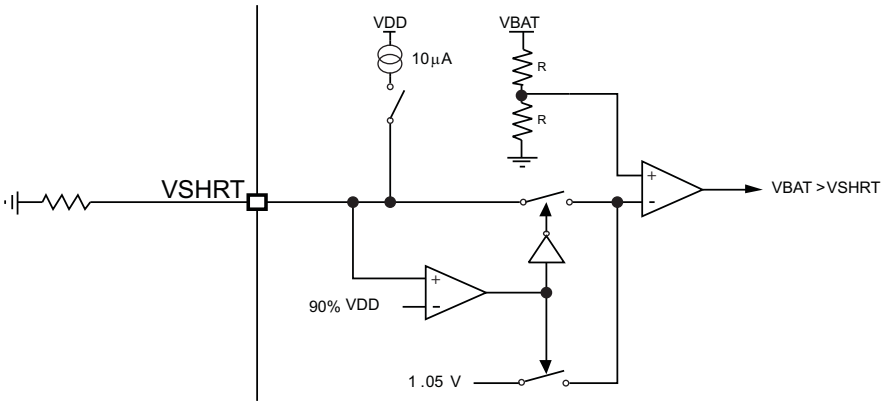
The LOW_CHG bit is automatically set when VBUS is asserted to limit the charge current to 150 mA. This ensures that a battery cannot be charged with high currents without host control.

7.4.1.4 Charge Profile

In charge mode, TPS65200 has five control loops to regulate input voltage, input current, charge current, charge voltage, and device junction temperature. During the charging process, all five loops are enabled and the one that is dominant will take over the control. The TPS65200 supports a precision Li-ion or Li-polymer charging system for single-cell applications. Figure 46 indicates a typical charge profile without input current regulation loop and it is similar to the traditional CC/CV charge curve, while Figure 47 shows a typical charge profile when input current limiting loop is dominant during the constant current mode, and in this case the charge current is higher than the input current so the charge process is faster than the linear chargers. For TPS65200, the input current limits, the charge current, termination current, and charge voltage are all programmable using I^2C interface.

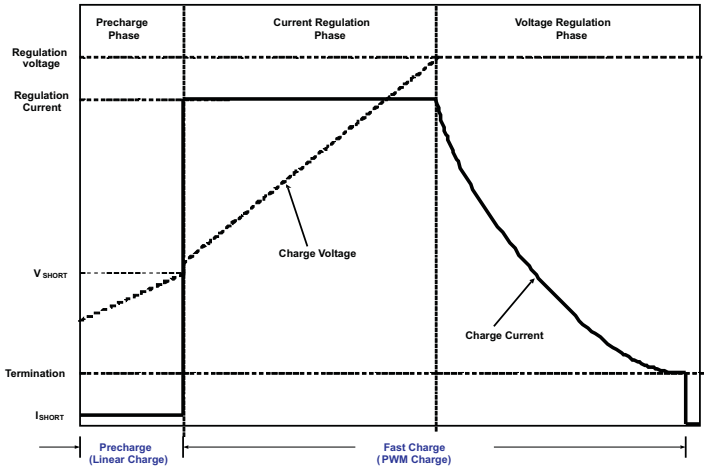
7.4.1.5 Precharge to Fast Charge Threshold (VSHORT)

A deeply discharged battery ($V_{BAT} < V_{SHORT}$) is charged with a constant current of I_{SHORT} (typically 30 mA) until the voltage recovers to > V_{SHORT} at which point fast charging begins. The pre-charge to fast-charge threshold has a default value of 2.1 V and can be adjusted by connecting a resistor from the VSHRT pin to ground. An internal current source forces a 10-µA current into the resistor and the resulting voltage is compared to half the battery voltage to determine if the battery is deeply discharged or shorted. Therefore the voltage on the VSHRT pin equals half of V_{SHORT} threshold. For example a 100-kΩ resistor connected from VSHRT to GND results in a 2-V precharge to fast charge transition point. If the VSHRT pin is left floating or is shorted to the VDD pin, an internal reference voltage of 1.05 V is used resulting in a 2.1-V pre-charge to fast-charge threshold.



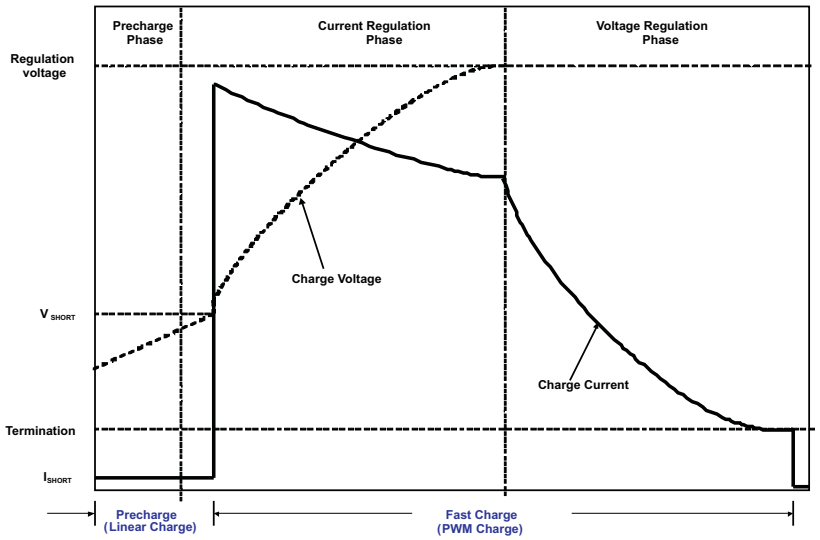
VSHORT can be adjusted by an external resistor. Note that the VSHRT pin voltage equals half VSHORT threshold. When VSHRT pin is left floating or is tied to VDD, an internal reference of 1.05 V is used resulting in a 2.1-V pre-charge to fast-charge transition threshold.

Figure 45. Precharge to Fast-Charge Transition Threshold (VSHORT)



The input current remains constant during current regulation phase.

Figure 46. Typical Charging Profile of TPS65200 Without Input Current Limit



The charging current during current regulation phase decreases as battery voltage increases. This mode ensures fastest charging of the battery without exceeding the adaptor current limit.

Figure 47. Typical Charging Profile of TPS65200 With Input Current Limit

7.4.1.6 PWM Controller in Charge Mode

The TPS65200 provides an integrated, fixed 3-MHz frequency voltage-mode controller with feed-forward function to regulate charge current or voltage. This type of controller is used to help improve line transient response, thereby simplifying the compensation network used for both continuous and discontinuous current conduction operation. The voltage and current loops are internally compensated using a Type-III compensation scheme that provides enough phase margin for stable operation, allowing the use of small ceramic capacitors with very low ESR. There is a 0.5-V offset on the bottom of the PWM ramp to allow the device to operate between 0% to 99.5% duty cycles.

The TPS65200 has two back-to-back common-drain N-channel MOSFETs at the high side and one N-channel MOSFET at the low side. An input N-MOSFET (Q1) prevents battery discharge when VBUS is lower than V_{CSOUT}. The second high-side N-MOSFET (Q2) behaves as the switching control switch. A charge pump circuit is used to provide gate drive for Q1, while a boot strap circuit with external boot-strap capacitor is used to boost up the gate drive voltage for Q2.

Cycle-by-cycle current limit is sensed through the internal sense MOSFETs for Q2 and Q3. The threshold for Q2 is set to a nominal 1.9-A peak current. The low-side MOSFET (Q3) also has a current limit that decides if the PWM controller will operate in synchronous or non-synchronous mode. This threshold is set to 100mA and it turns off the low-side N-channel MOSFET (Q3) before the current reverses, preventing the battery from discharging. Synchronous operation is used when the current of the low-side MOSFET is greater than 100 mA to minimize power losses.

7.4.1.7 Battery Charging Process

During precharge phase, while the battery voltage is below the V_{SHORT} threshold, the TPS65200 applies a short-circuit current, I_{SHORT}, to the battery. When the battery voltage is above V_{SHORT} and below V_{OREG}, the charge current ramps up to fast charge current, $I_{OCHARGE}$, or a charge current that corresponds to the input current of I_{IN_LIMIT}. The slew rate for fast charge current is controlled to minimize the current and voltage over-shoot during transient. Both the input current limit (default at 100 mA), I_{IN_LIMIT}, and fast charge current, $I_{OCHARGE}$, can be set by the host. Once the battery voltage is close to the regulation voltage, V_{OREG}, the charge current is tapered down as shown in Figure 46. The voltage regulation feedback occurs by monitoring the battery-pack voltage between the CSOUT and PGND pins. TPS65200 is a fixed single-cell voltage version, with adjustable regulation voltage (3.5 V to 4.44 V) programmed through I^2C interface.

The TPS65200 monitors the charging current during the voltage regulation phase. When the termination threshold, I_{TERM}, is detected and the battery voltage is above the recharge threshold, the TPS65200 terminates charge. The termination current level is programmable and charge termination is disabled by default. To enable the charge current termination, the host can set the charge termination bit TERM_EN of CONFIG_C register to 1. Refer to I^2C section for details.

A new charge cycle is initiated when one of the following events occur:

- VBUS is power-cycled.
- CH_EN[1:0] = 11b and the battery voltage drops below the recharge threshold (TERM_EN = 1).
- The RESET bit is set (host controlled).
- The device is in CHARGE DONE state (see Figure 40) and the TERM_EN bit is set from 1 to 0.

7.4.1.8 Thermal Regulation and Protection

During the charging process, to prevent overheating of the chip, TPS65200 monitors the junction temperature, T_J, of the die and begins to taper down the charge current once T_J reaches the thermal regulation threshold, T_{CF}. The charge current will be reduced to zero when the junction temperature increases about 10°C above T_{CF}. At any state, if T_J exceeds T_{SHTDWN}, TPS65200 will suspend charging and enter HiZ state. Charging will resume after T_J falls 10°C below T_{SHTDWN}.

7.4.1.9 Safety Timer in Charge and Boost Mode (CH32MI, BST32SI)

The TPS65200 charger hosts a safety timer that stops any boost or charging action if host control is lost. The timer is started when the CH_EN[1:0] bits are set to anything different from 00 and is continuously reset by any valid I^2C command. If the timer exceeds 32 s and boost mode is enabled (CH_EN[1:0] = 01b), the boost is disabled, CH_EN[1:0] is set to 00b, boost time-out fault is indicated in the INT2 register, and an interrupt is issued. Similarly, once the timer exceeds 32 minutes and the charger is enabled (CH_EN[1:0] = 10b or 11b), the charger is disabled, CH_EN[1:0] is set to 00b, charger time-out fault is indicated in INT2 register and an interrupt is issued. Time-out faults affect CH_EN[1:0] bits only and not charger parameters. The safety timer flow chart is shown in Figure 48.

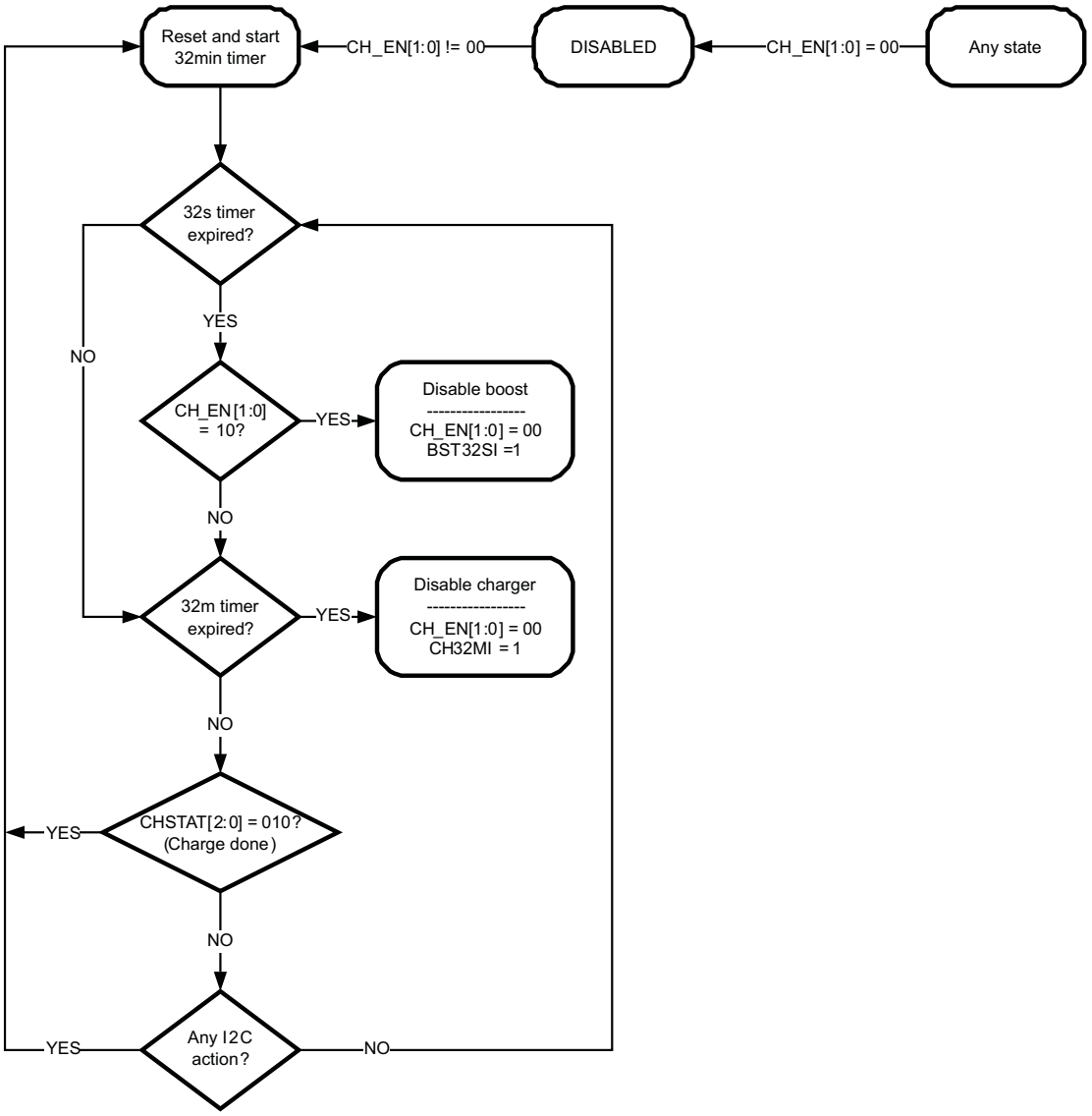


Figure 48. Timer Flow Chart for TPS65200 Charger

7.4.1.10 Input Voltage Protection in Charge Mode

7.4.1.10.1 Input Overvoltage Protection (VBUSOVPI)

The TPS65200 provides a built-in input overvoltage protection to protect the device and other components against damage if the input voltage (voltage from VBUS to PGND) gets too high. When an input overvoltage condition is detected, the TPS65200 turns off the PWM converter, sets the VBUSOVPI bit in the INT1 register and issues an interrupt. Once V_{VBUS} drops below the input overvoltage exit threshold, the fault is cleared and charge process resumes.

7.4.1.10.2 Reverse Current Protection (CHRVPI)

The TPS65200 charger enters Hi-Z state if the voltage on VBUS pin falls below V_{CSOUT} + V_{REV}, and V_{BUS} is still higher than the poor source detection threshold, $V_{IN(MIN)}$. The CHRVPI bit is set in the INT2 register and an interrupt is issued. This feature prevents draining the battery during the absence of V_{BUS}. In Hi-Z mode, both the reverse blocking switch Q1 and PWM are turned off.

7.4.1.10.3 Input Voltage Based Dynamic Power Management (CHDPMI)

During normal charging process, if the input power source is not able to support the charging current, V_{BUS} voltage will decease. Once V_{VBUS} drops to V_{IN_LOW} (default 4.36 V), the charge current will taper down to prevent further drop of V_{BUS}. This feature makes the IC compatible with adaptors with different current capabilities. Whenever the VDPM loop activates, the CHDPMI interrupt is set in the INT2 register and the INT pin is pulled low. The CHDPMI interrupt is delayed by 32 ms to prevent the interrupt to occur when the charging source is removed.

7.4.1.11 Battery Protection in Charge Mode

7.4.1.11.1 Battery Charge Current Limiting

Whenever a valid power source is connected to the charger, the LOW_CHG bit of the CONFIG_C register is set to 1 which limits the charging current to 150 mA. Once the host detects that that charging source has been inserted it needs to reset the LOW_CHG bit to 0 to achieve a higher charging current. This feature prevents charging of a battery at high currents when system voltage is too low for the system to boot.

7.4.1.11.2 Output Overvoltage Protection (CHBATOVPI)

The TPS65200 provides a built-in overvoltage protection to protect the device and other components against damage if the battery voltage gets too high, as when the battery is suddenly removed. When an overvoltage condition is detected, TPS65200 turns off the PWM converter, sets the CHBATOVPI bit in the INT2 register, issues an interrupt, and enters HiZ mode. Once V_{CSOUT} drops to the battery overvoltage exit threshold, charging resumes.

7.4.1.11.3 Battery Short Protection

During the normal charging process, if the battery voltage is lower than the short-circuit threshold, V_{SHORT}, the charger will operate in short circuit mode with a lower charge rate of I_{SHORT}.

7.4.1.12 Charge Status Output, STAT Pin

The STAT pin is used to indicate charging status of the IC and its behavior can be controlled by setting the STAT_EN bits of the CONTROL register. In AUTO mode, STAT is pulled low during charging and is high-impedance otherwise. STAT pin can also be forced low or to Hi-Z state by setting the STAT_EN bits accordingly. The STAT pin has enough pulldown strength to drive a LED and can be used for visual charge status indication.

7.4.2 Boost Mode Operation

In 32 second mode, when CH_EN[1:0] = 01 in CONTROL register, TPS65200 operates in boost mode and delivers power to VBUS from the battery. In normal boost mode, TPS65200 converts the battery voltage (2.5V to 4.5 V) to VBUS-B (5 V) and delivers a current as much as IBO (200 mA) to support other USB OTG devices connected to the USB connector. Boost mode can also be enabled through the OTG pin. By default the OTG pin is disabled and can be enabled by setting the OTG_EN bit to 1. The polarity of the OTG pin is user programmable through the OTG_PL bit. Both bits are located in the CONFIG_C register. The OTG pin allows the USB transceiver to take control of the boost function without involvement of the main processor.

7.4.2.1 PWM Controller in Boost Mode

Similar to charge mode operation, in boost mode, the TPS65200 provides an integrated, fixed 3-MHz frequency voltage-mode controller to regulate output voltage at PMID pin (V_{PMID}). The voltage control loop is internally compensated using a Type-III compensation scheme that provides enough phase margin for stable operation with a wide load range and battery voltage range.

In boost mode, the input N-MOSFET (Q1) prevents battery discharge when VBUS pin is over loaded. Cycle-by-cycle current limit is sensed through the internal sense MOSFET for Q3. The threshold for Q3 is set to a nominal 1.0-A peak current. The upper-side MOSFET (Q2) also has a current limit that decides if the PWM controller will operate in synchronous or non-synchronous mode. This threshold is set to 75 mA and it turns off the high-side N-channel MOSFET (Q2) before the current reverses, preventing the battery from charging. Synchronous operation is used when the current of the high-side MOSFET is greater than 75 mA to minimize power losses.

7.4.2.2 Boost Start Up

To prevent the inductor saturation and limit the inrush current, a soft-start control is applied during the boost start up.

7.4.2.3 PFM Mode at Light Load

In boost mode, TPS65200 will operate in pulse skipping mode (PFM mode) to reduce the power loss and improve the converter efficiency at light load condition. During boosting, the PWM converter is turned off once the inductor current is less than 75 mA; and the PWM is turned back on only when the voltage at PMID pin drops to about 99.5% of the rated output voltage. A unique pre-set circuit is used to make the smooth transition between PWM and PFM mode.

7.4.2.4 Safety Timer in Boost Mode (BST32SI)

At the beginning of boost operation, the TPS65200 starts a 32-second timer that is reset by the host through any valid I^2C transaction to the IC. Once the 32-second timer expires, TPS65200 will turn off the boost converter, issue an interrupt, set the BST32SI bit in the INT3 register, and return to Hi-Z mode. Fault condition is cleared by POR or reading the INT3 register.

7.4.2.5 Protection in Boost Mode

7.4.2.5.1 Output Overvoltage Protection (BSTBUSOVI)

The TPS65200 provides a built-in overvoltage protection to protect the device and other components against damage if the VBUS voltage gets too high. When an overvoltage condition is detected, TPS65200 turns off the PWM converter, resets CH_EN[1:0] bits to 00b (OFF), sets the BSTBUSOVI bit in the INT3 register, issues an interrupt, and enters HiZ mode. Once VVBUS drops to the normal level, the boost will start after host sets CH_EN[1:0] = 01b.

7.4.2.5.2 Output Over-Load Protection (BSTOLI)

The TPS65200 provides a built-in over-load protection to prevent the device and battery from damage when VBUS is over loaded. Once an over load condition is detected, Q1 will operate in linear mode to limit the output current while VPMID is kept in voltage regulation. If the over load condition lasts for more than 30 ms, the over-load fault is detected. When an over-load condition is detected, TPS65200 turns off the PWM converter, resets CH_EN[1:0] bits to 00b (OFF), sets the BSTOLI bit in the INT3 register, and issues an interrupt. The boost will not start until the host sets CH_EN[1:0] = 01b or the OTG pin is toggled.

7.4.2.5.3 Battery Voltage Protection (BSTLOWVI, BSTBATOVI)

During boosting, when battery voltage is above the battery overvoltage threshold, V_{BATMAX}, or below the minimum battery voltage threshold, V_{BATMIN}, TPS65200 will turn off the PWM converter, reset CH_EN[1:0] bits to 00b (OFF), set the BSTLOWVI or BSTBATOVI bit in the INT3 register, and issues an interrupt. Once the battery voltage goes back to the normal level, the boost will start if the host sets CH_EN[1:0] = 01b or the OTG pin is toggled.

7.4.3 High Impedance Mode

When CH_EN[1:0] bits in the CONTROL register are set to 00b, TPS65200 will operate in high impedance mode, with the impedance looking into VBUS pin higher than 500kΩ.

7.5 Programming

7.5.1 I²C Bus Operation

The TPS65200 hosts a slave I²C interface that supports data rates up to 400 kbit/s and auto-increment addressing and is compliant to I²C standard 3.0.

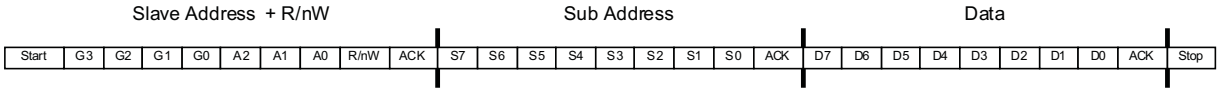


Figure 49. Subaddress in I²C Transmission

Start – Start Condition
G(3:0) – Group ID: Address fixed at 1101
A(2:0) – Device Address: Address fixed at 010
R/nW – Read / not Write Select Bit
ACK – Acknowledge
S(7:0) – Subaddress: defined per register map
D(7:0) – Data; Data to be loaded into the device
Stop – Stop Condition

The I²C bus is a communications link between a controller and a series of slave terminals. The link is established using a two-wired bus consisting of a serial clock signal (SCL) and a serial data signal (SDA). The serial clock is sourced from the controller in all cases where the serial data line is bi-directional for data communication between the controller and the slave terminals. Each device has an open drain output to transmit data on the serial data line. An external pull-up resistor must be placed on the serial data line to pull the drain output high during data transmission.

Data transmission is initiated with a start bit from the controller as shown in Figure 50. The start condition is recognized when the SDA line transitions from high to low during the high portion of the SCL signal. Upon reception of a start bit, the device will receive serial data on the SDA input and check for valid address and control information. If the appropriate group and address bits are set for the device, then the device will issue an acknowledge pulse and prepare the receive subaddress data. Subaddress data is decoded and responded to as per the Register Map section of this document. Data transmission is completed by either the reception of a stop condition or the reception of the data word sent to the device. A stop condition is recognized as a low to high transition of the SDA input during the high portion of the SCL signal. All other transitions of the SDA line must occur during the low portion of the SCL signal. An acknowledge is issued after the reception of valid address, sub-address and data words. The I²C interface will auto-sequence through register addresses, so that multiple data words can be sent for a given I²C transmission.

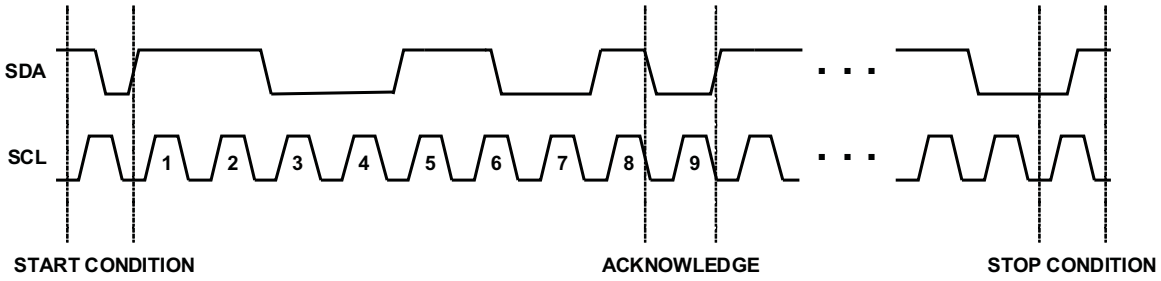


Figure 50. I²C Start/Stop/Acknowledge Protocol

7.6 Register Maps

Table 1. Register Address Map

REGISTER	ADDRESS (HEX)	NAME	DEFAULT VALUE	DESCRIPTION
0	0	CONTROL	0000 1010	Enable control register
1	1	CONFIG_A	0000 0001	Charger current register
2	2	CONFIG_B	0001 1001	Charger voltage register
3	3	CONFIG_C	1000 1010	Special charger settings
4	4	CONFIG_D	0100 0000	Charger safety limits settings
5	5	WLED	0001 1111	WLED feedback voltage setting
6	6	STATUS_A	0100 0000	Status register A
7	7	STATUS_B	0000 0001	Status register B
8	8	INT1	0000 0000	Interrupt bits
9	9	INT2	0000 0000	Interrupt bits (charger)
10	0A	INT3	0000 0000	Interrupt bits (boost)
11	0B	MASK1	0000 0000	Interrupt masking bits
12	0C	MASK2	0000 0000	Interrupt masking bits
13	0D	MASK3	0000 0000	Interrupt masking bits
14	0E	CHIPID	0000 0000	Chip ID register

7.6.1 Control Register (CONTROL)

Address – 0x00h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	STAT_EN[1:0]		SMON_EN	WLED_EN	LDO_EN	DPDM_EN	CH_EN [1:0]	
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET VALUE	0	0	0	0	1	0	1	0

FIELD NAME	BIT DEFINITION
STAT_EN[1:0	STAT enable bits 00 – AUTO (controlled by charger status) 01 – ON (low impedance) 10 – OFF (high impedance) 11 – not defined
SMON_EN	Shunt monitor enable bit 0 – Disabled 1 – Enabled
WLED_EN	WLED enable bit 0 – Disabled 1 – Enabled NOTE: WLED can also be enabled through CTRL pin.
LDO_EN	LDO enable bit 0 – Disabled 1 – Enabled
DPDM_EN	D+/D- detection enable 0 – Disabled 1 – Enabled NOTE: Bit is automatically reset after detection is completed.
CH_EN[1:0]	Charger enable bits 00 – Disabled / HiZ mode 01 – Boost mode 10 – Charge 11 – Charge with automatic recharge

7.6.2 Charger Config Register A (CONFIG_A)

Address – 0x01h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	LMTSEL	VICHRG[3:0]				VITERM[2:0]		
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET VALUE	0	0	0	0	0	0	0	1

FIELD NAME	BIT DEFINITION(1)
LMTSEL	Input Current Limit selction 0 – Input current limit is set to the higher of IIN_LIMIT[1:0] (CONFIG_B) and D+D- det. result 1 – IIN_LIMIT[1:0] (CONFIG_B) applied, D+D- detection result is ignored
VICHRG[3:0]	Charge current sense voltage (current equivalent for 20 mΩ shunt) 0000 – 11 mV (550 mA) 0001 – 13 mV (650 mA) 0010 – 15 mV (75 mA) 0011 – 17 mV (850 mA) 0100 – 19 mV (950 mA) 0101 – 21 mV (105 mA) 0101 – 21 mV (1050 mA) 0110 – 23 mV (1150 mA) 0111 – 25 mV (1250 mA) 1000 – 27 mV (1350 mA) 1001 – 29 mV (1450 mA) 1010 – 31 mV (1550 mA) ... 1111 – 31 mV (1550 mA)
VITERM[2:0]	Termination current sense voltage (current equivalent for 20 mΩ shunt) 000 – 1 mV (50 mA) 001 – 2 mV (100 mA) 010 – 3 mV (150 mA) 011 – 4 mV (200 mA) 100 – 5 mV (250 mA) 101 – 6 mV (300 mA) 110 – 7 mV (350 mA) 111 – 8 mV (400 mA)

(1) During charging the lower value of VMCHRG[3:0] (CONFIG_D register) and VICHRG[2:0] applies.

7.6.3 Charger Config Register B (CONFIG_B)

Address – 0x02h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	IIN_LIMIT[1:0]		VOREG[5:0]					
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET VALUE	0	0	0	1	1	0	0	1

FIELD NAME	BIT DEFINITION(1)
IIN_LIMIT[1:0]	Input current limit setting 00 – 100 mA 01 – 500 mA 10 – 975 mA 11 – No input current limit
VOREG[5:0]	Battery regulation voltage / boost output voltage 00 0000 – 3.50 V / 4.425 V 00 0001 – 3.52 V / 4.448 V 00 0011 – 3.56 V / 4.471 V ... 01 1000 – 3.98 V / 4.077 V 01 1001 – 4.00 V / 5 V 01 1010 – 4.02 V / 5.023 V ... 10 1111 – 4.44 V / 5.5 V ... 11 1111 – 4.44 V / 5.5 V

(1) During charging the lower value of VMREG[3:0] (CONFIG_D register) and VOREG[5:0] applies.

7.6.4 Charger Config Register C (CONFIG_C)

Address – 0x03h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	VS_REF	OTG_PL	OTG_EN	TERM_EN	LOW_CHG	VSREG[2:0]		
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET VALUE	1	0	0	0	1	0	1	0

FIELD NAME	BIT DEFINITION
VS_REF	VSHORT reference select 0 – Internal (2.1 V) reference 1 – Current source on VSHRT pin is enabled. Pin voltage is used as 0.5 x VSHORT threshold.
OTG_PL	OTG pin polarity 0 – Active low 1 – Active high
OTG_EN	OTG pin enable 0 – Pin is disabled 1 – Pin is enabled
TERM_EN	Charge termination enable 0 – Disabled 1 – Enabled
LOW_CHG	Low charge current enable bit (current equivalent for 20 mΩ shunt) 0 – Normal charge current sense voltage per register CONFIG_A 1 – 3 mV (150 mA)
VSREG[2:0]	Input voltage DPM regulation voltage 000 – 4.20 V 001 – 4.28 V 010 – 4.36 V 011 – 4.44 V 100 – 4.52 V 101 – 4.60 V 110 – 4.68 V 111 – 4.76 V

7.6.5 Charger Config Register D (CONFIG_D)

Address – 0x04h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	VMCHRG[3:0]				VMREG[3:0]			
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET VALUE	0	1	0	0	0	0	0	0

FIELD NAME	BIT DEFINITION(1)
VMCHRG[3:0]	Maximum charge current sense voltage (current equivalent for 20 mΩ shunt) 0000 – 11 mV (550 mA) 0001 – 13 mV (650 mA) 0010 – 15 mV (750 mA) 0011 – 17 mV (850 mA) 0100 – 19 mV (950 mA) 0101 – 21 mV (1050 mA) 0110 – 23 mV (1150 mA) 0111 – 25 mV (1250 mA) 1000 – 27 mV (1350 mA) 1001 – 29 mV (1450 mA) 1010 – 31 mV (1550 mA) … 1111 – 31 mV (1550 mA)
VMREG[3:0]	Maximum battery regulation voltage 0000 – 4.20 V 0001 – 4.22 V 0010 – 4.24 V … 1100 – 4.44 V ... 1111 – 4.44 V

(1) CONFIG_D register is reset to its default value when V_{CSOUT} voltage drops below V_{SHORT} threshold (typ.2.05 V). After V_{CSOUT} recovers to $V_{CSOUT} > V_{SHORT}$ CONFIG_D register value can be changed by the host until one of the other registers is written to. Writing to any other register locks the CONFIG_D register from subsequent writes. If CONFIG_D is not the first register to be written after reset, the default values apply. During charging the lower value of VMCHRG[3:0] and VICHRG[2:0] (CONFIG_A register), and VMREG[3:0] and VOREG[5:0] (CONFIG_B register) apply.

7.6.6 WLED Control Register (WLED)

Address – 0x05h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	Not used	Not used	Not used	VFB[4:0]				
READ/WRITE	R	R	R	R/W	R/W	R/W	R/W	R/W
RESET VALUE	0	0	0	1	1	1	1	1

FIELD NAME	BIT DEFINITION
Not used	N/A
Not used	N/A
Not used	N/A
VFB[4:0	WLED feedback voltage 0 0000 – 0% 0 0001 – 2.5% 0 0010 – 4% 0 0011 – 5.5% 0 0100 – 7.5% 0 0101 – 8.5% 0 0110 – 10% 0 0111 – 11.5% 0 1000 – 13% 0 1001 – 14.5% 0 1010 – 16% 0 1011 – 17.5% 0 1100 – 19% 0 1101 – 22% 0 1110 – 25% 0 1111 – 28% 1 0000 – 31% 1 0001 – 34% 1 0010 – 37% 1 0011 – 40% 1 0100 – 43% 1 0101 – 46% 1 0110 – 49% 1 0111 – 52% 1 1000 – 58% 1 1001 – 64% 1 1010 – 70% 1 1011 – 76% 1 1100 – 82% 1 1101 – 88% 1 1110 – 94% 1 1111 – 100%

7.6.7 Status Register A (STATUS_A)

Address – 0x06h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	Not used	STANDBY	MONITOR	CHSTAT [2:0]			LDO	WLED
READ/WRITE	R	R	R	R	R	R	R	R
RESET VALUE	0	1	0	0	0	0	0	0

FIELD NAME	BIT DEFINITION(1)
Not used	N/A
STANDBY	Standby status indicator 0 – Device is in ACTIVE mode 1 – Device is in STANDBY mode
MONITOR	Current shunt monitor status indicator 0 – Current shunt monitor is disabled 1 – Current shunt monitor is enabled
CHSTAT [2:0]	Charger status bit 000 – High impedance mode 001 – Charge in progress (fast charge) 010 – Charge done 011 – Boost mode 100 – Charge in progress (pre charge) 101 – Not defined 110 – Not defined 111 – Not defined
LDO	LDO status bit 0 – LDO is disabled (OFF) 1 – LDO is enabled (ON), no fault
WLED	WLED status bit 0 – WLED disabled (OFF) 1 – WLED enabled

(1) Default values reflect state after Power-ON Reset, no charger plugged in, no faults present.

7.6.8 Status Register B (STATUS_B)

Address – 0x07h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	RESET	Not used	Not used	Not used	Not used	DPDM_D	DPDM_R	OTG
READ/WRITE	W	R	R	R	R	R	R	R
RESET VALUE	0	0	0	0	0	0	0	1

FIELD NAME	BIT DEFINITION(1)
RESET	Reset 0 – No effect 1 – Reset all parameters to default values NOTE: Read always returns “0”
Not used	N/A
Not used	N/A
Not used	N/A
Not used	N/A
DPDM_D	D+/D- detection done bit 0 – DPDM detection in progress or not started after initial power-up reset 1 – DPDM detection is complete
DPDM_R	D+D- detection result 0 – Standard USB port (500-mA current limit) 1 – USB charger (1000-mA current limit)
OTG	OTG pin status 0 – OTG pin at low level 1 – OTG pin at high level

(1) Default values reflect state after Power-ON Reset, no charger plugged in, no faults present, OTG pin high..

7.6.9 Interrupt Register 1 (INT1)

Address – 0x08h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	TSDI	VBUSOVPI	Not used	Not used/ Reserved	Not used/ Reserved	Not used/ Reserved	Not used/ Reserved	WLEDI
READ/WRITE	R	R	R	R/W	R/W	R/W	R/W	R
RESET VALUE	0	0	0	0	0	0	0	0

FIELD NAME	BIT DEFINITION
TSDI	Thermal shutdown fault. Set if die temperature exceeds thermal shutdown threshold. Reset when die temperature drops below TSD release threshold.
VBUSOVPI	VBUS overvoltage protection. Set when $V_{BUS} > V_{OVP\text{-}IN\_USB}$ is detected.
Not used	N/A
Not used / Reserved	N/A / Reserved
Not used / Reserved	N/A / Reserved
Not used / Reserved	N/A / Reserved
Not used / Reserved	N/A / Reserved
WLEDI	WLED driver over voltage

7.6.10 Interrupt Register 2 (INT2)

Address – 0x09h

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	CHRVPI	CHBADI	CHBATOVI	CHTERMI	CHRCHGI	CH32MI	CHTREGI	CHDPMI
READ/WRITE	R	R	R	R	R	R	R	R
RESET VALUE	0	0	0	0	0	0	0	0

FIELD NAME	BIT DEFINITION(1)
CHRVPI	Charger fault. Reverse protection (VV_{BUS} > $V_{IN(MIN)}$ and V_{VBUS} < $V_{CSOUT+VREV}$ (fault)
CHBADI	Charger fault. Bad adaptor (V_{BUS} < $V_{IN(MIN)}$)
CHBATOVI	Charger fault. Battery OVP
CHTERMI	Charge terminated
CHRCHGI	Recharge request (V_{CSOUT} < $V_{OREG\ –\ VRCH}$)
CH32MI	Charger fault. 32 m time-out (fault)
CHTREGI	Charger warning. Thermal regulation loop active.
CHDPMI	Charger warning. Input voltage DPM loop active.

(1) All charger faults result in disabling the charger (CH_EN[1:0] = 00). Recharge request disables the charger only if CH_EN[1:0] = 10.

7.6.11 Interrupt Register 3 (INT3)

Address – 0x0Ah

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	BSTBUSOVI	BSTOLI	BSTLOWVI	BSTBATOVI	BST32SI	Not used	Not used	Not used
READ/WRITE	R	R	R	R	R	R	R	R
RESET VALUE	0	0	0	0	0	0	0	0

FIELD NAME	BIT DEFINITION(1)
BSTBUSOVI	Boost fault. VBUS OVP (V_{BUS} > V_{BUSOVP})
BSTOLI	Boost fault. Over load.
BSTLOWVI	Boost fault. Battery voltage is too low.
BSTBATOVI	Boost fault. Battery over voltage.
BST32SI	Boost fault. 32-s time-out fault.
Not used	N/A
Not used	N/A
Not used	N/A

(1) All BOOST faults result in disabling the boost converter (CH_EN[1:0] = 00).

7.6.12 Interrupt Mask Register 1 (MASK1)

Address – 0x0Bh

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	TSDM	VBUSOVPM	Not used	Not used	Not used	Not used	Not used	WLEDM
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET VALUE	0	0	0	0	0	0	0	0

FIELD NAME	BIT DEFINITION(1)
TSDM	TSD fault interrupt mask 0 – Interrupt not masked 1 – Interrupt masked
VBUSOVPM	VBUS OVP fault interrupt mask 0 – Interrupt not masked 1 – Interrupt masked
Not used	N/A
Not used	N/A
Not used	N/A
Not used	N/A
Not used	N/A
WLEDM	WLED fault interrupt mask 0 – Interrupt not masked 1 – Interrupt masked

(1) Setting any of the interrupt mask bits does not disable protection circuits. When set, the respective fault will not be signaled on the INT pin.

7.6.13 Interrupt Mask Register 2 (MASK2)

Address – 0x0Ch

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	CHRVPM	CHBADM	CHBATOVM	CHTERMM	CHRCHGM	CH32MM	CHTREGM	CHDPMM
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET VALUE	0	0	0	0	0	0	0	0

FIELD NAME	BIT DEFINITION(1)
CHRVPM	Charger reverse protection interrupt mask 0 – Interrupt not masked 1 – Interrupt masked
CHBADM	Charger Bad adaptor interrupt mask 0 – Interrupt not masked 1 – Interrupt masked
CHBATOVM	Charger battery overvoltage interrupt mask 0 – Interrupt not masked 1 – Interrupt masked
CHTERMM	Charge terminated interrupt mask 0 – Interrupt not masked 1 – Interrupt masked
CHRCHGM	Charger recharge request interrupt mask 0 – Interrupt not masked 1 – Interrupt masked
CH32MM	Charger 32m timeout interrupt mask 0 – Interrupt not masked 1 – Interrupt masked
CHTREGM	Charger thermal regulation loop active interrupt mask 0 – Interrupt not masked 1 – Interrupt masked
CHDPMM	Charger input current DPM active interrupt mask 0 – Interrupt not masked 1 – Interrupt masked

(1) Setting any of the interrupt mask bits does not disable protection circuits. When set, the respective fault will not be signaled on the INT pin

7.6.14 Interrupt Mask Register 3 (MASK3)

Address – 0x0Dh

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	BSTBUSOVM	BSTOLM	BSTLOWVM	BSTBATOVM	BST32SM	Not used	Not used	Not used
READ/WRITE	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
RESET VALUE	0	0	0	0	0	0	0	0

FIELD NAME	BIT DEFINITION(1)
BSTBUSOVM	Boost VBUS overvoltage interrupt mask 0 – Interrupt not masked 1 – Interrupt masked
BSTOLM	Boost over load interrupt mask 0 – Interrupt not masked 1 – Interrupt masked
BSTLOWVM	Boost low battery voltage interrupt mask 0 – Interrupt not masked 1 – Interrupt masked
BSTBATOVM	Boost battery overvoltage interrupt mask 0 – Interrupt not masked 1 – Interrupt masked
BST32SM	Boost 32s time out interrupt mask 0 – Interrupt not masked 1 – Interrupt masked
Not used	N/A
Not used	N/A
Not used	N/A

(1) Setting any of the interrupt mask bits does not disable protection circuits. When set, the respective fault will not be signaled on the INT pin.

7.6.15 Chip ID Register (CHIPID)

Address – 0x0Eh

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	VENDOR[1:0]		CHIP[2:0]			REV[2:0]		
READ/WRITE	R	R	R	R	R	R	R	R
RESET VALUE	0	0	0	0	0	0	0	1 (1)

(1) Device dependent.

FIELD NAME	BIT DEFINITION
VENDOR[1:0]	Vendor code 00 – default 00 – Default
CHIP[2:0]	Chip ID 000 – TPS65200 001 – Future use ... 111 – Future use
REV[2:0]	Revision code 000 – Revision 1.0 001 – Revision 1.1 010 – Future use ... 111 – Future use

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS65200 device is designed to serve as a Li+ battery charger with an additional WLED driver and current shunt monitor. A typical application design for this usage will be described in *Typical Application*.

8.2 Typical Application

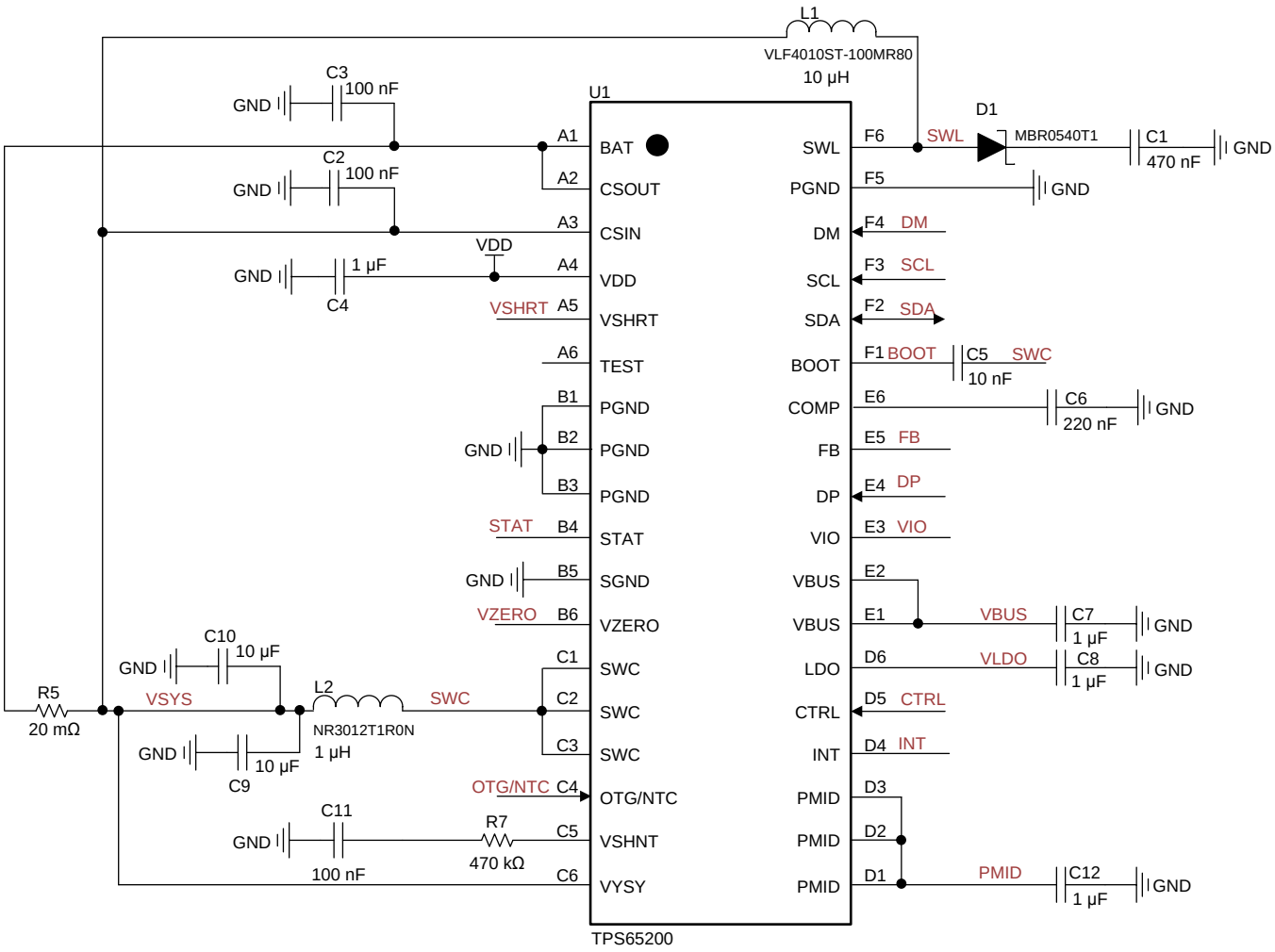


Figure 51. Typical Application Schematic

8.2.1 Design Requirements

The key elements to identify for the design are the value of R_{SET}, R_{SHRT}, and R_{SNS} as well as the desired LED brightness. All other values should reflect those required in *Pin Configuration and Functions* or in *Functional Block Diagram*.

Typical Application (continued)

8.2.2 Detailed Design Procedure

To determine the value for R_{SET}, simply take the desired I_{LED} and divide it by the FB voltage. The FB voltage is 200 mV by default, but can be changed by the VFB[4:0] bits.

To determine the value for R_{SHRT}, the desired pre-charge to fast-charge voltage threshold must be known. From there, divide the voltage by two to account for an internal divider and then by the reference current for V_{SHRT} of 10 uA to determine the resistance value.

To determine the value for R_{SNS}, determine the desired output voltage for the current being monitored. Divide this voltage by the gain, 25 V/V, and the output current to determine the sense resistor value.

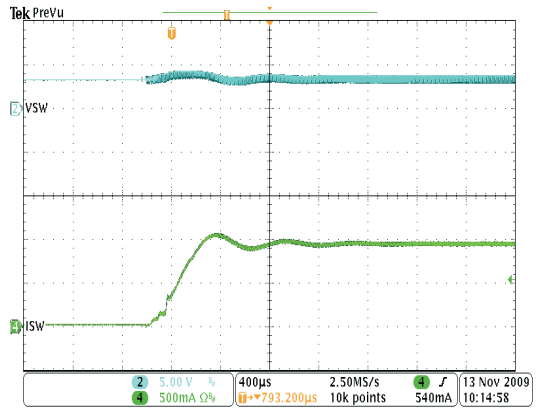
Finally, the LED brightness is a function of either changing the feedback voltage through I^2C or applying a PWM signal to the CTRL pin.[Current Figure 43 WLED Dimming Linearity] gives some estimate as to the VFB level as a function of the duty cycle of the input PWM. This should be fine-tuned for the particular LEDs being used.

Table 2. Recommended External Components(1)

PART NO.	VALUE	SIZE	MANUFACTURER
CHARGER INDUCTOR			
NR3012T1R0N	1 µH	3 × 3 × 1.2	Taiyo Yuden
CPL2512T1R0M	1 µH	2.5 × 1.5 × 1.2	TDK
MDT2520CN	1 µH		TOKO
WLED BOOST INDUCTOR			
ELL-VGG100M	10 µH	3 × 3 × 1.5	Panasonic
VLF4010ST-100MR80	10 µH	4.3 × 4 × 1	TDK
1098AS-100M	10 µH	3 × 3.2 × 1.2	TOKO
WLED BOOST SCHOTTKY DIODE			
MBR0540		SOD-123	ON-SEMI
ZHCS400		SOD-323	ZETEX

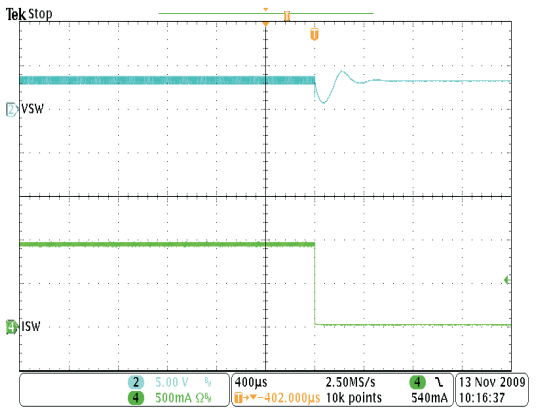
(1) Over operating free-air temperature range (unless otherwise noted).

8.2.3 Application Curves



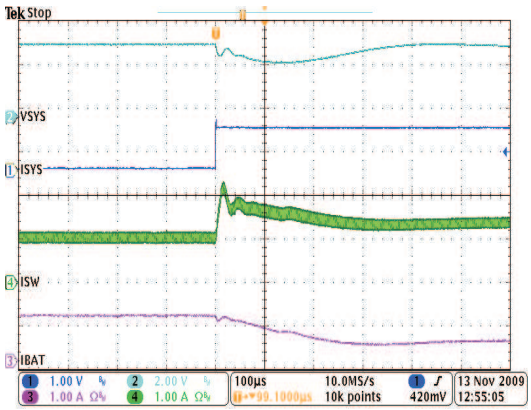
V_{BUS} = 5.5 V V_{BAT} = 3.3 V I_{IN_limit} = 975 mA
I_{CHARGE} = 950 mA

Figure 52. I^2C Controlled Start-Up



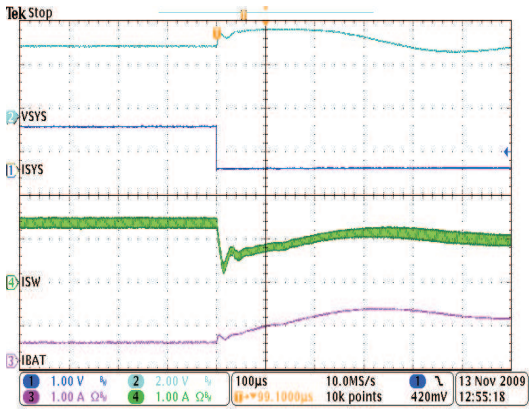
V_{BUS} = 5.5 V V_{BAT} = 3.3 V I_{IN} - limit = 975 mA
I_{CHARGE} = 950 mA

Figure 53. I^2C Controlled Start-Up



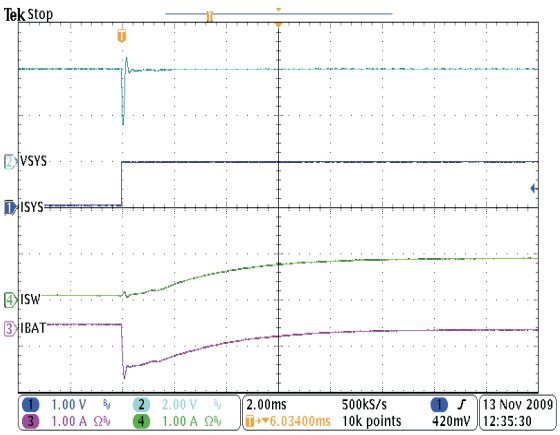
0-A - 1-A Transient on V_{SYS} V_{BUS} = 5.5 V V_{BAT} = 3.2 V
V_{OREG} = 4 V I_{CHARGE} = 950 mA I_{IN_limit} = 975 mA

Figure 54. Transient Response



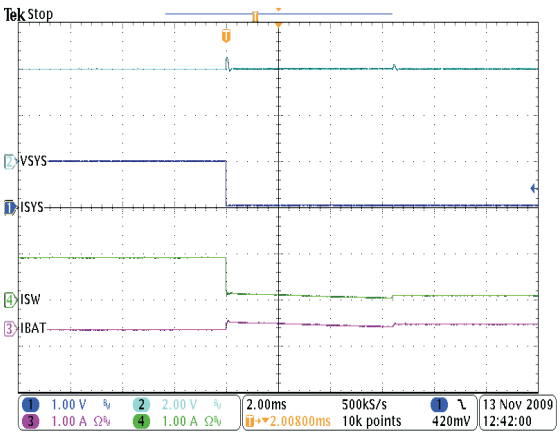
0-A - 1-A Transient on V_{SYS} V_{BUS} = 5.5 V V_{BAT} = 3.2 V
V_{OREG} = 4 V I_{CHARGE} = 950 mA I_{IN_limit} = 975 mA

Figure 55. Transient Response



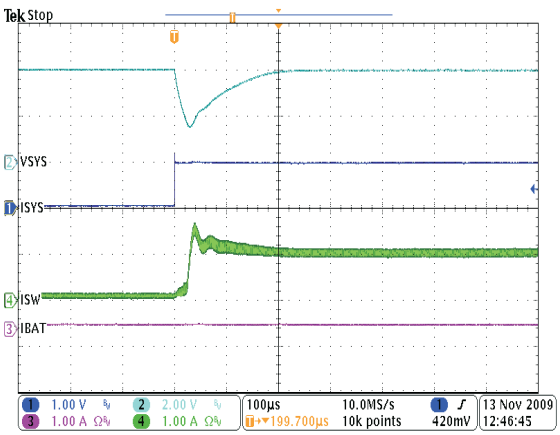
0-A - 1-A Transient on V_{SYS} V_{BUS} = 5.5 V V_{BAT} = 4 V
V_{OREG} = 4 V I_{CHARGE} = 950 mA I_{IN_limit} = 975 mA

Figure 56. Transient Response



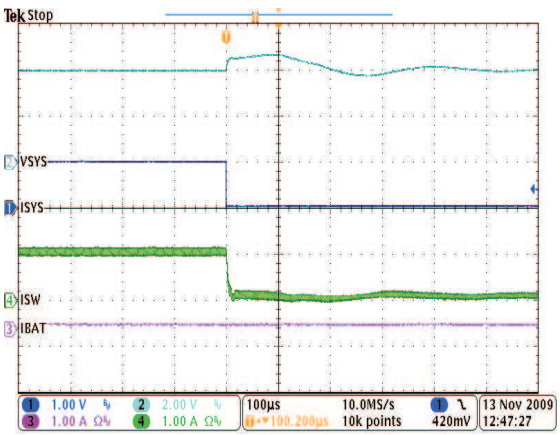
0-A - 1-A Transient on V_{SYS} V_{BUS} = 5.5 V V_{BAT} = 4 V
V_{OREG} = 4 V I_{CHARGE} = 950 mA I_{IN_limit} = 975 mA

Figure 57. Transient Response



0-A - 1-A Transient on V_{SYS} V_{BUS} = 5.5 V No Battery
V_{OREG} = 4 V I_{CHARGE} = 950 mA I_{IN_limit} = 975 mA

Figure 58. Transient Response



0-A - 1-A Transient on V_{SYS} V_{BUS} = 5.5 V No Battery
V_{OREG} = 4 V I_{CHARGE} = 950 mA I_{IN_limit} = 975 mA

Figure 59. Transient Response

9 Power Supply Recommendations

This device should be connected to a single cell Li+ battery or to a 5-V VBUS supply. The current required from VBUS will depend on the desired limit, maximum of 1.55 A.

10 Layout

10.1 Layout Guidelines

As for all switching power supplies, the layout is an important step in the design, especially at high peak currents and switching frequencies. If the layout is not carefully done, the DCDC converters might show noise problems and duty cycle jitter. The input capacitors on VBUS and PMID pins should be placed as close as possible to the input pins for good input voltage filtering. The inductors should be placed as close as possible to the switch pins to minimize the noise coupling into other circuits. The output capacitors must be placed directly from the inductor (charger buck) or Schottky diode (WLED boost) to GND to minimize the ripple current in these traces. All ground pins must be connected directly to the ground plane as should all passive components with ground connections. Figure 60 and Figure 61 show one example for placement and routing of the critical components on a four-layer PCB. In this example all components are placed on the top layer and all routing is done on the top layer or bottom layer. Layer 2 is a solid ground plane and layer 3 is not used for layout. All IC pin connections are notes as [pin number]. For example, the VSYS pin is referenced as [C6].

- Place C9 and C10 (VSYS) as close to L2 as possible, with short connections to ground.
- Place C4 close to the IC. Trace current is low (<1 mA).
- Place C8 as close to the IC as possible. Maximum trace current is 60 mA.
- Keep C6 - [E6] trace shielded from SWL node to avoid noise coupling.
- Place C2 and C3 as close to the IC as possible.Connections for C2 - [A3] and C3 - [A2] must not be in any current path; and, must be kept as short as possible. Traces must connect directly to sense resistor R5.
- Place L1 as close to the IC as possible. Keep traces between L1, D1 and [F6] short and wide.Maximum trace current is 700 mA.
- Pins [A1] and [A2] must not be shorted at the IC. Route them separately to R5.
- Place C12 (PMID) as close to the IC as possible.
- Place input capacitor C7 (VBUS) as close to the IC as possible.
- Place C1 close to D1 and keep the trace short and wide.
- Keep [C1], [C2], [C3] (SWC) to L2 connection shortand wide. Adding vias is OK. Maximum trace current is 2 A.
- Keep VSYS to L1 connection short and wide. Maximum trace current is 700 mA.

10.2 Layout Example

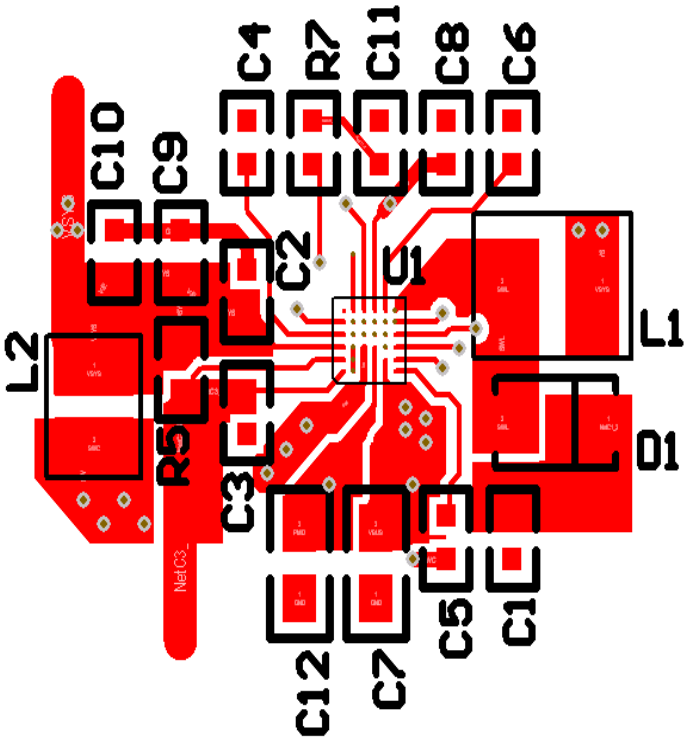


Figure 60. Layout Example – Top PCB Layer

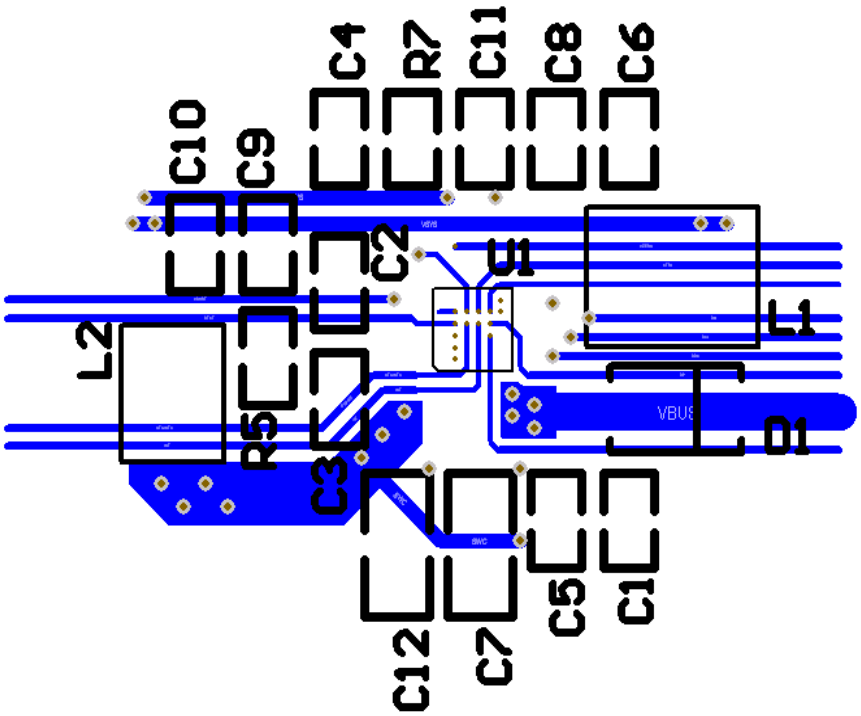


Figure 61. Layout Example – Bottom PCB Layer

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

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All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS65200YFFR	ACTIVE	DSBGA	YFF	36	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	TPS65200	Samples
TPS65200YFFT	OBSOLETE	DSBGA	YFF	36		TBD	Call TI	Call TI	-40 to 85	TPS65200	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

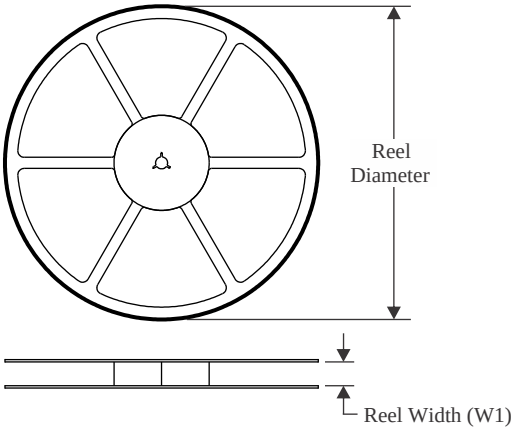
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

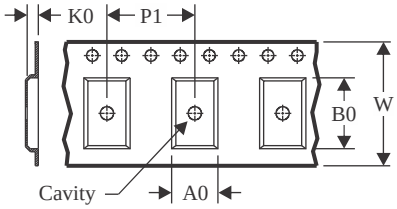
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

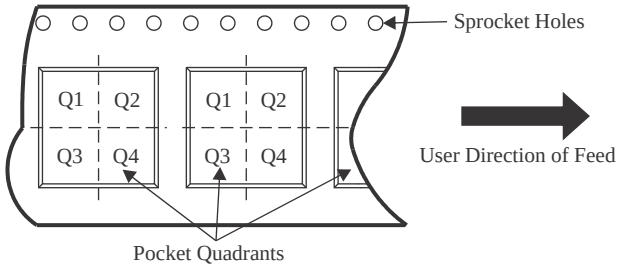


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

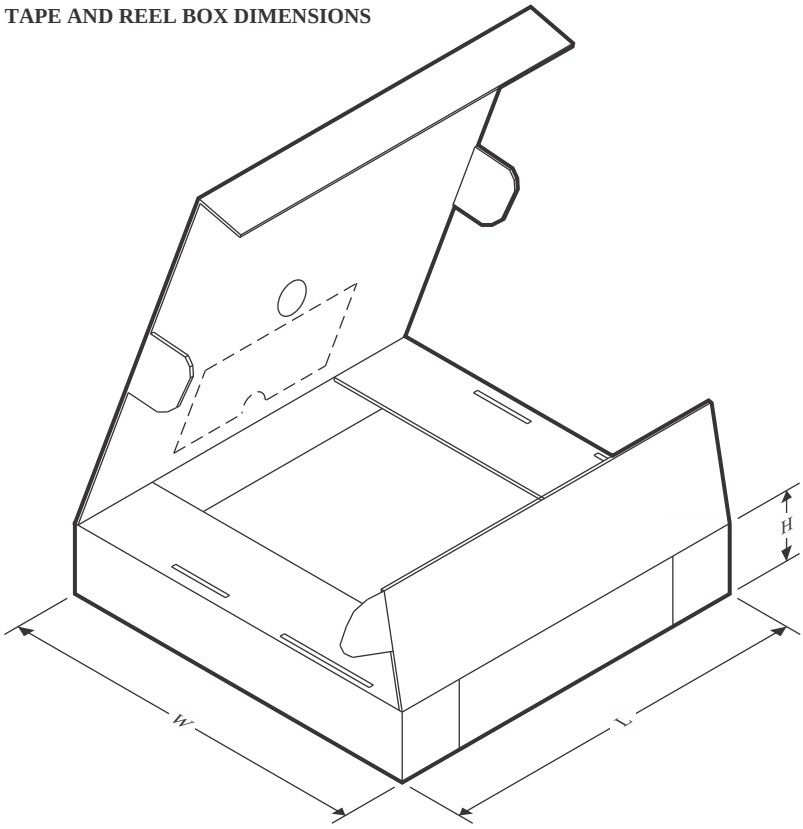
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65200YFFR	DSBGA	YFF	36	3000	180.0	8.4	2.76	3.02	0.83	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

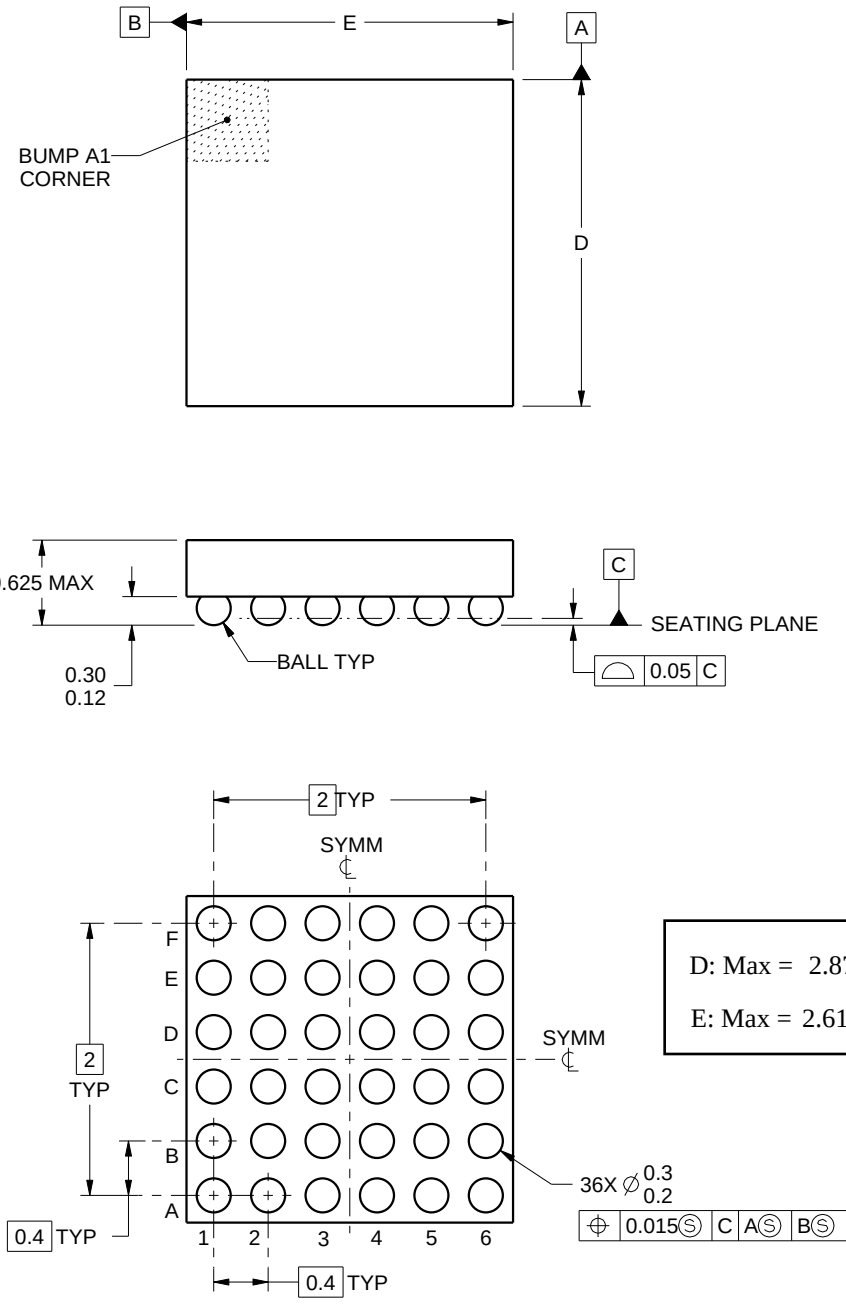
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65200YFFR	DSBGA	YFF	36	3000	182.0	182.0	20.0

PACKAGE OUTLINE

YFF0036

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



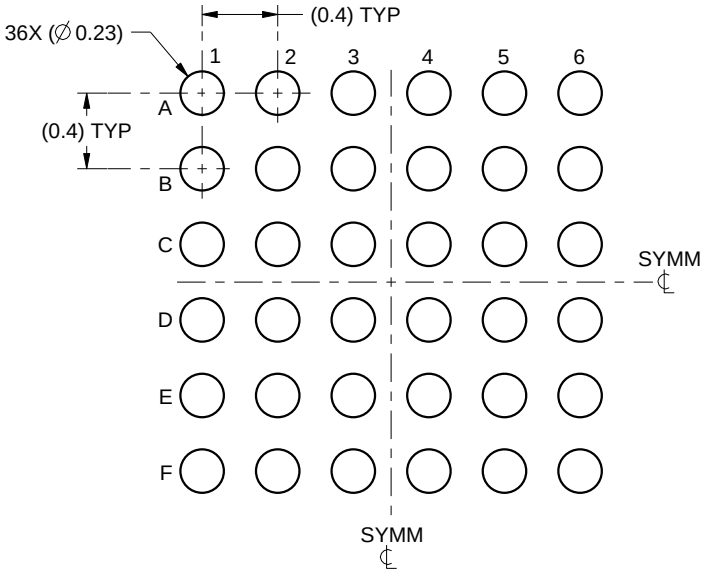
D: Max = 2.87 mm, Min = 2.81 mm

E: Max = 2.612 mm, Min =2.552 mm

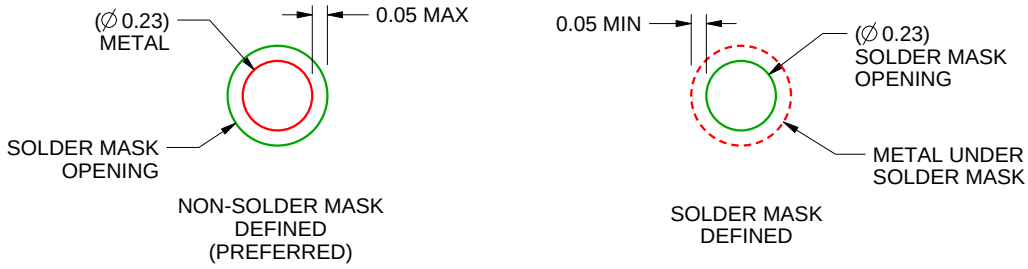
4222008/A 03/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:25X



SOLDER MASK DETAILS
NOT TO SCALE

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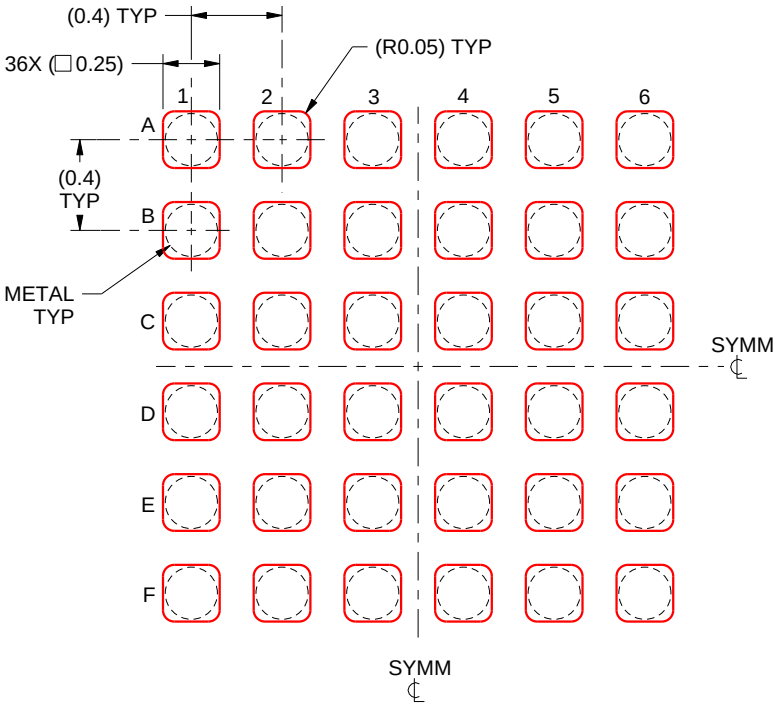
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.
For more information, see Texas Instruments literature number SNVA009 (www.ti.com/lit/snva009).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

4222008/A 03/2015

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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