高级电源管理单元

查询样品: TPS658629-Q1

1 介绍

1.1 主要特性

- 符合汽车应用要求
- 具有下列结果的 **AEC-Q100** 测试指南：
  - 器件温度 **3** 级：**-40°C** 至 **85°C** 的环境运行温度范围
  - 器件人体模型 **(HBM)** 静电放电 **(ESD)** 分类等级 **H1C**
  - 器件充电器件模型 **(CDM) ESD** 分类等级 **C2**
- 集成电源
  - **3** 个可编程降压转换器
    - 受软件控制的使能/强制脉宽调制 **(PWM)** 模式
    - 自动节能模式
    - 最大 **1.5A** 输出（**SM0** 和 **SM2**）
    - 最大 **1.3A** 输出 **(SM1)**
  - **11** 个可编程的通用低压降稳压器 **(LDO)**
    - 其中 **7** 个的输出电压介于 **1.25V** 至 **3.3V** 之间
    - 其中 **2** 个的输出电压介于 **0.725V** 至 **1.5V** 或者 **1.25V** 至 **2.586V** 之间（厂家可配置）
    - **1** 个“常开”，输出电压介于 **1.25V** 至 **3.3V** 之间
    - **1** 个的输出电压介于 **1.7V** 至 **2.475V** 之间
- 显示支持功能
  - **4** 个带有可设定频率和占空比的 **PWM** 输出
  - 双 **RGB** 发光二级管 **(LED)** 驱动器
  - 恒定电流白光发光二级管 **(WLED)** 驱动器
    - **25mA** 时为 **26.5V**（最大值）
    - 过压保护
    - 可编程电流电平和亮度控制
- 主机接口
  - 带有可屏蔽中断的中断控制器
  - 外部模数转换器 **(ADC)** 触发和降压转换器模式控制
- 系统管理
  - 双输入电源路径
    - **USB** 电流感测
    - 最大 **18V** 过压保护
  - 所有电源输出上的电源良好监控
  - 软件复位功能
  - 硬件打开/关闭和重新引导控制
  - **AUTOBOOT**（重新引导）支持
  - **11** 个通道模数转换器 **(ADC)**，每一个都有 **3** 个运行模式
    - 单一转换
    - 峰值检测
    - 取平均值

1.2 应用范围

- 便携式导航设备
- 便携式媒体播放器

1.3 说明

TPS658629-Q1 在一个小型封装内为手持器件、集成型多稳压电源、系统管理和显示功能提供了一个易于使用、完全集成的解决方案。 I^2C 接口实现了对于宽范围子系统参数的控制。 内部寄存器存有状态信息的完整集合，从而实现了对故障状态的简便诊断和主机控制处理。

如需完整数据表，请发电子邮件到msapmu_contact@list.ti.com索取。

1.4 订购信息(1)

T_A	部件号(2) (3)	封装(4)	封装标识符	订购(2)	封装标识
-40°C 至 85°C	TPS658629	169 引脚细间距球状引脚栅格阵列 (nFBGA)	ZWS	TPS658629IZWSRQ1	TPS658629I

(1) 要获得最新的封装和订购信息，请参见本文档末尾的封装选项附录，或者访问德州仪器 (TI) 的网站 www.ti.com。
(2) TPS658629 只提供卷带封装。 数量为每卷 1000 个器件。
(3) 具有唯一部件号的器件有针对电源缺省、排序和其它功能的唯一出厂配置。 针对每个部件的配置信息请查阅此配置。
(4) 这个产品与 RoHS 标准兼容，其中包括铅浓度不超过产品总重量的 0.1%，并且适合应用于特定的无铅焊接工艺中。 此外，这个产品使用不包含卤素的封装材料，包括溴 (Br) 或者锑 (Sb) 高于产品总重量的 0.1%。

2 ELECTRICAL SPECIFICATIONS

2.1 ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

	VALUE / UNITS
AC and USB with respect to AGND1	–0.3 V to 18 V
ANLG1, ANLG2, ANLG3 with respect to AGND2	–0.3 V to 6.5 V
V(SYS) with respect to AGND1	–0.3 V to 6.5 V
VIN_LDO01, VIN_LDO23, VIN_LDO4, VIN_LDO678, VIN_LDO9 with respect to AGND1	–0.3 V to 6.5 V
ADC_REF with respect to AGND2	–0.3 V to 3.6 V
RTC_OUT with respect to V(SYS)	–5.5 V to 3.6 V
RTC_OUT with respect to AGND1	–0.3 V to 3.6 V
LDO0, LDO1, LDO2, LDO3, LDO4, LDO5, LDO6, LDO7, LDO8, LDO9, V2V2 and TS with respect to AGND1	–0.3 V to 3.6 V
V32K with respect to AGND1	–0.3 V to 3.6 V
TS with respect to V2V2	–2.3 V to 0.3 V
SM0, L0, VIN_SM0 with respect to PGND0	–0.3 V to 6.5 V
SM1, L1, VIN_SM1 with respect to PGND1	–0.3 V to 6.5 V
SM2, L2, VIN_SM2 with respect to PGND2	–0.3 V to 6.5 V
SM3 , L3 with respect to PGND3	–0.3 V to 29 V
SM3SW with respect to PGND3	–0.3 V to 29 V
FB3 with respect to PGND3	–0.3 V to 0.5 V
V(BAT) with respect to AGND1, Battery power only	–0.3 V to 5.5 V
All other pins (except AGNDn and PGNDn) with respect to AGND1	–0.3 V to 6.5 V
AGND2, AGND3, , DGND1, DGND2DT, PGND0, PGND1, PGND2, PGND3 with respect to AGND1	–0.3 V to +0.3 V
Input Current, AC pin	Defined by ILIM
Input Current, USB pin	Defined by ILIM
Output continuous current, SYS, VIN_CHG pins	2500 mA
Output continuous current, BAT pin	–3000 mA
Continuous Current at L0, PGND0, L1, PGND1	1500 mA
Continuous Current at L3, PGND3	1000 mA
Continuous Current at L2, PGND2	2000 mA
Operating free-air temperature, T_A	–40°C to 85°C
Maximum junction temperature, T_J	125°C
Storage temperature, T_{STG}	–65°C to 150°C
ESD (Human Body Model) rating , all pins	2000 V
ESD (Charged-Device Model) rating, all pins	250 V
ESD (Machine Model) rating, all pins	150V

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

2.2 THERMAL INFORMATION

THERMAL METRIC		ZWS	UNITS
		169 PINS	
θ_{JA}	Junction-to-ambient thermal resistance(1)	33.1	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance(2)	8.8	
θ_{JB}	Junction-to-board thermal resistance(3)	18	
ψ_{JT}	Junction-to-top characterization parameter(4)	0.2	
ψ_{JB}	Junction-to-board characterization parameter(5)	17	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance(6)	n/a	

(1) 在 JESD51-2a 描述的环境中，按照 JESD51-7 的规定，在一个 JEDEC 标准高 K 电路板上进行仿真，从而获得自然对流条件下的结至环境热阻抗。
(2) 通过在封装顶部模拟一个冷板测试来获得结至芯片外壳（顶部）的热阻。 不存在特定的 JEDEC 标准测试，但可在 ANSI SEMI 标准 G30-88 中找到内容接近的说明。
(3) 按照 JESD51-8 中的说明，通过在配有用于控制 PCB 温度的环形冷板夹具的环境中进行仿真，以获得结至电路板的热阻。
(4) 结至顶部的特征参数，(ψ_{JT})，估算真实系统中器件的结温，并使用 JESD51-2a（第 6 章和第 7 章）中描述的程序从仿真数据中提取出该参数以便获得 θ_{JA}。
(5) 结至电路板的特征参数，(ψ_{JB})，估算真实系统中器件的结温，并使用 JESD51-2a（第 6 章和第7 章）中描述的程序从仿真数据中提取出该参数以便获得 θ_{JA}。
(6) 通过在外露（电源）焊盘上进行冷板测试仿真来获得结至芯片外壳（底部）热阻。 不存在特定的 JEDEC 标准测试，但可在 ANSI SEMI 标准 G30-88 中找到了内容接近的说明。

2.3 DISSIPATION RATINGS

PACKAGE	Psi_Jb	$T_A \le 25°C$ POWER RATING	$T_A = 55°C$ POWER RATING	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
ZWS(1)	20°C/W	5000 mW	3500 mW	2750 mW	2000 mW

(1) This data is based on using the JEDEC High-K board and the exposed die pad is connected to a Cu pad on the board. This is connected to the ground plane by a via matrix.

2.4 RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
AC and USB with respect to AGND1	4	16.5(1)	V
V(SYS) with respect to AGND1	2.9	5.5	V
V(BAT) with respect to AGND1, battery power only	2.9	3.25	V
V(BAT) with respect to AGND1, battery connected, AC or USB power selected, Selected power source >2.9 V	2.15	4.6	V
ANLG1,ANLG2, ANLG3 with respect to AGND2	0	2.6	V
VIN_LDO01, VIN_LDO23, VIN_LDO678, VIN_LDO4, VIN_LDO9 with respect to AGND1	Greater of : 1.7 V OR Minimum input voltage required for LDO/Converter operation outside dropout region	5.5	V
VIN_SM0 with respect to PGND0	Greater of : 2.3 V OR Minimum input voltage required for LDO/Converter operation outside dropout region. 2.9 V to meet parametric specifications.	5.5	V
VIN_SM1 with respect to PGND1		5.5	V
VIN_SM2 with respect to PGND2		5.5	V
SM3 with respect to PGND3		28	V
GPIOx with respect to AGND1	0	5.5	V
All other pins (except AGNDn and PGNDn) with respect to AGND1	0	5.5	V
Operating free-air temperature, T_A	-40	85	°C
Maximum junction temperature, T_J , functional operation	-40	125	°C
Maximum junction temperature, T_J , electrical characteristics	0	125	°C
External supply ramp rate, AC or USB pins	1 V/mSec	1 V/µSec	

(1) Thermal operating restrictions are reduced or avoided if input voltage does not exceed 5 V.

2.5 ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
QUIESCENT CURRENT – V(BAT) = 4.2V NO EXTERNAL LOADS AT SYS PIN OR SUPPLY OUTPUTS						
$I_{Q(ON)}$	Quiescent current, 6586x in normal or sleep mode. All supplies and peripherals off	Power path active, control logic in low power mode(1)		260	375	µA
$I_{Q(DIGITAL)}$	Quiescent current, control logic	Control logic in high power mode(2)	584	716	870	µA
$I_{Q(SMn)}$	SM0, SM1, SM2 operating quiescent current	SM0, SM1: enabled, PFM mode, from SYS pin		14	25	µA
		SM2: enabled, PFM mode, from SYS pin when Vout=3.3V		19	32	µA
		SM0, SM1, SM2: enabled, PWM mode, from VINSMn pin		6		mA
		disabled via I^2C		1		µA
$I_{Q(LDOx)}$	LDO quiescent current, All but one LDOx disabled	$I_{(LDOx)}$ = no external load		24	29	µA
		$I_{(LDOx)}$ = –1 mA		24	150	µA
		$I_{(LDOx)}$ = –50 mA		160		µA
		LDO disabled, T_J = 85°C		1	3	µA
$I_{Q(SM3)}$	SM3 operating quiescent current(3)	SM3 enabled, not switching		15	30	µA
		Enabled, switching			200	µA
		Disabled via I^2C		1		µA
$I_{Q(ADC)}$	ADC operating quiescent current	Conversion active		1		mA
		Not converting, waiting for trigger		170		µA
		ADC disabled via I^2C		1		µA
$I_{Q(RTC)}$	RTC_OUT pin quiescent current	RTC_OUT LDO enabled		27	45	µA
		RTC_OUT disabled via I^2C, T_J = 85°C . Externally applied(4) $V_{(RTC\_OUT)}$ = 2 V supplies real time clock counters and xtal oscillator			15	µA
$I_{Q(V32K)}$	V32K supply bias current , 32k buffer enabled	32k buffer enabled, 100 pF external load			24	µA
		Disabled via I^2C			8	µA
I^2C INTERFACE TIMING – SDA, PSDA, PSCLK, SCLK(3)						
t_R	SCLK/SDATA rise time	Pull-up resistors connected to 2.2V			300	ns
t_F	SCLK/SDATA fall time				300	ns
$t_{W(H)}$	SCLK pulse width high		600			ns
$t_{W(L)}$	SCLK Pulse Width Low		1.3			µs
$t_{SU(STA)}$	Setup time for START condition		600			ns
$t_{H(STA)}$	START condition hold time after which first clock pulse is generated		600			ns
$t_{SU(DAT)}$	Data setup time		100			ns
$t_{H(DAT)}$	Data hold time		0			ns
$t_{SU(STOP)}$	Setup time for STOP condition		600			ns
$t_{(BUF)}$	Bus free time between START and STOP condition		1.3			µs
F_{SCL}	Clock Frequency				400	kHz
I^2C BUFFERS – SDA, PSDA, PSCLK, SCLK						
$V_{IL(I2C)}$	Low level input voltage				0.4	V
$V_{IH(I2C)}$	High level input voltage		1.15			V
$V_{OL(I2C)}$	Low level output voltage	SDA, PSDA configured as output, I_{OL}=3mA			0.4	V
$I_{O(I2C)}$	Maximum load current(3)	SDA, PSDA configured as output			8	mA
$I_{LKG(I2C)}$	Input current	V(pin) = 5V or 0V			1	µA
C_{I2C}	Input pin capacitance	SDAT, SCLK, PSDAT, PSCLK pins		10		pF
C_{I2CBUS}	I^2C bus capacitance	SDAT, SCLK, PSDAT, PSCLK		400		pF

(1) Control logic in low power mode when all functions are off and no I^2C communication is on going
(2) Control logic in high power mode when one of the following events happen: 6586x in power-up/rtc/rtc_on/supplyseq states, any converter in PWM mode, SM3 enabled, PWM driver enabled, ADC conversion on-going, I^2C communication on-going, voltage transition for DVM supplies on-going, AC or USB supply detected.
(3) Not production tested.
(4) External voltage supplied by supercap or coin cell connected to RTC_OUT pin, see application diagram for details.

ELECTRICAL CHARACTERISTICS *(continued)*

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUT BUFFERS: RESUME, SM0EN, SM1EN, $\overline{\text{HOTRST}}$, LDO4EN, SYNCEN						
$V_{IL(DIG)}$	Low level input voltage				0.4	V
$V_{IH(DIG)}$	High level input voltage		1.15			V
$I_{LKG(DIG)}$	Input current	V(pin) = 5V			0.1	µA
R_{DIG}	Internal resistor	RESUME pin , pull-down to AGND	55	100	150	kΩ
		$\overline{\text{HOTRST}}$ pin, pull-up to V2V2	55	100	175	
PUSH-PULL OUTPUT BUFFERS, USER SELECTABLE OUTPUT VOLTAGE – $\overline{\text{NORTC}}$, $\overline{\text{NOPOWER}}$						
V_{BFRPWR}	Buffer positive supply	Internally connected to V32K pin	1.1 to 3.3			V
$V_{OL(OBFR)}$	Low level output voltage	I_{OL} = 3 mA, V32K = 1.5 V			0.6	V
		I_{OL} = 10 µA, V32K > 1.1 V			0.1	
$V_{OH(OBFR)}$	High level output voltage, referenced to output buffer supply, $\overline{\text{NORTC}}$	I_{OH} = 1.4 mA, V32K = 1.5 V	V32K-0.6			V
		I_{OH} = -10 µA, V32K = 1.1 V	V32K-0.11			
$V_{OH(OBFR)}$	High level output voltage, referenced to output buffer supply,$\overline{\text{NOPOWER}}$	I_{OH} = 1.4 mA, V32K = 1.5 V	V32K-0.6			V
		I_{OH} = -10 µA, V32K = 1.1 V	V32K-0.11			
$I_{OL(OBFR)}$	Maximum low level sink current load(1)	V(pin) = 2.5 V			5	mA
$I_{OH(OBFR)}$	Maximum high level source current load(1)	V(pin) = 0 V	–5			mA
OPEN DRAIN OUTPUT BUFFERS – $\overline{\text{INT}}$						
$V_{OL(OBFR)}$	Low level output voltage	I_{OL} = 3 mA, V32K = 1.5 V			0.6	V
		I_{OL} = 10 µA, V32K > 1.1 V			0.1	
$I_{LKG(OBFR)}$	Output leakage current	Output buffer, open-drain mode, V(pin)=5.5V			0.1	µA
PUSH-PULL OUTPUT BUFFERS – LDO4PG, SM0PG, SM1PG						
$V_{OL(DBFR)}$	Low level output voltage	I_{OL} = 3 mA			0.6	V
		I_{OL} = 10 µA			0.1	
$V_{OH(DBFR)}$	High level output voltage , buffer configured as push-pull via I^2C	I_{OH} = 3 mA	1.5			V
		I_{OH} = –10 µA	1.8			
$I_{OL(DBFR)}$	Maximum low level sink current load(1)	V(pin) = 2.5 V			5	mA
$I_{OH(DBFR)}$	Maximum high level source current load(1)	V(pin) = 0 V	–5			mA
32kHz OUTPUT BUFFER , V(32K)=1.7V (min), UNLESS OTHERWISE STATED						
V_{32B}	Externally applied bias rail for output driver(1)	Buffer supply voltage	1.0		3.6	V
V_{OL}	Output low level	$V_{(32K)}$ = 1.1 V, I_{OL} = 100 µA			0.05	V
		$V_{(32K)}$ = 1.1 V, I_{OL} = 1 mA			0.2	
		$V_{(32K)}$ = 1.5 V, I_{OL} = 5 mA			0.5	
V_{OH}	Normal operation	$V_{(32K)}$ = 1.1 V, I_{OH} = -1 µA	V32K-0.05			V
		$V_{(32K)}$ = 1.5 V, I_{OH} = 5 mA	V32K-0.5			
t_F, t_R	Rise/fall time	32 kHz clock driving 50pF load cap		15		ns
V_{JITTER}	Output jitter	Peak to peak		15		ns
		RMS		15		
32kHz CLOCK AND 32K SWITCHING TIMING						
t_{XTAL}	XTAL oscillator stabilization time(1)	Frequency within 2% of typical value, frequency defined by XTAL characteristics			320	ms
F_{32K}	Internal 32 kHz clock	Frequency	28	32	36	kHz
INTERNAL REFERENCES AND POR						
UVLO	Internal UVLO detection threshold	$V_{(2V2)}$ decreasing	-3%	1.85	3%	V
V_{UVLO_HYS}	UVLO detection hysteresis	$V_{(2V2)}$ increasing from decreasing trigger point		120		mV
$V_{O(2V2)}$	Output Voltage	Always on,	2.1	2.2	2.3	V
I_{SH2V2}	Short Circuit current limit	$V_{(2V2)}$ = 0V	18			mA

(1) Not production tested.

2.6 ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RTC_OUT LDO						
$V_{O(RTC\_OUT)}$	RTC_OUT output voltage	Output Voltage, Selectable via I^2C(1)	$V_{O(RTC_OUT)}$TYP=1.25, 1.50, 1.8, 2.5, 2.7,2.85,3.1,**3.3**			V
		Dropout voltage, I(RTC_OUT) = –15 mA V(SYS) = 2.8 V			600	mV
		Total accuracy, V(AC):2V to 4.7V, –15mA load, V(BAT1)=V(BAT2)=V(USB)=0V	–5%		5%	
		Load regulation, V(AC)=3.5V, load: 1mA → –15mA		1%		
		Line regulation, 5mA load,V(AC): 3.5V→18V, V(BAT1) =V(BAT2) =V(USB) =0V		1%		
I_{SHRTC}	Short Circuit current limit		20			mA
$V_{(RTCGOOD)}$	RTC_OUT power good fault detection threshold	Falling RTC_OUT pin voltage, set via I^2C	2.3	2.35	2.45	V
			1.8	1.9	2	
$V_{HYS(RTC)}$	Power good fault detection hysteresis	Rising RTC_OUT pin voltage (Referenced to $V_{(RTCGOOD)}$ threshold)	50	75	145	mV
V_{UVLO_RTC}	Internal RTC UVLO detection threshold	VRTC Decreasing	–10%	1.5	10%	V
$V_{UVLO\_RTC\_HYS}$	UVLO detection hysteresis	VRTC Increasing	100	150	200	mV
BOOT-UP TIMING						
t_{POR}	Power-on-reset delay(2)	Fixed time, measured from 2V2 > UVLO	7.2	8	8.8	ms
t_{BOOT}	Boot-up time	Fixed time		75		ms
		Accuracy, referenced to $t_{BOOT(tTYP)}$	–10%		10%	
$t_{HOTPLUG}$	Hot plug deglitch time	Fixed time	675	750	825	ms
t_{WAKEUP}	Wakeup pulse width	Fixed time	225	250	275	µs
t_{CHECK}	RTC check wait time	Fixed time	2.7	3	3.3	ms
t_{MAX}	RTC_ON watchdog timer	Fixed time		$4\times T_{NORTC}$		ms
t_{NORTC}	$\overline{\text{NORTC}}$ pin pulse width value	Fixed time		10		ms
		Accuracy, relative to $t_{NORTC\ (TYP)}$(3)	–10%		10%	
$K_{NOPOWER}$	$\overline{\text{NOPOWER}}$ pin pulse width const.	$t_{NOPOWER} = K_{NOPOWER} \times C_{NOPOWER}$		0.25		ms/nF
		Pulse width accuracy, $C_{NOPOWER}$ < 400nF	–25%		25%	
t_{WAIT}	Reboot and sleep request timeout	Fixed time	18	20	22	ms
t_{WAIT1}			4.5	5	5.5	ms
$t_{SYNCEND}$	Synchronization complete delay	Measured from all supplies synchronized	4.5	5	5.5	ms
$T_{SYNCDLY}$	Supply sync delay time	Regulator specific. See Table 3-10	$T_{SYNCDLY(TYP)}$ = 1.25, 2.5, 3.75, 15, 20, 32, 40, 64			ms
		Accuracy, relative to $T_{SYNCDLY(TYP)}$(3)	-10		+10	
POWER GOOD AND THERMAL FAULT DETECTION						
$t_{DGL(PGFLT)}$	Power good deglitch time	Applies to all non-masked power good signals, output voltage falling edge.	4	5	6	ms
t_{SHUT}	Thermal shutdown	Increasing junction temperature		150		°C
$t_{HYS(SHUT)}$	Thermal shutdown hysteresis	Decreasing junction temperature		30		°C
$t_{DGL(TSHUT)}$	Thermal shutdown detection delay	Rising temperature	15	20	25	µs

(1) Setting the RTC_OUT output voltage below the RTC_OUT power good threshold will result in a $\overline{\text{NORTC}}$ pulse being always generated during reboot cycles or when exiting sleep.
Setting the RTC_OUT output voltage below VUVLO_RTC disables the use of the internal real time clock counter and xtal oscillator.
(2) Not production tested.
(3) Not production tested.

ELECTRICAL CHARACTERISTICS *(continued)*

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RESUME CONTROL TIMING						
$t_{RESUME(H)}$	RESUME pulse width high(1)		550			ms
$t_{RESUME(L)}$	RESUME pulse width low(1)		220			ms
SEQUENCER REBOOT CONTROL						
V_{HOTRST}	Reboot control threshold	Reboot started when normal state is set and $V(\overline{HOT\_RST}) < V_{REBOOT}$ for $t > T_{DT(HRST)}$			0.4	V
$T_{HRST(H)}$	$\overline{HOT\_RST}$ max pulse width				60	ms
$T_{DT(HRST)}$	$\overline{HOT\_RST}$ min detection pulse width	$\overline{HOT\_RST}$ deglitch	4		16	µs
EXTERNAL SUPPLY DETECTION AND STATUS						
V_{LOWSYS}	Minimum system voltage detection threshold	System voltage V(SYS) decreasing.		2.8		V
		Total accuracy, referenced to $V_{(LOWSYS)}$TYP	-2		2	%
$V_{HYS(LOWSYS)}$	Minimum system voltage detection hysteresis	V(SYS) increasing from decreasing trigger point		200		mV
$T_{DGL(LOWSYS)}$	Minimum system voltage detection deglitch time	V(SYS) decreasing		5		ms
$V_{IN(DT)}$	Input voltage detection threshold. Input voltage increasing, referenced to battery voltage	AC detected when $V_{(AC)} - V_{(BAT)} > V_{IN(DT)}$ AND $V_{(AC)} > V_{ACMIN}$ USB detected when $V_{(USB)} - V_{(BAT)} > V_{IN(DT)}$	180			mV
$V_{IN(NDT)}$	Input voltage removal threshold. Input voltage decreasing, referenced to battery voltage	AC not detected: when $V_{(AC)} - V_{(BAT)} < V_{IN(NDT)}$ USB not detected when V(USB) – $V_{(BAT)} < V_{IN(NDT)}$			65	mV
V_{ACMIN}	AC detection threshold, relative to GND	AC voltage increasing , AC not detected when $V_{(AC)} < V_{ACMIN}$	3.5		3.8	V
		AC voltage decreasing , AC not detected when $V_{(AC)} < V_{ACMIN}$	3.3		3.6	
		Hysteresis		185		mV
t_{ACSYS}	AC threshold to SYS delay	AC=3.8V to SYS=HIGH		40	50	ms
$t_{DGLAC(DT)}$	AC Power detected deglitch	AC voltage increasing		22.5		ms
$t_{DGLUSB(DT)}$	USB Power detected deglitch	USB voltage increasing		5.5		ms
$V_{IN(OVP)}$	Input over voltage detection		5.8	6.0	6.3	V
$t_{DLY(INOVP)}$	Input over voltage detection delay	Rising AC or USB voltage		100		µs
ANALOG COMPARATOR						
V_{COMP}	Voltage threshold	Enabled at sleep mode	1.21	1.245	1.28	V
$I_{LK(COMP)}$	COMP pin leakage current(1)				0.1	µA
t_P	Propagation time	V(COMP):0→1.5V→0, measured from input to $\overline{NOPOWER}$:HI→LO		50		µs

(1) Not production tested.

2.7 ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
POWER PATH CURRENT LIMIT AND PROTECTION FUNCTIONS							
I_{USB100}	Selected input current limit, applies to USB input only	Selected Input switch not in dropout. I^2C settings: USBMODE=HI, USBLIMIT=LO	–40°C < T_A < 85°C	85		100	mA
			–25°C < T_A < 85°C	92		100	
I_{USB500}		Selected Input switch not in dropout. I^2C settings: USBMODE=HI, USBLIMIT=HI		380		500	mA
I_{INLIM}	Selected input current limit, applies to AC input	Input current limit range, AC input			2.75		A
		Total accuracy, relative to $I_{INLIM(TYP)}$		–20%		20%	
	Selected input current limit, applies to USB input	Input current limit range, USB input configured with USBMODE=LO			2.11		A
		Total accuracy, relative to $I_{INLIM(TYP)}$		–12.5%		12.5%	
t_{OVSH}	Input current limit transient time	Load at SYS pin: 80% of current limit value to 120% of regulation value (I_{INLIM}, I_{USB100} or I_{USB500}). Time measured from load transient to input current within regulation limits.			20		µs
$I_{OVSHPKUSB}$	Input current limit overshoot	Load at SYS pin: 80% of current limit value to 120% of regulation value (I_{INLIM}, I_{USB100} or I_{USB500}), t < T_{OVSH}			20%		
$V_{SH(SYS)}$	SYS power path Short Circuit detection threshold	All power path switches set to OFF if V(SYS) < $V_{SH(SYS)}$		1.6	1.8	2.0	V
$R_{FLT(USB)}$	SYS short circuit recovery pull-up resistor	V(SYS) < $V_{SH(SYS)}$, internal resistor connected from USB to SYS			550		Ω
$R_{FLT(AC)}$	SYS short circuit recovery pull-up resistor	V(SYS) < $V_{SH(SYS)}$, internal resistor connected from AC to SYS			550		Ω
I_{BATSYS}	Battery Switch over-current detection			3.0		6.0	A
$t_{DGL(BATSYS)}$	Battery Switch over-current detection delay	Short circuit detection blanked for TDGL(BATSYS), measured from batt switch: OFF->ON or initial sys power path enable		100	110	120	ms
		Battery switch already turned on or sys power path enabled			1		ms
$I_{FLT(SYS)}$	Battery Switch over-current recovery pull-up current source	V(BAT) –V(SYS) > $V_{OC(SYS)}$, internal current source connected from BAT to SYS			30		mA
$V_{SUP(SYS)}$	Supplement detection threshold	Battery switch ON at V(BAT)-V(SYS) > $_{VSUP(SYS)}$		40			mV
$V_{SUPNDT(SYS)}$	Supplement mode not detected threshold	Battery switch OFF at V(BAT)-V(SYS)<$V_{SUPNDT(SYS)}$		7			mV
POWER PATH INTEGRATED MOSFETS CHARACTERISTICS							
V_{ACDO}	AC switch dropout voltage	V_{ACDO} = V(AC)-V(SYS); V(AC)=4V AC input current limit set to 2.0A (typ) $I_{O(SYS)}$ = 1.0A				190	mV
V_{USBDO}	USB switch dropout voltage	V_{USBDO} = V(USB)-V(SYS); V(USB)=4.6V	I(SYS)+I(BAT)= 0.425A			240	mV
			I(SYS)+I(BAT)= 85mA			240	
$V_{BATDODCH}$	Battery Switch dropout voltage, discharge	$V_{BATDODCH}$ = V(BAT)-V(SYS), V(BAT)=3V, I(BAT)= 1A			40	155	mV
POWER PATH TIMING CHARACTERISTICS							
t_{SW}	Switching from AC to BAT	No USB, AC power removed			150		µs
t_{SW}	Switching from USB to BAT	No AC, USB power removed			150		µs
POWER PATH DISCHARGE SWITCHES							
$I_{DCH(AC)}$	AC pin discharge current	Always ON, V(AC) > 1 V			100		µA
$I_{DCH(USB)}$	USB pin discharge current	Always ON, V(USB) > 1 V			100		µA
SM0, SM1, SM2 DC/DC CONVERTERS							
V_{SMUV}	Low input voltage detection threshold, input voltage decreasing	Converter turned OFF at V(VIN_SMn) < V_{SMUV}				2.0	V
		Hysteresis , rising input voltage			100		mV
$R_{DS(ON)}$	High side MOSFET on-resistance	V_{IN_SMx} = 3.6V, 100% duty cycle			200		mΩ
	Low side MOSFET on-resistance	V_{IN_SMx} = 3.6V, 0% duty cycle			200		mΩ
I_{LK_HS}	High side leakage current	T_J = 85°C				1	µA
I_{LK_LS}	Low side leakage current					1	µA
I_{LIM}	High side and low side current limit	2.9V ≤ V_{IN_SMx} ≤ 5.5V	SM0	1550	2400		mA
			SM1	1550	2400		
			SM2	1300	1900		
f_{SW}	Oscillator frequency	PWM mode		2.025	2.25	2.475	MHz
V_{SMPG}	Power good threshold	Power fault detection, Voltage decreasing, referenced to programmed output voltage		–13.0%	–10%	–7.0%	
		Hysteresis, voltage increasing, referenced to V_{SMPG}			5%		

ELECTRICAL CHARACTERISTICS *(continued)*

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{O(SMx)}$	Adjustable output voltage range, Selectable via I²C	VIN_SMx = 2.9V to 5.5V	SM0, low range, 25mV steps	$V_{O(SMx)TYP}$ = 0.725 to 1.50			V
			SM1, low range, 25mV steps	$V_{O(SMx)TYP}$ = 0.725 to 1.50			
			SM2, low range, 25mV steps	$V_{O(SMx)TYP}$ = 3 to 4.55			
	Output Voltage Accuracy, relative to VO(SMx)TYP	V_{IN_SMx} = 2.9V to 5.5V, PFM mode		–1%	1%	3%	
		V_{IN_SMx} = 2.9V to 5.5V, PWM mode, 0mA < I_{OUT}< 1A		–2%		2%	
	DC output voltage load regulation	PWM mode, VIN_SMn>2.7V, Load<1A			0.25		%/A
	DC output voltage line regulation	V_{IN_SMx} = VOUT + 0.5V (min. 2.5V), PWM mode VIN_SMn>2.7V, Load<1A			0.1		%/V
$K_{RAMP(SMx)}$	Voltage change ramp constant	Value set via I²C, available options:		SM0, SM1: typical values:Instantaneous, 0.11, 0.22, 0.44, 0.88, 1.76, 3.52, 7.04			mV/µs
t_{Start}	Start-up time	Time to start switching, measured from end of I²C command enabling converter			210		µs
t_{Ramp}	V_{OUT} Ramp UP time	Time to ramp from 5% to 95% of V_{OUT}			250		µs
R_{DCH}	Discharge switch resistance	SMx disabled			250		Ω
$I_{PFM(ENTER)}$	Load current to enter PFM mode	V_{IN_SMx} = 2.9V to 5.5V, duty cycle > 85%			VIN_SMx/34Ω		A
C_{LC}	External LC capacitor(1)			4.7		22	µF
L_{LC}	External LC inductor(1)			1.5		4.7	µH
C_{SMINP}	External Input capacitor(2)			10		47	µF
LDO'S : LDO0, LDO1, LDO2, LDO3, LDO4, LDO5, LDO6, LDO7, LDO8, LDO9							
V_{INMIN}	Input voltage range(2)	Electrical characteristics over the output current range IO(LDOx)		2.3		5.5	V
		Electrical characteristics specified , max load current = 75mA		1.7		5.5	
I_O	Output current(2)					300	mA
		Output Voltage, Selectable via I²C. LDO6, LDO0, LDO3, LDO5, LDO7,LDO8,LDO9		Available output voltages: $V_{(LDO6)TYP}$ = 1.20 (LDO0 only), 1.25, 1.5, 1.8, 2.5, 2.7, 2.85, 3.1,3.3			V
$V_{(LDOx)}$	LDOx Output Voltage, Selectable via I²C	LDO1 Output Voltage, Selectable via I²C	Low range, 25mV steps	$V_{(LDO1)TYP}$ = 0.725 to 1.5			V
		LDO4 Output Voltage, Selectable via	High range, 25mV steps	$V_{(LDO4)TYP}$ = 1.7 to 2.475			
		LDO2 Output Voltage, Selectable via I²C	Low range, 25mV steps	$V_{(LDO2)TYP}$= 0.725 to 1.5			
		Dropout, $V_{(IN)}$ = $V_{(LDOx)TYP}$ - 0.1V , $V_{(IN)}$ = 2.3V, 250mA load. 1 LDO active at a time per input pin group(3)				415	mV
		Total accuracy, $V_{(VIN\_LDOx)}$ = $V_{(LDOx)TYP}$ + 0.5V, 10mA → 250 mA		See (4)		3.5%	
		Line Regulation, 100mA load, $V_{(VIN\_LDOx)}$: $V_{(LDOx)\ TYP}$ + 0.5V→ 4.7V		–0.5%		0.5%	
		Load regulation, load change from 10mA → 250 mA $V_{(VIN\_LDOx)}$ > $V_{(LDOx)\ TYP}$ + 0.5V		See (5)			%
PSRR	PSRR at 20 kHz	250mA load, 1V input to output ,C_L = 4.7 µF			40		dB
		100mA load, 0.5V input to output, C_L = 1 µF			40		
I_{SC}	Short circuit current limit	Output grounded	LDOnILIM=HI	310		700	mA
R_{DCH}	Discharge resistor	LDOx disabled			415		Ω
K_{RAMP}	Voltage change ramp constant	LDO2, LDO4 only. Fixed value, hardwired at top level			7.04		mV/µs
C_{COMP}	External output capacitor value(2)	Stable operation	load <100 mA	1			µF
			load>100 mA	0.01µF/mA, min cap value = 1µF			
P_{GOOD}	Power good threshold	LDO output voltage increasing			95%		
	Hysteresis	Decreasing voltage from increasing trigger			5%		

(1) Not production tested
(2) Not production tested
(3) Dropout not measured for devices with V(IN)<2.3V because minimum VIN is 2.3V
(4) MIN = –3.2 – (0.105 × I_{LOAD} / $V_{(LDOX)TYP)}$, I_{LOAD} = load current in amps
(5) MIN = –2.5 – (0.105 × I_{LOAD}, I_{LOAD} = load current in amps

2.8 ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SM3 BOOST CONVERTER – CONTROL CIRCUIT AND POWER STAGE						
$V_{VIN(SM3)}$	Input Voltage range(1)	$V_{(VIN)}$	2.5		6.5	V
$V_{O(SM3)}$	Output voltage range(1)	$V_{(SM3)}$	$V_{VIN(SM3)}$		26.5	V
$V_{(OVP3)}$	Output over-voltage trip	OVP detected at V(SM3) > $V_{(OVP3)}$ rising	26.5	28	29	V
$V_{HYS(OVP3)}$	Output over-voltage hysteresis	OVP not detected at $V_{(SM3)} < V_{(OVP3)} - V_{HYS(OVP3)}$		1.8		V
$V_{(SM3REF)}$	FB3 voltage sense threshold(1)	$V_{(FB3)}$ below regulation point at $V_{(FB3)} < V_{(SM3REF)}$	238	248	258	mV
			1.237	1.25	1.263	V
$I_{O(SM3)}$	LED current(1)	$I_{O(SM3)} = \frac{V_{(SM3REF)}}{R_{FB3}}$ Current range,	0		25	mA
$D_{(SM3SW)}$	LED switch duty cycle, selectable via I^2C	Duty cycle range	$D_{(SM3SW)}$ = 0% to 99.96%, set via I^2C, 2048 steps 0.05% minimum step			%
$F_{(REP\_SM3)}$	LED switch duty cycle pattern repetition rate, selectable via I^2C	2048 pulses within repetition rate time, repetition rate set via I^2C	$F_{(REP\_SM3)TYP}$ = 550Hz, 366Hz, 275Hz or 220Hz			Hz
		Total accuracy, relative to $F_{(REP\_SM3)TYP}$	–12%		12%	
$R_{DSON(SM3SW)}$	LED switch FET on-resistance(1)	$V_{(VIN)}$ = 3.8 V; $I_{(SM3SW)}$ = 20 mA		1	2	Ω
$I_{LKG(SM3SW)}$	LED switch FET leakage			1	4	µA
$R_{DSON(L3)}$	Power stage FET on-resistance	$V_{(VIN)}$ = 3.8 V; $I_{(L3)}$ = 200 mA		300	600	mΩ
$I_{LKG(L3)}$	Power stage FET leakage			1	4	µA
$I_{MAX(L3)}$	Power stage FET current limit	2.5V< V(IN) <5.5V	400	500	600	mA
$T_{SM3PWR(ON)}$	Maximum on time detection threshold		5	6	15	µs
$T_{SM3PWR(OFF)}$	Minimum off time detection threshold		310	400	500	ns
HIGH/LOW BRIGHTNESS CONTROL						
$R_{DSON(ISM3G)}$	Output buffer switch on resistance	V(VIN)=2.5V, I(ISM3G)=25mA		1	2	Ω
$I_{LKG(ISM3G)}$	Leakage current	Hi-Z mode, V(ISM3G)=5V			1	µA
SWITCHING FREQUENCY						
F_{SM3}	Maximum switching frequency(1)	At nominal load			1	MHz
GPIO1-4 – DIGITAL OUTPUT BUFFER						
$V_{OL(GPIO)}$	Low level output voltage	I_{OL} = 3 mA			0.6	V
		I_{OL} = 10 µA			0.1	
$V_{OH(GPIO)}$	High level output voltage GPIO	I_{OH} = –3 mA	1.5			V
		I_{OH} = –10 µA	1.8			
$I_{OL(GPIO)}$	Maximum low level sink current	$V_{(GPIOn)}$ = 2.5V			5	mA
$I_{OH(GPIO)}$	Maximum high level source current(1)	$V_{(GPIOn)}$ = 0V	–5			mA
GPIO1-4 – DIGITAL INPUT BUFFER						
$V_{IL(GPIO)}$	Low level input voltage				0.4	V
$V_{IH(GPIO)}$	High level input voltage		1.15			V
$I_{LKG(GPIO)}$	Input current	$V_{(GPIOn)}$ = 5V or 0V, GPIO configured, GPIO input current sink OFF			0.5	µA
GPIO1-4 - INPUT CURRENT SINK						
$I_{SNK(GPIO)}$	Input current sink	ON if TPS658629-Q1 is not in sleep mode and GPIO is not configured.		2.5	3.5	µA

(1) Not production tested

2.9 ELECTRICAL CHARACTERISTICS (Continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
PWM DRIVER, PWM OPEN DRAIN OUTPUT							
I_{PWM}	Maximum operating current(1)	PWM driver ON				200	mA
V_{OL}	Low level output voltage	IOL = 100mA , V(AVDD6)=3V				0.2	V
$F_{(PWM)}$	PWM driver frequency	Frequency range		Set via I^2C $F_{(PWM)TYP}$ = 0.75, 1.5, 2.3, 3.0, 4.5, 6.7,11.7,23.4			kHz
$D_{(PWM)}$	PWM driver duty cycle	Duty cycle range		$D_{(PWM)}$ = 6.25% to 100%, set via I^2C, 15 steps, 6.25% minimum step			%
$I_{LKG(PWM)}$	Output off leakage current	Output voltage = 5V, driver set to OFF			1	5	µA
LED_PWM DRIVER, LED_PWM OPEN DRAIN OUTPUT							
I_{LEDPWM}	Maximum operating current(1)	PWM driver ON				200	mA
$D_{(LEDPWM)}$	LED_PWM driver duty cycle	Duty cycle range, 128Hz repetition rate		$D_{(LEDPWM)}$ = 0% to 99.6%, set via I^2C, 255 steps, 0.4% minimum step			%
		Total accuracy, relative to selected value		–10%		10%	
$V_{OL(LEDPWM)}$	Low level output voltage	I_{OL} = 50mA , $V_{(AVDD6)}$ = 3 V				0.2	V
$I_{LKG(LEDPWM)}$	Output off leakage current	Output voltage = 5 V, driver set to OFF			1	5	µA
RGB DRIVER, RED/GREEN/BLUE OPEN DRAIN OUTPUTS							
$T_{FLASH(RGB)}$	RGB1, RGB2 flashing period	Flashing period range		$T_{FLASH(RGB)}$ = 1 to 8 sec, set via I^2C, 0.5sec minimum step, 15 steps			s
$T_{FLASH(ON)}$	RGB1, RGB2 flash on time	Flash on time range, value selectable by I^2C		Set via I^2C, $T_{FLASH(ON)}$ = 0.1, 0.15, 0.2, 0.25, 0.3, 0.4, 0.5, 0.6			s
$D_{(RGB)}$	RGB1, RGB2 duty cycle	Duty cycle range, value selectable via I^2C		$D_{(RGB)}$ = 0% to 96.875%, set via I^2C, 3.125% minimum step			%
$I_{SINK(RGB1)}$	RGB1 output sink current	$V_{(RED1)}$ = $V_{(GREEN1)}$ = $V_{(BLUE1)}$ = 0.25V	Sink current, set via I^2C	$I_{SINK(RGB1)TYP}$ = 0, 3.7, 7.4, 11.1			mA
			Absolute accuracy relative to selected value	–35%		35%	
			Relative accuracy between sink current outputs	–10%		10%	
$I_{SINK(RGB2)}$	RGB2 output sink current	$V_{(RED2)}$ = $V_{(GREEN2)}$ = $V_{(BLUE2)}$ = 0.25V	Sink current, set via I^2C	$I_{SINK(RGB\ at\ TYP}$ = 0, 3.7, 7.4, 11.1, 14.9, 18.6, 23.2, 27.3,			mA
			Absolute accuracy relative to selected value	–35%		35%	
			Relative accuracy between sink current outputs	–10%		10%	
$V_{LO(RGB1)}$	Low level output voltage	Output low voltage, RED1/GREEN1/BLUE1 pins, one current source ON (4 or 8 or 12mA source) ON at a time, $V_{(AVDD6)}$=3V				0.25	V
$V_{LO(RGB2)}$	Low level output voltage	Output low voltage, 16mA load, RED2/GREEN2/BLUE2 pins, one current source ON (4 or 8 or 16mA source) ON at a time, $V_{(AVDD6)}$ =3V				0.25	V
$I_{LKG(RGB)}$	Output off leakage current	Output voltage = 5V, driver set to OFF			1	2	µA
DIG_PWM , DIG_PWM1 DRIVER , PUSH PULL OUTPUT							
$F_{(PWM)}$	PWM driver frequency	Frequency range		110	125	140	Hz
		Total accuracy, relative to selected value		–10%		10%	
$V_{HI(DIGPWM)}$	Output level, HI	$V_{(DIG\_PWM)}$ at $I_{(DIG\_PWM)}$ = –5 mA		1.7			V
		$V_{(DIG\_PWM)}$ at $I_{(DIG\_PWM)}$ = –10 µA		2			
$V_{LO(DIGPWM)}$	Output level, LO	$V_{(DIG\_PWM)}$ at $I_{(DIG\_PWM)}$ = 5 mA				0.5	V
		$V_{(DIG\_PWM)}$ at $I_{(DIG\_PWM)}$ = –10 µA				0.1	

(1) Not production tested

2.10 ELECTRICAL CHARACTERISTICS

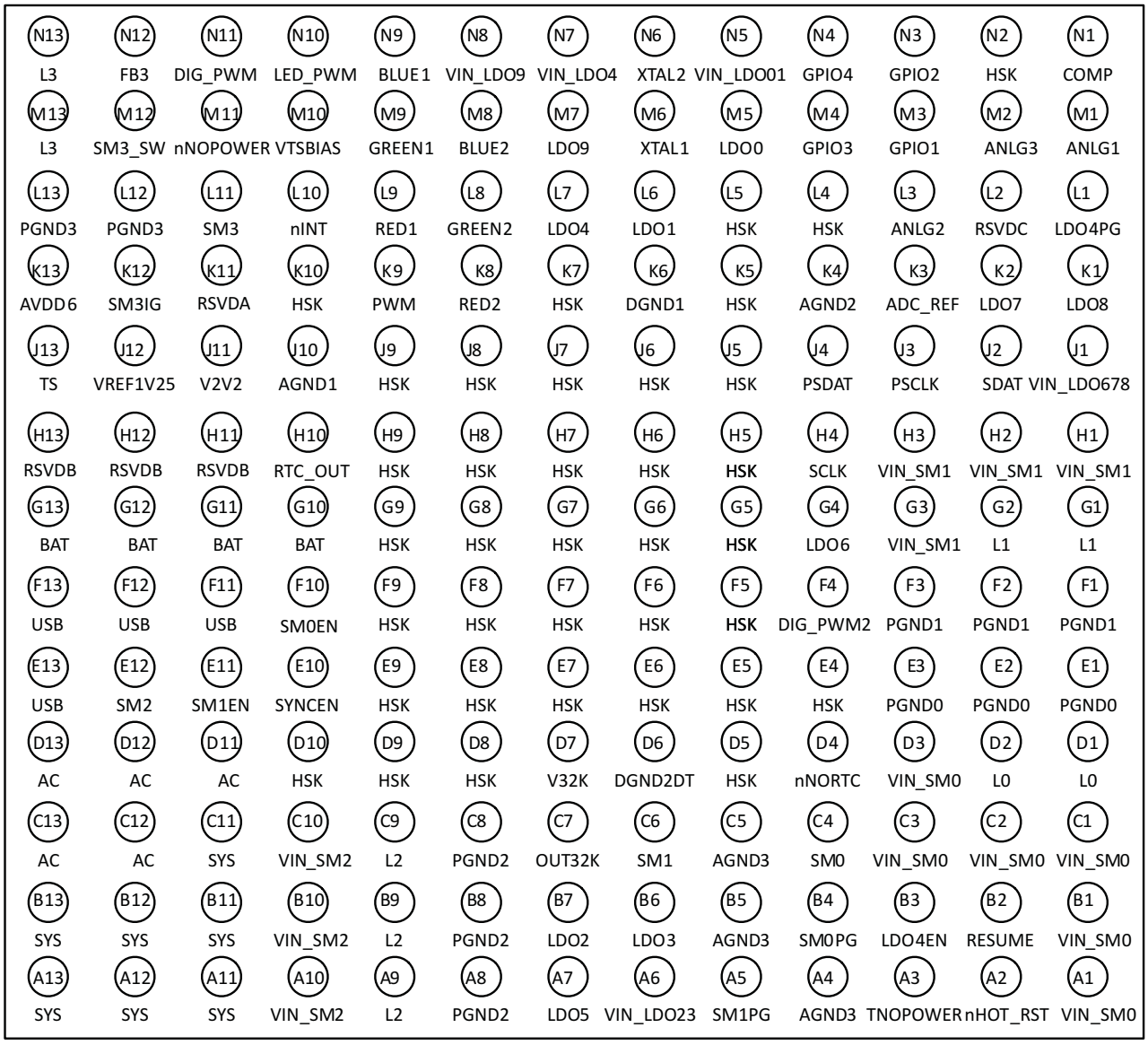
over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ADC REFERENCE							
$V_{REF(ADC)}$	Internal ADC reference voltage	T_A = 25°C		2.595	2.6	2.605	V
		Over full temp range		2.577	2.595	2.607	
$I_{SHRT(ADCREF)}$	Internal reference short circuit limit	V(ADC_REF)=AGND1		3.0	4.5		mA
C_{REFADC}	Maximum capacitance for internal ADC reference supply(1)					6.8	µF
ADC ANALOG INPUTS							
$V_{RNG(CH1\_6)}$	Full scale input range Channels 1–6(1)	Positive inputs, Full scale ~ 2.60 V		0		$V_{REF(ADC)}$	V
$V_{RNG(CH7\_10)}$	Full scale input range Channels 7, 10(1)	Positive inputs, Full scale ~ 4.622 V		0		$V_{REF(ADC)}$ × 1.78	V
$V_{RNG(CH8\_9)}$	Full scale input range Channels 8, 9(1)	Positive inputs , Full scale ~ 5.54 V		0		$V_{REF(ADC)}$ × 2.13	V
$C_{IN(ADC)}$	Input capacitance (all channels)				15		pF
$R_{INADC(CH1\_6)}$	Input resistance (all channels)	AVDD6-V(ANLG) >= 500mV		1			MΩ
$I_{LKGADC(CH1\_6)}$	Leakage current (all channels)	ADC disabled			0.1	1	µA
ADC – DC ACCURACY							
$RES_{(ADC)}$	Resolution	SAR ADC			10		Bits
$MCD_{(ADC)}$	Missing codes				None		
$INL_{(ADC)}$	Integral linearity error				±3		LSB
$DNL_{(ADC)}$	Differential non-linearity error				±1		LSB
$OFF_{ZERO(ADC)}$	Offset error	Deviation from the first code transition (00..00) to (00.001) fro m the ideal AGND + 1LSB			1	5	LSB
$OFF_{CH(ADC)}$	Offset error match between channels(1)				1	5	LSB
$GAIN_{(ADC)}$	Gain error	Deviation in code from the ideal full scale code (11…111) for the full scale voltage			±8		LSB
$GAIN_{CH(ADC)}$	Gain error match	Any two channels			2		LSB
ADC THROUGHPUT SPEED							
ADC_{CLK}	Sampling clock(1)			506	562	619	kHz
ADC_{TCONV}	Sampling and conversion time	Sampling time - 9X ADCCLK			16		µs
		conversion and settling time -11X ADCCLK			20		µs
ANLGx (USER_DEFINED INPUTS) BIAS CURRENTS							
$I_{(ANLGx)}$	ANLG1, 2, or 3 pin internal pull-up current source	ADC channel 1 bias current, set via I^2C register ADC_WAIT bits (ADICH2_1, ADICH2_2)	00 =		0		µA
			01 =		3		
			10 =		10		
			11 =		50		
		Total accuracy		–20%		20%	

(1) Not production tested

2.11 PIN DESCRIPTION, REQUIRED EXTERNAL COMPONENTS

2.11.1 ZWS Package Pinout (Top View)



PIN FUNCTIONS

NAME	PIN	I/O	DESCRIPTION	EXTERNAL REQUIRED COMPONENTS (See Application Diagram)
SYSTEM POWER PATH				
AC	C12,C13, D11,D12, D13	I	Adapter input voltage, connect to AC_DC adapter positive output terminal (DC voltage)	1µF(minimum) capacitor to AGND1 pin to minimize over-voltage transients during AC power hot-plug events.
USB	E13,F11, F12,F13	I	USB input voltage, connect to USB port positive power output	1µF(minimum) capacitor to AGND1 pin, to minimize over-voltage transients during USB power hot-plug events.
BAT	G10,G11, G12,G13	I/O	Battery power	Connect to battery positive terminal. Connect 4.7µF capacitor (minimum) from BAT pin to clean analog ground plane
SYS	A11,A12, A13,B11, B12,B13, C11	O	AC/BAT/USB power path output. Connect to System main power rail (system power bus)	10µF capacitor to AGND1 pin

PIN FUNCTIONS (continued)

NAME	PIN	I/O	DESCRIPTION	EXTERNAL REQUIRED COMPONENTS (See Application Diagram)
REFERENCE SYSTEM				
TNOPOWER	A3	I	NOPOWER pin pulse width	Capacitor to AGND1. Capacitor value sets pulse width
AVDD6	K13	O	Internal supply rail	Connect 4.7µF capacitor to AGND1. Place close to pin.
V2V2	J11	O	Internal 2.2V supply rail	1µF (minimum) decoupling capacitor to AGND1. Place close to pin.
VREF1V25	J12	O	Internal 1.25V reference filter capacitor	100nF (minimum) decoupling cap to AGND1. Do not exceed 1 µF. Place close to pin.
TEMPERATURE SENSOR				
TS	J13	I/O	Temperature sense input, current source output	Connect to battery pack thermistor to sense battery pack temperature
RSVDA	K11	I		
VTSBIAS	M10	O	Thermistor network bias supply, internally connected to 2V2 via integrated switch	Connect to external thermistor pull-up resistor
RSVDB	H11,H12, H13	I/O		
RSVDC	L2	O		
SM3 BOOST CONVERTER				
L3	M13,N13	O	Drain of the integrated boost power stage switch	4.7µH inductor to SYS pin, external Schottky diode to SM3 pin
FB3	N12	I	White LED duty cycle switch output, LED current setting	External resistor from FB3 pin to PGND3 pin sets LED peak current. Connect 100pF (minimum) filter capacitor to PGND3 pin.
SM3_SW	M12	I	Integrated white LED duty cycle switch input	
SM3IG	K12	I/O	General purpose input/output	HI-Z Output, controlled via I^2C. May be used to set SM3 current gain step, implementing a high/low brightness control
SM3	L11	I	White LED driver output over-voltage detection	Connect 1µF capacitor to PGND3 pin. Connect SM3 pin to the positive side of white LED ladder.
PGND3	L12,L13	I	Power ground, SM3 converter	Connect to the power ground plane
DRIVERS				
RED2	K8	O	Programmable LED driver, open drain output, current sink output when active.	Connect to RED input of RGB LED
GREEN2	L8	O		Connect to GREEN input of RGB LED
BLUE2	M8	O		Connect to BLUE input of RGB LED
RED1	L9	O		Connect to RED input of RGB LED
GREEN1	M9	O		Connect to GREEN input of RGB LED
BLUE1	N9	O		Connect to BLUE input of RGB LED
LED_PWM	N10	O	LED_PWM driver output, open drain, programmable duty cycle.	Can be used to drive a keyboard backlight LED or other external functions
PWM	K9	I	PWM driver, open drain output	May be used to control external vibrator motor
DIG_PWM	N11	O	PWM, digital push-pull output	2V2 output voltage level
DIG_PWM2	F4	O	PWM, digital push-pull output	2V2 output voltage level
DC/DC CONVERTERS				
VIN_SM0	A1,B1,C1, C2,C3,D3	I	SM0 synchronous buck converter positive supply input	2 x 10µF capacitor to PGND0 pin
SM0	C4	I	SM0 synchronous buck converter output voltage sense	LC filter: 1.5µH Inductor and 10µF Capacitor. Connect capacitor to PGND0 pin
L0	D1,D2	O	SM0 synchronous buck converter power stage output	1.5µH inductor to SM0 pin
PGND0	E1,E2,E3	I	Power ground, SM0 converter	Connect to the power ground plane
VIN_SM1	G3,H1, H2,H3	I	SM1 synchronous buck converter positive supply input	2 x 10µF capacitor to PGND1 pin
SM1	C6	I	SM1 synchronous buck converter output voltage sense	LC filter: 1.5µH Inductor and 10µF Capacitor. Connect capacitor to PGND1 pin
L1	G1,G2	O	SM1 synchronous buck converter power stage output	1.5µH inductor to SM1 pin
PGND1	F1,F2,F3	I	Power ground, SM1 converter	Connect to the power ground plane
VIN_SM2	A10,B10, C10	I	SM2 synchronous buck converter positive supply input	2 x 10µF capacitor to PGND2 pin
SM2	E12	I	SM2 synchronous buck converter output voltage sense	LC filter: 1.5µH Inductor, 10µF Capacitor. Connect capacitor to PGND2 pin

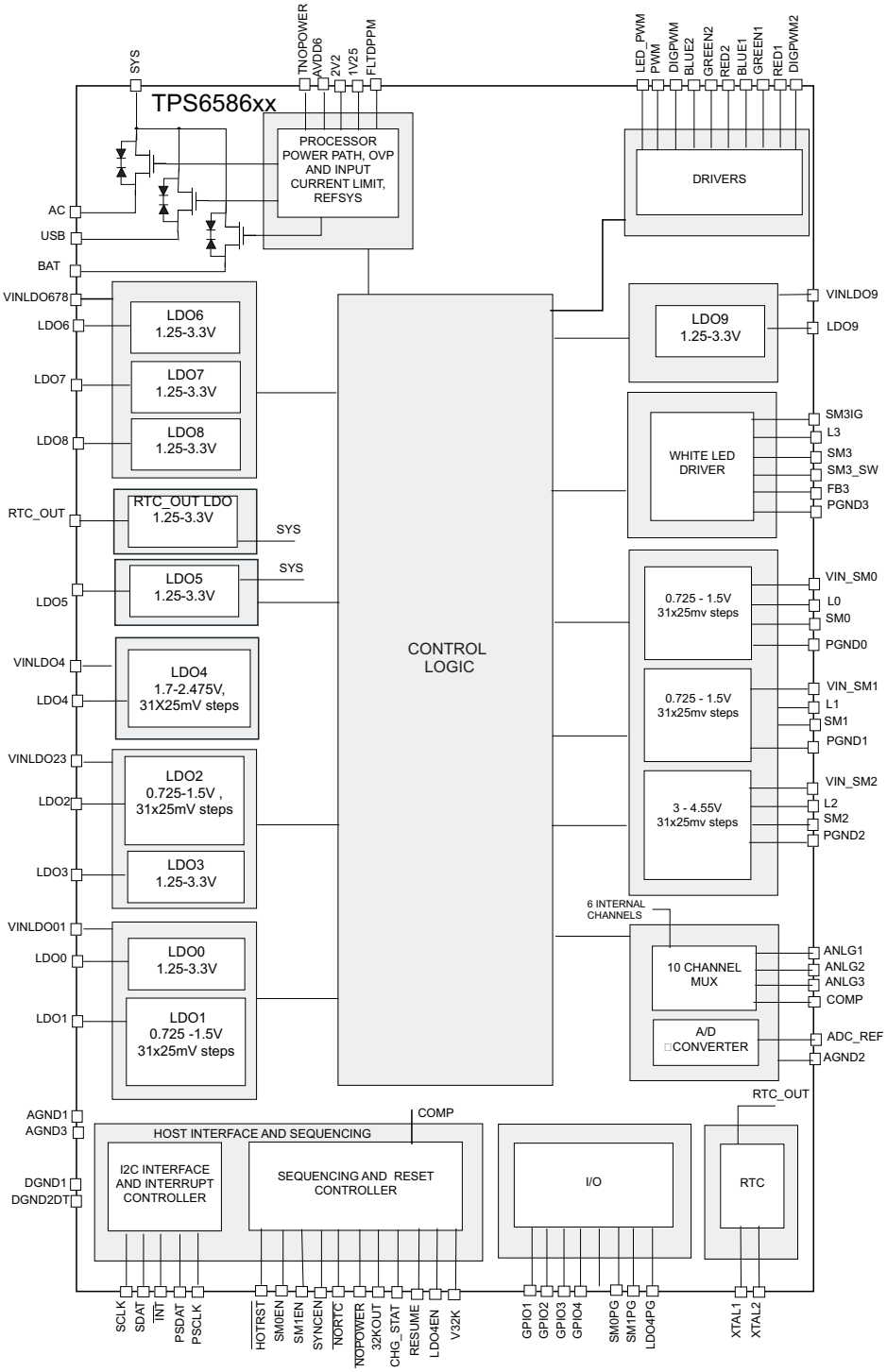
PIN FUNCTIONS (continued)

NAME	PIN	I/O	DESCRIPTION	EXTERNAL REQUIRED COMPONENTS (See Application Diagram)
L2	A9,B9,C9	O	SM2 synchronous buck converter power stage output	1.5µH inductor to SM2 pin
PGND2	A8,B8,C8	I	Power ground pin, SM2 converter	Connect to power ground plane
ADC				
AGND2	K4	I	Analog ground, ADC subsystem	Connect to analog ground plane
ANLG1	M1	I	Analog input1 to ADC, programmable current source output	Can be used to monitor additional system or pack parameters
ANLG2	L3	I	Analog input2 to ADC, programmable current source output	
ANLG3	M2	I	Analog input3 to ADC, programmable current source output	
ADC_REF	K3	I/O	ADC internal reference filter or ADC external reference input	Connect a maximum capacitance of 6.8uF referenced to the AGND2 pin.
EXTERNAL SYSTEM RESET AND CLOCK OUTPUTS, ADJUSTABLE LEVEL				
V32K	D7	I	Power supply for host interface buffers	
$\overline{\text{INT}}$	L10	O	Interruption pin nINT pin is LO when interrupt is requested by TPS658XX.	Open drain output
OUT32K	C7	O	32kHz clock from external XTAL	Push-pull output, V32K level
$\overline{\text{NOPOWER}}$	M11	O	Host reset output, LO level, adjustable width	
$\overline{\text{NORTC}}$	D4	O	RTC_OUT POR pulse, LO level, fixed width	
SEQUENCING CONTROL INPUTS				
$\overline{\text{HOT\_RST}}$	A2	I/O	Reboot cycle request	Hardware reboot cycle control
RESUME	B2	I	Sleep on/off request	Hardware sleep on/off control
LDO4EN	B3	I	LDO4 enable control	
SM0EN ($\overline{\text{CORECTRL}}$)	F10	I	Supply enable control	Active low signal.
SM1EN	E11	I	Supply enable control	
SYNCEN	E10	I	Supply enable control	
I^2C INTERFACE				
PSDAT	J4	I/O	Power I^2C clock line	Connect to external host power I^2C clock. Connect 2K external pull-up resistor. Connect to 2V2 pin if not used
PSCLK	J3	I		
SDAT	J2	I/O	I^2C interface data line	Connect 2K external pull-up resistor.
SCLK	H4	I	I^2C interface clock line	
RTC OSCILLATOR				
XTAL1	M6	I	Xtal oscillator	Connect to external xtal
XTAL2	N6	I		
INPUT / OUTPUT				
GPIO1	M3	I/O	General purpose input/output	Input: SM0, SM1, SM2 power saving mode and output voltage setting control
GPIO2	N3	I/O	General purpose input/output	Input: ADC external trigger or LDO0, LDO1 enable
GPIO3	M4	I/O		Input: LDO2, LDO3 enable
GPIO4	N4	I/O		Input: ADC external trigger or LDO6, LDO7, LDO8 enable
COMP	N1	I	General purpose comparator input, ADC input	
SM0PG	B4	O	SM0 power good status	
SM1PG	A5	O	SM1 power good status	
LDO4PG	L1	O	LDO4 power good status	
LINEAR REGULATORS				
VIN_LDO01	N5	I	Positive supply input for LDO0, LDO1	1µF (minimum) decoupling capacitor to AGND1
LDO0	M5	O	LDO0 output	1µF(minimum) capacitor to AGND1
LDO1	L6	O	LDO1 output	1µF(minimum) capacitor to AGND1
VIN_LDO23	A6	I	Positive supply input for LDO2, LDO3	1µF (minimum) decoupling capacitor to AGND1
LDO2	B7	O	LDO2 output	1µF(minimum) capacitor to AGND1
LDO3	B6	O	LDO3 output	1µF(minimum) capacitor to AGND1

PIN FUNCTIONS (continued)

NAME	PIN	I/O	DESCRIPTION	EXTERNAL REQUIRED COMPONENTS (See Application Diagram)
VIN_LDO4	N7	I	Positive supply input for LDO4	1µF (minimum) decoupling capacitor to AGND1
LDO4	L7	O	LDO4 output	1µF(minimum) capacitor to AGND1
LDO5	A7	O	LDO5output	1µF(minimum) capacitor to AGND1
VIN_LDO678	J1	I	Positive supply input for LDO0, LDO1	1µF (minimum) decoupling capacitor to AGND1
LDO6	G4	O	LDO6 output	1µF(minimum) capacitor to AGND1
LDO7	K2	O	LDO7 output	1µF(minimum) capacitor to AGND1
LDO8	K1	O	LDO8 output	1µF(minimum) capacitor to AGND1
VIN_LDO9	N8	I	Positive supply input for LDO9	1µF (minimum) decoupling capacitor to AGND1
LDO9	M7	O	LDO9 output	1µF(minimum) capacitor to AGND1
RTC_OUT	H10	O	Low leakage LDO output. Can be connected to a super-capacitor or secondary cell, if used as a RTC backup output.	1µF (minimum) capacitor to AGND1 pin or supercap
ANALOG AND DIGITAL GROUND PINS				
DGND1	K6	I	Digital ground pin	Connect to digital ground plane
AGND1	J10	I	Analog ground pin	Connect to analog ground plane
AGND3	A4,B5,C5	I	Analog ground pin	Connect to analog ground plane
DGND2DT	D6	I/O	Digital ground pin	Connect to analog ground plane
HSK	See Package Drawing	N/A	There is an internal electrical connection between all HSK pins of the IC. The HSK pins must be connected to the same potential as the AGND1 pin on the printed circuit board. ***Do not use the HSK pins as the primary ground input for the IC.***	

2.11.2 Block Diagram



2.12 TYPICAL CHARACTERISTICS

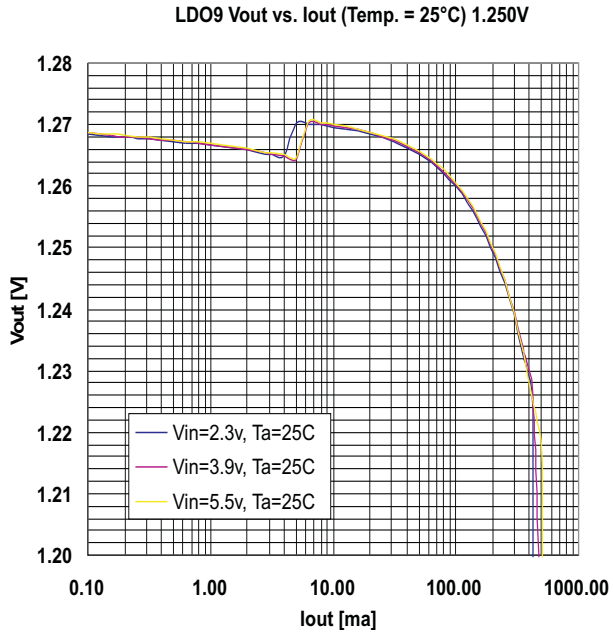


Figure 2-1.

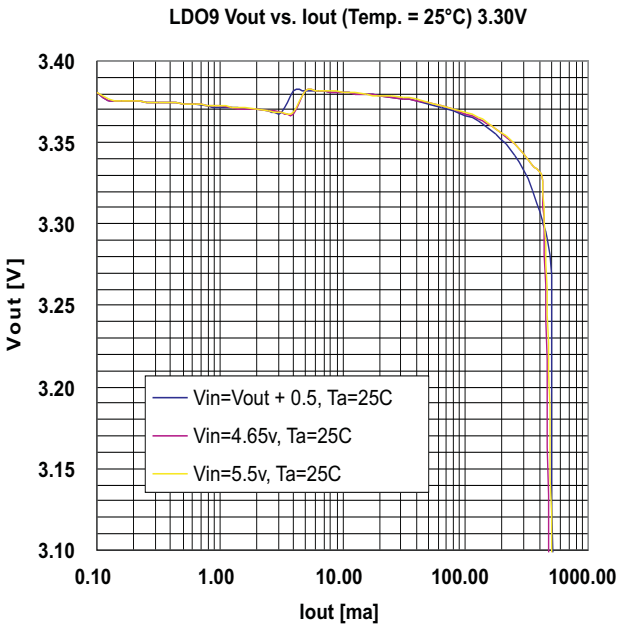


Figure 2-2.

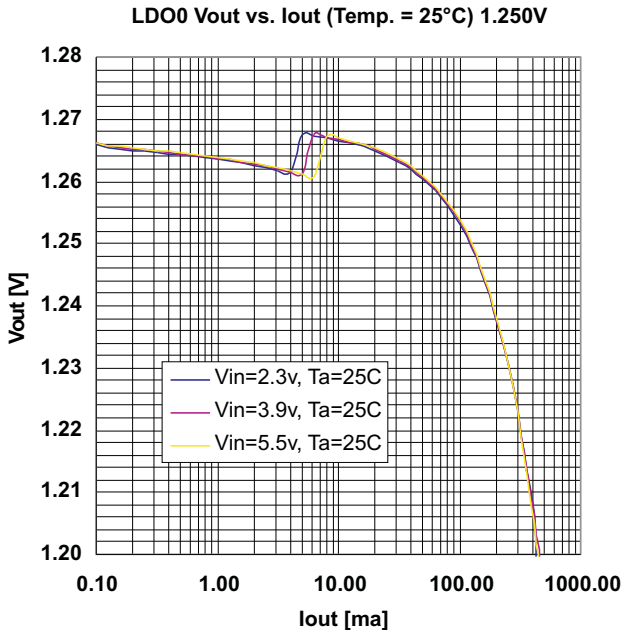


Figure 2-3.

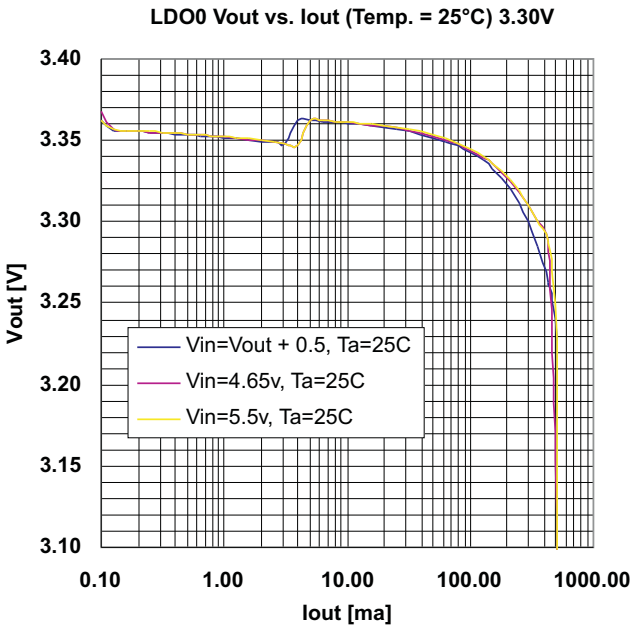


Figure 2-4.

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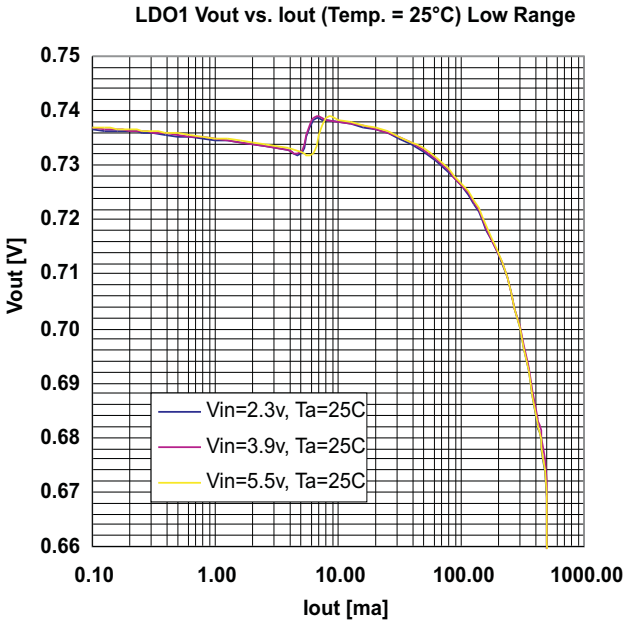


Figure 2-5.

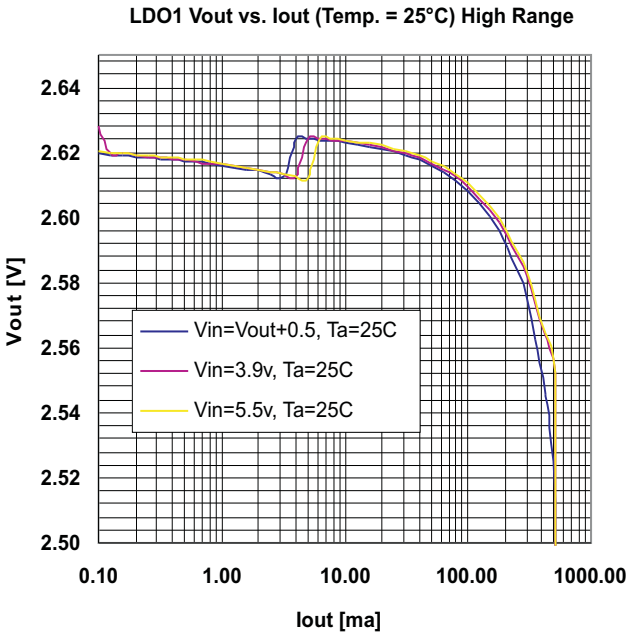
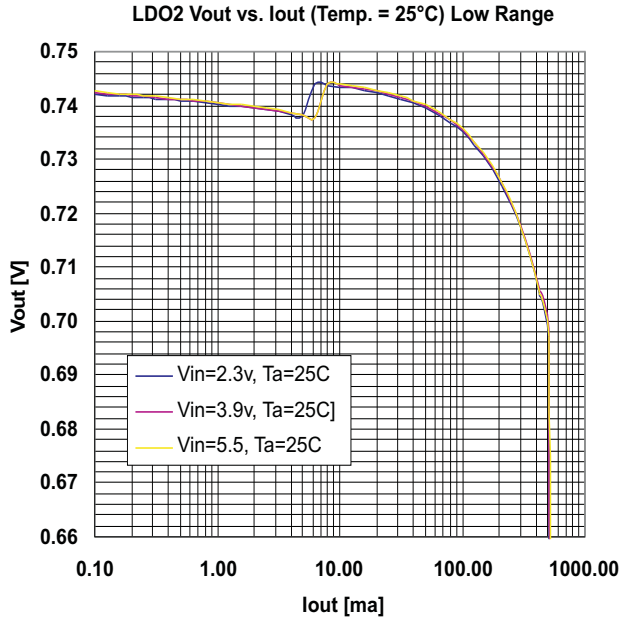


Figure 2-6.



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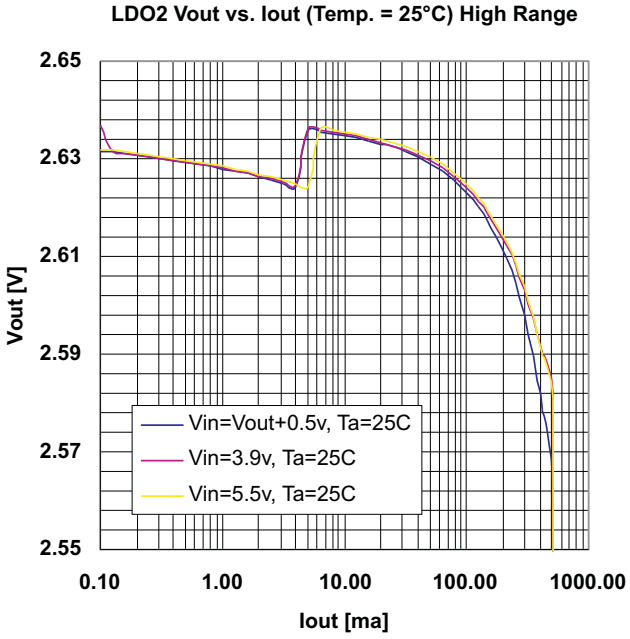

Figure 2-8.

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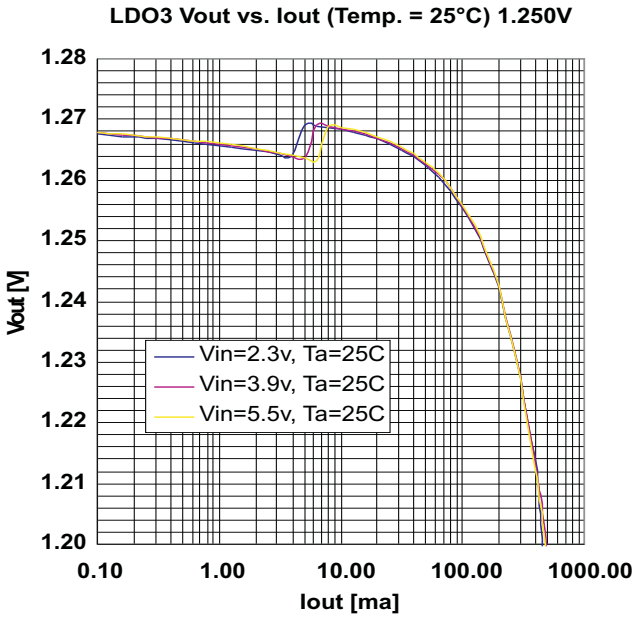


Figure 2-9.

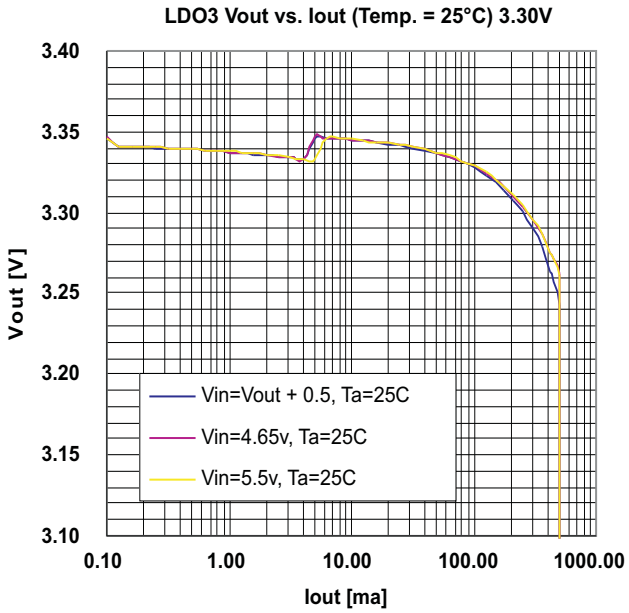
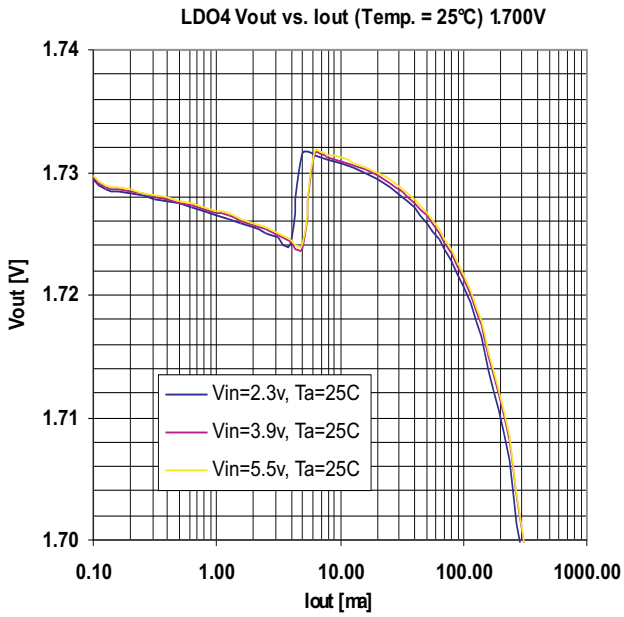


Figure 2-10.



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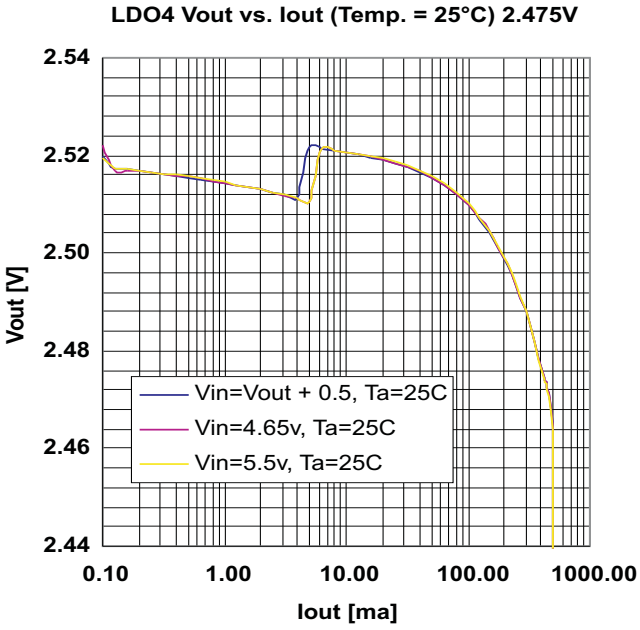

Figure 2-12.

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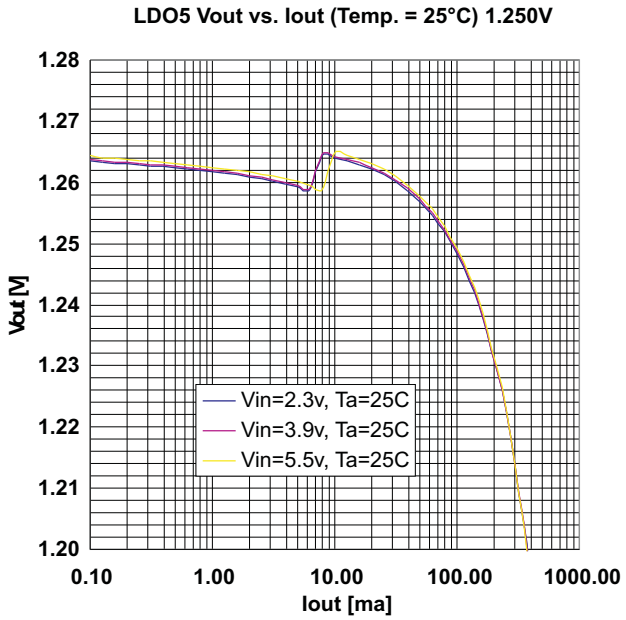

Figure 2-13.

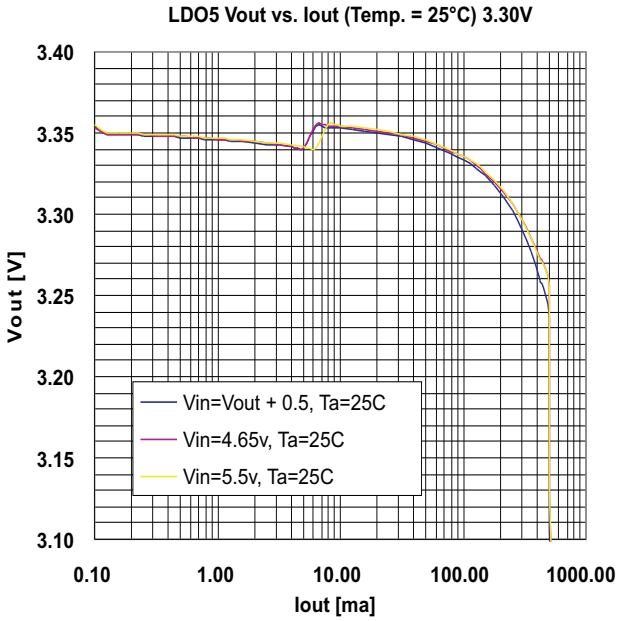

Figure 2-14.

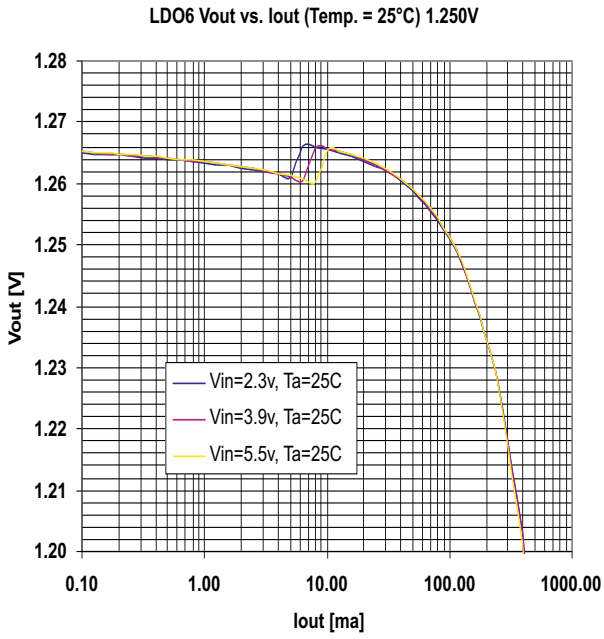

Figure 2-15.

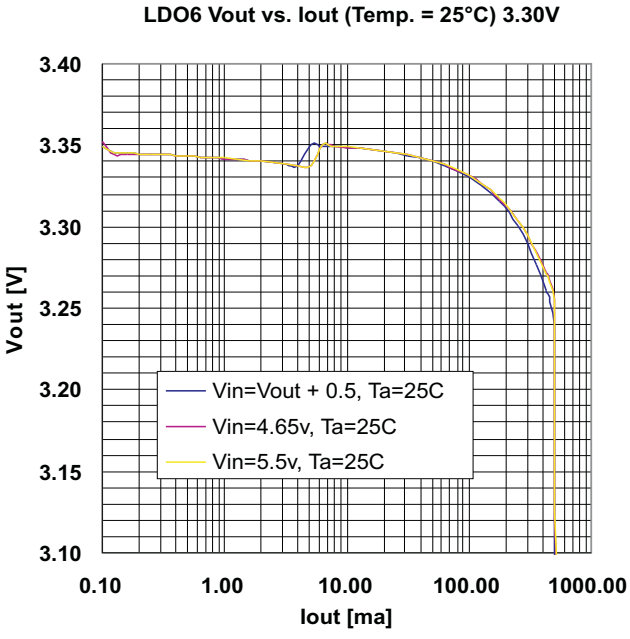

Figure 2-16.

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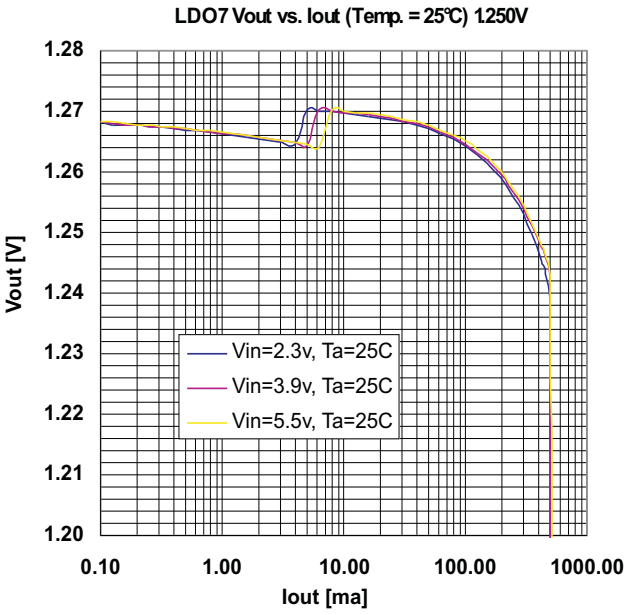

Figure 2-17.

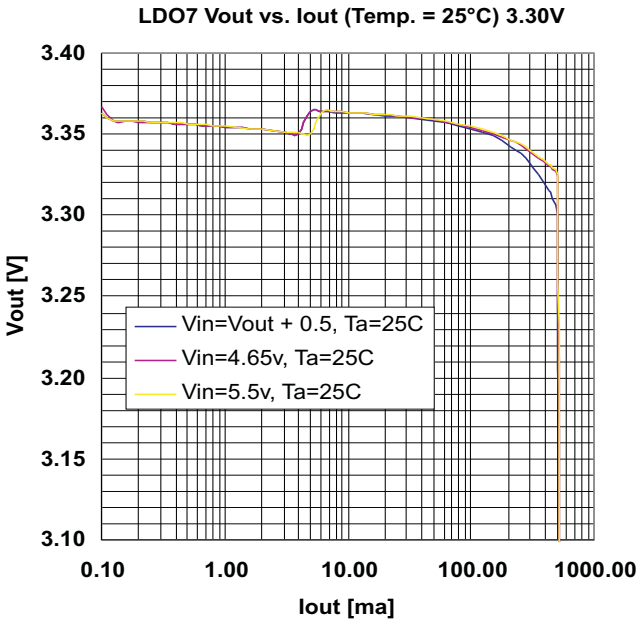

Figure 2-18.

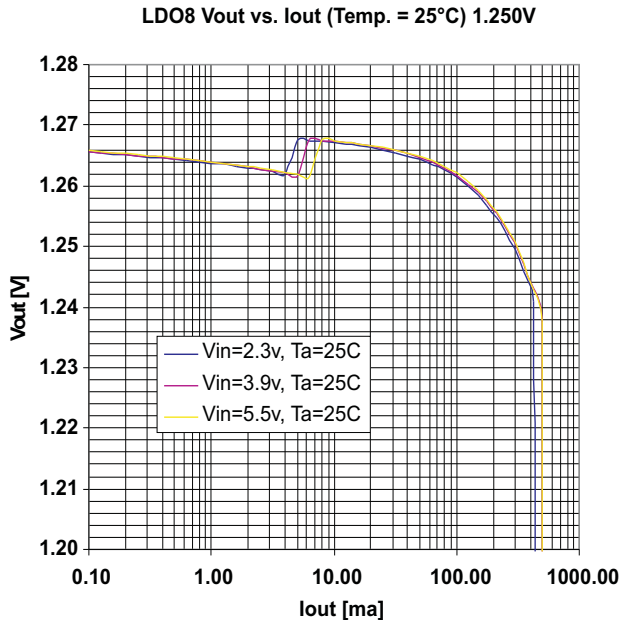

Figure 2-19.

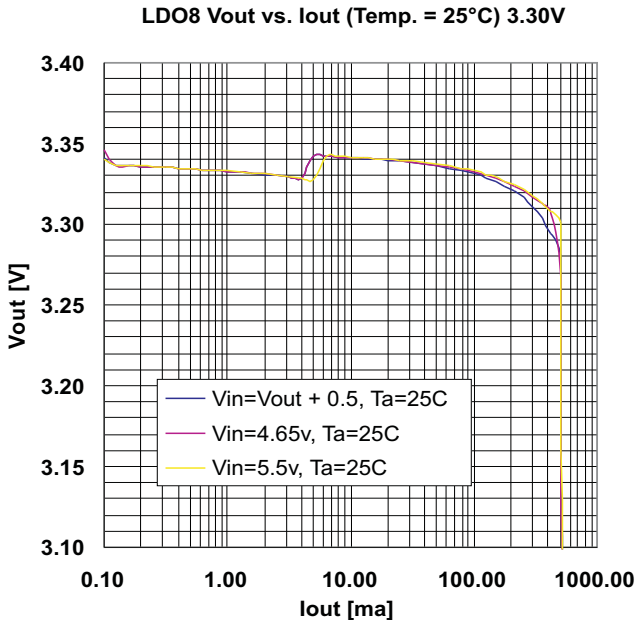

Figure 2-20.

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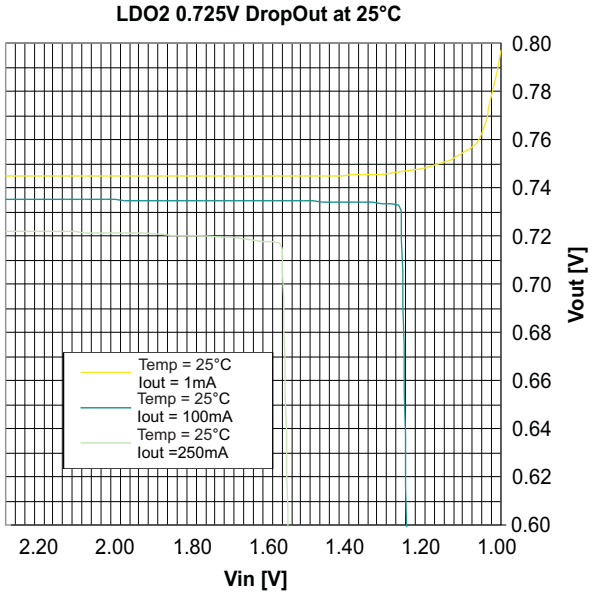
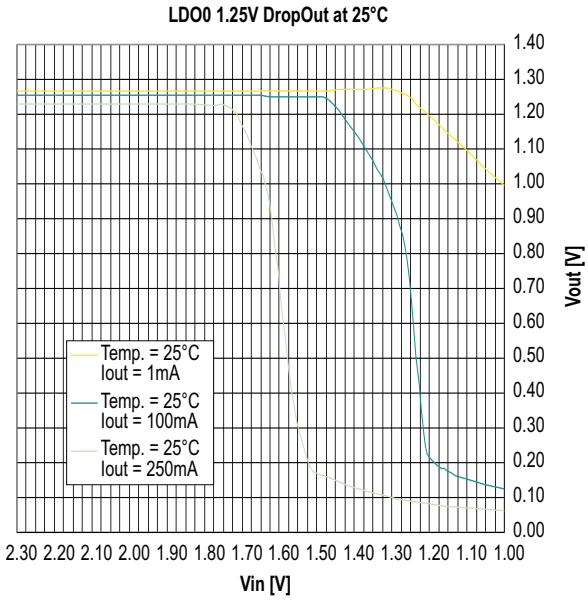


Figure 2-21.



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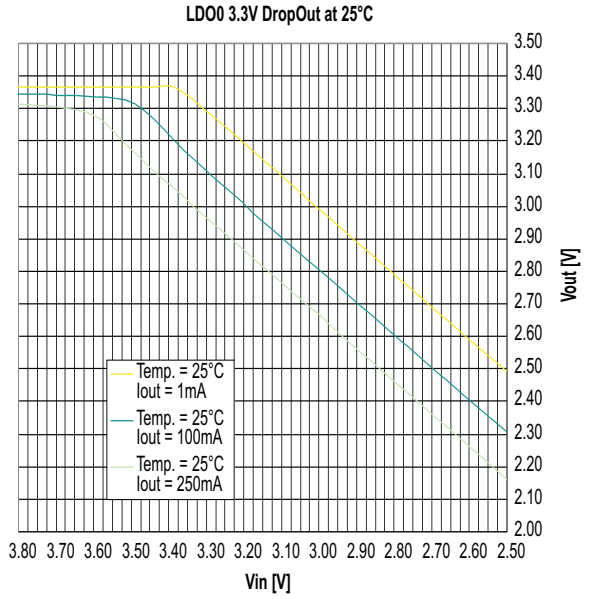

Figure 2-23.

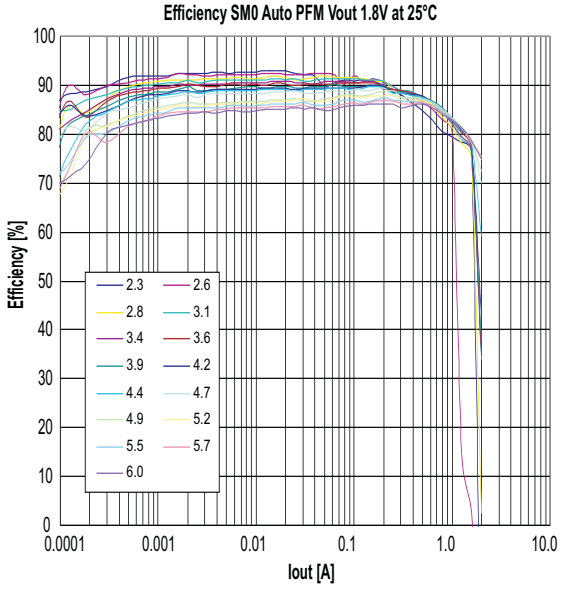

Figure 2-24.

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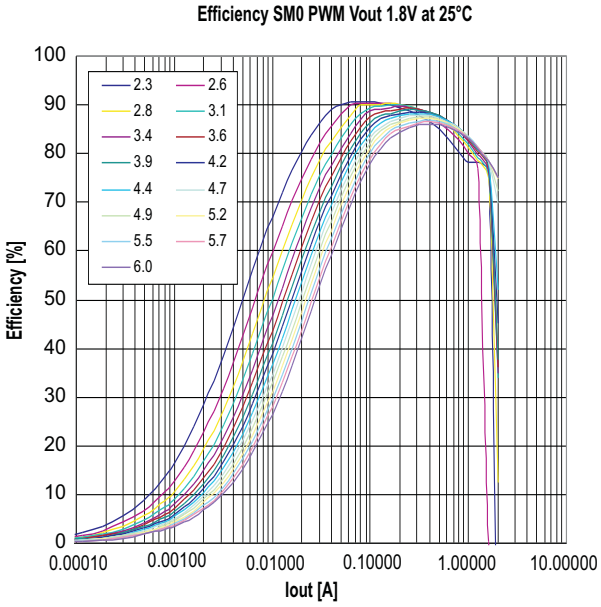

Figure 2-25.

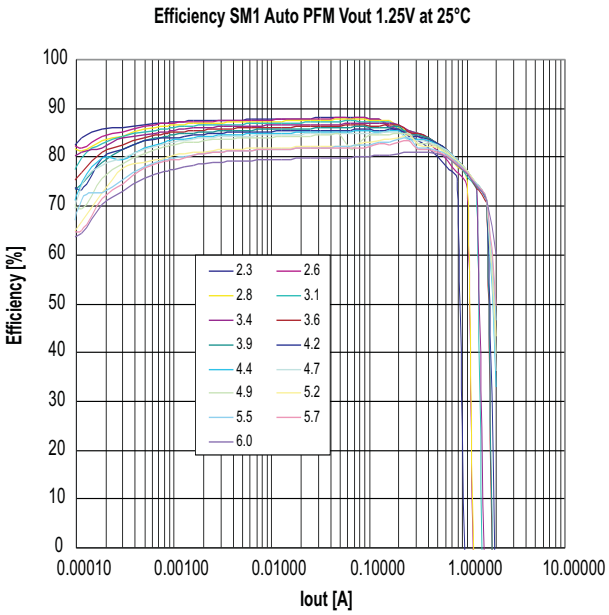

Figure 2-26.

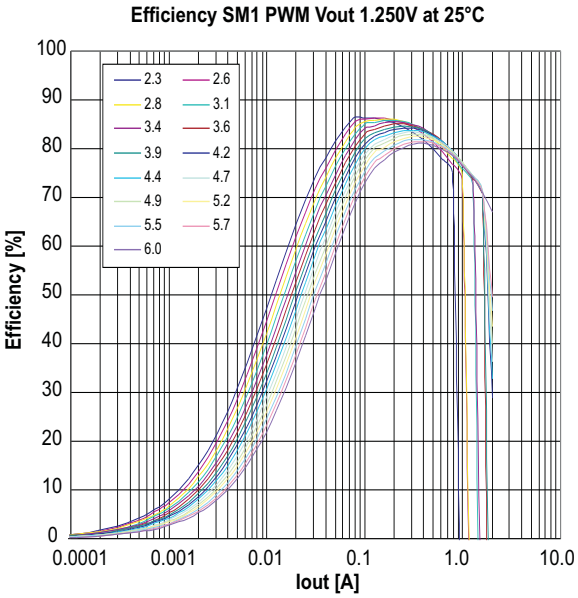

Figure 2-27.

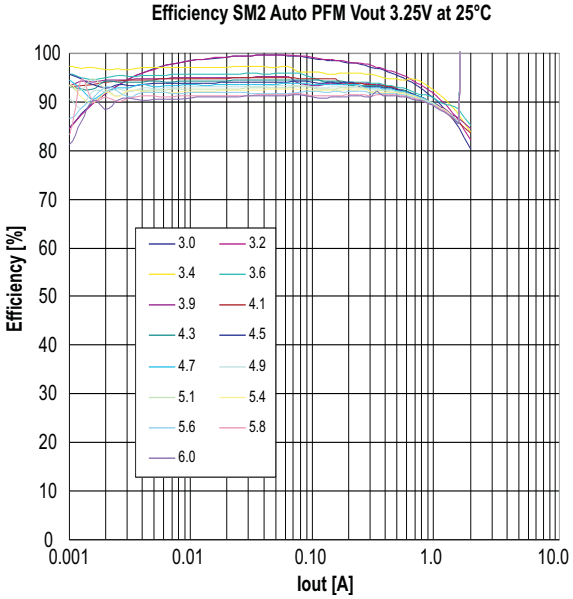

Figure 2-28.

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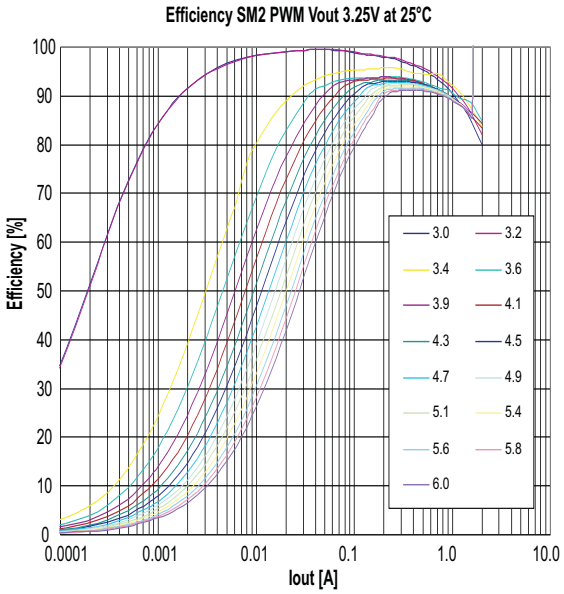


Figure 2-29.

3 DETAILED DESCRIPTION

3.1 I²C INTERFACE

Two I²C configurations are implemented in the TPS658629-Q1 device:

A –Standard I²C interface (SDAT/SCLK engine) : A single I²C communication port provides a simple way for an I²C compatible host to access system status information, reset fault modes, and set supply output voltages. The I²C port functions as a SLAVE enabling I²C compatible hosts (MASTER) to perform WRITES and READS to/from internal registers. The I²C port is a 2-wire bidirectional interface using the SCLK (clock) and SDAT (data) pins. The I²C is designed to operate at SCLK frequencies up to 400 kHz. The standard 8 bit command is supported. The CMD part of the sequence is the 8 bit register address to read or write.

B – Power I²C interface (PSDAT/PSCLK engine): The TPS658629-Q1 supports processors that use a dedicated I²C bus to dynamically adjust critical supply voltages by adding a second I²C bus (Power I²C) connected to a second, dedicated I²C engine. The Power I²C port is a 2-wire bidirectional interface using the PSCLK (clock) and PSDAT (data) pins. The Power I²C is designed to operate at PSCLK frequencies up to 400 kHz. A multiple-byte data-register pair command protocol, not compatible with the standard I²C protocol, is supported by the Power I²C engine. The Power I²C engine does not support read operations.

NOTE

The Standard and Power I²C engines are always reset by the sequencer when the TPS658629-Q1 is in the POWER-UP state and when the SLEEP state is set.

3.2 I²C ADDRESS

The TPS658629-Q1 will acknowledge (ACK) addresses 0x68 (writes) and 0x69 (reads) and will NACK any other address.

3.3 DVM REGISTER ACCESS

The sequencer state machine disables write access to specific supply voltage setting registers when the TPS658629-Q1 is initially powered and when the integrated supplies are being sequenced. See the sequencer functional description for details.

3.4 SCLK/SDAT AND PSCLK/PSDAT TIMEOUT

The TPS658629-Q1 monitors the SCLK/PSCLK clock lines, and it identifies a timeout condition if the clock line is held at a logic low for longer than 30ms. The I²C engine is NOT reset when the clock line timeout is identified.

The TPS658629-Q1 monitors the SDAT/PSDAT data lines. The I²C engine will be reset when the data line is held at a logic low for more than 30ms.

3.5 I²C BUS RELEASE

The TPS658629-Q1 I²C engine does not create START or STOP states on the I²C bus during normal operation.

3.6 I²C BUS ERROR RECOVERY

The I²C bus specification does not define a method to be used when recovering from a host side bus error. During a read operation the SDAT pin can be left in a LO state if the host has not sent enough SCLK pulses to complete a transaction (i.e. host side bus error). The TPS658629-Q1 will clear any SDAT LO condition if 10 SCLK pulses are sent by the host, enabling recovery from host side bus error events.

3.7 I²C COMMUNICATION PROTOCOL

The following conventions will be used when describing the communication protocol:

CONDITION	CODE
START sent from host	S
STOP sent from host	P
TPS658629-Q1 I²C slave address sent from host (WRITE)	hA0
TPS658629-Q1 register address sent from TPS658629-Q1 (READ)	hA1
Non-valid I²C slave address sent from host	hA_N
Valid TPS658629-Q1 register address sent from host	HCMD
Non-valid TPS658629-Q1 register address sent from host	HCMD_N
I/O data byte (8 bits) sent from host to TPS658629-Q1	hDATA
I/O data byte (8 bits) sent from TPS658629-Q1 to host	bqDATA
Acknowledge (ACK) from host	hA
Not acknowledge (NACK) from host	hN
Acknowledge (ACK) from TPS658629-Q1	bqA
Not acknowledge (NACK) from TPS658629-Q1	bqN

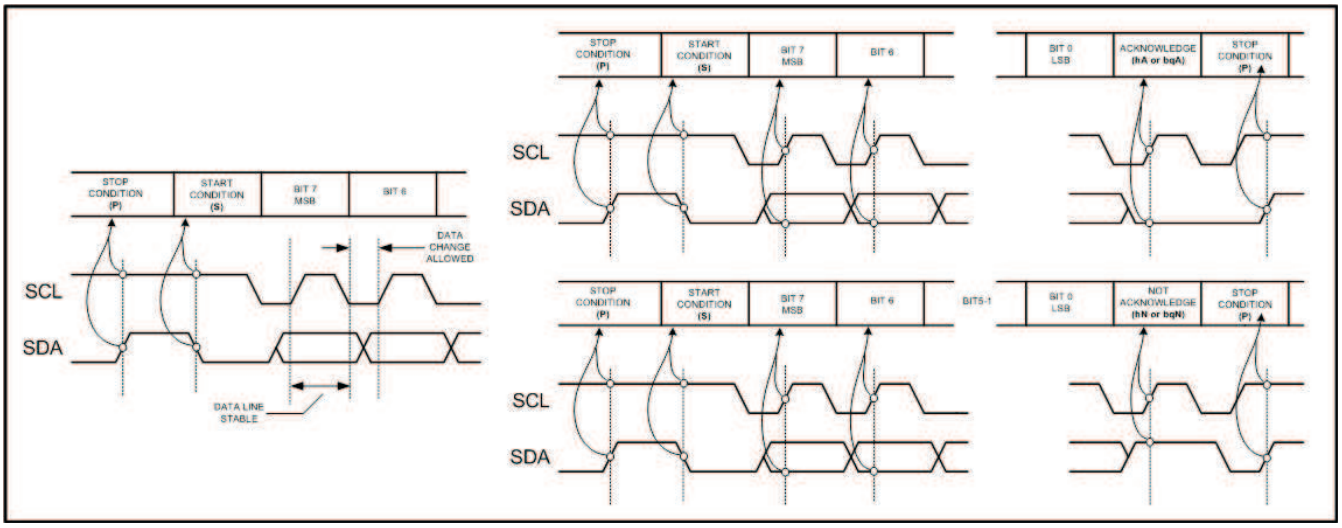


Figure 3-1. I²C Conditions

For normal data transfers, the data line (SDAT or PSDAT) is allowed to change only when the clock line (SCLK or PSCLK) is low, and one clock pulse is used per bit of data. The data line must remain stable whenever the clock line is high, as data changes when the clock is high are reserved for indicating the start and stop conditions. Each data transfer is initiated with a start condition and terminated with a stop condition.

When addressed, the TPS658629-Q1 device generates an acknowledge bit after the reception of each byte by pulling the data line Low. The master device (microprocessor) must generate an extra clock pulse that is associated with the acknowledge bit. After the acknowledge/not acknowledge bit, the TPS658629-Q1 leaves the data line high, enabling a STOP condition generation.

3.8 I²C READ AND WRITE OPERATIONS

The TPS658629-Q1 supports the standard I²C one byte Write. The basic I²C read protocol has the following steps:

1. Host sends a start and sends TPS658629-Q1 address
2. TPS658629-Q1 ACK's that this is a valid I²C address and that the bus is configured for write

3. Host sends TPS658629-Q1 register address
4. TPS658629-Q1 ACK's that this is a valid register and stores the register address to be read
5. Host sends a repeated start and TPS658629-Q1 I^2C slave address, reconfiguring the bus for read
6. TPS658629-Q1 ACK's that this is a valid address and that bus is reconfigured
7. Bus is in read mode, TPS658629-Q1 starts sending data from selected register

The I^2C write protocol is similar to the read, without the need for a repeated start and bus being set in write mode. In a WRITE, it is not necessary to end each 1 byte WRITE command with a STOP as a START will have the same effect (repeated start).

The host can complete a READ or a WRITE sequence with either a STOP or a START.

NOTE

Read operations are not supported for the PSDAT/PSCLK I^2C engine.

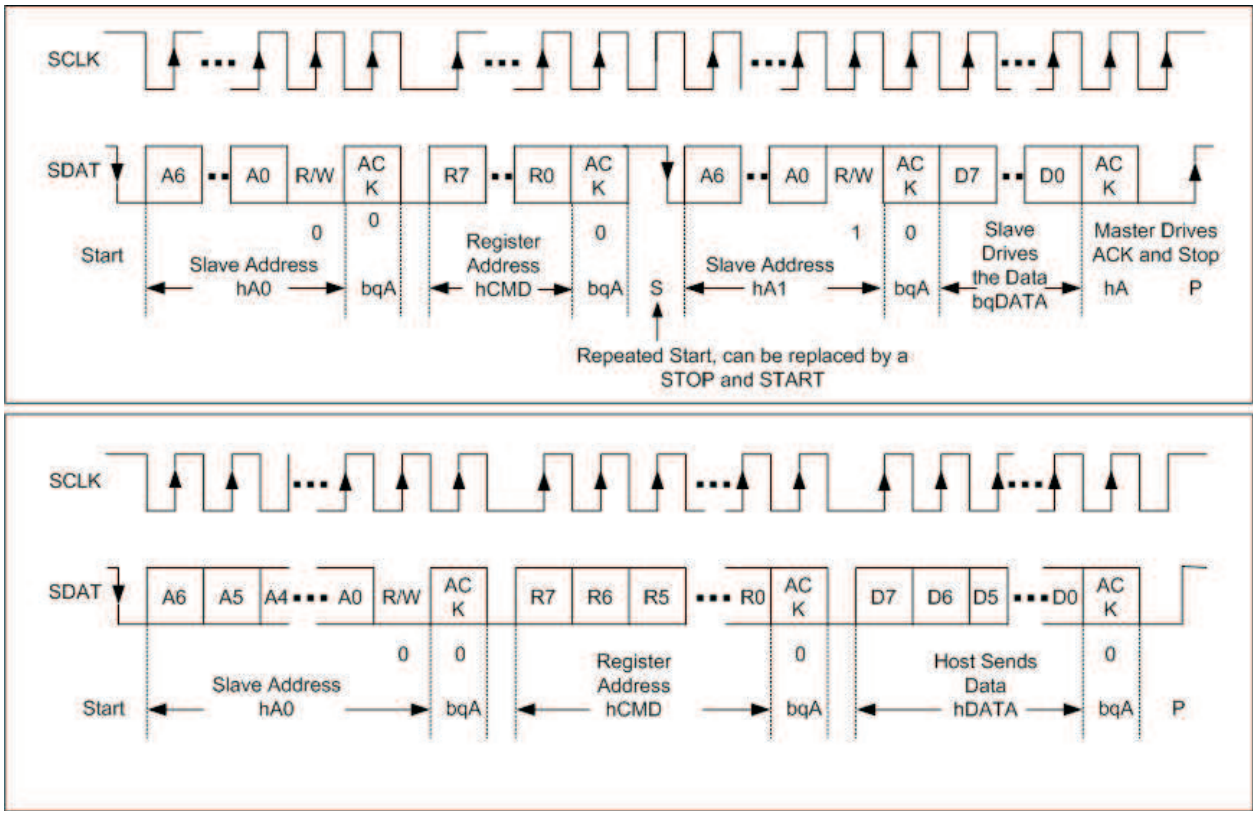


Figure 3-2. I^2C Read/Write Example

3.9 VALID WRITE SEQUENCES (SDAT/SCLK, PSDAT/PSCLK)

The TPS658629-Q1 will always ACK its own address. If CMD points to an allowable READ or WRITE address, the device writes the address into its RAM address register and sends an ACK. If CMD points to a non-allowed address, the device does NOT write the address into its RAM address register and sends a NACK.

S	hA0	bqA		S	hA0	bqA	hCMD	bqA		S	hA0	bqA	hCMD_N	bqN

3.10 ONE BYTE WRITE (SDAT/SCLK, PSDAT/PSCLK)

The data is written to the addressed register at the end of the bq ACK, ending the one byte write sequence when the RAM address and the data byte are stored in the I^2C registers. The host can cancel a WRITE by sending a STOP or START before the trailing edge of the ACK clock pulse.

S	hA0	bqA	hCMD	bqA	hDATA	bqA

3.11 VALID READ SEQUENCES (SDAT/SCLK ONLY)

The TPS658629-Q1 will always ACK its own address.

S	hA1	bqA

Upon receiving hA1, TPS658629-Q1 starts at the current location of the RAM address register. The START and the STOP both act as priority interrupts. If the host has been interrupted and is not sure where it left off, it can send a STOP and reset the TPS658629-Q1 state machine to the WAIT state; once in the WAIT state, the TPS658629-Q1 will ignore all activity on the SCLK and SDAT lines until it receives a START. A repeated START and START in the I^2C specification are both treated as a START.

S	hA0	bqA	hCMD	bqA	P

S	hA0	bqA	hCMD	bqA	S	hA1	bqA	bqDATA	hN	P

3.12 VALID READ SEQUENCES (SDAT/SCLK ONLY)

S	hA1	bqA	bqDATA	hN	P

Incremental read sequences

S	hA1	bqA	bqData	hA	bqDATA	hA	. . .	bqDATA	hN	P

3.13 NON-VALID SEQUENCES

START and non-hA0 or non-hA1 Address: A START followed by an address which is not hA0 or hA1 will be NACKED.

S	hA_1	bqN

Attempt to Specify Non-Allowed READ Address

If the CMD points to a non-allowed READ address (reserved registers), bq will send a NACK back to the host and it will not load the address in the RAM address register. Note that the TPS658629-Q1 NACKS whether a stop is sent or not.

S	hA0	bqA	hCMD_N	bqA	P		S	hA0	bqA	hCMD_N	bqN

Attempt to Specify Non-Allowed WRITE Address

If the host attempts to WRITE to a READ-ONLY or non-accessible address, the TPS658629-Q1 ACKS the CMD containing the allowed READ address, loads the address into the address register and ACKS after the host sends the next data byte. A subsequent hA1 READ could read this address, but the data sent by the host will not have been written.

S	hA0	bqA	hCMD	bqA	hDATA	bqA

3.14 INCREMENTAL READ (SDAT/SCLK ONLY)

The SDAT/SCLK I²C interface supports incremental read operations. Each register must be accessed in a single read operation. A valid WRITE address is required to write to the RAM, and a valid READ address is required to specify the initial RAM address where the READ starts. Once a read command is received, the RAM data for the specified address is output to the host. If the host chooses, it can loop through the remaining addresses; the address is automatically incremented by one at the end of each read. If the loop gets to the top address, it automatically rolls over to address 0x00 and the sequence stops.

3.15 I²C COMMUNICATION PROTOCOL – POWER I²C INTERFACE, PINS PSDAT/PSCLK

The Power I²C interface is designed to support fast write operations using multiple register-data pair sequences. The Power I²C engine is a write-only engine, and it does not support read operations.

During a write sequence, the host sends the start command, followed by the TPS658629-Q1 address. Then the host sends the register address byte, followed by eight bits of the data for the respective register (Register1 Address/Data in Figure 3-3). From this point on the TPS658629-Q1 will accept all the following 2 byte pairs as a random register address, followed by the data content to be written to that register. This process continues until the host sends a valid stop condition after the last register (Register N in Figure 3-3) is written. A typical multi-byte sequence is shown in Figure 3-3.

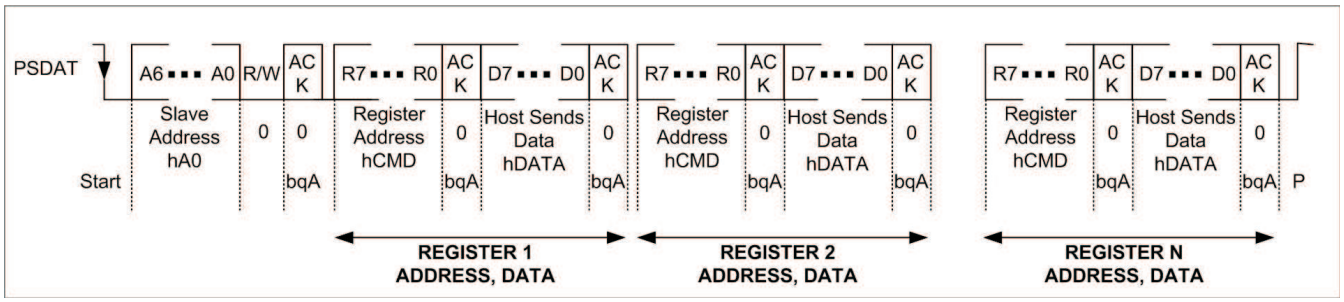


Figure 3-3. Power I²C Protocol

3.16 SIMULTANEOUS STANDARD AND POWER I²C OPERATION

The TPS658629-Q1 has individual address pointers for the Power I²C engine and Standard I²C engine. The value written to the register will be defined by the relative timing between read/write pulses when simultaneous I²C read/write operations happen. Simultaneous write/read operations to the same register will be handled as follows:

1. Both Standard I²C and Power I²C are executing operations accessing distinct registers at the same time (simultaneous read/read, read/write, write/read or write/write): No conflict exists in this case.
2. Power I²C writes and Standard I²C reads the same register at the same time
   (a) Standard I²C will read the old register value if the Standard I²C read pulse is generated at least 110nsec (typ) before the Power I²C write pulse happens.
   (b) Standard I²C will read the new register value if the Standard I²C read pulse is generated at least 110nsec (typ) after the Power I²C write pulse happens.
3. Power I²C and Standard I²C write to the same register at the same time
   (a) If both write operations are more than 110nsec (typ) apart, the register final value will be set by the engine that executes the last write operation.
   (b) a. If both write operations are less than 110nsec (typ) apart, the priority will be given to the Power I²C engine. The value from the Power I²C engine will be written into the register, and the data received by the Standard I²C operation is not written to the TPS658629-Q1 internal memory.

THERE IS NO CLOCK STRETCH FUNCTION IN EITHER SCLK OR PSCLK WHEN A CONFLICT SITUATION HAPPENS. THE CONFLICT IS HANDLED INTERNALLY BY GIVING PRIORITY TO PSDAT/PSCLK ENGINE.

3.17 POWER PATH

3.17.1 RAM Control Bits

The power path circuit connects one of the power sources plugged into the AC, USB or BAT pins to the SYS pin. The supply selection is made based on system parameters monitored by the power path circuit and internal RAM control bits in register 0x4C.

Table 3-1. Power Path Control

PPATH1 [Addr 0x4C]								Defaults in BOLD
Bit Number	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**
Bit Name	USBSUSP	USBDCH	ACDCH	CHGRNG	BOOTOFF	USBLIMIT	USBMODE	PWRSYS
Function	USB SUSPEND MODE	SPARE	SPARE	CHARGE VOLTAGE RANGE	USB INPUT ILIMIT at BOOT PHASE	USB INPUT CURRENT LIMIT SETTING	USB INPUT CURRENT LIMIT	AUTO SYS POWER SELECTION
When 0	**SUSPEND OFF**	NOT USED	NOT USED	**3.95V-4.2V**	SET BY USBLIMIT ONLY	**100mA**	**SET BY USBLIMIT**	BAT TO SYS
When 1	SUSPEND ON	**NOT USED**	**NOT USED**	4.3V-4.45V	**SET BY USBMODE AND USBLIMIT**	500mA	2.25 A	**AUTO MODE ENABLED**

The input power priority is hard-wired internally, with the AC input having the higher priority, followed by the USB input (2nd) and the battery pack (3rd). The SYS pin voltage is **not** regulated and it will be equal to the input voltage (AC, USB or BAT value) minus the voltage drop across the switch that is ON when the selected input current limit is not active.

Setting the control bit PWRSYS (bit 0) to **0**, the user can override the power path priority, connecting the battery to the SYS pin even if AC or USB are detected. When PWRSYS is **0** and the battery is removed, the SYS pin ***will not*** be connected back to the AC or USB inputs and thereby will discharge to ground.

The USB power will be ignored when USBSUSP (bit 7) is **1**, connecting only the AC or BAT power sources to the SYS pin. If neither AC nor BAT is connected the SYS pin, it will discharge to ground.

The USB input current is limited to the maximum value programmed by the host via the I^2C interface by setting bits USBLIMIT (bit 2) and USBMODE (bit 1) as shown in Table 3-2.

Table 3-2. Power Path Current Limit

USBMODE	USBLIMIT	USB INPUT CURRENT LIMIT	AC INPUT CURRENT LIMIT
0	0	100 mA max	2.2 A min
0	1	500 mA max	
1	X	2.1 A min	

If the system current requirements exceed the input current limit, the SYS pin voltage will be reduced until the power path is set in supplement mode (if pack is connected).

3.18 SYSTEM STATUS DETECTION

The TPS658629-Q1 has integrated comparators that monitor the BAT, AC, USB and SYS pin voltages. Table 3-3 lists the system power detection conditions:

Table 3-3. Power Path Detection Functions

SYSTEM STATUS	DETECTION CONDITIONS(1)
AC input voltage detected	$V_{IN(OVP)}$ > V(AC) > V(BAT) + $V_{IN(DT)}$
USB input voltage detected	$V_{IN(OVP)}$ > V(USB) > V(BAT) + $V_{IN(DT)}$
AC over-voltage detected	V(AC) > $V_{IN(OVP)}$
USB over-voltage detected	V(USB) > $V_{IN(OVP)}$
SYS pin short detected	V(SYS) < $V_{SH(SYS)}$
Battery switch over-current detection	I(BAT) > I_{BATSYS}
Supplement mode detection	V(SYS)<V(BAT)–$V_{SUP(SYS)}$ AND I(BAT)< I_{BATSYS}

(1) $V_{IN(DT)}$, $V_{SH(SYS)}$, V_{BATSH}, $V_{IN(OVP)}$, $V_{SUP(SYS)}$ are TPS658629-Q1 internal references, refer to the electrical characteristics for additional details

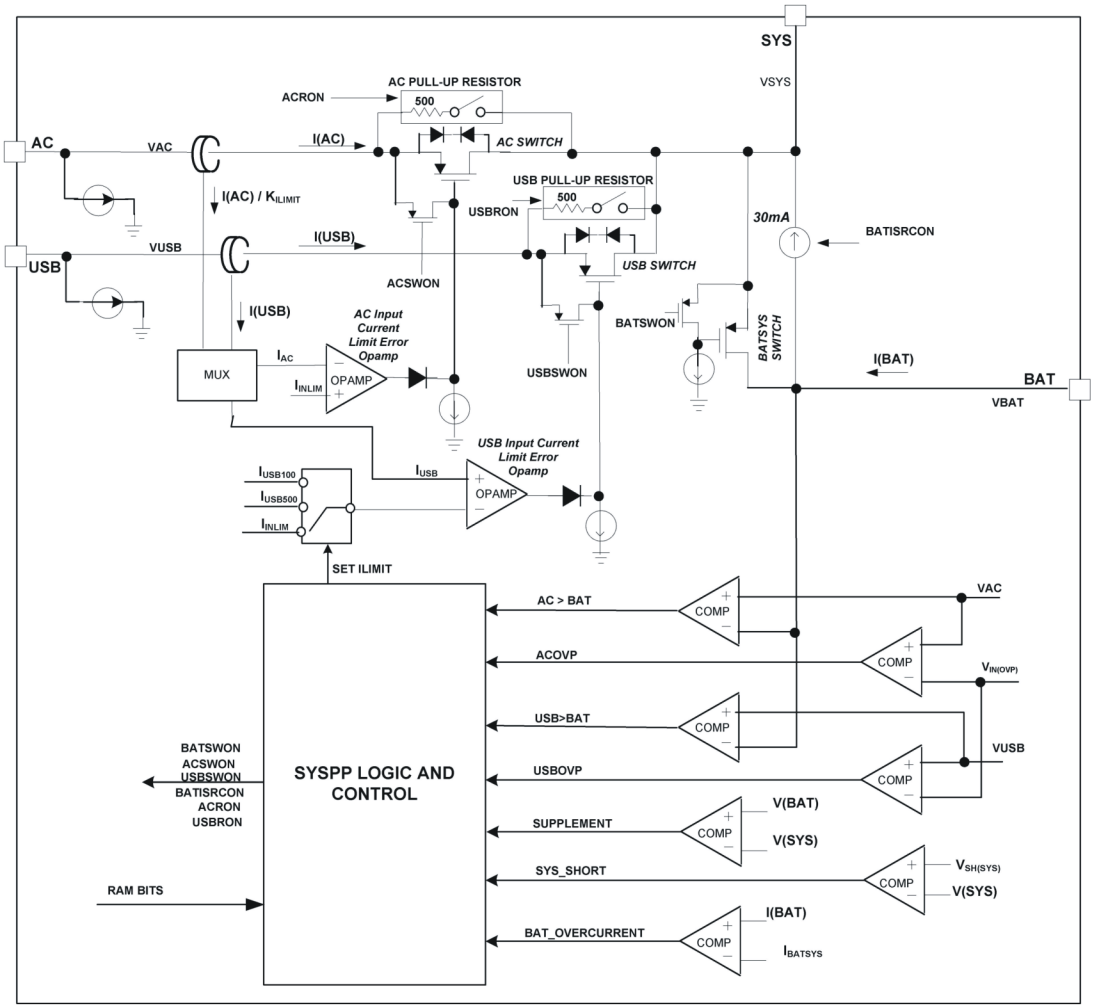


Figure 3-4. Simplified Power Path Block

The I^2C control bits and system status are used by the power path control logic to define the state of the power path switches as shown below; a fault condition will be detected when the SYS pin is shorted or a battery switch over-current condition is detected.

Table 3-4. Power Path Control

6586xx MODE	PWRSYS	USBSUSP	AC DETECTED	USB DETECTED	FAULT DETECTED	AC SWITCH	USB SWITCH	BATTERY SWITCH	SYS PIN CONNECTED TO
UVLO	X	X	X	X	X	OFF	OFF	OFF	NONE
NOT UVLO	X	X	X	X	YES	OFF	OFF	OFF	PULL-UP RES/ISRC
NOT UVLO	1	X	YES	X	NO	ON	OFF	ON if Supplement mode is required, OFF otherwise	AC
NOT UVLO		0	NO	YES	NO	OFF	ON		USB
NOT UVLO		1	NO	YES	NO	OFF	OFF	ON	BATTERY
NOT UVLO		X	NO	NO	NO	OFF	OFF	ON	BATTERY
NOT UVLO	0	X	X	X	NO	OFF	OFF	ON	BATTERY

When a fault condition is detected, the fault recovery method (resistor or current source) is defined by the input power supply detection:

Table 3-5. Power Path Fault Recovery Control

AC DETECTED	USB DETECTED	RECOVERY METHOD
YES	X	AC PULL-UP RESISTOR ON
NO	YES	USB PULL-UP RESISTOR ON
NO	NO	30mA CURRENT SOURCE ON

3.19 POWER PATH STATUS

The power path status is available at register 0xB9, bits BATSYSON, ACSWON, USBSWON , and register 0xBB, bits LOWSYS, ACDET, USBDET, AC_OVP and USB_OVP. See the STATUS REGISTER section for bit function description.

3.20 CHG1 AND CHG2 RAM REGISTERS

Table 3-6. Control Registers

CHG1 [Addr 0x49]								Defaults in **BOLD**
Bit Number	B7	B6	B5	B4	B3	B2	B1	B0
Bit Name	RSVD	RSVD	BATDCH	TSON	RSVD	RSVD	RSVD	RSVD
Function			BATTERY DISCHARGE SWITCH	THERMISTOR BIAS CONTROL				
When 0			OFF	**OFF**				
When 1			**ENABLED**	ON				
CHG2 [Addr 0x4A]								Defaults in **BOLD**
Bit Number	B7	B6	B5	B4	B3	B2	B1	B0
Bit Name	DTCON	RSVD	TSBYP	RSVD	RSVD	RSVD	RSVD	RSVD
Function	DYNAMIC TIMER FUNCTION		ENABLE CHARGER LDO MODE					
When 0	OFF		OFF					
When 1	**ON**		**ON**					

3.21 BATTERY DETECTION, TEMPERATURE QUALIFICATION

Battery pack insertion and battery pack temperature are detected by three comparators that monitor the thermistor voltage. The thermistor supply is enabled via I^2C when control bit TSON=HI in register CHG1. This control bit enables the host software to turn on the thermistor bias when the pack temperature needs to be measured via the ADC, minimizing system quiescent current when operating under battery power.

3.22 BATTERY DISCHARGE SWITCH

An internal switch will discharge the BAT pin to ground when the battery is not detected. This switch is enabled via I^2C control bit BATDCH on register CHG1.

3.23 TPS658629-Q1 OPERATING MODES

The TPS658629-Q1 has an internal state machine that sets the operating modes based on the system status and host commands. The state machine directly controls the state of the integrated supplies during power-up sequences and normal operation. It also can change the on/off state of all integrated power supplies and peripherals to implement protection functions or execute external hardware control or host software commands.

3.24 STATE MACHINE DIAGRAM

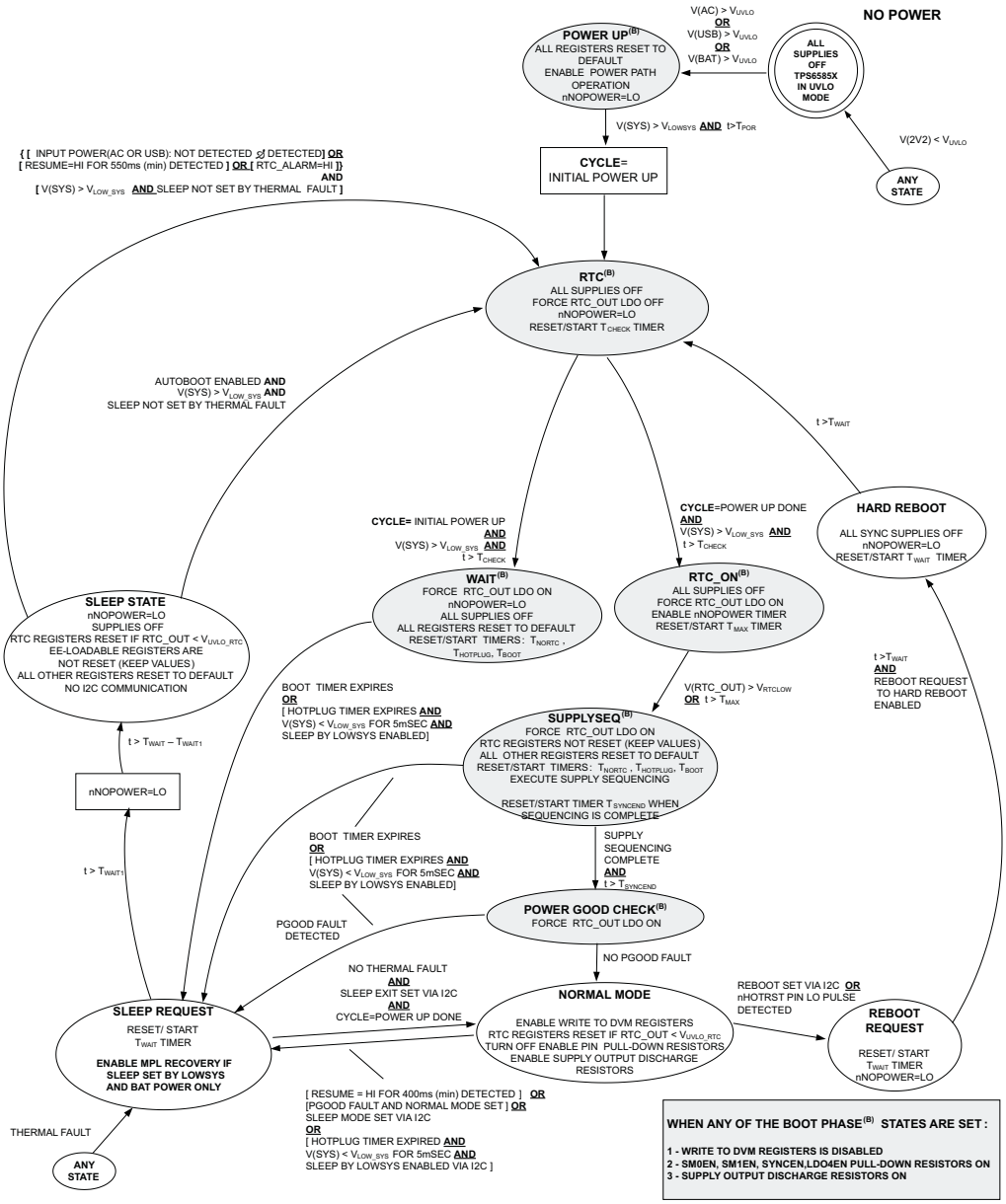


Figure 3-5. TPS658629-Q1 Operation Mode State Machine

The state machine transitions for the TPS658629-Q1 have been defined as shown below.

1. Supply sequencing started only when LDO4EN voltage level is a logic high
2. REBOOT REQUEST state transitions to the HARD REBOOT state
3. Supply sequencing is considered complete only if SM0 is turned ON
4. Sequencer goes into sleep during initial power-up cycle

3.25 STATE MACHINE DESCRIPTION

In a normal power-up sequence the state machine will step through the following states:

POWER-UP: If the internal digital supply (2V2) is below the internal UVLO threshold, V_{UVLO} (2V typ), all IC blocks are disabled and the TPS658629-Q1 is not operational. When the 2V2 supply voltage rises above V_{UVLO}, the POWER-UP state is entered, an internal delay (T_{POR}, 8ms typ) is started and the SYS power path is enabled. The SYS pin voltage is sensed by an internal comparator, and compared to the internal threshold V_{LOW_SYS}. When the power-on-reset delay expires and V(SYS) > V_{LOW_SYS} the TPS658629-Q1 enters the RTC mode.

RTC: When the RTC state is set the nNOPOWER pin is pulled to ground, discharging the external capacitor connected to pin TNOPOWER and resetting the NOPOWER timer. The RTC_OUT LDO is turned off, and the voltage at pin RTC_OUT is flagged as low if V(RTC_OUT) < V_{RTCLOW} The RTC state ends when the timer T_{CHECK} expires.

RTC_ON: When the state RTC_ON is set the integrated current source connected to the TNOPOWER pin and the RTC_OUT LDO are enabled. If the RTC_OUT voltage was flagged as low in the RTC state the T_{NORTC} timer is enabled, and the $\overline{NORTC}$ pin is pulled low until V(RTC_OUT) > V_{RTC_PGOOD}. The T_{NORTC} timer starts counting when RTC_OUT > V_{RTCLOW}, and $\overline{NORTC}$ will be set to hi when t > T_{NORTC}.

The TNOPOWER current source will remain ON until a new reboot cycle or sleep cycle is set, charging the external capacitor connected to the TNOPOWER pin. The $\overline{NOPOWER}$ pin will be at a low logic level until the TNOPOWER pin voltage is above an internal threshold (1.23v typ). When $\overline{NOPOWER}$ pin transitions from LO→HI, a 250µsec (typ) positive going pulse is generated at CHG_STAT pin. The TNOPOWER external capacitor is discharged whenever the sequencer sets the $\overline{NOPOWER}$ pin to a low state.

The RTC_ON state ends when V(RTC_OUT) > V_{RTC_PGOOD} or when the internal watchdog timer T_{MAX} expires.

WAIT: The TPS658629-Q1 will go into the WAIT state when exiting the RTC state during the initial power-up cycle. To avoid undesired lockup conditions this operational mode should be used only when the boot timer is enabled.

Three internal timers are started when the state machine enters the WAIT state. These timers run independent of the sequencing state and have the following functionality:

- BOOT Timer (T_{BOOT}): Sets the TPS658629-Q1 in the SLEEP REQUEST state if it expires during WAIT state.
- HOTPLUG Timer ($T_{HOTPLUG}$): SLEEP REQUEST state set by V(SYS) < V_{LOWSYS} is inhibited until this timer expires
- NORTC Timer (T_{NORTC}): $\overline{NORTC}$ pin will be set to a logic low level until this timer expires

The BOOT timer value is set to 500ms and the $\overline{NORTC}$ pulse width is set to 10ms.

SUPPLYSEQ: During the SUPPLYSEQ state all the internal supplies, with exception of RTC_OUT, are initially turned off and then turned on according to a pre-programmed internal sequencing. Three internal timers are started when the state machine enters the SUPPLYSEQ state. These timers run independent of the sequencing state and have the following functionality:

- BOOT Timer (T_{BOOT}): Sets the TPS658629-Q1 in the SLEEP REQUEST state if it expires during SUPPLYSEQ state.
- HOTPLUG Timer ($T_{HOTPLUG}$): SLEEP REQUEST state set by V(SYS) < V_{LOWSYS} is inhibited until this timer expires
- NORTC Timer (T_{NORTC}): $\overline{NORTC}$ pin will be set to a logic low level until this timer expires

The BOOT timer value is set to 500ms and the $\overline{NORTC}$ pulse width is set to 10ms.

The I^2C engines are available while the device is in the SUPPLYSEQ state, however write operations to the DVM registers are disabled, refer to DVM register section for more details. The TPS658629-Q1 remains in this state until all the supplies are sequenced and the internal delay $T_{SYNCEND}$ (5ms typ) has expired.

POWER GOOD CHECK: Supplies that were powered up during the SUPPLYSEQ state will have their power good flags checked during the POWER GOOD CHECK state (with exception of RTC_OUT ldo). The POWER GOOD CHECK state ends and the NORMAL state is set when a power good fault is not present. If a power good fault is detected, the POWER GOOD CHECK state will move to the SLEEP REQUEST state when the boot timer expires.

NORMAL STATE: In this state write operations to the DVM registers are enabled and the external host controls all the TPS658629-Q1 functions. The normal state operation ends if a fault condition (defined as either a thermal fault, V(SYS) < V_{LOW_SYS} or a supply power good fault) is detected or if hardware or software commands trigger a sleep or reboot request. While in NORMAL mode, the host can mask any of the power supply power good fault detection via I^2C registers PGFLTMASK1 and PGFLTMASK2. Supplies that have their power good fault detection masked will not end the normal state operation. However, the status bit for the supply indicates that the output voltage is out of regulation. A RTC_OUT LDO power good fault does not trigger a transition to SLEEP REQUEST.

Table 3-7. Sequencer Power Good Fault Masking

PGFLTMASK1 [Addr 0x4D]								Defaults in **BOLD**
Bit Number	B7	B6	B5	B4	B3	B2	B1	B0
Bit Name	MASK_PLDO8	MASK_PLDO7	MASK_PLDO6	MASK_PLDO4	MASK_PLDO3	MASK_PLDO2	MASK_PLDO1	MASK_PLDO0
Function	MASK PGOODLDO8	MASK PGOODLDO7	MASK PGOODLDO6	MASK PGOODLDO4	MASK PGOODLDO3	MASK PGOODLDO2	MASK PGOODLDO1	MASK PGOODLDO0
When 0	**UNMASKED**	**UNMASKED**	**UNMASKED**	**UNMASKED**	**UNMASKED**	**UNMASKED**	**UNMASKED**	**UNMASKED**
When 1	MASKED	MASKED	MASKED	MASKED	MASKED	MASKED	MASKED	MASKED
PGFLTMASK2 [Addr 0x4E]								Defaults in **BOLD**
Bit Number	B7	B6	B5	B4	B3	B2	B1	B0
Bit Name	MASK_PSM3	MASK_PSM2	MASK_PSM1	MASK_PSM0	MASK_PLDO9	MASK_PLDO5	RSVD4E1	RSVD4E0
Function	MASK PGOODSM3	MASK PGOODSM2	MASK PGOODSM1	MASK PGOODSM0	MASK PGOODLDO9	MASK PGOODLDO5	NOT USED	NOT USED
When 0	**UNMASKED**	**MASKED**	**UNMASKED**	**UNMASKED**	**UNMASKED**	**UNMASKED**	**NOT USED**	**NOT USED**
When 1	MASKED	UNMASKED	MASKED	MASKED	MASKED	MASKED	NOT USED	NOT USED

SLEEP REQUEST: The SLEEP REQUEST state is set at anytime when a thermal fault condition is detected. It is also set when the TPS658629-Q1 is in the NORMAL state followed by one of the events shown below.

1. A hardware sleep request is detected at the RESUME pin.
2. A power good fault is detected at any of the integrated supplies
3. V(SYS_IN) < V_{LOW_SYS} and the HOTPLUG timer has expired (t > $T_{HOTPLUG}$)
4. SLEEP MODE is 1 (register 0x14, bit B3)

When the SLEEP REQUEST state is set an internal timer is started and bit SLEEPREQ=**1** is set in register STAT3 (address 0xBB). Writing EXITSLREQ to 1 (0x14, bit B1) returns the TPS658629-Q1 to the NORMAL state. If no action is taken by the host, while SLEEP_REQUEST state is set, the $\overline{\text{NOPOWER}}$ pin is pulled low when T_{WAIT1} expires and the SLEEP state is entered after the T_{WAIT} timer expires.

Table 3-8. Sequencer Control, LDO5/LDO9 Enable

SUPPLYENE [Addr 0x14]							Defaults in **BOLD**	
Bit Number	B7	B6	B5	B4	B3	B2	B1	B0
Bit Name	LDO9_ON	LDO5_ON	SYSINEN	HOTDLY	SLEEP MODE	RSVD	EXITSLREQ	SOFT RST
Function	LDO9 ON/OFF CONTROL	LDO5 ON/OFF CONTROL	SYS_IN LOW VOLTAGE SETS SLEEP MODE	HOT RESET DEGLITCH	SET TPS658629-Q1 IN SLEEP MODE		SLEEP REQUEST EXIT CONTROL	SOFTWARE RESET CONTROL
When 0	**OFF**	**OFF**	DISABLED	**5µsec min, 16µsec max**	**NOT ACTIVE**		**GO TO SLEEP at T>T_{wait}**	**NOT ACTIVE**
When 1	ON	ON	**ENABLED**	5ms	SET SLEEP		FORCE TRANSITION TO NORMAL STATE	REBOOT REQUEST

SLEEP STATE: When the SLEEP state is set all supplies are set to OFF mode (with exception of RTC_LDO) and the $\overline{\text{NOPOWER}}$ output is pulled low. A few internal blocks are still active, enabling detection of system status changes that trigger the SLEEP state exit.

All I^2C engines are reset and all RAM registers are reset to their default condition when the SLEEP state is set. The RAM bits that have a default set via the non-volatile memory will keep the value they had before the SLEEP state was set.

The SLEEP state ends when one of the following sequences is executed:

A. *If SLEEP was set by thermal fault:* The SLEEP state will end only when all external input supplies and battery pack are removed and an UVLO condition is detected by the TPS658629-Q1, setting the POWER UP state.

B. *If SLEEP was not set by thermal fault:* The SLEEP state will end when a hardware sleep exit request is detected at RESUME pin or the Momentary Power Loss (MLP) feature is triggered bt the conditions in either of the following scenarios:

- **Scenario 1**: If $V_{(SYS)} < V_{LOW\_SYS}$ for greater than 5 ms and V2V2 is above the UVLO threshold, the part transitions from normal to SLEEP state. For the part to exit from the SLEEP state and go to the RTC_CHECK state, the following conditions must be true 1 second after entering the SLEEP state:
  - V_{BAT} is greater than the voltage present on the COMP pin ***AND***
  - $V_{(SYS)} > V_{LOW\_SYS}$ ***AND***
  - V2V2 > UVLO
- **Scenario 2**: If $V_{(SYS)}$ and V2V2 drop below the UVLO threshold before or after the transition to the SLEEP state, the part will go to the power off state. If battery is re-inserted and the part enters the SLEEP state in the first power cycle, it was in the SLEEP state until the MPL timer (programmed to 1 second) expires. After 1 second, the part will exit from SLEEP if the following conditions are met:
  - V_{BAT} is greater than the voltage present on the COMP pin ***AND***
  - $V_{(SYS)} > V_{LOW\_SYS}$ ***AND***
  - V2V2 > UVLO

EXITING THE SLEEP STATE USING THE RESUME PIN: The figure below shows the timing relationship needed on the RESUME pin to exit the sleep mode. This applies for all cases where the sleep mode entry was triggered by any event other than a thermal fault.

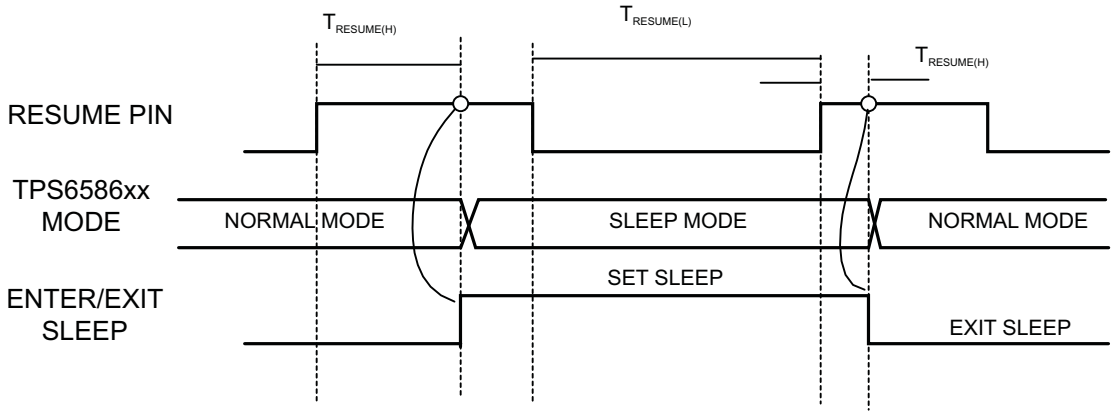


Figure 3-6. Entering and Exiting Sleep Mode Resume

EXITING THE SLEEP STATE USING AUTOBOOT: With the AUTOBOOT feature enabled, the TPS658621D will transition from SLEEP state to normal state upon power-up if the following conditions are met:

- AC/USB detected
- $V_{(SYS)} > V_{LOW\_SYS}$

REBOOT REQUEST: The REBOOT REQUEST state is entered from the NORMAL state. It can be set via software (SOFT_RST set to **1**, register 0x14 Bit B0) or by a V_{IL} level detection at $\overline{\text{HOTRST}}$ pin. When the reboot request state is set an internal timer T_{WAIT} (10ms typ) is started, and the $\overline{\text{NOPOWER}}$ pin is pulled to ground. The reboot request ends when $t > T_{WAIT}$. The REBOOT REQUEST will transition the device state machine to the HARD REBOOT state. The REBOOT REQUEST is set if the $\overline{\text{HOTRST}}$ low pulse width is greater than 10µsec (typ).

The status bit COMPDET=**1** (register STAT2, address 0xBA) when the NORMAL state is entered after a reboot cycle triggered by the $\overline{\text{HOTRST}}$ pin. The status bit COMPDET=**0** when the NORMAL state is entered, after a power-up, sleep cycle or software triggered reboot cycle.

The bit COMPDET is reset to **0** when bit SPARECC0=**1**, in register SPARE2 (address 0xCC). After resetting the COMPDET bit the host needs to set SPARECC0=0 to enable detection of another reboot cycle set via the $\overline{\text{HOTRST}}$ pin.

An interrupt is generated when the TPS658629-Q1 transitions from the POWER GOOD CHECK state to the NORMAL state , COMPDET=**1** and IMASK_COMP=**0** in register INTMASK4 (address 0xB3). An interrupt request is generated after the NORMAL state is set if IMASK_COMP=**0** and COMPDET value changes from **1** to **0**.

Table 3-9. Reboot Flag Control

SPARE2 [Addr 0xCC]								Defaults in **BOLD**
Bit Number	B7	B6	B5	B4	B3	B2	B1	B0
Bit Name	SPARECC7	LDO6PG	SPARECC5	SPARECC4	SPARECC3	SPARECC2	SPARECC1	SPARECC0
Function	SPARE	SECONDARY LDO6PG MASK	SPARE	SPARE	SPARE	SPARE	SPARE	RESET REBOOT BY HOTRST STATUS BIT
When 0	NOT USED	UNMASKED	NOT USED	NOT USED	**NOT USED**	**NOT USED**	**NOT USED**	**DO NOT RESET**
When 1	**NOT USED**	**MASKED**	**NOT USED**	**NOT USED**	NOT USED	NOT USED	NOT USED	RESET

HARD REBOOT: The HARD REBOOT state powers down all the TPS658629-Q1 supplies, with exception of the RTC_OUT LDO.

3.26 $C_{NOPOWER}$ CAPACITOR DISCHARGE

The external capacitor connected to the TNOPOWER pin is always discharged when the sequencer sets $\overline{\text{NOPOWER}}$=LO in the following states: POWER-UP, RTC, REBOOT REQUEST, HARD REBOOT and SLEEP. For large capacitance values (above 330nF) the external capacitor may not be fully discharged during reboot cycles, and as a result the $\overline{\text{NOPOWER}}$ pulse width may be slightly reduced when compared to the value indicated in the parametric tables.

3.27 SEQUENCER STATUS

Sequencer status information is available at registers 0xBA, bit COMPDET and register 0xBB bits SLEEPREQ and RESUME. See STATUS REGISTERS section for functional description of these bits.

3.28 SUPPLY SEQUENCING AND HOST INTERFACE

3.28.1 Integrated Supply Sequencing

The TPS658629-Q1 enables the implementation of complex supply sequencing. With the exception of RTC_OUT, the integrated power-up sequencing starts when the TPS658629-Q1 state machine enters the SUPPLYSEQ state. The RTC_OUT LDO is always enabled in the RTC state, which occurs before the SUPPLYSEQ state, and the output of this LDO can be used to power an external processor or circuitry in systems where the supply sequencing is controlled externally using pins SM0EN, SM1EN or SYNCEN.

Each supply rail is controlled by a combination of its default status (ON or OFF), its assigned sequencing trigger group (INTERNAL, SM0EN, SM1EN or SYNCEN), and a delay time.

The default status (ON or OFF) of each rail is shown in Table 3-10.

If the default for a supply rail is ON the trigger group associated to the supply determines the control signal that initiates the delay time to the start of the rail power up. There are four trigger groups, one internal and three external pins:

INTERNAL This group is controlled by an internal signal that goes high when the TPS658629-Q1 goes from the RTC_ON state to the SUPPLYSEQ state.

SM0EN This group is controlled by the falling edge of the SM0EN pin and starts when the pin voltage is below its V_{IL} level.

SM1EN This group is controlled by the rising edge of the SM1EN pin and starts when the pin voltage is above its V_{IH} level.

SYNCEN This group is controlled by the rising edge of the SYNCEN pin and starts when the pin voltage is above its V_{IH} level.

The trigger group of each rail and its associated delay is shown in Table 3-10. If a supply rail has a default state of ON and the appropriate trigger is high, the rail will be turned on after the delay time for that rail has expired. The delay time starts when the trigger signal for that supply has gone high, while SUPPLYSEQ state is set. No delays are available after NORMAL mode is set.

Table 3-10. TPS658629 Integrated Supply Power-Up Defaults

TPS658629 SETTINGS				
SUPPLY	**DEFAULT STATE**	**DEFAULT VOLTAGE**	**TRIGGER**	**DELAY**
LDO0	OFF	1.2V	SYNCEN	3.75ms Value applies to LDO0, LDO1
LDO1	ON	1.1V	INTERNAL	
LDO2	ON	1.2V	INTERNAL	2.5ms Value applies to LDO2, LDO3
LDO3	OFF	3.3V	SYNCEN	

Table 3-10. TPS658629 Integrated Supply Power-Up Defaults (continued)

TPS658629 SETTINGS				
SUPPLY	**DEFAULT STATE**	**DEFAULT VOLTAGE**	**TRIGGER**	**DELAY**
LDO4	ON	1.8V	INTERNAL	15ms
LDO6	OFF	2.85V	SYNCEN	15ms Value applies to LDO6, LDO7 and LDO8
LDO7	OFF	3.3V	SYNCEN	
LDO8	OFF	1.8V	SYNCEN	
LDO5	OFF	2.85V	SYNCEN Trigger applies to both LDO5 and LDO9	2.5ms Value applies to LDO5, LDO9
LDO9	ON	2.85V		
SM0	ON	1.2V	SM0EN	3.75ms
SM1	OFF	1.050V	SM1EN	3.75ms
SM2	ON	3.3V	INTERNAL	0ms

3.29 INTEGRATED SUPPLY SEQUENCING – SUPPLY ENABLE CONTROL

The ON or OFF mode for each supply is defined by the supply enable RAM control bits and enable pins SM0EN, SM1EN and LDO4EN. The supply enable bits are located in registers SUPPLYENA, SUPPLYENB, SUPPLYENC, SUPPLYEND, SUPPLYENE (see supply functional description for more details). The functionality of the RAM bits and enable pins is dependent on the state set in the state machine as follows:

When the NORMAL state is NOT set : The pins SM1EN , SM0EN and LDO4EN will always control the ON or OFF modes for all supplies that use them as triggers. The supply enable RAM bits will control the ON or OFF modes for the supplies.

When the NORMAL state is set: The supply enable RAM bits will always control the ON or OFF modes for the supplies. The pins SM1EN, SM0EN and LDO4EN may control the ON or OFF modes for supplies SM1, SM0 and LDO4. The enable pins do not control the ON or OFF modes of any other supplies.

During sequencing, the following RAM bits control the supply ON/OFF mode: LDO2 RAM bits, LDO4 RAM bits, SM0 RAM bits and SM1 RAM bits.

When the NORMAL mode is set, SM0EN controls the SM0 ON/OFF mode, SM1EN controls the SM1 ON/OFF mode and LDO4EN controls the LDO4 ON/OFF mode.

3.30 INTEGRATED SUPPLY SEQUENCING – POWER-DOWN

To start a power down sequence the SLEEP REQUEST or REBOOT REQUEST states must be set. Once one of those two states is set the trigger pins are active again and they will control the ON/OFF state of the supplies associated with that trigger group. The device will enter the SLEEP or HARD REBOOT state 10ms after the SLEEP REQUEST or REBOOT REQUEST is initiated. Any supply still active when the SLEEP or HARD REBOOT state is entered will be immediately disabled. This is the default turn off condition for any supply associated with the INTERNAL sequencing trigger group.

For example, if a supply has a default state of OFF and it has SM1EN as the selected factory trigger: this supply will not power up during the SUPPLYSEQ state when SM1EN goes high. If it is enabled during the NORMAL state and is still enabled when the SLEEP REQUEST or REBOOT REQUEST states are entered, this supply will be turned off on the falling edge of SM1EN as this is its assigned trigger group programmed at the factory.

If LDO4EN is set LO by the host when the TPS658629-Q1 enters the SLEEP REQUEST or REBOOT REQUEST states, the LDO4 supply will turn off only when the HARD REBOOT or SLEEP states are set. The LDO4PG pin will be pulled low when LDO4EN is below V_{IL}, with no delay.

All the supplies are turned off at the same time when the TPS658629-Q1 enters the SLEEP or HARD REBOOT state.

3.31 HOST INTERFACE PINS

The TPS658629-Q1 devices have multiple signals that can be used by the external system to execute power sequencing operations or verify the system status. Those signals are generated as follows:

1. Power supply status (2V2 logic level) : SM0PG, SM1PG, LDO4PG – A HI level indicates that the supply is on and the regulation voltage is valid. A LO level indicates either that the supply voltage is out of regulation or that the supply has been disabled.
2. External system and host control (V32K pin logic level): The $\overline{\text{NOPOWER}}$, $\overline{\text{NORTC}}$, and OUT32K pins may be used to interface to external hosts, controlling the host reset and executing host-controlled power-up sequencing.

3.32 EXTERNAL 32 kHz

The TPS658629-Q1 outputs a 32 kHz clock (pin OUT32K) that can be used by the external system. The OUT32K output starts when the $\overline{\text{NORTC}}$ pin is above V_{IH} and V32K is valid. The 32 kHz can be derived either from an internal 32kHz oscillator or from a crystal-based clock, selectable via I^2C using bit 6 of the RTC_CTRL (Addr 0xC0) register (see the Real Time Clock section). However, only the crystal-based clock is output to the OUT32K pin.

3.33 SUPPLY INPUT PIN CONNECTION

The input pins for all supplies (VIN_LDO01, VIN_LDO23, VIN_LDO4, VIN_LDO678, VIN_LDO9) enable optimization of the overall system power architecture by connecting lower output voltage supplies to intermediate rails or external rails. Care must be taken to ensure that the input pin for each integrated supply is powered when the supply is enabled during the power-up sequencing. Failure to do so will result in a power good fault detection with a potential lock-up situation. The input pins VIN_SM0, VIN_SM1, VIN_SM2 must be connected to the SYS pin

3.34 HOST INTERFACE

The TPS658629-Q1 may be used in systems where the sequencing is controlled by an external host or housekeeping circuit, as well as in systems where stand-alone sequencing is a requirement. For host controlled systems the RTC_OUT LDO can be used as the supply that powers the external sequencing control and the $\overline{\text{NOPOWER}}$ and $\overline{\text{NORTC}}$ pin signals are used as resets for the external circuit.

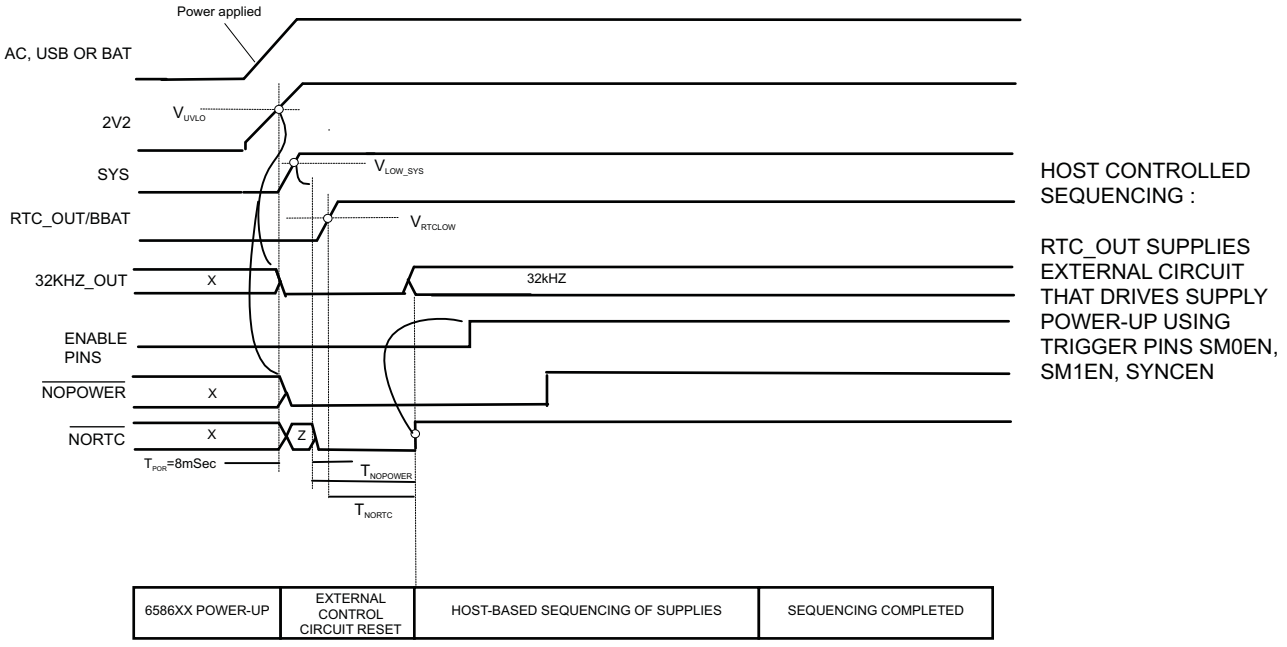
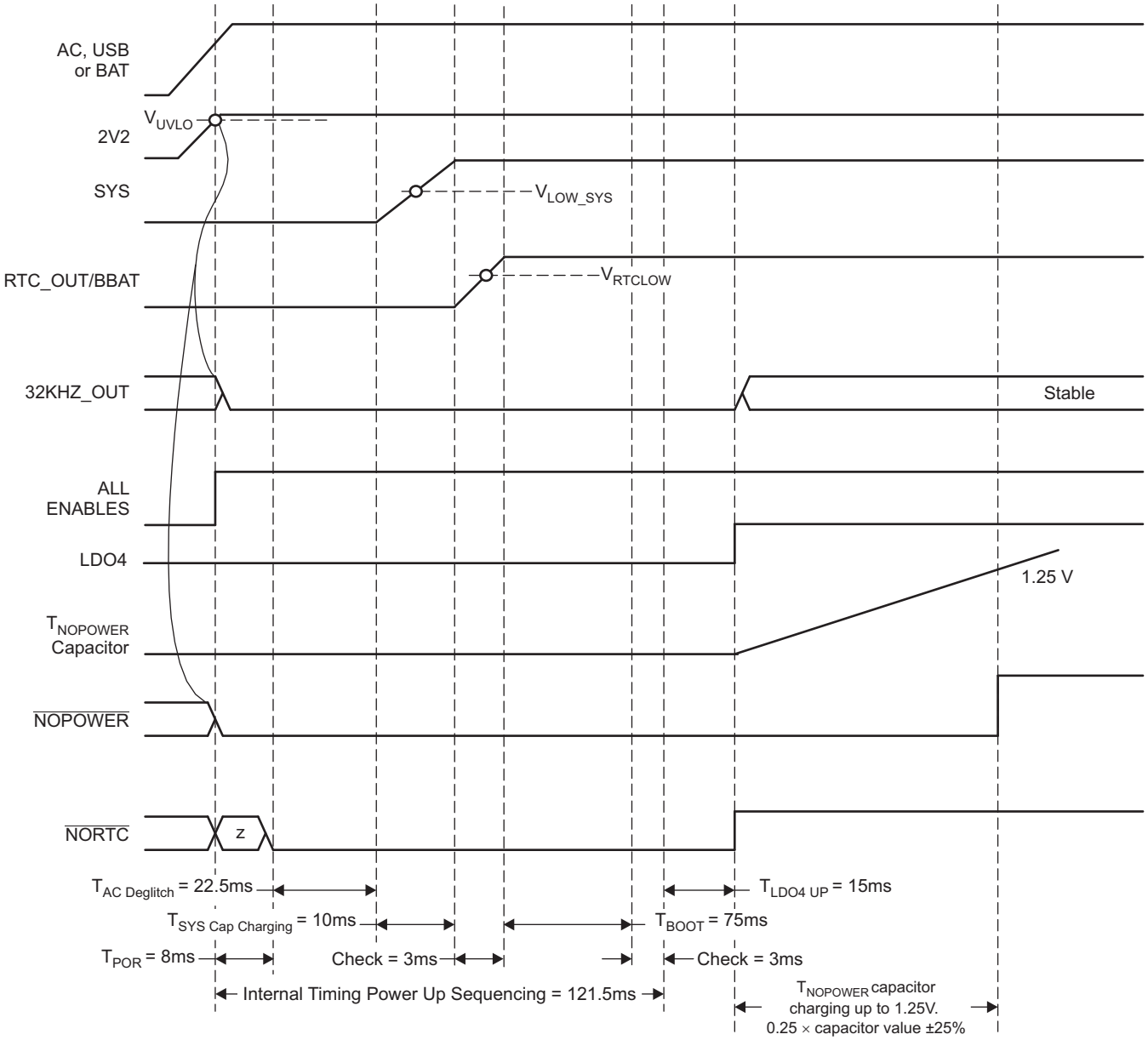


Figure 3-7. Host Controlled Startup



NOTE: For the 32kHz clock to stabilize by 320ms, the T_{NOPWER} capacitor should be greater than (185ms/0.25)nF.

Figure 3-8. TPS658629-Q1 Controlled Startup

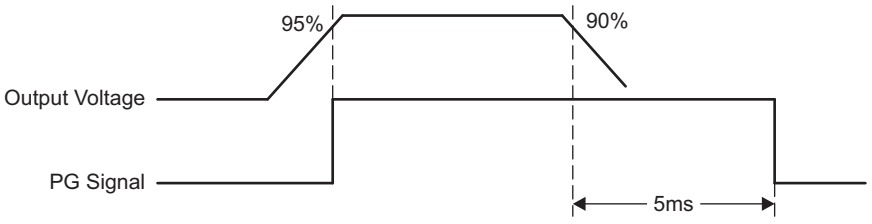


Figure 3-9. Power Good Timing

3.35 INTEGRATED SUPPLIES – ENABLE CONTROL, DVM CONTROL

3.35.1 DVM and Non-DVM Supplies

The TPS658629-Q1 has two types of voltage control for the integrated supplies:

1. DVM supplies: SM0, SM1, LDO2 and LDO4 are DVM supplies with dedicated register sets that enable a controlled transition from an initial voltage to a final voltage. The initial voltage, final voltage, and voltage transition start time are set via I^2C. SM0 and SM1 have I^2C programmable slew rate.
2. NON-DVM supplies: LDO0, LDO1, LDO3, LDO5, LDO6, LDO7, LDO8, LDO9, SM2 and RTC_OUT outputs can be changed, but without slew rate and transition start time control. The output of these supplies will be changed to the new value as soon as TPS658629-Q1 sends the ACK of the I^2C command setting the new output voltage.

3.35.2 DVM and Non-DVM Supply Enable

All the integrated supplies can be turned on/off by RAM enable bits. All the supplies (with exception of LDO5, LDO9 and RTC_OUT LDO's) have two enable bits on distinct registers (registers 0x10, 0x11, 0x12, 0x13, 0x14). A supply will be enabled when ANY of its enable bits, in the registers below, are set to **1**. Each supply will be disabled when ALL of the enable bits for that supply are set to **0**. For example: SM0 enabled: SM0_ENA=**1** ***OR*** SM0_ENB=**1**, SM0 disabled: SM0_ENA=**0** ***AND*** SM0_ENB=**0**

Table 3-11. SM0-2, LDO0-9 Control

SUPPLYENA [Addr 0x10]							Defaults in **BOLD**	
Bit Number	B7	B6	B5	B4	B3	B2	B1	B0
Bit Name	RSVD107	RSVD106	RSVD105	RSVD104	LDO2_ENA1	LDO2_ENA0	SM0_ENA	SM1_ENA
Function	**NOT USED**	**NOT USED**	**NOT USED**	**NOT USED**	LDO2 CONTROL	LDO2 CONTROL	SM0 CONTROL	SM1 CONTROL
SUPPLYENB [Addr 0x11]							Defaults in **BOLD**	
Bit Number	B7	B6	B5	B4	B3	B2	B1	B0
Bit Name	RSVD117	RSVD116	RSVD115	RSVD114	LDO2_ENB1	LDO2_ENB0	SM0_ENB	SM1_ENB
Function	**NOT USED**	**NOT USED**	**NOT USED**	**NOT USED**	LDO2 CONTROL	LDO2 CONTROL	SM0 CONTROL	SM1 CONTROL
SUPPLYENC [Addr 0x12]								
Bit Number	B7	B6	B5	B4	B3	B2	B1	B0
Bit Name	SM2_ONC	LDO8_ONC	LDO7_ONC	LDO6_ONC	LDO4_ONC	LDO3_ONC	LDO1_ONC	LDO0_ONC
Function	SM2 CONTROL	LDO8 CONTROL	LDO7 CONTROL	LDO6 CONTROL	LDO4 CONTROL	LDO3 CONTROL	LDO1 CONTROL	LDO0 CONTROL
SUPPLYEND [Addr 0x13]								
Bit Number	B7	B6	B5	B4	B3	B2	B1	B0
Bit Name	SM2_OND	LDO8_OND	LDO7_OND	LDO6_OND	LDO4_OND	LDO3_OND	LDO1_OND	LDO0_OND
Function	SM2 CONTROL	LDO8 CONTROL	LDO7 CONTROL	LDO6 CONTROL	LDO4 CONTROL	LDO3 CONTROL	LDO1 CONTROL	LDO0 CONTROL
SUPPLYENE [Addr 0x14]							Defaults in **BOLD**	
Bit Number	B7	B6	B5	B4	B3	B2	B1	B0
Bit Name	LDO9_ON	LDO5_ON	SYSINEN	HOTDLY	SLEEP MODE	RSVD	EXITSLREQ	SOFT RST
Function	LDO9 ON/OFF CONTROL	LDO5 ON/OFF CONTROL	SYS_IN LOW VOLTAGE SETS SLEEP MODE	HOT RESET DEGLITCH	SET TPS658629-Q1 IN SLEEP MODE		SLEEP REQUEST EXIT CONTROL	SOFTWARE RESET CONTROL
When 0	OFF	OFF	DISABLED	**5µsec min, 16µsec max**	**NOT ACTIVE**		**GO TO SLEEP at T>Twait**	**NOT ACTIVE**

Table 3-11. SM0-2, LDO0-9 Control (continued)

When 1	ON	ON	**ENABLED**	5ms	SET SLEEP		FORCE TRANSITION TO NORMAL STATE	REBOOT REQUEST

LDO5 and LDO9 will be turned on when LDO5_ON is **1** or LDO9_ON is **1**, respectively. The RTC_OUT LDO enable bits are located in the RTC control register, see real time clock section for details.

The supply enable defaults are unique for each device. See App Notes for device specific settings.

3.35.3 DVM Supplies - Voltage Transition Control

The output voltage for the DVM supplies can be set to one of the values programmed in the voltage setting registers SM0V1, SM0V2, SM1V1, SM2V2, LDO2AV1, LDO2AV2, LDO2BV1, LDO2BV2, LDO4V1 and LDO4V2 as defined in registers VCC1 and VCC2.

The voltage change for the DVM supplies is usually done with 2 I^2C write commands:

1. The host writes the new voltage to the voltage setting register for the supply(s) that will have an output voltage modification.
2. The voltage change starts by setting specific control bits in registers VCC1 and VCC2.

Bits $\overline{VS}$ in registers VCC1 and VCC2 select the next voltage for the DVM supplies. A voltage change is started when ANY of the $\overline{GO}$ bits for the supply is set to **1**. At the end of the voltage transition the GO bits are cleared by the internal logic.

Table 3-12. DVM Supply Control

VCC1 [Addr 0x20]								Defaults in **BOLD**
Bit Number	B7	B6	B5	B4	B3	B2	B1	B0
Bit Name	LDO4VS	LDO4GO	LDO2AVS2	LDO2AGO2	SM0VS1	SM0GO1	SM1VS1	SM1GO1
Function	LDO4 VOLTAGE SELECTION		LDO2 VOLTAGE SELECTION		SM0 VOLTAGE SELECTION		SM1 VOLTAGE SELECTION	
When 0	**SELECT VOLTAGE SET BY LDO4V1**	**HOLD CURRENT VOLTAGE**	**NOT USED**	**HOLD CURRENT VOLTAGE**	**SELECT VOLTAGE SET BY SM0V1**	**HOLD CURRENT VOLTAGE**	**SELECT VOLTAGE SET BY SM1V1**	**HOLD CURRENT VOLTAGE**
When 1	SELECT VOLTAGE SET BY LDO4V2	RAMP TO VOLTAGE SELECTED BY LDO4VS	NOT USED	RAMP TO VOLTAGE SELECTED BY LDO2BVS1	SELECT VOLTAGE SET BY SM0V2	RAMP TO VOLTAGE SELECTED BY SM0VS1	SELECT VOLTAGE SET BY SM1V2	RAMP TO VOLTAGE SELECTED BY SM1VS1
VCC2 [Addr 0x21]								Defaults in **BOLD**
Bit Number	B7	B6	B5	B4	B3	B2	B1	B0
Bit Name	LDO2BVS1	LDO2BGO1	LDO2AVS1	LDO2AGO1	SM0VS2	SM0GO2	SM1VS2	SM1GO2
Function	LDO2 VOLTAGE SELECTION		LDO2 VOLTAGE SELECTION I		SM0 VOLTAGE SELECTION		SM1 VOLTAGE SELECTION	
When 0	**SELECT VOLTAGE SET BY LDO2BV1**	**HOLD CURRENT VOLTAGE**	**NOT USED**	**HOLD CURRENT VOLTAGE**	**SELECT VOLTAGE SET BY SM0V1**	**HOLD CURRENT VOLTAGE**	**SELECT VOLTAGE SET BY SM1V1**	**HOLD CURRENT VOLTAGE**
When 1	SELECT VOLTAGE SET BY LDO2BV2	RAMP TO VOLTAGE SELECTED BY LDO2BVS1	NOT USED	RAMP TO VOLTAGE SELECTED BY LDO2BVS1	SELECT VOLTAGE SET BY SM0V2	RAMP TO VOLTAGE SELECTED BY SM0VS2	SELECT VOLTAGE SET BY SM1V2	RAMP TO VOLTAGE SELECTED BY SM1VS2

Table 3-13. SM0 and SM1 Voltage Selection Register Settings

SM0 OUTPUT VOLTAGE SELECTION				SM1 OUTPUT VOLTAGE SELECTION		
SM0VS1	SM0VS2	SM0GO1=1 OR SM0GO2=1 STARTS VOLTAGE TRANSITION TO VALUE SET BY REGISTER :		SM1VS1	SM1VS2	SM1GO1=1 OR SM1GO2=1 STARTS VOLTAGE TRANSITION TO VALUE SET BY REGISTER
0	0	SM0V1		0	0	SM1V1
0	1	SM0V2		0	1	SM1V2
1	0	SM0V2		1	0	SM1V2
1	1	SM0V2		1	1	SM1V2

Table 3-14. SM0 Voltage Selection by SM0EN

SM0 ACTIVE LEVEL	SM0EN	SM0 OUTPUT VOLTAGE
0	0	1.2V
0	1	OFF

The SM0 output voltage value and transition is controlled by the SM0EN pin and SM0VS1/SMVS2.

NOTE

During a HI to LO transition of SM0EN (enabling SM0), the SM0 output will power up to the pre-defined default state regardless of the setting set via I^2C prior to SM0 being disabled.

Table 3-15. SM0 Output Voltage Settings Available for SM0EN Selection

RANGE	[4:0]	VOUT (V)	[4:0]	VOUT (V)	[4:0]	VOUT (V)	[4:0]	VOUT (V)
0.725V–1.50V	00000	0.725	01000	0.925	10000	1.125	11000	1.325
	00001	0.750	01001	0.950	10001	1.150	11001	1.350
	00010	0.775	01010	0.975	10010	1.175	11010	1.375
	00011	0.800	01011	1.000	**10011**	**1.200**	11011	1.400
	00100	0.825	01100	1.025	10100	1.225	11100	1.425
	00101	0.850	01101	1.050	10101	1.250	11101	1.450
	00110	0.875	01110	1.075	10110	1.275	11110	1.475
	00111	0.900	01111	1.100	10111	1.300	11111	1.500

Table 3-16. LDO4 Voltage Selection Register Settings

LDO4 OUTPUT VOLTAGE SELECTION	
LDO4VS	LDO4GO=1 STARTS VOLTAGE TRANSITION TO VALUE SET BY REGISTER
0	LDO4V1
1	LDO4V2

The LDO2 output voltage selection and GO bit functionality is shown below.

1. LDO2AGOn bits are not active
2. LDO2BGO1=1 starts a voltage transition to the voltage selected by LDO2BV1, LDO2BV2 and LDO2BVS1
3. LDO2 voltage transition starts when SM0EN is set to LO

When the LDO2 output voltage is controlled by the SM0EN ($\overline{\text{CORECTRL}}$) pin, registers LDO2AV2 and LDO2AV1 define the output voltage:

3.35.4 DVM Supply Voltage Transition

During a voltage transition the output voltage will be stepped from the currently programmed voltage to the new target voltage as shown below. The slew rate from the initial voltage to the final voltage for SM0 and SM1 can be selected using the I²C registers SM0SL (ADDRESS = 0x25) and SM1SL (ADDRESS = 0x28) respectively. LDO2 and LDO4 have the slew rate fixed internally to 7mV/µSec(typ).

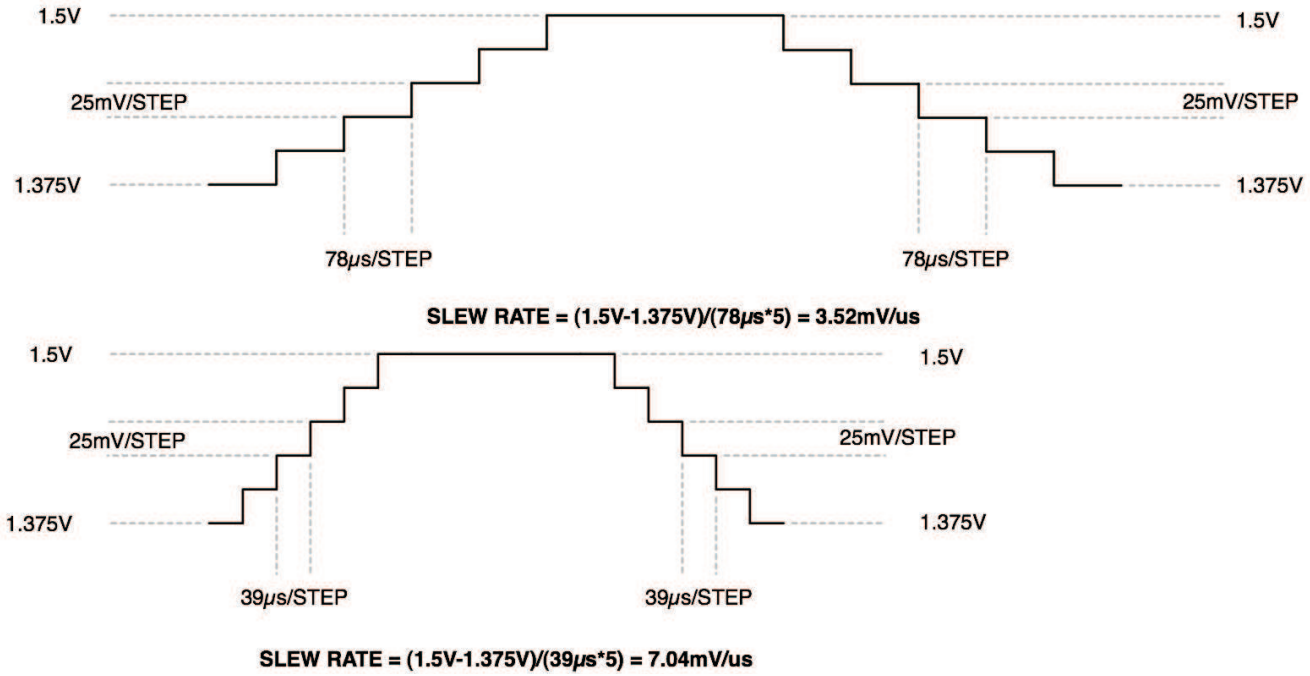


Figure 3-10. SM0 and SM1 Dynamic Voltage Slew Rate Example

3.36 SM0, SM1, SM2 CONVERTERS

The TPS658629-Q1 has three highly efficient step down synchronous converters. The integration of the power stage switching FETs reduces the external component count, and only the external output inductor and filter capacitor are required. The integrated power stage supports 100% duty cycle operation. The converters have two possible modes of operation: a 2.25MHz fixed frequency pulse width modulation (PWM) mode at moderate to heavy loads, and a pulse frequency modulation (PFM) mode at light loads. The converters SM0, SM1 and SM2 output voltages are programmable via I²C registers SMnV1 and SMnV2 (SM0 and SM1) and SUPPLYV2 (SM2):

NOTE

VIN_SM0, VIN_SM1 AND VIN_SM2 PINS SHOULD ALWAYS BE EXTERNALLY CONNECTED TO SYS PIN

3.36.1 SM0, SM1 DVM Buck Converters - Output Voltage Registers

Table 3-17. DVM Supply Voltage and Slew Rate Selection – SM0 and SM1

SM1V1 [Addr 0x23]								
Bit Number	B7	B6	B5	B4	B3	B2	B1	B0
Bit Name	RSVD237	RSVD236	RSVD235	SM1V1[4]	SM1V1[3]	SM1V1[2]	SM1V1[1]	SM1V1[0]
Function	NOT USED	NOT USED	NOT USED	SM1 SUPPLY OUTPUT VOLTAGE				
SM1V2 [Addr 0x24]								

Table 3-17. DVM Supply Voltage and Slew Rate Selection – SM0 and SM1 (continued)

Bit Number	B7	B6	B5	B4	B3	B2	B1	B0
Bit Name	RSVD247	RSVD246	RSVD245	SM1V2[4]	SM1V2[3]	SM1V2[2]	SM1V2[1]	SM1V2[0]
Function	NOT USED	NOT USED	NOT USED	SM1 SUPPLY OUTPUT VOLTAGE				
SM1SL [Addr 0x25]								
Bit Number	B7	B6	B5	B4	B3	B2	B1	B0
Bit Name	RSVD257	RSVD256	RSVD255	RSVD254	RSVD253	SM1SL[2]	SM1SL[1]	SM1SL[0]
Function	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	SM1 SUPPLY RAMP RATE		
SM0V1 [Addr 0x26]								
Bit Number	B7	B6	B5	B4	B3	B2	B1	B0
Bit Name	RSVD267	RSVD266	RSVD265	SM0V1[4]	SM0V1[3]	SM0V1[2]	SM0V1[1]	SM0V1[0]
Function	NOT USED	NOT USED	NOT USED	SM0 SUPPLY OUTPUT VOLTAGE				
SM0V2 [Addr 0x27]								
Bit Number	B7	B6	B5	B4	B3	B2	B1	B0
Bit Name	RSVD277	RSVD276	RSVD275	SM0V2[4]	SM0V2[3]	SM0V2[2]	SM0V2[1]	SM0V2[0]
Function	NOT USED	NOT USED	NOT USED	SM0 SUPPLY OUTPUT VOLTAGE				
SM0SL [Addr 0x28]								
Bit Number	B7	B6	B5	B4	B3	B2	B1	B0
Bit Name	RSVD287	RSVD286	RSVD285	RSVD284	RSVD283	SM0SL[2]	SM0SL[1]	SM0SL[0]
Function	NOT USED	NOT USED	NOT USED	NOT USED	NOT USED	SM0 SUPPLY RAMP RATE		

The available output voltages and slew rates are shown below.

Table 3-18. SM0V1[4:0] / SM0V2[4:0] / Output Voltage Settings

RANGE	[4:0]	VOUT (V)	[4:0]	VOUT (V)	[4:0]	VOUT (V)	[4:0]	VOUT (V)
0.725V–1.50V	00000	0.725	01000	0.925	10000	1.125	11000	1.325
	00001	0.750	01001	0.950	10001	1.150	11001	1.350
	00010	0.775	01010	0.975	10010	1.175	11010	1.375
	00011	0.800	01011	1.000	**10011**	**1.200**	11011	1.400
	00100	0.825	01100	1.025	10100	1.225	11100	1.425
	00101	0.850	01101	1.050	10101	1.250	11101	1.450
	00110	0.875	01110	1.075	10110	1.275	11110	1.475
	00111	0.900	01111	1.100	10111	1.300	11111	1.500

Table 3-19. SM1V1[4:0] / SM1V2[4:0] Output Voltage Settings

RANGE	[4:0]	VOUT (V)	[4:0]	VOUT (V)	[4:0]	VOUT (V)	[4:0]	VOUT (V)
0.725V–1.50V	00000	0.725	01000	0.925	10000	1.125	11000	1.325
	00001	0.750	01001	0.950	10001	1.150	11001	1.350
	00010	0.775	01010	0.975	10010	1.175	11010	1.375
	00011	0.800	01011	1.000	10011	1.200	11011	1.400
	00100	0.825	01100	1.025	10100	1.225	11100	1.425
	00101	0.850	**01101**	**1.050**	10101	1.250	11101	1.450
	00110	0.875	01110	1.075	10110	1.275	11110	1.475
	00111	0.900	01111	1.100	10111	1.300	11111	1.500

Table 3-20. SM0SL[2:0] and SM1SL[2:0] Slew Rate Settings

SMxSL [2:0]	SLEW RATE (mV/µs)	SMxSL [2:0]	SLEW RATE (mV/µs)	SMxSL [2:0]	SLEW RATE (mV/µs)	SMxSL [2:0]	SLEW RATE (mV/µs)
000	INSTANTLY	001	0.11	010	0.22	011	0.44
100	0.88	101	1.76	110	3.52	**111**	**7.04**

Table 3-21. Non-DVM supply Voltage selection - SM2, LDO8

SUPPLYV2 [Addr 0x42]								
Bit Number	B7	B6	B5	B4	B3	B2	B1	B0
Bit Name	VLDO8[2]	VLDO8[1]	VLDO8[0]	VSM2[4]	VSM2[3]	VSM2[2]	VSM2[1]	VSM2[0]
Function	LDO8 OUTPUT VOLTAGE			SM2 OUTPUT VOLTAGE				

Table 3-22. VSM2[4:0] Output Voltage Settings

RANGE	[4:0]	VOUT (V)	[4:0]	VOUT (V)	[4:0]	VOUT (V)	[4:0]	VOUT (V)
3.0V–4.55V	00000	3.000	01000	3.400	10000	3.800	11000	4.200
	00001	3.050	01001	3.450	10001	3.850	11001	4.250
	00010	3.100	01010	3.500	10010	3.900	11010	4.300
	00011	3.150	01011	3.550	10011	3.950	11011	4.350
	00100	3.200	01100	3.600	10100	4.000	11100	4.400
	00101	3.250	01101	3.650	10101	4.050	11101	4.450
	00110	3.300	**01110**	**3.700**	10110	4.100	11110	4.500
	00111	3.350	01111	3.750	10111	4.150	11111	4.550

3.36.2 PWM Operation

During PWM operation the converters use a fast response voltage mode controller scheme with input voltage feed-forward, enabling the use of small ceramic input and output capacitors. At the beginning of each clock cycle the high side channel MOSFET switch is turned on, and the oscillator starts the voltage ramp. The inductor current will ramp-up until the ramp voltage reaches the error amplifier output voltage, when the comparator trips and the high-side channel MOSFET switch is turned off. Internal adaptive break-before-make circuits turn on the integrated low-side MOSFET switch after an internal, fixed dead-time delay, and the inductor current ramps down, until the next cycle is started. When the next cycle starts the ramp voltage is reset to its low value and the high-side channel MOSFET switch is turned on again.

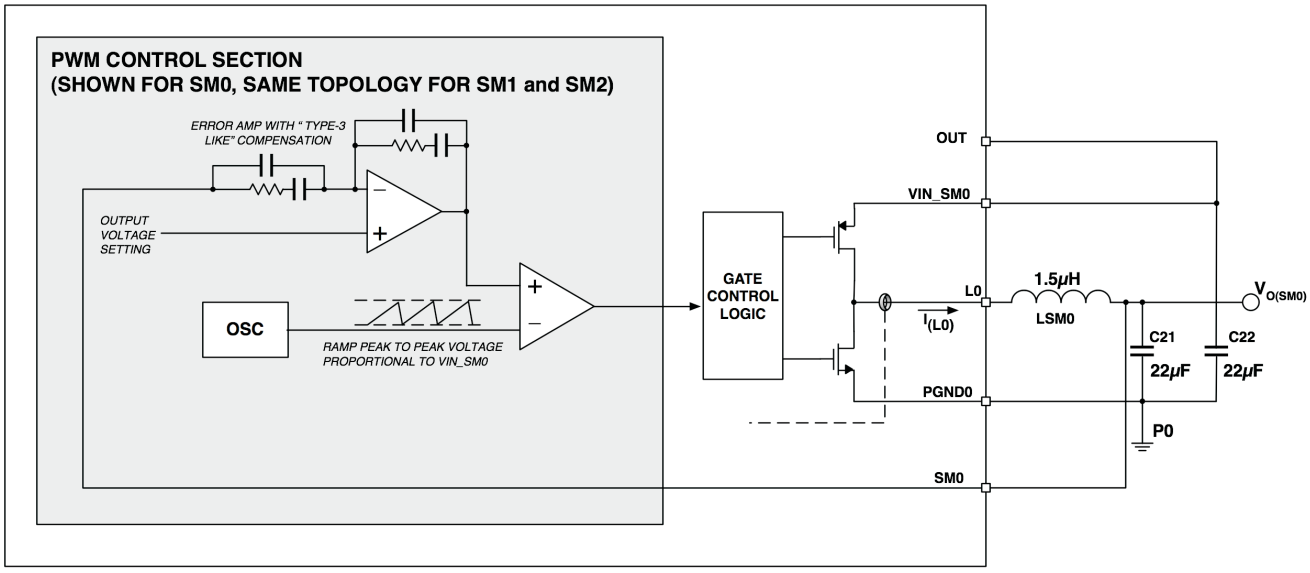


Figure 3-11. PWM Control

3.36.3 PFM Mode Operation

The TPS658629-Q1 SM0, SM1 and SM2 buck converters can be set to operate only in PWM mode or to switch automatically between PFM and PWM modes, via the I^2C interface. While in the Pulsed Frequency Mode the converters operate with reduced switching frequency and with a minimum quiescent current to maintain high efficiency.

In PFM mode the converter will regulate the output voltage to 1% above the nominal output voltage. To determine when to transition between the modes, the inductor current is monitored, and the PFM mode is set when the inductor ripple current approaches zero. For duty cycles above 85% the PFM mode is entered for load currents below the threshold IPFM(ENTER).

$$I_{PFM(ENTER)} = \frac{V_{(VIN\_SMx)}}{34\Omega} \quad (1)$$

In PFM mode the output voltage is monitored by a voltage comparator, which regulates the output voltage to the programmed value $V_{O(SM1)}$. If the output voltage is below $V_{O(SM1)}$ the PFM control circuit turns on the power stage, applying a burst of pulses to increase the output voltage. When the output voltage exceeds the target regulation voltage $V_{O(SM1)}$ the power stage is disabled, and the output voltage will drop until it is below the regulation voltage target, when the power stage is enabled again.

The PFM operation is disabled and PWM operation set if one of the following events happens during PFM operation:

1. The burst operation exceeds 7µs, typ.
2. The output voltage falls below 3% of the target regulation voltage in PFM mode (2% of the nominal output voltage in PWM mode)

3.36.4 Setting the PWM/PFM Mode

In TPS658629-Q1 the PWM mode can be forced for each converter by setting the bit SMn_PWM to 1 in the SMODE1 register. If bits SMn_GPIO is 1, the GPIO will control the PWM or PFM mode setting, and bits SMn_PWM are ignored.

Table 3-23. SM0,SM1, SM2 PWM/PFM Mode Selection

SMODE1 [Addr 0x47]								Default to 0
Bit Number	B7	B6	B5	B4	B3	B2	B1	B0
Bit Name	RSVD477	SM2_GPIO	SM1_GPIO	SM0_GPIO	RSVD473	SM2_PWM	SM1_PWM	SM0_PWM
Function	SPARE	SM2 AUTO PFM CONTROL SELECTION	SM1 AUTO PFM CONTROL SELECTION	SM0 AUTO PFM CONTROL SELECTION	SPARE	SM2 PWM MODE ON	SM1 PWM MODE ON	SM0 PWM MODE ON

Table 3-24 details how the GPIO control is implemented. Note that the GPIO1 polarity indicated in Table 3-24 is controlled by bit GPIOINV, register 0x5E.

Table 3-24. GPIO1 PWM/PFM Mode Control

SMx_GPIO	SMx_PWM	GPIO1 POLARITY	GPIO1	CONVERTER MODE
0	0	x	x	Auto PWM/PFM
0	1	x	x	PWM Only
1	x	Inverted	0	PWM Only
1	x	Inverted	1	Auto PWM/PFM
1	x	Not Inverted	0	Auto PWM/PFM
1	x	Not Inverted	1	PWM Only

3.36.5 Output Discharge Switches

When the SM0, SM1 and SM2 converters are disabled, an integrated switch automatically discharges the converter output capacitor.

The converter output discharge switches are always enabled when NORMAL state is set and during the SUPPLYSEQ state.

3.36.6 Dynamic Voltage Positioning

This feature reduces the voltage under/overshoots at load steps from light to heavy load and vice versa. It provides more headroom for both the voltage drop at a load step and the voltage increase at a load throw-off. This improves load transient behavior.

At light loads, in which the converter operate in PFM Mode, the output voltage is regulated typically 1% higher than the nominal value. In case of a load transient from light load to heavy load, the output voltage will drop until it reaches the COMP LOW threshold set to 2% below the nominal value and enters PWM mode. During a load throw off from heavy load to light load, the voltage overshoot is also minimized due to active regulation turning on the low-side channel switch.

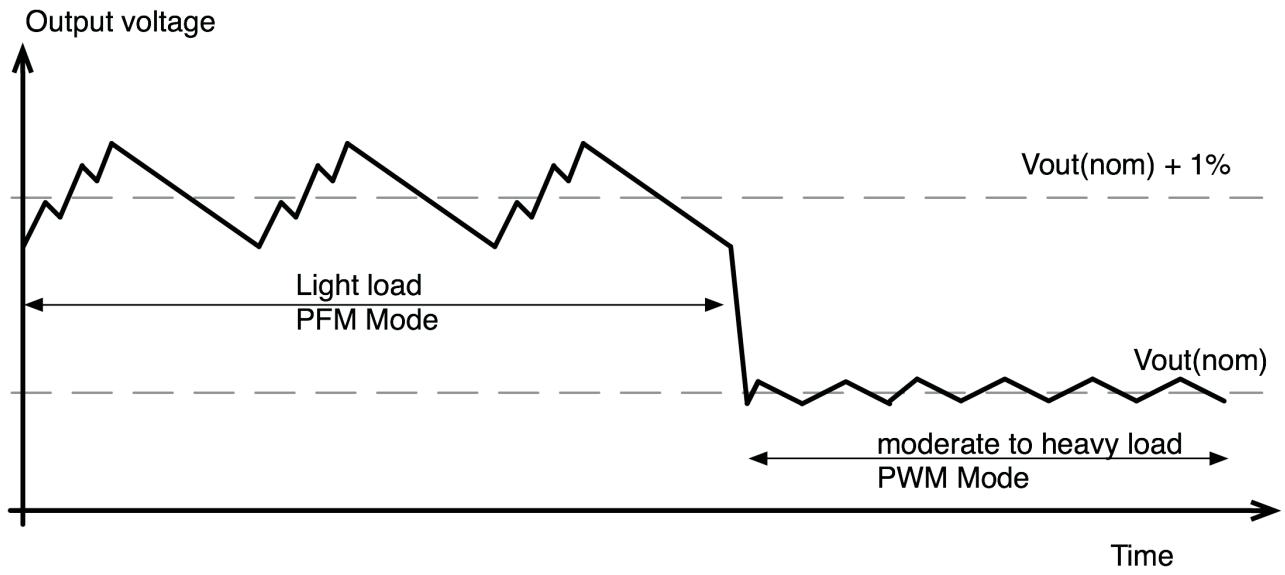


Figure 3-12. Voltage Positioning

3.36.7 Soft Start

SM0, SM1 and SM2 have an internal soft start circuit that limits the inrush current during start-up. An initial delay (170µs typ) from the converter enabled command to the converter effectively being operational is required to ensure that the internal circuits of the converter are properly biased. At the end of that initial delay the soft start is initiated and the internal compensation capacitor is charged with a low value current source. The soft start time is typically 250µs, with the output voltage ramping from 5% to 95% of the final target value.

3.36.8 Dropout Operation at 100% Duty Cycle

The TPS658629-Q1 buck converters offer a low input to output voltage difference while still maintaining operation when the duty cycle is set to 100%. In this mode of operation the high-side FET is constantly turned on to enable operation with a low input voltage. The dropout operation will start if :

$$V_{(VIN\_SMx)} \leq V_{(SMx)} + I_{Lx} \times (R_{DSON(PSMx)} + R_L) \quad (2)$$

where I_{Lx} is the output current plus ½ inductor ripple current and R_L is the DC resistance of the inductor.

3.36.9 Output Voltage Monitoring

The output voltage of converters SM0, SM1 and SM2 is monitored by internal comparators, and an output low voltage condition is detected when the output voltage is below 90% of the programmed value. The power good comparator is disabled for all converters during output voltage transitions. The power comparator on SM2 power good is also disabled when battery tracking mode is set.

3.36.10 Phase Control in PWM Mode

By default the SM0, SM1 and SM2 converters operate with phased clocking when they are in PWM mode, with converter SM0 as the master. Converters SM0 and SM1, when enabled, will run 90 and 180 degrees out of phase with SM0.

3.36.11 Integrated Snubber and Current Limit

The SM2 converter has an integrated electronic snubber that is used to improve transient response when operating under conditions which cause the inductor current to flow in the negative direction (into the Ln node).

3.37 LINEAR REGULATORS

The TPS658629-Q1 offers ten integrated linear dropout regulators (LDOs), designed to be stable over the operating load range with use of external ceramic capacitors. The output voltage can be programmed via I^2C. All of the LDOs, with the exception of LDO5 and RTC_OUT LDO, have uncommitted input power supply pins (VIN_LDO01, VIN_LDO23, VIN_LDO4, VIN_LDO678, VIN_LDO9) which should be externally connected to a number of system rails including SYS and the output of SM2.

The LDO5 and RTC_OUT regulators are internally connected to the SYS pin.

3.37.1 Output Voltage Monitoring

Internal power good comparators monitor the LDO outputs and detect when the output voltage is below 95% of the programmed value. This information is used by the TPS658629-Q1 to generate interrupts or to trigger distinct operating modes, depending on specific I^2C register settings. See interrupt and sequencing controller section for additional details.

3.37.2 LDO2 DVM LDO - Output Voltage Registers

Registers 0x29, 0x2A, 0x2F and 0x30 set the output voltage for LDO2. The slew rate is internally fixed to 7mV/µSec (typ).

Table 3-25. DVM Supply Voltage Selection – LDO2

LDO2AV1 [Addr 0x29]								Defaults in **BOLD**
Bit Number	B7	B6	B5	B4	B3	B2	B1	B0
Bit Name	RSVD297	RSVD296	RSVD295	LDO2AV1[4]	LDO2AV1[3]	LDO2AV1[2]	LDO2AV1[1]	LDO2AV1[0]
Function	**NOT USED**	**NOT USED**	**NOT USED**	LDO2 SUPPLY OUTPUT VOLTAGE (See Table 3-26)				
LDO2AV2 [Addr 0x2A]								Defaults in **BOLD**
Bit Number	B7	B6	B5	B4	B3	B2	B1	B0
Bit Name	RSVD2A7	RSVD2A6	RSVD2A5	LDO2AV2[4]	LDO2AV2[3]	LDO2AV2[2]	LDO2AV2[1]	LDO2AV2[0]
Function	**NOT USED**	**NOT USED**	**NOT USED**	LDO2 SUPPLY OUTPUT VOLTAGE (See Table 3-26)				
LDO2BV1 [Addr 0x2F]								Defaults in **BOLD**
Bit Number	B7	B6	B5	B4	B3	B2	B1	B0
Bit Name	RSVD2F7	RSVD2F6	RSVD2F5	LDO2BV1[4]	LDO2BV1[3]	LDO2BV1[2]	LDO2BV1[1]	LDO2BV1[0]
Function	**NOT USED**	**NOT USED**	**NOT USED**	LDO2 SUPPLY OUTPUT VOLTAGE (See Table 3-26)				
LDO2BV2 [Addr 0x30]								Defaults in **BOLD**
Bit Number	B7	B6	B5	B4	B3	B2	B1	B0
Bit Name	RSVD307	RSVD306	RSVD305	LDO2BV2[4]	LDO2BV2[3]	LDO2BV2[2]	LDO2BV2[1]	LDO2BV2[0]
Function	**NOT USED**	**NOT USED**	**NOT USED**	LDO2 SUPPLY OUTPUT VOLTAGE (See Table 3-26)				

The available output voltages for LDO2 are shown below:

Table 3-26. LDO2AV1/2[4:0] and LDO2BV1/2[4:0] Settings

RANGE	**[4:0]**	**VOUT (V)**	**[4:0]**	**VOUT (V)**	**[4:0]**	**VOUT (V)**	**[4:0]**	**VOUT (V)**
0.725V–1.50V	00000	0.725	01000	0.925	10000	1.125	11000	1.325
	00001	0.750	01001	0.950	10001	1.150	11001	1.350
	00010	0.775	01010	0.975	10010	1.175	11010	1.375
	00011	0.800	01011	1.000	**10011**	**1.200**	11011	1.400
	00100	0.825	01100	1.025	10100	1.225	11100	1.425
	00101	0.850	01101	1.050	10101	1.250	11101	1.450
	00110	0.875	01110	1.075	10110	1.275	11110	1.475
	00111	0.900	01111	1.100	10111	1.300	11111	1.500

3.37.3 LDO4 DVM LDO – Output Voltage Registers

Registers 0x32 and 0x33 set the output voltage for LDO4. The slew rate is internally fixed to 7mV/µSec (typ).

Table 3-27. DVM Supply Voltage Selection – LDO4

LDO4V1 [Addr 0x32]								
Bit Number	B7	B6	B5	B4	B3	B2	B1	B0
Bit Name	RSVD327	RSVD326	RSVD325	LDO4V1[4]	LDO4V1[3]	LDO4V1[2]	LDO4V1[1]	LDO4V1[0]
Function	NOT USED	NOT USED	NOT USED	LDO4 SUPPLY OUTPUT VOLTAGE (See Table 3-28)				
LDO4V2 [Addr 0x33]								
Bit Number	B7	B6	B5	B4	B3	B2	B1	B0
Bit Name	RSVD337	RSVD336	RSVD335	LDO4V2[4]	LDO4V2[3]	LDO4V2[2]	LDO4V2[1]	LDO4V2[0]
Function	NOT USED	NOT USED	NOT USED	LDO4 SUPPLY OUTPUT VOLTAGE (See Table 3-28)				

The available output voltages are shown below:

Table 3-28. LDO4V1[4:0] and LDO4V2[4:0] Output Voltage Settings

RANGE	[4:0]	VOUT (V)	[4:0]	VOUT (V)	[4:0]	VOUT (V)	[4:0]	VOUT (V)
1.7V–2.475V	00000	1.700	01000	1.900	10000	2.100	11000	2.300
	00001	1.725	01001	1.925	10001	2.125	11001	2.325
	00010	1.750	01010	1.950	10010	2.150	11010	2.350
	00011	1.775	01011	1.975	10011	2.175	11011	2.375
	00100	**1.800**	01100	2.000	10100	2.200	11100	2.400
	00101	1.825	01101	2.025	10101	2.225	11101	2.425
	00110	1.850	01110	2.050	10110	2.250	11110	2.450
	00111	1.875	01111	2.075	10111	2.275	11111	2.475

3.37.4 LDO Output Discharge Switches

All LDO's, with exception of RTC_OUT LDO, have internal discharge resistors that are connected to ground via internal switches when the LDO is turned OFF, thus discharging the output capacitor.

The LDO output discharge switches are always enabled when NORMAL state is set and during the SUPPLYSEQ state.

3.37.5 Non-DVM Supply Voltage Settings

Registers SUPPLYV1, SUPPLYV2, SUPPLYV3, SUPPLYV4 and SUPPLYV6 define the voltage settings for the non-DVM supplies.

Register SUPPLYV4 has two bits that control the RTC_OUT LDO functionality. The RTC_OUT LDO will be enabled when LDORTC_ON is **1**. The power good threshold for the RTC_OUT LDO can be set as follows: 2.4V (RTC_PGOOD is **1**), 2.0V (RTC_PGOOD is **0**).

Table 3-29. Non-DVM Supply Voltage Selection

SUPPLYV1 [Addr 0x41]								
Bit Name	VLDO0[2]	VLDO0[1]	VLDO0[0]	VLDO1[4]	VLDO1[3]	VLDO1[2]	VLDO1[1]	VLDO1[0]
Function	LDO0 OUTPUT VOLTAGE (See Table 3-31)			LDO1 OUTPUT VOLTAGE (See Table 3-30)				
SUPPLYV3 [Addr 0x43]								
Bit Name	LDO7_SW	LDO6_SW	VLDO7[2]	VLDO7[1]	VLDO7[0]	VLDO6[2]	VLDO6[1]	VLDO6[0]
Function	SPARE	SPARE	LDO7 OUTPUT VOLTAGE (See Table 3-31)			LDO6 OUTPUT VOLTAGE (See Table 3-31)		
SUPPLYV4 [Addr 0x44]								

Table 3-29. Non-DVM Supply Voltage Selection (continued)

Bit Name	LDORTC_ON	RTC_PGOOD	VRTC[2]	VRTC[1]	VRTC[0]	VLDO3[2]	VLDO3[1]	VLDO3[0]
Function	RTC_LDO ON/OFF CONTROL	RTC_OUT LOW VOLTAGE THRESHOLD	RTC OUTPUT VOLTAGE (See Table 3-31)			LDO3 OUTPUT VOLTAGE (See Table 3-31)		
SUPPLYV6 [Addr 0x46]								
Bit Name	RSVD467	RSVD466	VLDO9[2]	VLDO9[1]	VLDO9[0]	VLDO5[2]	VLDO5[1]	VLDO5[0]
Function	NOT USED	NOT USED	LDO9 OUTPUT VOLTAGE (See Table 3-31)			LDO5 OUTPUT VOLTAGE (See Table 3-31)		

The available output voltages for the non-DVM supplies are shown below:

Table 3-30. VLDO1[4:0] Settings

RANGE	[4:0]	VOUT (V)	[4:0]	VOUT (V)	[4:0]	VOUT (V)	[4:0]	VOUT (V)
0.725V–1.50V	00000	0.725	01000	0.925	10000	1.125	11000	1.325
	00001	0.750	01001	0.950	10001	1.150	11001	1.350
	00010	0.775	01010	0.975	10010	1.175	11010	1.375
	00011	0.800	01011	1.000	10011	1.200	11011	1.400
	00100	0.825	01100	1.025	10100	1.225	11100	1.425
	00101	0.850	01101	1.050	10101	1.250	11101	1.450
	00110	0.875	01110	1.075	10110	1.275	11110	1.475
	00111	0.900	**01111**	**1.100**	10111	1.300	11111	1.500

Table 3-31. VLDO3/5/6/7/8/9[2:0] and VRTC[2:0] Settings

VLDOx[2:0]	VOUT (V)	VLDOx[2:0]	VOUT (V)
000	1.25	100	2.70
001	1.50	101	2.85
010	1.80	110	3.10
011	2.50	111	3.30

Table 3-32. VLDO0[2:0] Settings

VLDOx[2:0]	VOUT (V)	VLDOx[2:0]	VOUT (V)
000	1.20	100	2.70
001	1.50	101	2.85
010	1.80	110	3.10
011	2.50	111	3.30

Setting the RTC_OUT output voltage below the RTC_OUT power good threshold will result in a $\overline{\text{NORTC}}$ pulse always being generated during the reboot cycle or when exiting sleep. Setting the RTC_OUT output voltage below V_{UVLO_RTC} disables the use of the internal real time clock counter and xtal oscillator.

3.38 BOOST CONVERTER

The TPS658629-Q1 has an integrated boost converter (SM3) that is optimized to drive white LED's connected in a series configuration. Up to six series white LED's can be driven, with programmable current and duty cycle adjustable via a dedicated I^2C register.

The SM3 boost Converter (SM3) has a 29v, 500mA low side integrated power stage switch, which drives the external inductor. Another integrated 29V, 25mA switch (LED switch) is used to modulate the external white LED's brightness.

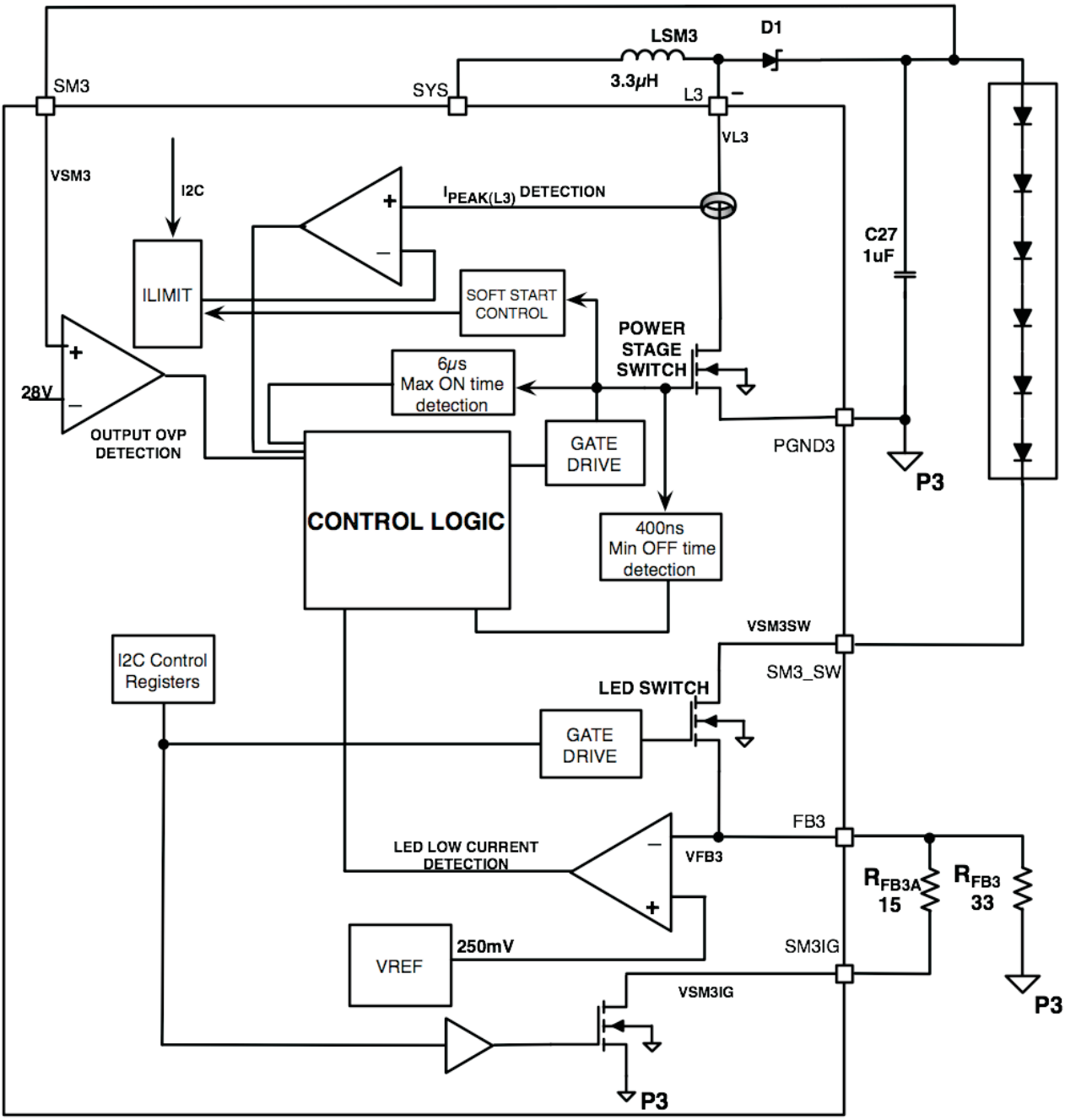


Figure 3-13. Boost Converter Block Diagram

The SM3 boost converter operates in a pulse frequency modulation (PFM) scheme with constant peak current control. This control scheme maintains high efficiency over the entire load current range and enables the use of small external components, as the switching frequency can reach up to 1 MHz depending on the load conditions. The LED current ripple is defined by the external inductor size.

The converter monitors the sense voltage at pin FB3, and turns on the integrated power stage switch when V(FB3) is below the 250mV (typ) internal reference voltage. The integrated power switch turns off when the inductor current reaches the internal peak current limit or if the switch is on for a period longer than the maximum on-time of 6 µs (typ).

As the integrated power switch is turned off the external Schottky diode is forward biased, delivering the stored inductor energy to the output. The main switch remains off until the FB3 pin voltage is below the internal 250mV reference voltage, when it is turned on again.

This PFM peak current control sets the converter in discontinuous conduction mode (DCM), and the switching frequency depends on the inductor, input/output voltage and LED current. Lower LED currents reduce the switching frequency, with high efficiency over the entire LED current range. This regulation scheme is inherently stable, allowing a wide range for the selection of the inductor and output capacitor.

3.38.1 SM3 RAM Registers

Table 3-33. SM3 Control

SM3_SET0 [Addr 0x57]							Defaults in **BOLD**	
Bit Number	B7	B6	B5	B4	B3	B2	B1	B0
Bit Name	SM3_SET7	SM3_SET6	SM3_SET5	SM3_SET4	SM3_SET3	SM3_SET2	SM3_SET1	SM3_SET0
Function	SM3 PWM SWITCH DUTY CYCLE							
When 0	**ADD 0 TO DUTY CYCLE**							
When 1	ADD 6.25%	ADD 3.125%	ADD 1.5625%	ADD 0.78125%	ADD 0.390%	ADD 0.195%	ADD 0.0976%	ADD 0.048%
SM3_SET1 [Addr 0x58]							Defaults in **BOLD**	
Bit Number	B7	B6	B5	B4	B3	B2	B1	B0
Bit Name	SM3SOFTOFF	SM3_ILIM	SM3_PRESC1	SM3_PRESC0	SM3_IGAIN	SM3_SET10	SM3_SET9	SM3_SET8
Function	SOFTSTART ENABLE	SM3 CURRENT LIMIT	SM3PWM REPETITION RATE[1]	SM3PWM REPETITION RATE[0]	ISM3G OUTPUTBUFFER MODE	SM3 PWM DUTY CYCLE		
When 0	**ENABLED**	**300 mA**	**SEE SM3 PWM REPETITION TABLE**		**Hi-Z**	**ADD 0 TO DUTY CYCLE**		
When 1	DISABLED	500 mA	SEE SM3 PWM REPETITION TABLE		LO	ADD 50%	ADD 25%	ADD 12.5%

Table 3-34. SM3 PWM Repetition Settings

SM3PRESC[1]	SM3PRESC[0]	REPETITION RATE (Hz)
0	0	550
0	1	366
1	0	275
1	1	220

The internal LED switch, in series with the external LED's, disconnects the LEDs from ground during shutdown. In addition, the LED switch is driven by a PWM signal generated internally, enabling adjusting the average LED current by setting the LED switch duty cycle. The duty cycle is adjusted with control bits $\overline{\text{SM3\_SET}}$, on register SM3_SET0. With this control method the LED brightness depends on the LED switch duty cycle only and is independent of the boost converter operating frequency. The duty cycle control used in the SM3 converter LED switch is implemented by a single PWM pulse with a fixed repetition rate. An example of distinct duty cycles is shown IN Figure 3-14

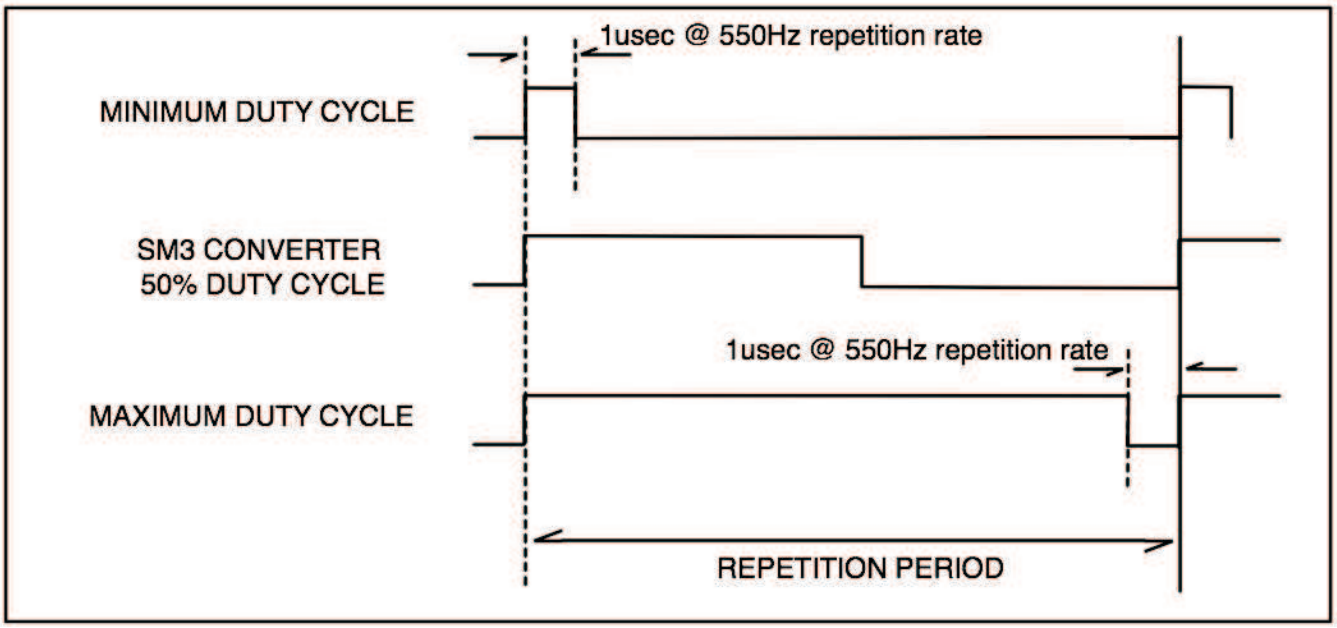


Figure 3-14. SM3 Duty Cycle Example

The repetition period can be set using control bits SM3_PRESCn in the register SM3_SET1 to either 220/275/366/550 Hz (HI). Each repetition period has a total of 2048 steps, enabling a resolution of 0.05% when programming the duty cycle.

3.38.2 Peak Current Control (Boost Converter)

The SM3 integrated power stage switch is turned on until the inductor current reaches the DC current limit $I_{MAX(L3)}$ (500 mA or 300mA, typ), selectable via bit SM3_ILIM , register SM3_SET1. Due to internal delays, typically around 100ns, the actual current exceeds the DC current limit threshold by a small amount. The typical peak current limit can be calculated as follows:

$$I_{P(typ)} = I_{MAX(L3)} + \frac{V_{SM3}}{L} \times 100\ ns \quad (3)$$

The peak current will be directly proportional to the input voltage and inversely proportional to the inductor value. The internal current limit may be set to either 300mA or 500mA via I^2C.

Note that under PWM operation the slew rate of the converter output (SM3) is dependent of the $I_{MAX(L3)}$ value selected.

3.38.3 Soft Start

All inductive step-up converters exhibit high in-rush current during start-up. If no special precautions are taken voltage drops can be observed at the input supply rail during start-up, with unpredictable results in the overall system operation.

The SM3 boost converter limits the inrush current during start-up by increasing the current limit in two steps, starting from $I_{MAX(L3)}$ /4 for 256 power stage switch cycles (1cycle=power stage switch OFF→ON→OFF) to $I_{MAX(L3)}$ /2 for the next 256 power stage switch cycles and then full current limit $I_{MAX(L3)}$. The softstart function can be disabled via control bit SM3SOFTOFF, in register SM3_SET1.

3.38.4 Enabling the SM3 Converter

The converter is enabled when an I^2C command sets the duty cycle to a value different than zero.

3.38.5 Overvoltage Protection

The output voltage of the boost converter is sensed at pin SM3, and the integrated power stage switch is turned OFF when V(SM3) exceeds the internal over-voltage threshold $V_{(OVP3)}$. The converter returns to normal operation when V(SM3) < $V_{(OVP3)} - V_{HYS(OVP3)}$.

3.38.6 Under Voltage Lockout Operation

The power stage mosfet switch and the LED switch are open (off) when the TPS658629-Q1 enters the sleep mode or if the SM3 converter is set to OFF mode.

3.38.7 SM3 Output Current - High and Low Current Settings

A dedicated, open-drain pin (ISM3G) enables I^2C selection of a low and high brightness setting for the SM3 output current, by modifying the external FB3 resistor value. See application diagram for details. This pin is configured as an open drain and it can be turned on/off with bit SM3_IGAIN on register SM3_SET1.

3.39 RGB AND PWM DRIVERS

The TPS658629-Q1 has integrated open drain and push-pull drivers with programmable duty cycle and frequency, targeted at driving external RGB drivers, keyboard LED's, vibrator motor and other system peripherals.

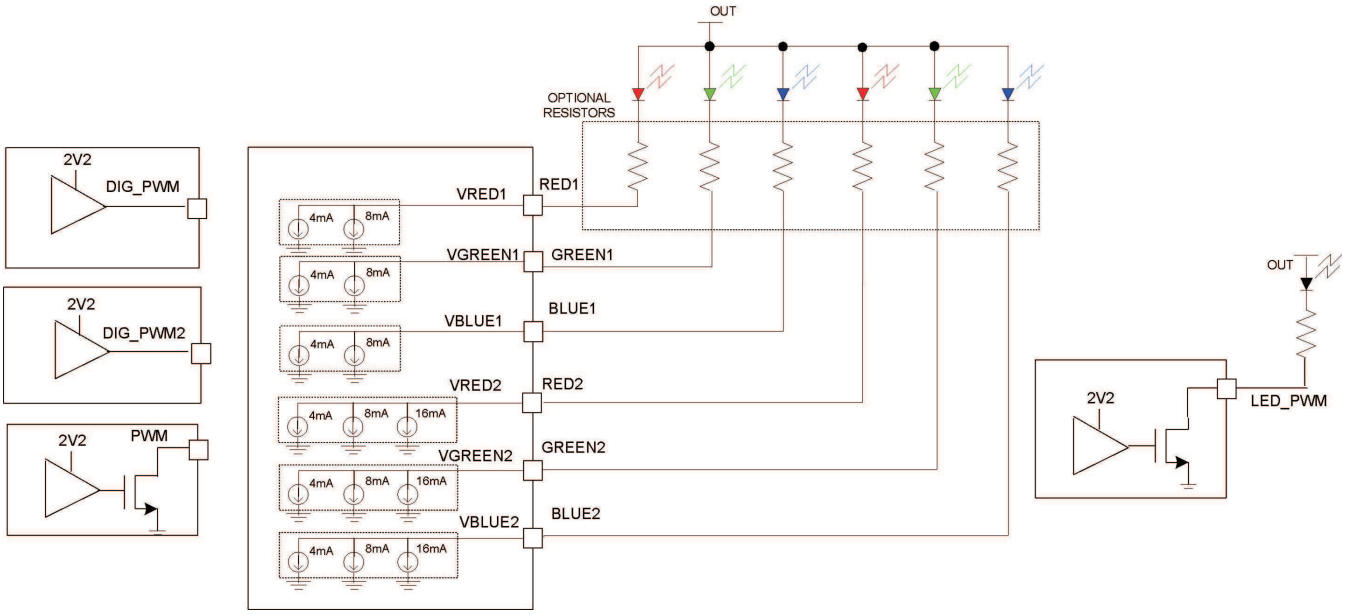


Figure 3-15. RGB and PWM Driver Blocks

3.39.1 PWM Pin Driver

The TPS658629-Q1 offers one high current (150mA max) open-drain PWM driver. The PWM driver is enabled when PWM_EN is 1 in register PWM.

Table 3-35. PWM Control

PWM [Addr 0x5B]								Default to 0
Bit Number	B7	B6	B5	B4	B3	B2	B1	B0
Bit Name	PWM_EN	PWM_F[2]	PWM_F[1]	PWM_F[0]	PWM_D[3]	PWM_D[2]	PWM_D[1]	PWM_D[0]
Function	PWM DRIVER ON/OFF	PWM DRIVER FREQUENCY			PWM DRIVER DUTY CYCLE			

The PWM frequency and duty cycle are defined by the PWM register settings as shown below.

Table 3-36. PWM Settings

PWM_F[2:0)	FREQUENCY(kHz)	PWM_D[3:0]	DUTY CYCLE (%)	PWM_D[3:0]	DUTY CYCLE (%)
000	23.4	0000	6.25	1000	56.25
001	11.7	0001	12.5	1001	62.5
010	6.7	0010	18.75	1010	68.75
011	4.5	0011	25	1011	75
100	3.0	0100	31.25	1100	81.25
101	2.3	0101	37.5	1101	87.5
110	1.5	0110	43.75	1110	93.75
111	0.75	0111	50	1111	100

3.39.2 DIG_PWM, DIG_PWM2 Drivers

The TPS658629-Q1 provides two push-pull outputs with programmable duty cycle at pins DIGPWM and DIGPWM2. The DIG_PWM register controls the DIGPWM pin duty cycle, register DIG_PWM2 controls the DIGPWM2 pin duty cycle. The DIG_PWM functions and register bit controls detailed below apply to the DIGPWM2 pin and DIG_PWM2 register as well. Both registers default to 0x00 upon power-up.

Table 3-37. DIGPWM, DIGPWM2 Control

DIG_PWM [Addr 0x5A]								**Default to 0**
Bit Number	B7	B6	B5	B4	B3	B2	B1	B0
Bit Name	DPWM_MODE	DPWM_SET[6]	DPWM_SET[5]	DPWM_SET[4]	DPWM_SET[3]	DPWM_SET[2]	DPWM_SET[1]	DPWM_SET[0]
DIG_PWM2 [Addr 0x5C]								**Default to 0**
Bit Number	B7	B6	B5	B4	B3	B2	B1	B0
Bit Name	DPWM2_MODE	DPWM2_SET[6]	DPWM2_SET[5]	DPWM2_SET[4]	DPWM2_SET[3]	DPWM2_SET[2]	DPWM2_SET[1]	DPWM2_SET[0]

Mode 0 (DPWM_MODE is **0**): The pulse width modulated output is a single PWM pulse of the selected duty cycle, with a nominal 250Hz repetition rate. The DIG_PWM register bits [6:0] sets the pulse width value as shown below:

$$T_{ON}(ms) = \frac{DPWM\_SET[6:0]}{32}, \text{ if } DPWM\_SET[6:0] \leq 126 \quad (4)$$

$$T_{ON}(ms) = \text{Always On, if } DPWM\_SET[6:0] = 127 \quad (5)$$

Mode 1 (DPWM_MODE is 1): The bit DPWMx_SET[6] of the DIG_PWMx register selects the pulse time range, bits DIG_PWMx[5:3] set the ON times and bits DIG_PWMx[2:0] set the off times.

Table 3-38. Digital PWM Settings, DPWM_MODE=1

DPWMx_SET[6] = 0				DPWMx_SET[6] = 1			
DIG_PWMx[5:3]	ON TIME (µs)	DIG_PWMx[2:0]	OFF TIME (ms)	DIG_PWMx[5:3]	ON TIME (ms)	DIG_PWMx[2:0]	OFF TIME (ms)
000	31	000	0.49	000	5	000	40
001	61	001	1.01	001	10	001	60
010	92	010	1.50	010	15	010	80
011	122	011	2.01	011	20	011	100
100	153	100	2.50	100	30	100	120
101	183	101	2.99	101	40	101	140
110	214	110	4.00	110	50	110	160
111	244	111	5.00	111	60	111	180

3.39.3 LED_PWM Driver

The LED PWM open drain pin has the duty cycle set by a pulse width modulation circuit. The LED_SET register bits (7:0) set the pulse width value in 256 steps. The pulse width modulated output is not a single pulse of the selected duty cycle but a collection of semi-equally spaced pulses that sum to the required duty cycle, with repetition rate of 125Hz (typ)

Table 3-39. LEDPWM Control

LED_PWM [Addr 0x59]								**Default to 0**
Bit Number	B7	B6	B5	B4	B3	B2	B1	B0
Bit Name	LED_SET[7]	LED_SET[6]	LED_SET[5]	LED_SET[4]	LED_SET[3]	LED_SET[2]	LED_SET[1]	LED_SET[0]

$$T_{ON}(ms) = \frac{LED\_SET[7:0]}{32}, \text{ if } LED\_SET[7:0] \leq 254 \quad (6)$$

T_{ON}(ms) = Always On, if LED_SET[7:0] = 255 (7)

3.39.4 RGB Drivers

The TPS658629-Q1 has two dedicated drivers for RGB external LED's. Three outputs are available for each driver (pins REDn, GREENn, BLUEn), with I^2C selection of operation mode and LED current.

3.39.5 RGB1 Driver

The RGB1 driver is enabled when RGB1_EN=HI, in RGB1_GREEN register. Each RGB1 pin (RED1, GREEN1 or BLUE1) will sink the current selected by RGB1_ISET[1:0], RGB1_RED register.

The RGB1 driver can be set in a flashing mode, the flash operation parameters are configured in register RGB1FLASH. During the flashing ON time the duty cycle for each driver can be set individually using control bits PWMIR[4:0], PWMIG[4:0] and PWMIB[4:0] on registers RGB1_RED, RGB1_GREEN and RGB1_BLUE. The modulated output is not a single pulse of the selected duty cycle but a collection of semi-equally spaced pulses that sum to the required duty cycle, with repetition rate of 160Hz (typ). The start of 1 of the modulated pulses on RGB1 can be phased by 200 µs from the others so that for duty cycles below 50% the ON times of 2 of the LEDs will not overlap. When RGB1_PHASE is **0** (RGB1_GREEN[6]), the Red and Blue are drivers are in phase and Green is out of phase. For RGB1_PHASE is **1** the Red and Green are in phase and Blue is out of phase.

Table 3-40. RGB1 Control

RGB1FLASH [Addr 0x50]								Default is **0**
Bit Number	B7	B6	B5	B4	B3	B2	B1	B0
Bit Name	RSVD507	FLASH1_ON[2]	FLASH1_ON[1]	FLASH1_ON[0]	FLASH1_PER[3]	FLASH1_PER[2]	FLASH1_PER[1]	FLASH1_PER[0]
Function	SPARE	RGB1 RED/BLUE/GREEN FLASHING ON-TIME			RGB1 RED/BLUE/GREEN FLASHING PERIOD			
RGB1RED [Addr 0x51]								Default is **0**
Bit Number	B7	B6	B5	B4	B3	B2	B1	B0
Bit Name	RSVD517	RGB1_ISET[1]	RGB1_ISET[0]	PWM1R[4]	PWM1R[3]	PWM1R[2]	PWM1R[1]	PWM1R[0]
Function	NOT USED	RGB1 RED/BLUE/GREEN DRIVER CURRENT SINK		RGB1 RED DRIVER INTENSITY CONTROL				
RGB1GREEN [Addr 0x52]								Default is **0**
Bit Number	B7	B6	B5	B4	B3	B2	B1	B0
Bit Name	RGB1_EN	RGB1_PHASE	RSVD535	PWM1G[4]	PWM1G[3]	PWM1G[2]	PWM1G[1]	PWM1G[0]
Function	RGB1 DRIVERS ON/OFF CONTROL	DRIVER ON TIME PHASE CONTROL	NOT USED	RGB1 GREEN DRIVER INTENSITY CONTROL				
RGB1BLUE [Addr 0x53]								Default is **0**
Bit Number	B7	B6	B5	B4	B3	B2	B1	B0
Bit Name	RSVD537	RSVD536	RSVD535	PWM1B[4]	PWM1B[3]	PWM1B[2]	PWM1B[1]	PWM1B[0]
Function	NOT USED	NOT USED	NOT USED	RGB1 BLUE DRIVER INTENSITY CONTROL				

Table 3-41. RGB1 Sink Current Settings

RGB1_ISET[1:0]	RGB1 SINK CURRENT (mA)
00	0
01	3.7
10	7.4
11	11.1

Table 3-42. FLASH1_ON Settings

FLASH1_ON[2:0]	FLASH ON TIME (s)
000	0.10
001	0.15
010	0.20
011	0.25
100	0.30
101	0.40
110	0.50
111	0.60

Table 3-43. FLASH1_PER Settings

FLASH1_PER[3:0]	FLASH PERIOD (s)	FLASH1_PER[3:0]	FLASH PERIOD (s)
0000	1.0	1000	5.0
0001	1.5	1001	5.5
0010	2.0	1010	6.0
0011	2.5	1011	6.5
0100	3.0	1100	7.0
0101	3.5	1101	7.5
0110	4.0	1110	8.0
0111	4.5	1111	Always On

Equation 8 indicates the duty cycle values for each driver, set with bit PWM1R[4:0], PWM1G[4:0] and PWM1B[4:0]:

$$T_{ON}(ms) = \frac{PWM1R/G/B[4:0]}{5.4} \quad (8)$$

3.39.6 RGB2 Driver

The RGB2 driver is enabled when RGB2_EN is **1**, in RGB2_GREEN register. Each RGB2 pin (RED2, GREEN2 or BLUE2) will sink the current selected by RGB2_ISET[2:0], set in RGB2_RED register.

The RGB2 does not support a flashing mode, and will be turned on when RGB2_EN is **1**. When turned ON the duty cycle for each driver can be set individually using control bits PWMIR[4:0], PWMIG[4:0] and PWMIB[4:0] on registers RGB2_RED, RGB2_GREEN and RGB2_BLUE. The modulated output is not a single pulse of the selected duty cycle but a collection of semi-equally spaced pulses that sum to the required duty cycle, with repetition rate of 160Hz (typ). The start of one of the modulated pulses on RGB2 can be phased by 200 µs from the others, so that for duty cycles below 50% the ON times of 2 of the LEDs will not overlap. When RGB2_PHASE is **0** (RGB2_GREEN[6]), the Red and Blue drivers are in phase and Green is out of phase. When RGB2_PHASE is **1** the Red and Green are in phase and Blue is out of phase.

Table 3-44. RGB2 Control

RGB2RED [Addr 0x54]							Default to **0**	
Bit Number	B7	B6	B5	B4	B3	B2	B1	B0
Bit Name	RGB2_ISET[2]	RGB2_ISET[1]	RGB2_ISET[0]	PWM2R[4]	PWM2R[3]	PWM2R[2]	PWM2R[1]	PWM2R[0]
Function	RGB2 RED/BLUE/GREEN DRIVER CURRENT SINK			RGB2 RED DRIVER INTENSITY CONTROL				
RGB2GREEN [Addr 0x55]							Default to **0**	
Bit Number	B7	B6	B5	B4	B3	B2	B1	B0
Bit Name	RGB2_EN	RGB2_PHASE	RSVD565	PWM2G[4]	PWM2G[3]	PWM2G[2]	PWM2G[1]	PWM2G[0]
Function	RGB2 DRIVERS ON/OFF CONTROL	RGB2 DRIVERS ON TIME PHASE CONTROL	SPARE	RGB2 GREEN DRIVER INTENSITY CONTROL				
RGB2BLUE [Addr 0x56]							Default to **0**	
Bit Number	B7	B6	B5	B4	B3	B2	B1	B0
Bit Name	RSVD577	RSVD576	RSVD575	PWM2B[4]	PWM2B[3]	PWM2B[2]	PWM2B[1]	PWM2B[0]
Function	NOT USED	NOT USED	NOT USED	RGB2 GREEN DRIVER INTENSITY CONTROL				

Table 3-45. RGB2 Sink Current Settings

RGB2_ISET[2:0]	RGB2 SINK CURRENT (mA)
000	0
001	3.7
010	7.4
011	11.1
100	14.9
101	18.6
110	23.2
111	27.3

The on time for each driver, set with bits PWM2R[4:0], PWM2G[4:0] and PWM2B[4:0], is set by the equation:

$$T_{ON}(ms) = \frac{PWM2R/G/B[4:0]}{5.4} \quad (9)$$

3.40 REAL TIME CLOCK

The TPS658629-Q1 has an integrated real time clock circuit that maintains an accurate timer/counter register under all potential operating conditions (AC power input, USB power input, main battery power, backup coincell / SuperCap power source, or any combination of the above). The internal oscillator for the RTC can be driven by an external 32.768 kHz crystal. The TPS658629-Q1 has also been design with integrated, I^2C selectable, capacitors which can be used with the external 32.768 kHz crystal such that a wide range of commercial crystals can be used without the need for external load capacitors.

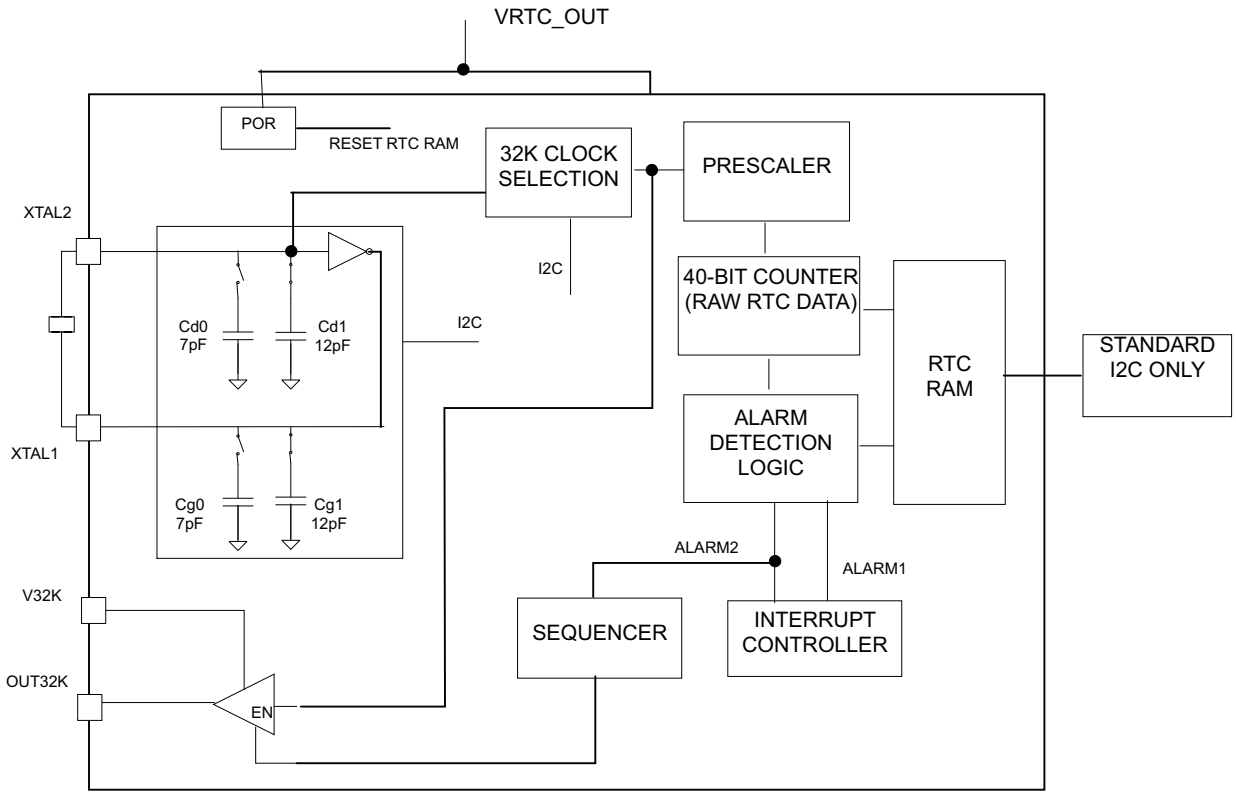


Figure 3-16. Simplified RTC Block

The following functions are provided:

- A 40-bit counter, driven by a low-power 32 kHz oscillator
- The 32 kHz oscillator can be switched using I^2C, RTC_CTRL Register bit 6 (OSC_SRC_SEL), between the TPS658629-Q1 internal (RC) oscillator source and the crystal driven oscillator source.
- Externally biased buffer to supply the crystal driven oscillator to an external device via the OUT32K pin.
- Selectable pre-scaler divides the raw (32KHz) oscillator output, enabling clocking the RTC counter at 1.024 kHz or 32 kHz
- A 24-bit alarm register (ALARM1)
- A 16-bit alarm register (ALARM2)

The RTC registers are accessible only via the I^2C bus. When an I^2C read access is in progress, the RTC counter update is postponed. At the end of the I^2C read access, the accumulated missing counts are added to the RTC counter.

NOTE

The RTC registers (0xC0-0xCA) **ARE NOT** reset when the TPS658629-Q1 is in the POWER DOWN or SLEEP STATE as long as V(RTC_OUT) is greater than V_{UVLO_RTC} . All the RTC registers will be reset to their default settings, independent of the TPS658629-Q1 state, when V(RTC_OUT) is less than V_{UVLO_RTC}.

The host software must read all five RTC counter bytes when accessing the RTC counter data, as the counter update is postponed starting at the first I^2C byte read of a sequential I^2C read of the five RTC_COUNT bytes and negated on the fifth I^2C byte read.

To assure proper operation of the RTC counter the following steps should always be followed:

1. The I^2C address pointer must not be left pointing in the range 0xC6 to 0xCA

2. The maximum time for the address pointer to be in this range is 1 ms
3. Always read RTC_ALARM2 in the following order to prevent the address pointer from stopping at 0xC6: RTC_ALARM2_LO, then RTC_ALARM2_HI

When the RTC_OUT voltage falls below the internal RTC circuit Power On Reset threshold, V_{UVLO_RTC}, the RTC_CTRL register is reset. The host can identify this situation by reading the bit, POR_RESET_N, which will be **0**.

The clock selection is controlled by OSC_SRC_SEL (RTC_CTRL [6]). The internal 32kHz oscillator is connected to the RTC when the OSC_SRC_SEL bit is reset. Once the processor is running, the software can set this bit to **1**, thereby connecting the 32.768 kHz crystal oscillator clock to the RTC. After being set, the OSC_SRC_SEL bit will remain **1** selecting the crystal oscillator clock, as long as the VRTC_OUT voltage remains above the RTC_OUT Power On Reset threshold. POR_RESET_N=HI when OSC_SRC_SEL is set HI, indicating to the host that the crystal clock is being delivered to the RTC.

The RTC_ENABLE (RTC_CTRL [5]) bit is cleared to **0** by the RTC_OUT Power On Reset, disabling the RTC counter. To enable incrementing of the RTC_COUNT [39:0] from an initial value set by the host, the RTC_ENABLE bit should be written to **1** only after the RTC_OUT voltage reaches the operating range. The RTC_ENABLE bit must be cleared to **0** before any new value is written to the RTC_COUNT register.

Table 3-46. RTC Control(1)

RTC_CTRL [Addr 0xC0]								**Defaults in BOLD**
Bit Number	B7	B6	B5	B4	B3	B2	B1	B0
Bit Name	POR_RESET_N	OSC_SRC_SEL	RTC_ENABLE	BUF_ENABLE	PRE_BYPASS	CL_SEL[1]	CL_SEL[0]	RSVDC00
Function	RESET RTC COUNTER	32K CLOCK SELECTION	RTC COUNTER CLOCK AND ALARM1/2	32KHZ BUFFER ENABLE	RTC COUNTER SCALING	INTERNAL XTAL1, XTAL2	PIN CAPACITANCE	RTC_ALARM2 DETECTION EXITS SLEEP
When 0	**RESET RTC COUNTER**	**INTERNAL 32K**	**DISABLED**	DISABLED	**USE 32K/32**	SEE CL_SEL SETTINGS TABLE		**DISABLED**
When 1	OSC_SRC_SEL BIT = 1	CRYSTAL 32K	ENABLED	**ENABLED**	USE 32K	SEE CL_SEL SETTINGS TABLE		ENABLED

(1) B7 is READ ONLY, all other bits have Read/Write access

The selected 32KHz clock is applied to a prescaler that can divide it by 32, resulting in a timer tick resolution of either 32,768 ticks per second (pre-scaler disabled, PRE_BYPASS is **1**) or 1,024 ticks per second (pre-scaler enabled, PRE_BYPASS is **0**). The 32,768 Hz or 1024 Hz clock increments a 40 bit counter that tracks the real time and which can be read at anytime via I^2C. With the prescaler enabled, the RTC count has a range of approximately 34 years. The RTC counter and alarm registers are shown below, the 40 bit RTC Counter is cleared only on when RTC_OUT is below the UVLO threshold.

Table 3-47. RTC Counter

RTC_COUNT4 [Addr 0xC6]								Default to **0**
Bit Number	B7	B6	B5	B4	B3	B2	B1	B0
Bit Name	RTC[39]	RTC[38]	RTC[37]	RTC[36]	RTC[35]	RTC[34]	RTC[33]	RTC[32]
RTC_COUNT3 [Addr 0xC7]								Default to **0**
Bit Name	RTC[31]	RTC[30]	RTC[29]	RTC[28]	RTC[27]	RTC[26]	RTC[25]	RTC[24]
RTC_COUNT2 [Addr 0xC8]								Default to **0**
Bit Name	RTC[23]	RTC[22]	RTC[21]	RTC[20]	RTC[19]	RTC[18]	RTC[17]	RTC[16]
RTC_COUNT1 [Addr 0xC9]								Default to **0**
Bit Name	RTC[15]	RTC[14]	RTC[13]	RTC[12]	RTC[11]	RTC[10]	RTC[9]	RTC[8]
RTC_COUNT0 [Addr 0xCA]								Default to **0**
Bit Name	RTC[7]	RTC[6]	RTC[5]	RTC[4]	RTC[3]	RTC[2]	RTC[1]	RTC[0]

The alarm logic compares the RTC_ALARM1 register bits to the RTC_COUNT registers as follows:

With prescaler enabled: ALM1[23:0] is compared to RTC[23:0]

With prescaler disabled: ALM1[23:0] is compared to RTC[28:5]

An interrupt is sent to the host (if enabled via I^2C, see interrupt controller section) when the alarm logic detects that the RTC_COUNT value is equal to the pre-programmed ALARM1 register value.

The alarm logic compares the RTC_ALARM2 register bits to the RTC_COUNT registers as follows:

With prescaler enabled: ALM2[23:0] is compared to RTC[22:7]

With prescaler disabled: ALM2[15:0] is compared to RTC[27:12]

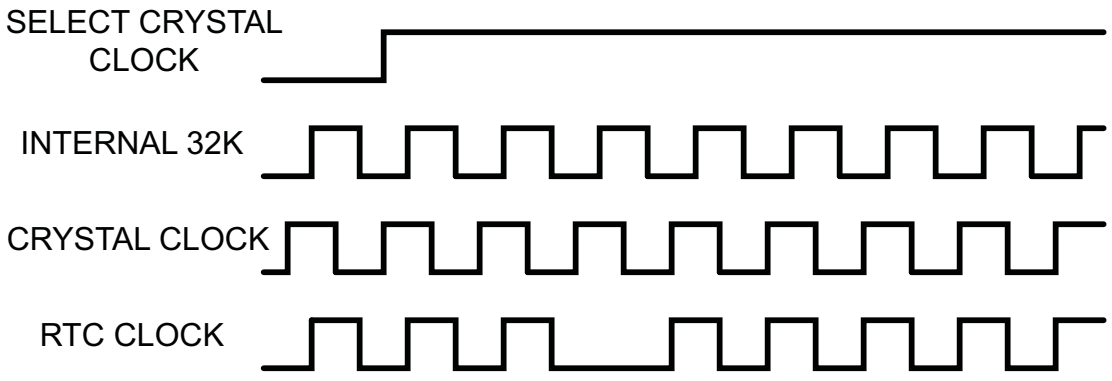
An interrupt is sent to the host (if enabled via I^2C, see interrupt controller section) and the sleep mode ends when the alarm logic detects that the RTC_COUNT value is equal to the pre-programmed ALARM2 register value.

Table 3-48. RTC Alarm

RTC_ALARM1_HI [ADDRESS=0xC1]								Default to **0**
Bit Number	B7	B6	B5	B4	B3	B2	B1	B0
Bit Name	ALM1[23]	ALM1[22]	ALM1[21]	ALM1[20]	ALM1[19]	ALM1[18]	ALM1[17]	ALM1[16]
RTC_ALARM1_MID [Addr 0xC2]								Default to **0**
Bit Name	ALM1[15]	ALM1[14]	ALM1[13]	ALM1[12]	ALM1[11]	ALM1[10]	ALM1[9]	ALM1[8]
RTC_ALARM1_LO [Addr 0xC3]								Default to **0**
Bit Name	ALM1[7]	ALM1[6]	ALM1[5]	ALM1[4]	ALM1[3]	ALM1[2]	ALM1[1]	ALM1[0]
RTC_ALARM2_HI [Addr 0xC4]								Default to **0**
Bit Name	ALM2[15]	ALM2[14]	ALM2[13]	ALM2[12]	ALM2[11]	ALM2[10]	ALM2[9]	ALM2[8]
RTC_ALARM2_LO [Addr 0xC5								Default to **0**
Bit Name	ALM2[7]	ALM2[6]	ALM2[5]	ALM2[4]	ALM2[3]	ALM2[2]	ALM2[1]	ALM2[0]

3.41 SWITCHING BETWEEN INTERNAL AND CRYSTAL CLOCK

When switching between the internal clock to the crystal clock, an internal logic extends the LO time of the clock sent to the counter to avoid undesired glitches. A typical clock switching timing diagram is shown below:



3.42 CRYSTAL OSCILLATOR

The crystal oscillator has internal load capacitances, in order to allow a typical 32K crystal to operate as described in the electrical characteristics tables. The TPS658629-Q1 has four integrated capacitors that can be connected to the XTAL1, XTAL2 pins as defined by control bits CL_SEL[1:0] in register RTC_CTRL, effectively applying a load capacitance to the external crystal.

Table 3-49. CL_SEL[1:0] Setting (Default in bold)

CL_SEL[1]	CL_SEL[0]	Total C_LOAD [pF] (typ)
0	0	1.5
0	1	6.5
1	**0**	**7.5**
1	1	12.5

3.43 ADC FUNCTIONAL OVERVIEW

The TPS658629-Q1 ADC is capable of running in a variety of modes programmable via I^2C. The ADC control and data registers are accessible only by the standard I^2C interface (SDA/SCLK). An internal 11:1 analog multiplexer is used to allow a single SAR converter to sequentially monitor up to 11 analog inputs, as shown inTable 3-50.

Table 3-50. ADC Channel Settings

CHANNEL	CONNECTION	PARAMETER SAMPLED	VOLTAGE RANGE	SPECIAL FEATURES	FULL SCALE READING
CH1	ANLG1 pin	User defined	0–2.6V AVDD6-V(ANLGn)> 400mV	Internal pull-up current source programmable via I^2C: 0/ 3/10/50 µA	2.6 V
CH2	ANLG2 pin				2.6 V
CH3	ANLG3 pin				2.6 V
CH4	RSVD	N/A	N/A	—	2.6 V
CH5	TS pin	Voltage proportional to pack temperature	0V (short) to 2.2V (no thermistor)	—	2.6 V
CH6	RSVD	N/A	N/A	—	2.6 V
CH7	LDO_RTC pin	Internal LDO output voltage	0V to 3.3V	—	4.622 V
CH8	SYS pin	System Power bus voltage	0V to 5.5V	—	5.547 V
CH9	RSVD	N/A	N/A	—	5.547 V
CH10	BAT pin	Battery pack positive terminal voltage	0V to 4.6V	—	4.622 V
CH11	RSVD	N/A	N/A	—	2.6 V

A simplified block diagram for the ADC analog section is show in Figure 3-17.

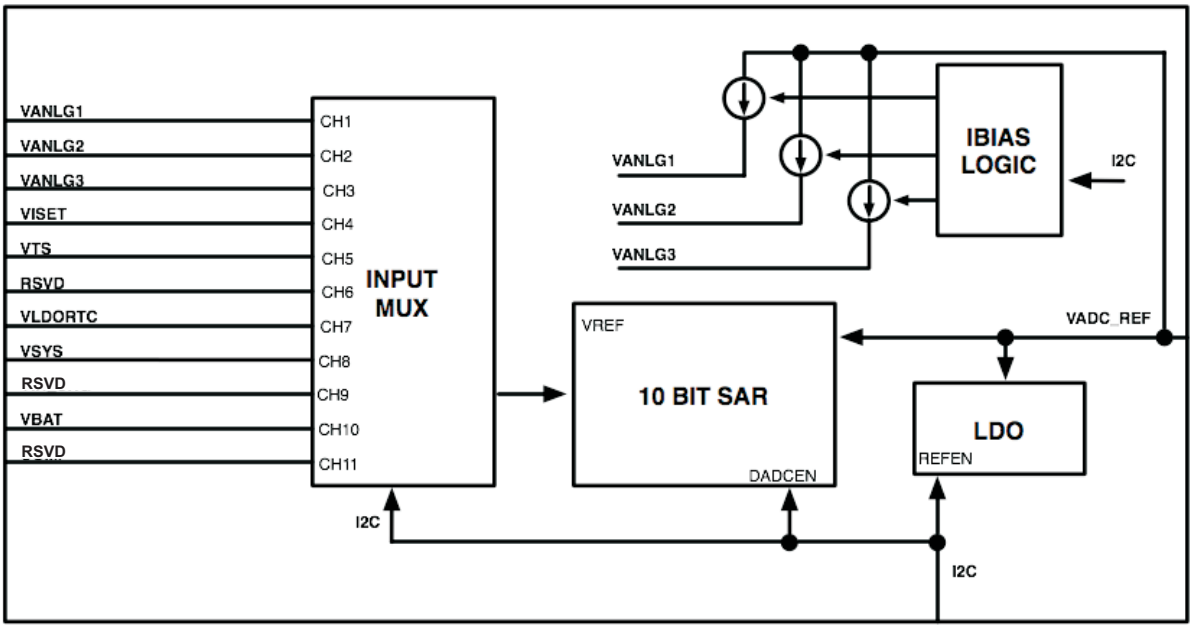


Figure 3-17. Simplified ADC Block

3.43.1 ADC External Input Pins – Bias Current Settings

The external pins ANLG1, ANLG2 and ANLG3 may be biased using internal pull-up current sources, with current source value set by register ADCANLG. The current sources are turned OFF when the ADC reference is disabled.

Table 3-51. ADC Input Bias Selection

ADCANLG [Addr 0x60]								Default to **0**
Bit Name	ANLG2FLT	ANLG3FLT	IANLG3[1]	IANLG3[0]	IANLG2[1]	IANLG2[0]	IANLG1[1]	IANLG1[0]
Function	SPARE	SPARE	ANLG3 BIAS CURRENT SOURCE		ANLG2 BIAS CURRENT SOURCE		ANLG1 BIAS CURRENT SOURCE	

Table 3-52. ANLG3/2/1 Current Source Settings

IANLG[1]	IANLG[0]	Current (µA)
0	0	0
0	1	3
1	0	10
1	1	50

3.43.2 ADC Timing Engine Overview

The ADC timing engine can be configured to perform either one reading, a single-trigger multiple set of readings, or to operate continuously until high or low limits are violated on any channel.

A *conversion cycle* includes the following steps:

1. Program the timing engine mode (single sample, multiple sample, etc.) and triggers
2. Enable the internal ADC reference and conversion start delay
3. Select the channel to be used as the SAR input and start the conversion cycle

The timing engine has an internal ALU that stores the converted data in an internal accumulator, executing mathematical operations with the stored data. A conversion cycle ends when the accumulator data is transferred to the TPS658629-Q1 ADC RAM data registers.

When the conversion cycle is completed, an interrupt request corresponding to indicate end of conversion operation is generated. The interrupt controller subsystem will set the ACK_ADC (bit B1, register 0xB6) to indicate the source of the interrupt was the ADC subsystem. Additional information is available in the ADC0_INT register (0x9A).

3.43.3 Configuring the ADC Conversion Cycle

3.43.3.1 Number of Samples and ADC Input Setup

Register ADC0_SET controls the following parameters for a conversion cycle: conversion start, continuous or fixed-interval sampling mode, number of samples to be taken and channel selection.

Setting the ADC0_EN bit to **1** will start the conversion process. While a conversion cycle is being executed (and conversions are being taken) the ADC0_INT register cannot be externally accessed.

The ADC engine has a BUSY signal generated by the ADC Digital Control Logic to indicate this condition. If the ADC0_EN bit is cleared to 0 during a conversion, the conversion cycle will continue until the number of samples specified with the RD_MODE bits has been taken so that the SUM (average) value from the accumulator will be valid. The ADC0_EN bit must be set to 0 before a new conversion configuration is set up.

Table 3-53. ADC0 Conversion Selection

ADC0_SET [Addr 0x61]								**Default in BOLD**
Bit Number	B7	B6	B5	B4	B3	B2	B1	B0
Bit Name	ADC0_EN	REPEAT0	RD0_MODE[1]	RD0_MODE[0]	CHSEL0[3]	CHSEL0[2]	CHSEL0[1]	CHSEL0[0]
Function	ADC0 CONVERSION START	ADC0 REPEAT MODE ENABLE	READINGS IN A CONVERSION		ADC0 INPUT CHANNEL SELECTION			
When 0	**DISABLED**	**DISABLED**	SEE ADC READING SETTINGS		SEE ADC CHANNEL SELECT SETTINGS			
When 1	ENABLED	ENABLED						

Table 3-54. ADC Readings Setting (Default in bold)

RD0_MODE[1]	RD0_MODE[0]	NUMBER OF READINGS
0	**0**	**1**
0	1	16
1	0	32
1	1	64

Table 3-55. ADC Channel Select Settings (Default in bold)

CHSELn[3:0]	CHANNEL	CHSELn[3:0]	CHANNEL
0000	**CH1**	1000	CH9
0001	CH2	1001	CH10
0010	CH3	1010	CH11
0011	CH4	1011	AGND
0100	CH5	1100	AGND
0101	CH6	1101	AGND
0110	CH7	1110	AGND

Table 3-55. ADC Channel Select Settings (Default in bold) (continued)

CHSELn[3:0]	CHANNEL	CHSELn[3:0]	CHANNEL
0111	CH8	1111	AGND

Continuous sampling mode can be set by writing $\overline{\text{REPEAT}}$ to **1** and RD0_MODE[1:0]=00. With those settings the conversions will be performed as single samples, without wait times, until the ADC_EN bit is cleared by the host or a limit violation occurs. If fixed-interval sampling mode (REPEAT0 = **0**) is chosen, the conversion cycle will consist of a specific number of samples (1, 16, 32, or 64) as specified by the RD0_MODE[1:0] bits. When a multiple sample conversion cycle is selected the time interval between individual samples is defined by the WAIT bits (register ADC0_WAIT). To exit the continuous conversion mode before a limit violation occurs, the host must first set the $\overline{\text{REPEAT}}$ bit to LO, and then set the ADC0_EN bit to **0**.

3.43.4 Timing and ADC Reference Setup

The ADC0_WAIT register controls the ADC0 timing engine reset, wait time value and the converter internal reference voltage enable. The ADC reference and SAR are disabled when AUTO_REF=0 AND REF_EN=0. The use of external references for the ADC is not supported.

Table 3-56. ADC0 Conversion Timing

ADC0_WAIT [Addr 0x62]							Defaults in BOLD	
Bit Number	B7	B6	B5	B4	B3	B2	B1	B0
Bit Name	ADC_RESET	RSVD626	AUTO_REF	REF_EN	WAIT0[3]	WAIT0[2]	WAIT0[1]	WAIT0[0]
Function	RESET CONVERSION CYCLE	NOT USED	ADC Conversion Control		WAIT TIME BETWEEN INDIVIDUAL CONVERSIONS, REPEAT MODE ENABLED (ms)			
When 0	**ALL ADC ENGINES ACTIVE**	**NOT USED**	Function is based on ADC Conversion Control		SEE WAIT0 SETTINGS TABLE			
When 1	RESET ALL ADC ENGINES	NOT USED						

Table 3-57. ADC Conversion Control (Default in bold)

AUTO_REF	REF_EN	DESCRIPTION
0	**0**	**Reference and ADC disabled**
0	1	Manual control of the Reference. WAIT=0 is not valid. 8ms must occur between REF_EN=1 and ADC0_EN=1
1	0	Automatic control of the Reference. Automatically enabled 8 ms before an ADC conversion is started.
1	1	Not a valid state

The relative timing between enabling the internal ADC reference / ANLGn pin bias currents and the start of a conversion cycle is controlled by bits AUTO_REF and REF_EN. Those bits allow implementation of a software only reference enable control or automatic reference enable control, as shown below:

Software enables ADC reference: Clear AUTO_REF bit to **0**. Software must set REF_EN to **1** at least 8 ms before enabling an ADC engine and not clear REF_EN until all ADC engines are stopped.

Automatic ADC reference enable, internal or external trigger, wait time < 8ms : Set AUTO_REF bit to **1**. The ADC logic will keep the ADC reference always on.

Automatic ADC reference enable, internal trigger, wait time > 8ms : Set AUTO_REF bit to **1**. The ADC logic enables the ADC reference 8 ms before the programmed wait time is reached

Setting ADC_RESET to **1** will return ALL the ADC timing engine to the idle state, ready to be re-enabled for a new conversion cycle. During the conversion cycle the ADC_RESET bit is internally set to LO prior to the first ADC conversion being started. $\overline{\text{WAIT}}$[3:0] sets the time interval between samples in the case where a multiple-sample conversion cycle is being executed. $\overline{\text{WAIT}}$[3:0] should be set LO in single sample conversion cycles.

Table 3-58. ADC0 Conversion Wait Settings (Default in bold); Valid for All Timing Engines

WAIT0[3:0]	WAIT TIME (ms)	WAIT0[3:0]	WAIT TIME (ms)
0000	**0.000**	1000	8.000
0001	0.062	1001	16.00
0010	0.125	1010	32.00
0011	0.250	1011	64.00
0100	0.500	1100	128.0
0101	1.000	1101	256.0
0110	2.000	1110	512.0
0111	4.000	1111	1024

3.43.5 External Trigger Setup

The ADC conversion cycle can be started via an internal or external trigger when using the ADC0 timing engine. The trigger is selectable by setting bits ADC0_TRIG4, ADC0_TRIG2 in registers ADC0_DELAY.

Table 3-59. Trigger Settings

ADC0_DELAY [Addr 0x67]								**Default to 0**
Bit Number	B7	B6	B5	B4	B3	B2	B1	B0
Bit Name	ADC0_TRIG4	ADC0_TRIG2	ADC0HOLD	ADC0_EDGE	RSVD673	DELAY0[2]	DELAY0[1]	DELAY0[0]
Function	GPIO4 IS ADC0 EXT TRIGGER	GPIO2 IS ADC0 EXT TRIGGER	ADC HOLDOFF ON/OFF CONTROL	NOT USED	NOT USED	ADC EXTERNAL TRIGGER DELAY (µs)		
When 0	**DISABLED**	**DISABLED**	**OFF**	**NOT USED**	**NOT USED**	**000=00** 001=50 010= 100 011=150 100=200 101=250 110=350 111=450		
When 1	ENABLED	ENABLED	ON	NOT USED	NOT USED			

When more than one GPIO trigger source is selected the GPIO signals are OR'ed prior to trigger detection. When both of those bits are cleared to **0** the internal trigger is selected.

ADC0_HOLDOFF (ADC0_DELAY[5]) enables the GPIOx trigger source to be used as a level-sensed gating signal which will suspend conversion cycles when the trigger source is low. The default for this bit is **0**. When ADC0HOLD is **0**, the conversion cycle will continue for the preset number of conversions selected with the RD_MODE bits once the initial trigger occurs. If the ADC0HOLD bit is **1**, any pending conversion cycle can be suspended if the GPIO trigger goes low (and resumes once the trigger signal goes high again and the trigger delay time has been met). ADC0_DELAY[2:0] are used to set the initial wait interval from the trigger event until the first conversion in a cycle is started. This delay may be from 0 to 450µs.

When the GPIO's are selected as external triggers the ADC conversion start will be dependent on the GPIO configuration. Table 3-60 shows the possible options:

Table 3-60. ADC0 GPIO Trigger Settings

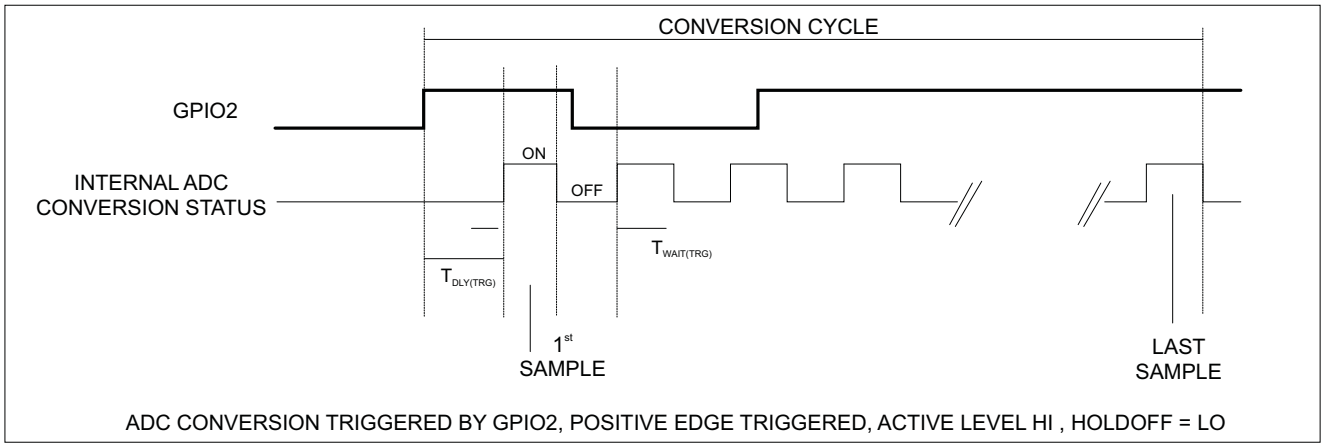
ADC0_TRIG2 = 1, ADC0_TRIG4 = 0				**ADC0_TRIG2 = 0, ADC0_TRIG4 = 1**		
GPIO2 PIN	**ADC TRIGGER SOURCE**	**WHEN HOLDOFF=HI**		**GPIO4 PIN**	**ADC TRIGGER SOURCE**	**WHEN HOLDOFF=HI**
NON-INVERTED	GPIO2 POSITIVE EDGE	SUSPEND TRIGGER at GPIO2=LO		NON-INVERTED	GPIO4 POSITIVE EDGE	SUSPEND TRIGGER at GPIO4=LO
INVERTED	GPIO2 NEGATIVE EDGE	SUSPEND TRIGGER at GPIO2=HI		INVERTED	GPIO4 NEGATIVE EDGE	SUSPEND TRIGGER at GPIO4=HI

ADC0_TRIG2=HI,ADC0_TRIG4=HI			
GPIO2 PIN	**GPIO4 PIN**	**ADC TRIGGER SOURCE**	**WHEN HOLDOFF=HI**
NON-INVERTED	NON-INVERTED	GPIO2 ***OR*** GPIO4 POSITIVE EDGE	SUSPEND TRIGGER at GPIO2 = LO AND GPIO4 = LO
NON-INVERTED	INVERTED	GPIO2 POSITIVE EDGE ***OR*** GPIO4 NEGATIVE EDGE	SUSPEND TRIGGER at GPIO2 = LO AND GPIO4 = HI
INVERTED	NON-INVERTED	GPIO2 NEGATIVE EDGE ***OR*** GPIO4 POSITIVE EDGE	SUSPEND TRIGGER at GPIO2 = HI AND GPIO4 = LO
INVERTED	INVERTED	GPIO2 ***OR*** GPIO4 NEGATIVE EDGE	SUSPEND TRIGGER at GPIO2 = HI AND GPIO4 = HI

The procedure to start an externally-triggered conversion cycle has the following steps:

1. Verify that the current conversion cycle has ended (ADC0_BUSY is **0**, I^2C register STAT4)
2. Clear ADC0_EN to **0** (ADC0_SET[7]).
3. Set the appropriate bit in the corresponding ADC0_DELAY register (example – write **1** to ADC0_DELAY bit B7 to use GPIO4 as trigger source for ADC0). Ensure that the selected GPIOs have the appropriate input and polarity selection – see GPIOSET1 and GPIOSET2 registers.
4. Set ADC0_EN to **1**

After step 4 the ADC will be armed, waiting for an external trigger detection to start a conversion cycle. In triggered mode the current cycle will not expire if the converter is armed and an external trigger is not detected.



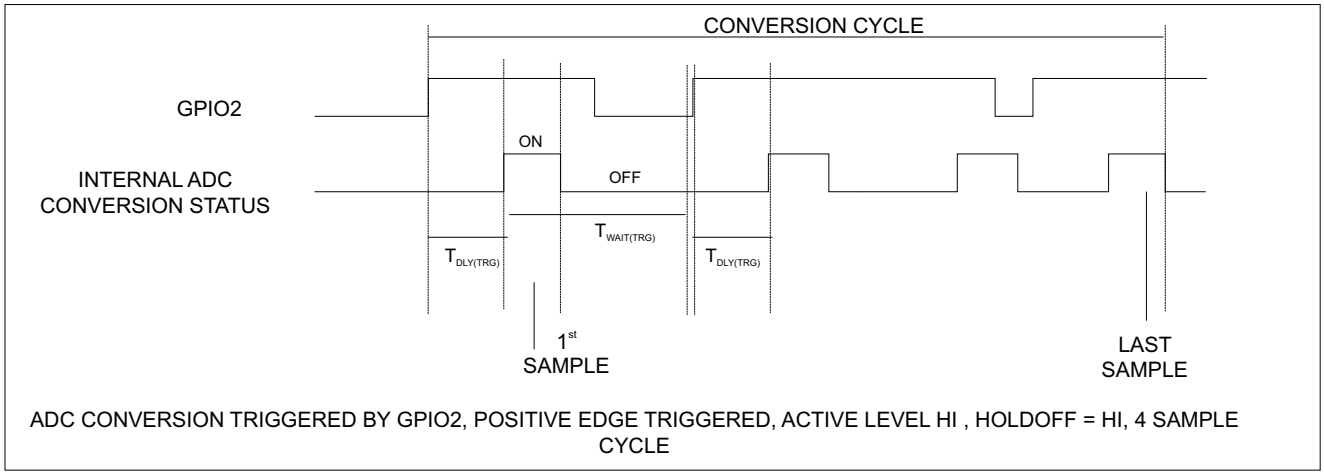


Figure 3-18. ADC Operation Example

3.43.6 ADC ALU Unit and Result Registers

The ALU performs mathematical operations on the ADC output data. It can execute average (SUM) calculations and minimum / maximum detection for a conversion cycle. The result of the SUM calculations is stored in a 16 bit accumulator register (ADC0SUM2, ADC0_SUM1) and the MIN/MAX data is stored in 10-bit registers (ADC0_MAX2, ADC0_MAX1, ADC0_MIN2, ADC0_MIN1).

Equation 10 indicates how to translate the register data into a voltage reading for each channel:

ADC_OUTPUT_COUNTS = [ADC_INPUT_VOLTAGE / FULL_SCALE_READING] × 1023 (10)

Table 3-61. ADC0 Output Data

ADC0_SUM2(1) [Addr 0x94]								
Bit Number	B7	B6	B5	B4	B3	B2	B1	B0
Bit Name	AVG[15]	AVG[14]	AVG[13]	AVG[12]	AVG[11]	AVG[10]	AVG[9]	AVG[8]
ADC0_SUM1 [Addr 0x95]								
Bit Name	AVG[7]	AVG[6]	AVG[5]	AVG[4]	AVG[3]	AVG[2]	AVG[1]	AVG[0]
ADC0_MAX2 [Addr 0x96]								
Bit Name	RSVD967	RSVD966	RSVD965	RSVD964	RSVD963	RSVD962	MAX[9]	MAX[8]
ADC0_MAX1 [Addr 0x97]								
Bit Name	MAX[7]	MAX[6]	MAX[5]	MAX[4]	MAX[3]	MAX[2]	MAX[1]	MAX[0]
ADC0_MIN2 [Addr 0x98]								
Bit Name	RSVD987	RSVD986	RSVD985	RSVD984	RSVD983	RSVD982	MIN[9]	MIN[8]
ADC0_MIN1 [Addr 0x99]								
Bit Name	MIN[7]	MIN[6]	MIN[5]	MIN[4]	MIN[3]	MIN[2]	MIN[1]	MIN[0]

(1) All bits in ADC0_SUM2 are read only.

3.43.7 Limit Check Setup

The ADC0 timing engine has configurable low and high thresholds to interrupt the host when conversion values, stored in registers ADC0_MAX and ADC0_MIN exceed a pre-selected range . A limit violation will be detected and an interrupt sent to the host when the sampled value stored in registers ADC0_MAX2, ADC0_MAX1 exceeds the maximum value set in registers ADC0_HILIM2, ADC0_HILIM1 or when the minimum sampled value stored in registers ADC0_MIN2, ADC0_MIN1 is lower than the minimum value programmed in registers and ADC0_HILIM2, ADC0_HILIM1.

Limit violations can not occur if Low Limit = 0x000 and High Limit = 0xFFF.

Table 3-62. ADC0 Limit Selection

ADC0_HILIM2 [Addr 0x63]								
Bit Number	B7	B6	B5	B4	B3	B2	B1	B0
Bit Name	RSVD637	RSVD636	RSVD635	RSVD634	HILIMA[11]	HILIMA[10]	HILIMA[9]	HILIMA[8]
ADC0_HILIM1 [Addr 0x64]								
Bit Name	HILIMA[7]	HILIMA[6]	HILIMA[5]	HILIMA[4]	HILIMA[3]	HILIMA[2]	HILIMA[1]	HILIMA[0]
ADC0_LOLIM2 [Addr 0x65]								
Bit Name	RSVD657	RSVD656	RSVD655	RSVD654	LOLIMA[11]	LOLIMA[10]	LOLIMA[9]	LOLIMA[8]
ADC0_LOLIM1 [Addr 0x66]								
Bit Name	LOLIMA[7]	LOLIMA[6]	LOLIMA[5]	LOLIMA[4]	LOLIMA[3]	LOLIMA[2]	LOLIMA[1]	LOLIMA[0]

The limit detection ADC conversion cycle should be configured with internal trigger and sampling sequences as follows:

1. To detect when an individual sample violates the max/min limits: Set $\overline{\text{RD}}$_MODE[1:0] to **00** and $\overline{\text{REPEAT}}$ to **1**. With these settings the ALU will compare the 10-bit ADC data returned from the SAR engine to the 10 bit values loaded in the ADC0_LIMIT values. The conversion sequence will repeat until either a violation interrupt occurs or the ADC0_EN bit is written to 0.

2. To detect when the average value violates the max/min limits: Set RD_MODE[1:0]) to **01**, **10** or **11** and REPEAT to **1**. At the end of the multiple sample conversion cycle the ALU will calculate the 12 bit average of the sample values by shifting the AVG[15:0] register (shift right 2 if 16 samples, shift right 3 if 32 samples and shift right 4 if 64 samples) . The shifted 12-bit average value is then compared to the value programmed in registers ADC0_LIMIT.

3.43.8 ADC Status Registers

The ADC conversion status for the timing engine is available in the ADC0_INT register. The ADC0_INT register is read-only. Reading the ADC0_INT register clears the ADC0INT bit in the STAT4 register (ADC0INT=0).

Table 3-63. ADC Conversion Status

ADC0_ INT [Addr 0x9A]								
Bit Number	B7	B6	B5	B4	B3	B2	B1	B0
Bit Name	ADC0_ DONE	ADC0_ ERROR	HILIM0_FLT	LOLIM0_FLT	RSVD9A3	RSVD9A2	ADC0_GPIO4ST	ADC0_GPIO2ST
Function	CONVERSION CYCLE STATUS	ADC_STATUS	HI LIMIT FAULT	LO LIMIT FAULT	NOT USED	NOT USED	GPIO4 LEVEL AT ADC0 EOC	GPIO2 LEVEL AT ADC0 EOC
When 0	BUSY	NO ERROR	NOT DETECTED	NO DETECTED	NOT USED	NOT USED	LOW	LOW
When 1	DONE	ERROR	DETECTED	DETECTED	NOT USED	NOT USED	HIGH	HIGH

3.44 GPIO

The TPS658629-Q1 integrates 4 general purpose push-pull ports (GPIOs) which can be configured as selectable inputs or outputs via register GPIOSET1 bits. When the GPIO is not configured the pull-down current source (2.5uA typ) is connected to the GPIOn pin. When configured as an input the GPIO can be set as inverting or non-inverting via bits GPIOnINV in the GPIOSET2 register.

When configured as an output, the GPIO output level is defined by bits GPIOnOUT in the GPIOSET2 register.

Table 3-64. GPIO Control(1)

GPIOSET1 [Addr 0x5D]								Default to **0**
Bit Number	B7	B6	B5	B4	B3	B2	B1	B0
Bit Name	GPIO4_MODE 1	GPIO4_MODE 0	GPIO3_MODE 1	GPIO3_MODE 0	GPIO2_MODE 1	GPIO2_MODE 0	GPIO1_MODE 1	GPIO1_MODE 0
Function	GPIO4 CONFIGURATION		GPIO3 CONFIGURATION		GPIO2 CONFIGURATION		GPIO1 CONFIGURATION	
GPIOSET2 [Addr 0x5E]								
Bit Number	B7	B6	B5	B4	B3	B2	B1	B0
Bit Name	GPIO4INV	GPIO3INV	GPIO2INV	GPIO1INV	GPIO4OUT	GPIO3OUT	GPIO2OUT	GPIO1OUT
Function	GPIO4 INPUT BUFFER MODE	GPIO3 INPUT BUFFER MODE	GPIO2 INPUT BUFFER MODE	GPIO1 INPUT BUFFER MODE	GPIO4 VOLTAGE, CONFIGURED AS OUTPUT	GPIO3 VOLTAGE, CONFIGURED AS OUTPUT	GPIO2 VOLTAGE, CONFIGURED AS OUTPUT	GPIO1 VOLTAGE, CONFIGURED AS OUTPUT
When 0	**NON-INVERTING**	**NON-INVERTING**	**NON-INVERTING**	**NON-INVERTING**	**LO**	**LO**	**LO**	**LO**
When 1	INVERTING	INVERTING	INVERTING	INVERTING	HI	HI	HI	HI

(1) All GPIO's default to the same configuration.

Table 3-65. GPIO4/3/2/1_MODE Settings

GPIOx_MODE[1]	**GPIOx_MODE[0]**	**GPIO4 Config**	**GPIO3 Config**	**GPIO2 Config**	**GPIO1 Config**
0	**0**	**Not Configured**	**Not Configured**	**Not Configured**	**Not Configured**
0	1	Output	Output	Output	Output
1	0	Input ADC Trigger	Input Not Used	Input ADC Trigger	Input PWM/PFM Control
1	1	Input LDO6/7/8 Enable	Input LDO2/3 Enable	Input LDO0/1 ENABLE	Input Not Used

3.45 STATUS REGISTERS

The system status is accessible via I²C registers listed below. The STATn registers are read only.

Table 3-66. Status Registers

ADC0_ INT [Addr 0x9A]								
Bit Number	B7	B6	B5	B4	B3	B2	B1	B0
Bit Name	ADC0_ DONE	ADC0_ ERROR	HILIM0_FLT	LOLIM0_FLT	RSVD9A3	RSVD9A2	ADC0_GPIO4ST	ADC0_GPIO2ST
Function	CONVERSION CYCLE STATUS	ADC_STATUS	HI LIMIT FAULT	LO LIMIT FAULT	NOT USED	NOT USED	GPIO4 LEVEL AT ADC0 EOC	GPIO2 LEVEL AT ADC0 EOC
When 0	BUSY	NO ERROR	NOT DETECTED	NOT DETECTED	NOT USED	NOT USED	LOW	LOW
When 1	DONE	ERROR	DETECTED	DETECTED	NOT USED	NOT USED	HIGH	HIGH
STAT1 [Addr 0xB9]								
Bit Number	B7	B6	B5	B4	B3	B2	B1	B0
Bit Name	BATSYSON	ACSWON	USBSWON	BATCHGSWON	RSVDB93	PACK_HOT	PACK_COLD	BATDET
Function	BAT TO SYS SWITCH ON/OFF STATUS	AC SWITCH ON/OFF STATUS	USB SWITCH ON/OFF STATUS	BAT TO VIN_CHG SWITCH ON/OFF STATUS	SPARE	PACK TEMP EXCEEDS HOT THRESHOLD	PACK TEMP BELOW COLD THRESHOLD	BATTTERY PACK TS THERMISTOR DETECTION
When 0	OFF	OFF	OFF	OFF	NOT USED	NO	NO	NOT DETECTED
When 1	ON	ON	ON	ON	NOT USED	YES	YES	DETECTED
STAT2 [Addr 0xBA]								
Bit Number	B7	B6	B5	B4	B3	B2	B1	B0
Bit Name	RSVD	RSVD	RSVD	RSVD	SLEEPTSHUT	RSVD	RSVD	COMPDET
Function					NOT USED			nHOTRST PULSE GENERATED REBOOT CYCLE
When 0					NOT USED			NO
When 1					NOT USED			YES
STAT3 [Addr 0xBB]								
Bit Number	B7	B6	B5	B4	B3	B2	B1	B0
Bit Name	SLEEPREQ	LOWSYS	RESUME	RTC_ALARM	ACDET	USBDET	AC_OVP	USB_OVP
Function	SLEEP REQUEST STATE SET	LOWSYS DETECTION STATUS	RESUME DETECTION STATUS	SPARE	AC INPUT POWER STATUS	USB INPUT POWER STATUS	AC INPUT OVP DETECTION	USB INPUT OVP DETECTION
When 0	NO	NOT DETECTED	NOT DETECTED	SPARE	NOT DETECTED	NOT DETECTED	NO OVP	NO OVP
When 1	YES	DETECTED	DETECTED	SPARE	DETECTED	DETECTED	OVP DETECTED	OVP DETECTED
STAT4 [Addr 0xBC]								
Bit Number	B7	B6	B5	B4	B3	B2	B1	B0
Bit Name	RSVDBC7	RSVDBC6	RSVDBC5	ADC0BUSY	RSVDBC3	RSVDBC2	RSVDBC1	ADC0INT
Function	SPARE	SPARE	SPARE	ADC ENGINE 0 MODE	SPARE	SPARE	SPARE	ADC ENGINE 0 INTERRUPT
When 0	SPARE	SPARE	SPARE	IDLE	SPARE	SPARE	SPARE	NOT ACTIVE
When 1	SPARE	SPARE	SPARE	BUSY	SPARE	SPARE	SPARE	ACTIVE

3.46 INTERRUPT CONTROLLER

The interrupt controller monitors the system status bus and internal signals continuously, generating an interrupt (INT = '0') when a system status change is detected. Individual bits that generated the interrupt will be set to **1** in the INT_ACK registers (read only registers), indicating which parameters generated the interrupt.

All the parameters monitored by the interrupt controller can be masked by registers INT_MASK (**0**=unmasked, **1**=masked). Masked parameters do not generate an interrupt when their state changes. When the host reads the INT_ACK registers, the interrupt is reset causing the INT pin to go to a logic 1 and the INT_ACK register bits are cleared.

The power good signals from the integrated supplies are level sensitive, and they will continue to cause an interrupt until the power good condition returns or the signal is masked. For non-masked power good parameters the INT_ACK bit will indicate the present state of the power good signals. The INTMASK register bits are cleared to **0** upon power-up.

Table 3-67. INT_ACK registers

INT_ACK1 [Addr 0xB5]								
Bit Number	B7	B6	B5	B4	B3	B2	B1	B0
Bit Name	ACK_PLDO7	ACK_PLDO6	ACK_PLDO5	ACK_PLDO4	ACK_PLDO3	ACK_PLDO2	ACK_PLDO1	ACK_PLDO0
INT_ACK2 [Addr 0xB6]								
Bit Name	ACK_PSM3	ACK_PSM2	ACK_PSM1	ACK_PSM0	ACK_PLDO9	ACK_PLDO8	ACK_ADC	ACK_ COMPDET(1)
INT_ACK3 [Addr 0xB7]								
Bit Name	ACK_PP	ACK_CHGTEMP	ACK_CHGSTAT	ACK_BATDET	ACK_ACDET	ACK_USBDET	ACKACUSBOVP	ACK_RTCALM1
INT_ACK4 [Addr 0xB8]								
Bit Name	RSVDB87	RSVDB86(2)	RSVDB85	RSVDB84	RSVDB83	ACK_RTCACM2	ACK_LOWSYS	ACK_RESUME

(1) ACK_COMPDET= ACK INT BY HOTRST FLAG SET
(2) RSVDB86= ACK INT BY SLEEP REQUEST

Table 3-68. INTMASK Registers

INTMASK1 [Addr 0xB0]								Default to **1 (Masked)**
Bit Name	IMASK_PLDO7	IMASK_PLDO6	IMASK_PLDO5	IMASK_PLDO4	IMASK_PLDO3	IMASK_PLDO2	IMASK_PLDO1	IMASK_PLDO0
INTMASK2 [Addr 0xB1]								Default to **1 (Masked)**
Bit Name	IMASK_PSM3	IMASK_PSM2	IMASK_PSM1	IMASK_PSM0	IMASK_PLDO9	IMASK_PLDO8	IMASKADC	RSVDB10
INTMASK3 [Addr 0xB2]								Default to **1 (Masked)**
Bit Name	IMASKSYSSW	IMASKACSW	IMASKUSBSW	IMASKBCHGSW	RSVDB23	IMASK_HOT	IMASK_COLD	IMASKBATDET
INTMASK4 [Addr 0xB3]								Default to **1 (Masked)**
Bit Name	RSVD	RSVD	RSVD	RSVD	IMASK_TSHUT	RSVD	IMASKRTCALM2	IMASK_COMP
INTMASK5 [Addr 0xB4]								Default to **1 (Masked)**
Bit Name	RSVDB47	IMASKLOWSYS	IMASKRESUME	IMASKRTCALM1	IMASKACDET	IMASKUSBDET	IMASKAC_OVP	IMASKUSB_OVP

The interrupt controller can monitor either level or edge transitions to generate the interrupt request:

PARAMETER	STATUS BIT	SET INT_ACK BIT ON	MASK reg/bit	INT_ACK reg/bit	ACK clear at
LDO0 power good fault	None	PGOOD FAULT DETECTED	INTMASK1 / IMASK_PLDO0	INT_ACK1 / ACK_LDO0	Read INT_ACK1
LDO1 power good fault	None	PGOOD FAULT DETECTED	INTMASK1 / IMASK_PLDO1	INT_ACK1 / ACK_PLDO1	Read INT_ACK1
LDO2 power good fault	None	PGOOD FAULT DETECTED	INTMASK1 / IMASK_PLDO2	INT_ACK1 / ACK_PLDO2	Read INT_ACK1
LDO3 power good fault	None	PGOOD FAULT DETECTED	INTMASK1 / IMASK_PLDO3	INT_ACK1 / ACK_PLDO3	Read INT_ACK1
LDO4 power good fault	None	PGOOD FAULT DETECTED	INTMASK1 / IMASK_PLDO4	INT_ACK1 / ACK_PLDO4	Read INT_ACK1
LDO5 power good fault	None	PGOOD FAULT DETECTED	INTMASK1 / IMASK_PLDO5	INT_ACK1 / ACK_PLDO5	Read INT_ACK1
LDO6 power good fault	None	PGOOD FAULT DETECTED	INTMASK1 / IMASK_PLDO6	INT_ACK1 / ACK_PLDO6	Read INT_ACK1
LDO7 power good fault	None	PGOOD FAULT DETECTED	INTMASK1 / IMASK_PLDO7	INT_ACK1 / ACK_PLDO7	Read INT_ACK1
LDO8 power good fault	None	PGOOD FAULT DETECTED	INTMASK2 / IMASK_PLDO8	INT_ACK2 / ACK_PLDO8	Read INT_ACK2
LDO9 power good fault	None	PGOOD FAULT DETECTED	INTMASK2 / IMASK_PLDO9	INT_ACK2 / ACK_PLDO9	Read INT_ACK2
SM0 power good fault	None	PGOOD FAULT DETECTED	INTMASK2 / IMASK_PSM0	INT_ACK2 / ACK_PSM0	Read INT_ACK2
SM1 power good fault	None	PGOOD FAULT DETECTED	INTMASK2 / IMASK_PSM1	INT_ACK2 / ACK_PSM1	Read INT_ACK2
SM2 power good fault	None	PGOOD FAULT DETECTED	INTMASK2 / IMASK_PSM2	INT_ACK2 / ACK_PSM2	Read INT_ACK2
SM3 over-voltage detection	None	SM3 OVER-VOLTAGE DETECTED	INTMASK2 / IMASK_PSM3	INT_ACK2 / ACK_PSM3	Read INT_ACK2
HOT RESET FLAG STATUS	STAT2 bit 0	HI→LO OR LO→HI	INTMASK4 / IMASK_COMP	INT_ACK2 / ACK_COMPDET	Read INT_ACK2
BATSYS switch STATUS	STAT1 bit 7	HI→LO OR LO→HI	INTMASK3 / IMASKSYSSW	INT_ACK3 / ACK_PP	Read INT_ACK3
ACSYS SWITCH STATUS	STAT1 bit 6	HI→LO OR LO→HI	INTMASK3 / IMASKACSW	INT_ACK3 /ACK_PP	Read INT_ACK3
USBSYS SWITCH STATUS	STAT1 bit 5	HI→LO OR LO→HI	INTMASK3 / IMASKUSBSW	INT_ACK3 /ACK_PP	Read INT_ACK3
BATCHG SW STATUS	STAT1 bit 4	HI→LO OR LO→HI	INTMASK3 / IMASK_TERM	INT_ACK3 /ACK_PP	Read INT_ACK3

PARAMETER	STATUS BIT	SET INT_ACK BIT ON	MASK reg/bit	INT_ACK reg/bit	ACK clear at
PACK HOT DETECTION	STAT1 bit 2	HI→LO OR LO→HI	INTMASK3 / IMASK_TSHUT	INT_ACK3 /ACK_CHGTEMP	Read INT_ACK3
PACK COLD DETECTION	STAT1 bit 1	HI→LO OR LO→HI	INTMASK3 / IMASKCHSTAT	INT_ACK3 /ACK_CHGTEMP	Read INT_ACK3
BATTERY INSERTION	STAT1 bit 0	HI→LO OR LO→HI	INTMASK3 / IMASKBATDET	INT_ACK3 /ACK_BATDET	Read INT_ACK3
SLEEP and tshut detected	STAT2 bit 3	HI→LO OR LO→HI	INTMASK4 / IMASK_TSHUT	INT_ACK3 /ACK_CHGSTAT	Read INT_ACK3
SLEEP REQUEST DETECTED	STAT3 bit7	LO→HI	INTMASK2/RSVDB10	INT_ACK4 / RSVDB86	Read INT_ACK4
AC DETection	STAT3 bit 3	HI→LO OR LO→HI	INTMASK5 / IMASKACDET	INT_ACK3 / ACK_ACDET	Read INT_ACK3
USB DETection	STAT3 bit 2	HI→LO OR LO→HI	INTMASK5 / IMAKSUSBDET	INT_ACK3 / ACKACUSBOVP	Read INT_ACK3
AC OVP	STAT3 bit 1	HI→LO OR LO→HI	INTMASK5 / IMAKSAC_OVP	INT_ACK3 / ACKACUSBOVP	Read INT_ACK3
USB OVP	STAT3 bit 0	HI→LO OR LO→HI	INTMASK5 / IMASKUSB_OVP	INT_ACK3 / ACKACUSBOVP	Read INT_ACK3
RTC ALARM1	NONE	ALARM1 DETECTED	INTMASK5 / IMAKSRTCALM1	INT_ACK3 / ACK_RTCALM1	Read INT_ACK3
RTC ALARM2	NONE	ALARM2 DETECTED	INTMASK4 / IMASKRTCALM2	INT_ACK4 / ACK_RTCALM2	Read INT_ACK4
RESUME command	STAT3 bit 5	HI→LO OR LO→HI	INTMASK5 / IMASKRESUME	INT_ACK4 / ACK_RESUME	Read INT_ACK4
LOWSYS detection	STAT3 bit 6	HI→LO OR LO→HI	INTMASK5 / IMASKLOWSYS	INT_ACK4 / ACK_LOWSYS	Read INT_ACK4
DADC0INT	STAT4 bit 0	LO→HI ONLY	INTMASK2 / IMASKADC	INT_ACK4 / ACK_ADC	Read ADC0_INT

3.47 DEVICE ID RAM REGISTER

This device has a unique 8-bit identifier stored in the read only register VERSIONID.

Table 3-69. Device ID Register

VERSIONID [Addr 0xCD]								
Bit Number	B7	B6	B5	B4	B3	B2	B1	B0
Bit Name	VCRC7	VCRC6	VCRC5	VCRC4	VCRC3	VCRC2	VCRC1	VCRC0
Device Number	VERSION IDENTIFICATION, FACTORY SET							
TPS658629-Q1	1	0	1	0	0	0	0	0

3.48 RAM MEMORY MAP

MEMORY AREA	ADDR	REGISTER NAME	R/W	DESCRIPTION
SUPPLY CONTROL AND VOLTAGE SETTING	0x10	SUPPLYENA	R/W	LDO2, SM0, SM1 ENABLE CONTROL
	0x11	SUPPLYENB	R/W	LDO2, SM0, SM1 ENABLE CONTROL
	0x12	SUPPLYENC	R/W	LDO0, LDO1. LDO3, LDO4, LDO6, LDO7, LDO8, SM2 ENABLE CONTROL
	0x13	SUPPLYEND	R/W	LDO0, LDO1. LDO3, LDO4, LDO6, LDO7, LDO8, SM2 ENABLE CONTROL
	0x14	SUPPLYENE	R/W	TPS658629-Q1 OPERATION MODE, LDO5, LDO9 ENABLE CONTROL
	0x20	VCC1	R/W	SM0, SM1, LDO2, LDO4 VOLTAGE SELECTION / CHANGE CONTROL
	0x21	VCC2	R/W	SM0, SM1, LDO2, LDO4 VOLTAGE SELECTION / CHANGE CONTROL
	0x23	SM1V1	R/W	SM1 VOLTAGE SETTING #1
	0x24	SM1V2	R/W	SM1 VOLTAGE SETTING #2
	0x25	SM1SL	R/W	SM1 SLEW RATE
	0x26	SM0V1	R/W	SM0 VOLTAGE SETTING #1
	0x27	SM0V2	R/W	SM0 VOLTAGE SETTING #2
	0x28	SM0SL	R/W	SM0 SLEW RATE
	0x29	LDO2AV1	R/W	LDO2 VOLTAGE SETTING #1
	0x2A	LDO2AV2	R/W	LDO2 VOLTAGE SETTING #2
	0x2F	LDO2BV1	R/W	LDO2 VOLTAGE SETTING #1
	0x30	LDO2BV2	R/W	LDO2 VOLTAGE SETTING #2
	0x32	LDO4V1	R/W	LDO4 VOLTAGE SETTING # 1
	0x33	LDO4V2	R/W	LDO4 VOLTAGE SETTING # 2
CONVERTER SETTINGS	0x41	SUPPLYV1	R/W	LDO1, LDO0 OUPUT VOLTAGE
	0x42	SUPPLYV2	R/W	SM2, LDO8 OUTPUT VOLTAGE
	0x43	SUPPLYV3	R/W	LDO6, LDO7 OUTPUT VOLTAGE
	0x44	SUPPLYV4	R/W	RTC_LDO, LDO3 OUTPUT VOLTAGE, RTC_LDO ON/OFF
	0x45	SUPPLYV5	R/W	SPARE
	0x46	SUPPLYV6	R/W	LDO5, LDO9 OUTPUT VOLTAGE
	0x47	SMODE1	R/W	SM0, SM1, SM2, PWM/PFM MODE SETTING
	0x48	SMODE2	R/W	SPARE
CONTROL SETTINGS	0x49	CHG1	R/W	CONTROL SETTINGS
	0x4A	CHG2	R/W	CONTROL SETTINGS
POWER PATH SETUP RAM	0x4C	PPATH2	R/W	OUT POWER PATH SETTINGS
TPS658629-Q1 SEQUENCING	0x4D	PGFLTMSK1	R/W	POWER GOOD FAULT MASK
	0x4E	PGFLTMSK2	R/W	POWER GOOD FAULT MASK
	0xCC	SPARE2	R/W	REBOOT CYCLE FLAG RESET

MEMORY AREA	ADDR hex	REGISTER NAME	ACC	DESCRIPTION
PERIPHERAL CONTROL RAM	0X50	RGB1FLASH	R/W	RGB1R/G/B DRIVERS FLASH MODE SETTINGS
	0X51	RGB1RED	R/W	RGB1 RED DRIVER INTENSITY CONTROL
	0X52	RGB1GREEN	R/W	RGB1 GREEN DRIVER INTENSITY CONTROL
	0X53	RGB1BLUE	R/W	RGB1 BLUE DRIVER INTENSITY CONTROL
	0X54	RGB2RED	R/W	RGB2 RED DRIVER INTENSITY CONTROL
	0X55	RGB2GREEN	R/W	RGB2 GREEN DRIVER INTENSITY CONTROL
	0X56	RGB2BLUE	R/W	RGB2 BLUE DRIVER INTENSITY CONTROL
	0X57	SM3_SET0	R/W	WHITE LED DUTY CYCLE SETTINGS
	0X58	SM3_SET1	R/W	WHITE LED DUTY CYCLE SETTINGS
	0X59	LED_PWM	R/W	LED_PWM DRIVER DUTY CYCLE SETTINGS
	0X5A	DIG_PWM	R/W	DIG_PWM DRIVER DUTY CYCLE SETTINGS
	0X5B	PWM	R/W	PWM DRIVER DUTY CYCLE SETTINGS
	0X5C	DIG_PWM1	R/W	DIG_PWM1 DRIVER DUTY CYCLE SETTINGS
	0X5D	GPIOSET1	R/W	GPIO CONFIGURATION
	0X5E	GPIOSET2	R/W	GPIO CONFIGURATION
ADC0 ENGINE SETUP RAM	0x60	ADCANLG	R/W	ADC INPUT BIAS AND FILTER CONTROL
	0X61	ADC0_SET	R/W	ADC0 CONVERSION CYCLE SETUP
	0X62	ADC0_WAIT	R/W	ADC0 CONVERSION CYCLE SETUP
	0X63	ADC0_HILIMIT2	R/W	ADC0 HI LIMIT THRESHOLD
	0X64	ADC0_HILIMIT1	R/W	ADC0 HI LIMIT THRESHOLD
	0X65	ADC0_LOLIMIT2	R/W	ADC0 LO LIMIT THRESHOLD
	0X66	ADC0_LOLIMIT1	R/W	ADC0 LO LIMIT THRESHOLD
	0X67	ADC0_DELAY	R/W	ADC0 TRIGGER MODE
ADC0 ENGINE DATA RAM	0x94	ADC0_SUM2	R	SUM OF ALL SAMPLES
	0x95	ADC0_SUM1	R	SUM OF ALL SAMPLES
	0x96	ADC0_MAX2	R	MAX SAMPLE VALUE
	0x97	ADC0_MAX1	R	MAX SAMPLE VALUE
	0x98	ADC0_MIN2	R	MIN SAMPLE VALUE
	0x99	ADC0_MIN1	R	MIN SAMPLE VALUE
	0x9A	ADC0_INT	R	ADC0 STATUS
INTERRUPT CONTROL RAM	0xB0	INT_MASK1	R/W	INT_MASK
	0xB1	INT_MASK2	R/W	INT MASK
	0xB2	INT_MASK3	R/W	INT MASK
	0xB3	INT_MASK4	R/W	INT MANAGEMENT
	0xB4	INT_MASK5	R/W	INT MANAGEMENT
	0xB5	INT_ACK1	R/W	INT MANAGEMENT REGISTER
	0xB6	INT_ACK2	R/W	INT MANAGEMENT REGISTER
	0xB7	INT_ACK3	R/W	INT MANAGEMENT REGISTER
	0xB8	INT_ACK4	R/W	INT MANAGEMENT REGISTER
SYSTEM STATUS RAM	0xB9	STAT1	R	POWER PATH SWITCHES, PACK STATUS
	0xBA	STAT2	R	STATUS
	0xBB	STAT3	R	RTC, INPUT POWER STATUS
	0xBC	STAT4	R	ADC STATUS

MEMORY AREA	ADDR hex	REGISTER NAME	ACC	DESCRIPTION
RTC	0xC0	RTC_CTRL	R/W	RTC CONTROL REGISTER
	0XC1	RTC ALARM		RTC ALARM
	0xC2			
	0xC3			
	0xC4			
	0xC5			
	0xC6	RTC COUNTER	R/W	RTC DATA
	0xC7			
	0xC8			
	0xC9			
	0xCA			
DEVICE ID	0XCD	VERSIONCRC	R	DEVICE IDENTIFICATION

4 APPLICATION INFORMATION

4.1 DC/DC CONVERTER OUTPUT FILTER

4.1.1 Inductor Selection

The typical value for the converter inductor is 2.2µH output inductor. Larger or smaller inductor values can be used to optimize the performance of the device for specific operation conditions. The selected inductor has to be rated for its DC resistance and saturation current. The DC resistance of the inductance will influence directly the efficiency of the converter. Therefore an inductor with lowest DC resistance should be selected for highest efficiency. See document SLVA157 for more information on inductor selection.

Equation 11 calculates the maximum inductor current under static load conditions. The saturation current of the inductor should be rated higher than the maximum inductor current as calculated with Equation 11. This is recommended because during heavy load transient the inductor current will rise above the calculated value.

$$\Delta I_L = Vout \times \frac{1 - \frac{Vout}{Vin}}{L \times f} \qquad I_{Lmax} = I_{outmax} + \frac{\Delta I_L}{2} \tag{11}$$

with:

f = Switching Frequency (2.25MHz typical)
L = Inductor Value
ΔI_L= Peak to Peak inductor ripple current
I_{Lmax} = Maximum Inductor current

The highest inductor current will occur at maximum Vin.

Open core inductors have a soft saturation characteristic and they can usually handle higher inductor currents versus a comparable shielded inductor. A more conservative approach is to select the inductor current rating just for the maximum switch current of the corresponding converter. It must be considered, that the core material from inductor to inductor differs and will have an impact on the efficiency especially at high switching frequencies.

Refer to Table 4-1 and the typical applications for possible inductors.

Table 4-1. Inductors

SUPPLY	INDUCTOR TYPE	INDUCTANCE [µH]	SUPPLIER	TYP DIMENSIONS [mm]
SM0	LPS4012-152	1.5	Coilcraft	4x4x1
	VLS4012-1R5N1R5	1.5	TDK	4x4x1
SM1	LPS4012-152	1.5	Coilcraft	4x4x1
	VLS4012-1R5N1R5	1.5	TDK	4x4x1
SM2	LPS4414-152MLx	1.5	Coilcraft	4x4x1.5
	1008PS-152Kx	1.5	Coilcraft	4x4x2.5
SM3	DO2010-472	4.7	Coilcraft	2x2x1
	VLS3012-47M1R0	4.7	TDK	3x3x1

4.1.2 Output Capacitor Selection

The advanced Fast Response voltage mode control scheme of the two converters allow the use of small ceramic capacitors with a typical value of 22µF, without having large output voltage under and overshoots during heavy load transients. Ceramic capacitors having low ESR values result in lowest output voltage ripple and are therefore recommended. Refer to for recommended components.

If ceramic output capacitors are used the capacitor RMS ripple current rating will always meet the application requirements. Just for completeness the RMS ripple current is calculated as:

$$I_{RMSCout} = Vout \times \frac{1 - \frac{Vout}{Vin}}{L \times f} \times \frac{1}{2 \times \sqrt{3}} \quad (12)$$

At nominal load current the inductive converters operate in PWM mode and the overall output voltage ripple is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by charging and discharging the output capacitor:

$$\Delta Vout = Vout \times \frac{1 - \frac{Vout}{Vin}}{L \times f} \times \left(\frac{1}{8 \times Cout \times f} + ESR \right) \quad (13)$$

Where the highest output voltage ripple occurs at the highest input voltage Vin.

At light load currents the converters operate in Power Save Mode and the output voltage ripple is dependent on the output capacitor value. The output voltage ripple is set by the internal comparator delay and the external capacitor. The typical output voltage ripple is less than 1% of the nominal output voltage.

4.1.3 Input Capacitor Selection

Because of the nature of the buck converter having a pulsating input current, a low ESR input capacitor is required for best input voltage filtering and minimizing the interference with other circuits caused by high input voltage spikes. The converters need a ceramic input capacitor of 10µF. The input capacitor can be increased without any limit for better input voltage filtering.

Table 4-2. Capacitors

22 µF	0805	TDK C2012X5R0J226MT	Ceramic
22 µF	0805	Taiyo Yuden JMK212BJ226MG	Ceramic
10 µF	0805	Taiyo Yuden JMK212BJ106M	Ceramic
10 µF	0805	TDK C2012X5R0J106M	Ceramic

4.2 XTAL OSCILLATOR PCB – GENERAL GUIDELINES

Table 4-3. External Crystal Specifications

EXTERNAL CRYSTAL REQUIREMENTS [TYP CRYSTAL – EPSON MC146]					
PARAMETER	**DESCRIPTION**	**MIN**	**TYP**	**MAX**	**UNIT**
F_{OSC}	Nominal crystal resonant frequency		32.768		kHz
Frequency Tolerance	$\Delta F/F_{OSC}$	–20		20	ppm
B	Parabolic Temp Co			0.04×10^{-6}	$1/°C^2$
ESR	Equivalent Series Resistance			65	kΩ
C_{LOAD}	Load Capacitance		7		pF
C_{SHUNT}	Shunt capacitance	0.5	0.8	1.2	pF
P_{DRIVE}	Drive power		0.5	1	µW
Aging		–3		3	ppm/Yr

The jitter observed in the OUT32K pin is heavily dependent on the board layout close to the XTAL1 and XTAL2 pins. The following layout/assembly procedures are recommended :

- Layout a good ground plane around the oscillator pins.
- Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.

- Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
- Use assembly materials and praxis to avoid any parasitic load on the oscillator XIN and XOUT pins.
- If conformal coating is used, ensure that it does not induce capacitive/resistive leakage between the oscillator pins.
- External capacitance is recommended for precision real-time clock applications.

4.3 APPLICATION CIRCUIT

4.3.1 Power Path, ADC, RTC and Ground Plane

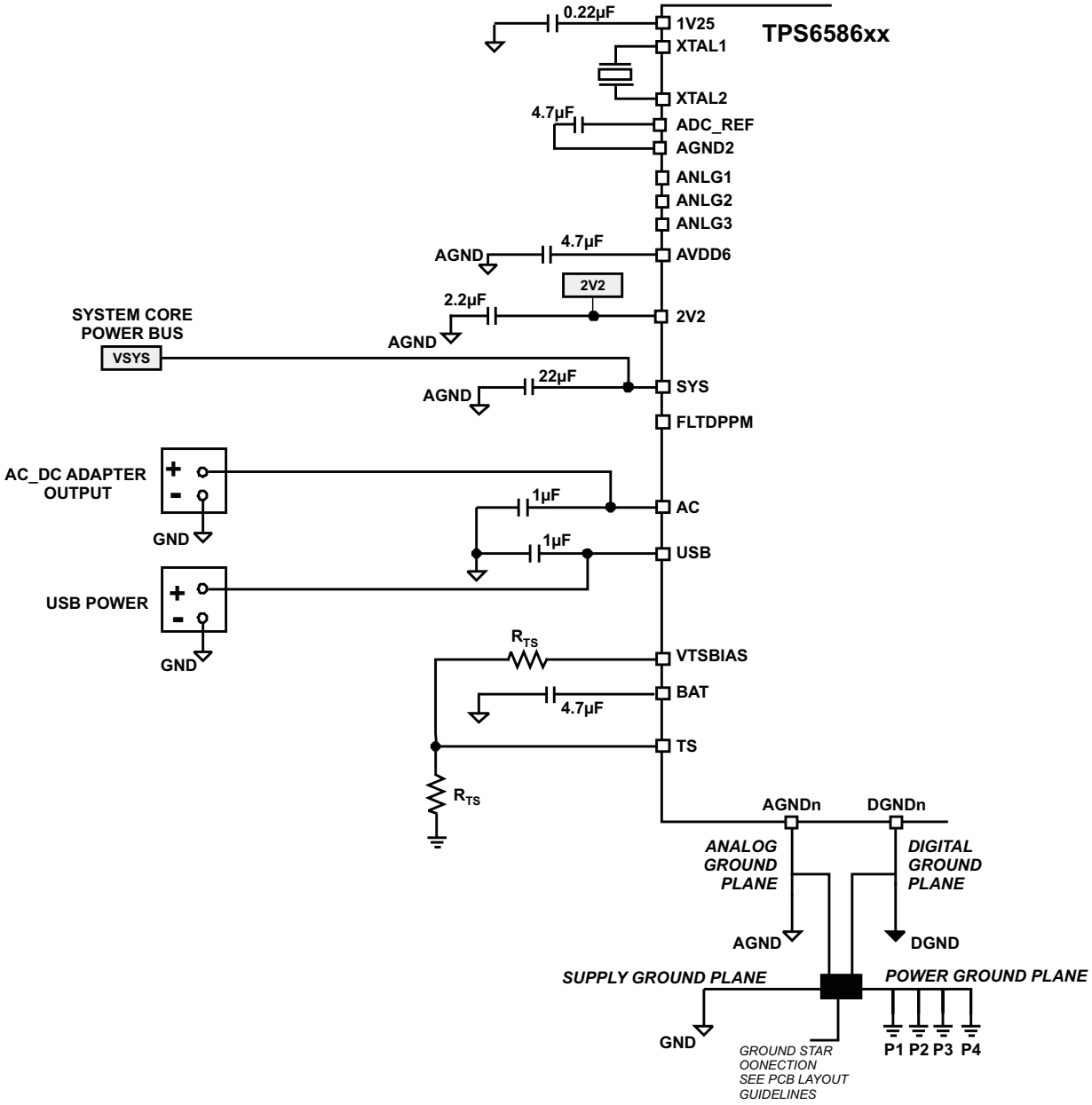
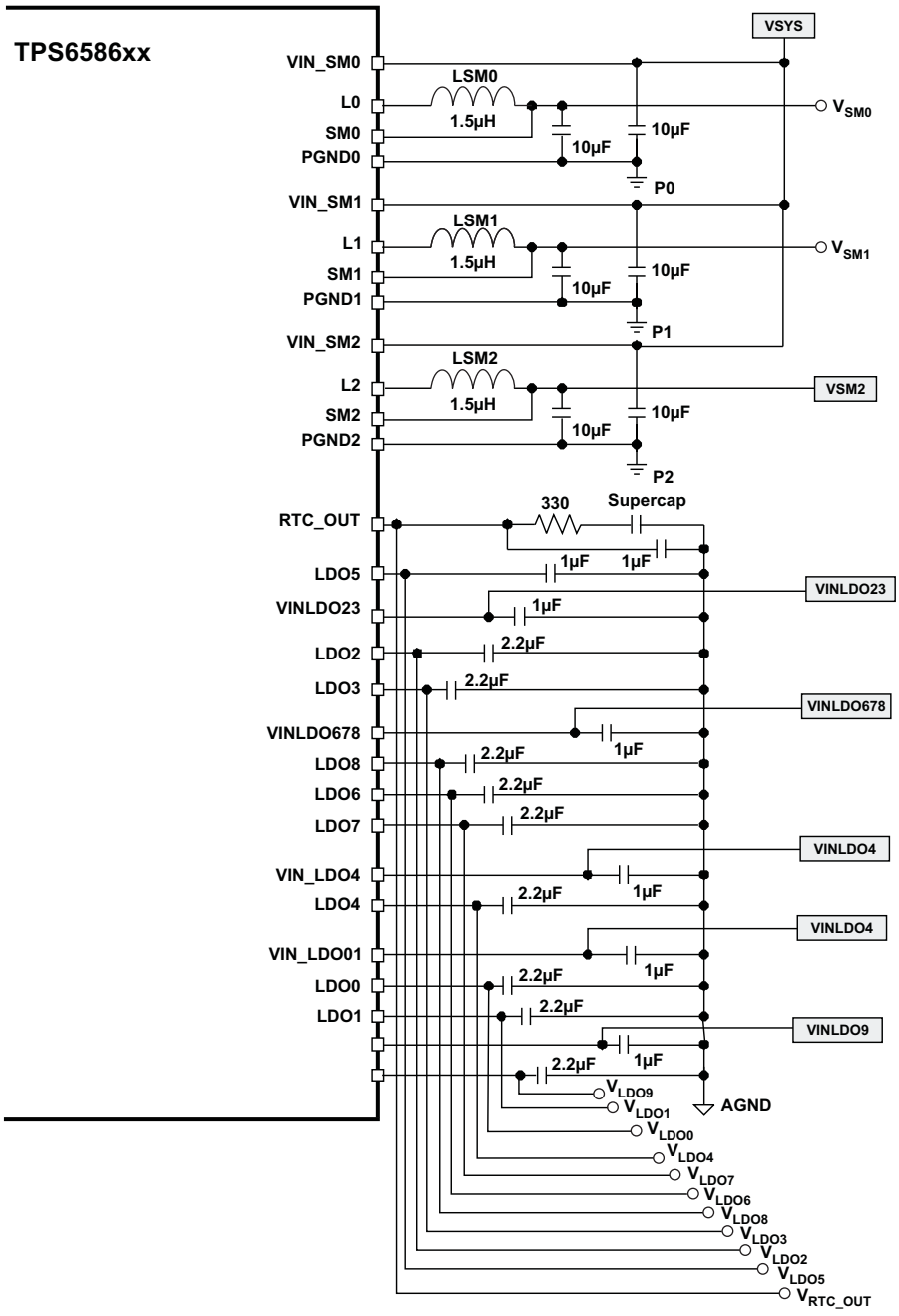


Figure 4-1. Power Path, ADC, RTC Connections

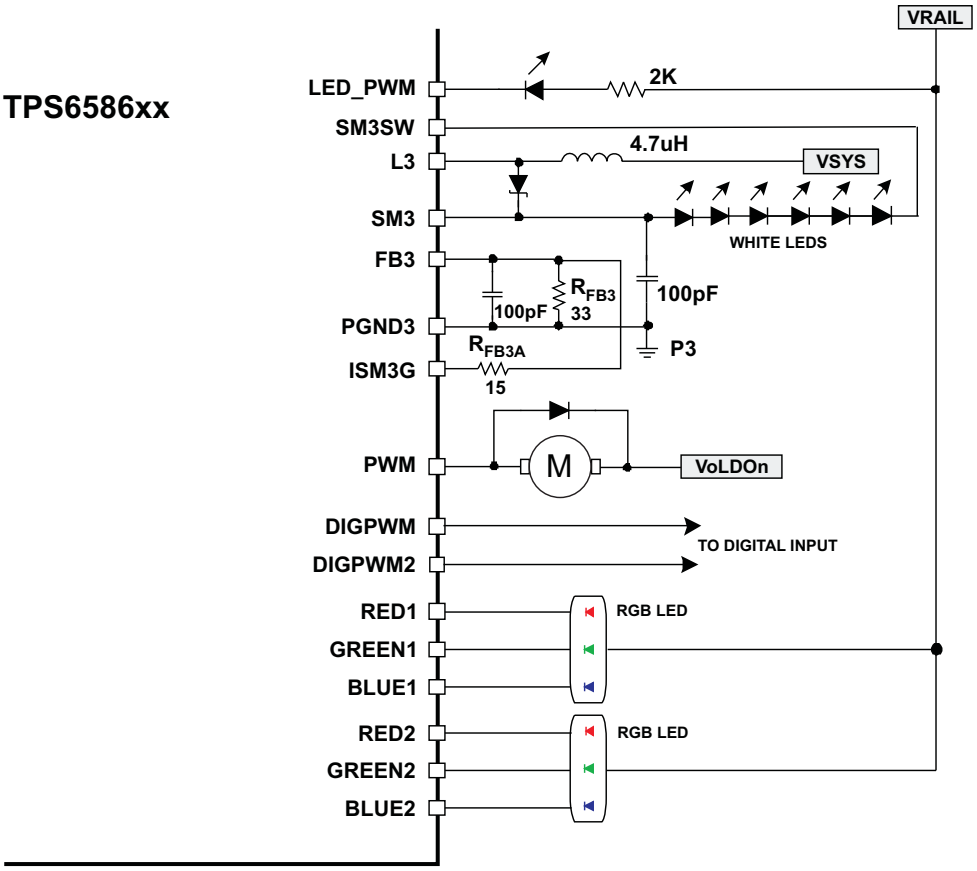
4.3.2 Integrated Supplies



(1) VIN_SMn pins must be always connected to VSYS .
(2) The supply input pins must be connected to VSYS or to the output of a supply which is powered from VSYS

Figure 4-2. Supply Rail Connections

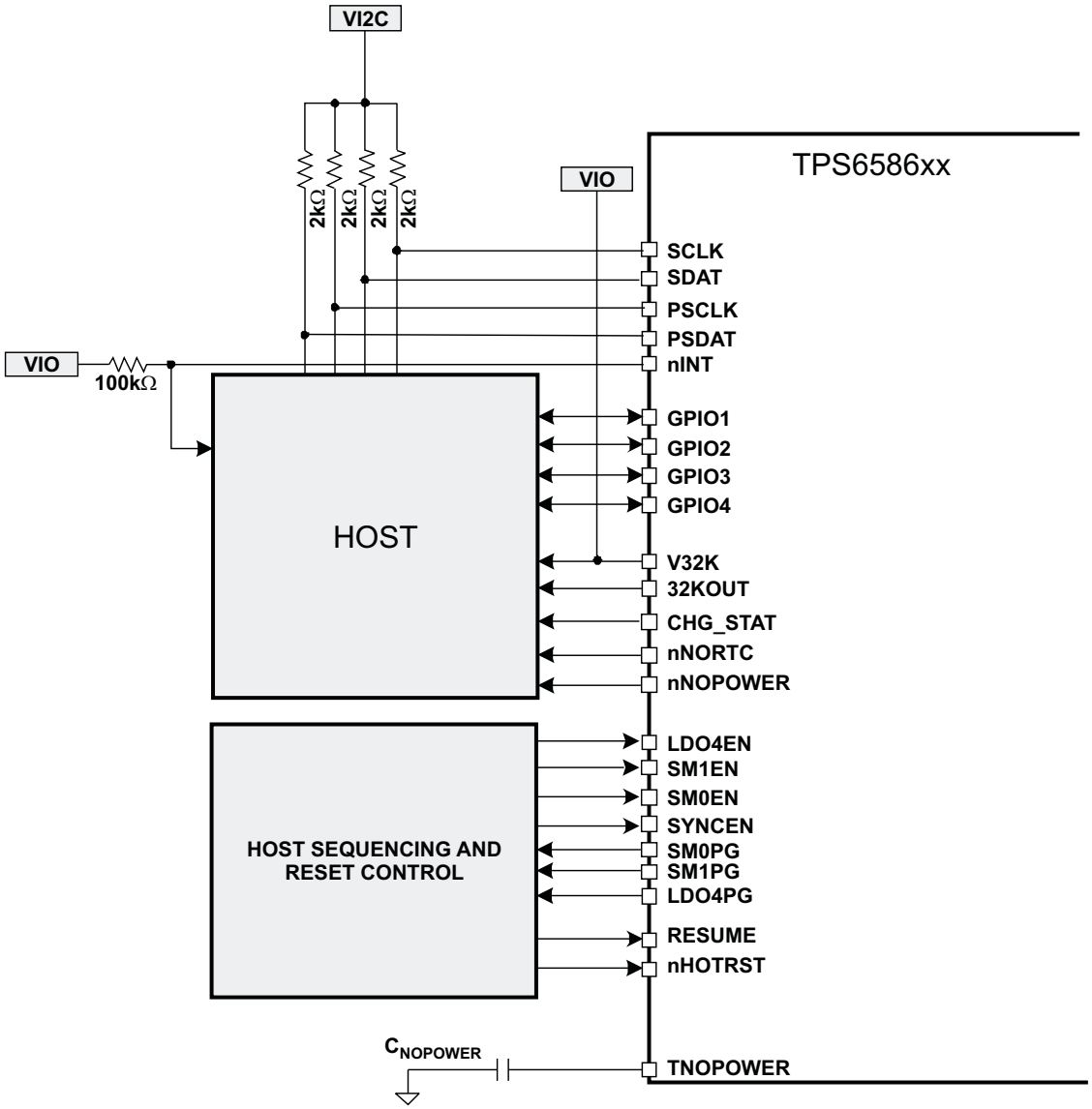
4.3.3 Display and Peripherals



(1) PWM pin shown as driving an external vibrator motor, with vibrator supply connected to LDOn output
(2) VRAIL can be the output of any of the TPS658629-Q1 integrated supplies or the SYS pin
(3) 1. DIGPWM, DIGPWM2 are push-pull outputs

Figure 4-3. Display and PWM Connections

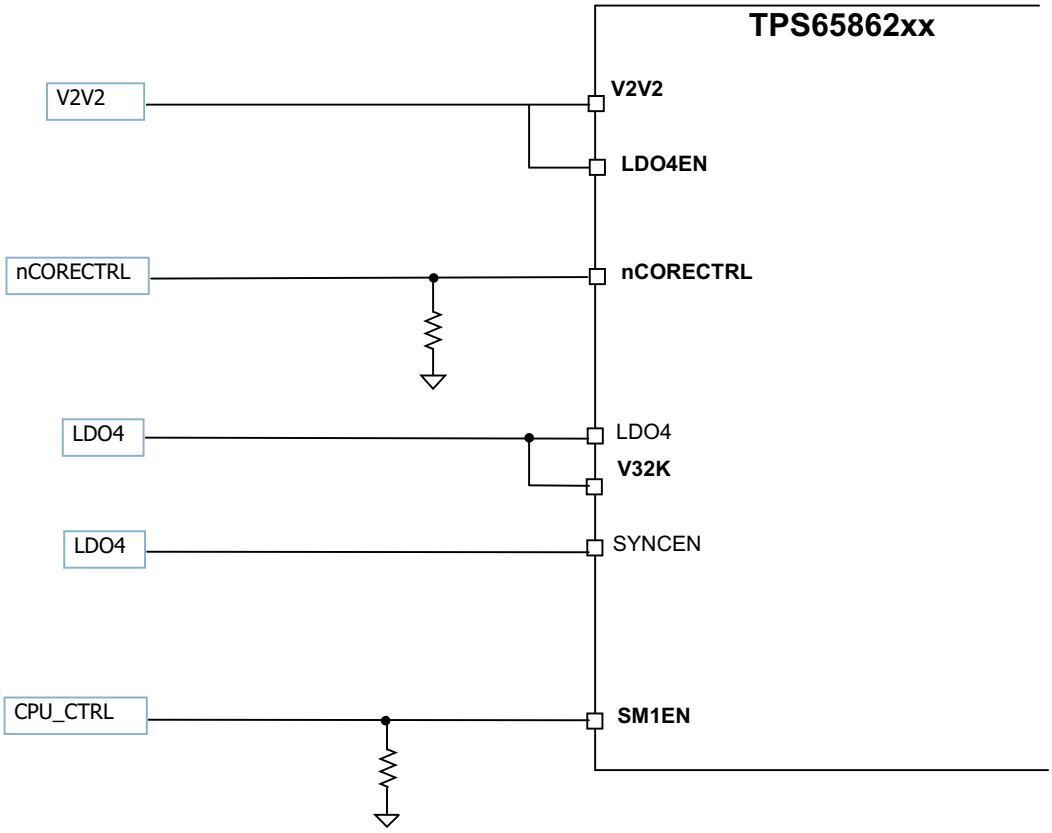
4.3.4 Host Connections



(1) Those are generic connections only
(2) VIO should be connected to the TPS658629-Q1 rail that powers the host I/O domain
(3) VI2C should be connected to 2v2 or to the TPS658629-Q1 rail that powers the host I^2C engine domain

Figure 4-4. Generic Host and Sequencing Circuit Connections

4.3.5 Sequence Connections



4.3.6 Sequence Timing (TPS658629-Q1)

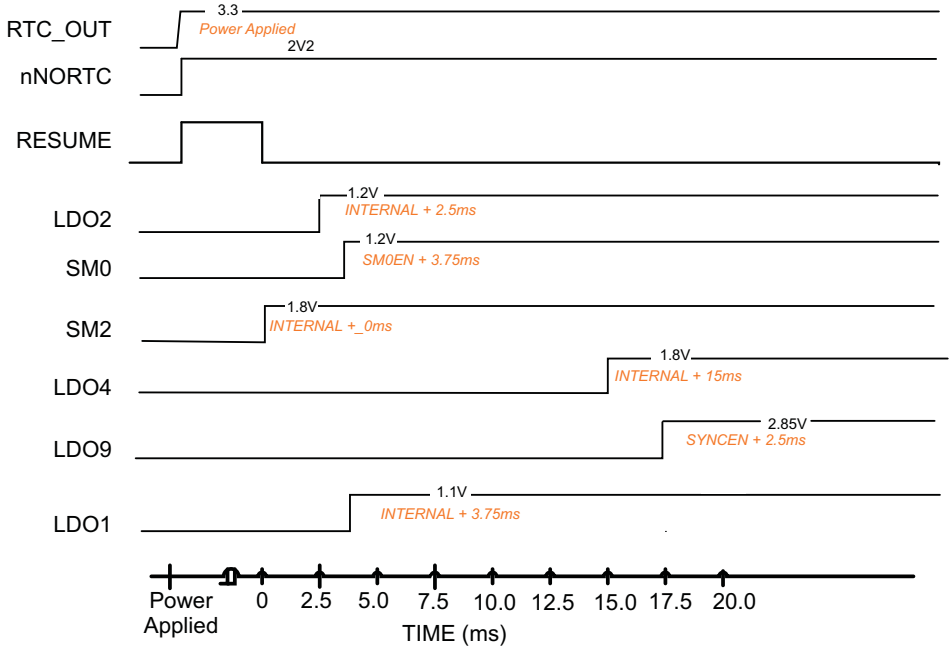


Figure 4-5. Sequence Timing

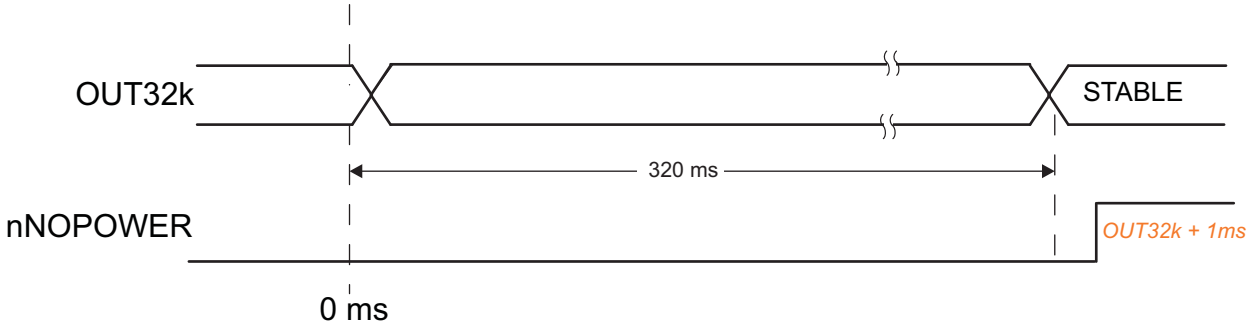


Figure 4-6. Sequence Timing

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (June, 2011) to Revision A **Page**

- 将 AEC-Q100 信息添加到了特性中。 1
- Changed max value of R_{DIG} to 175. 5
- Changed max value of $V_{(RTCGOOD)}$ to 145. 6
- Changed min value of I_{USB100} to 85. 8
- Changed min value of I_{USB500} to 380. 8
- Changed min value of I_{SC} to 310. 9
- Added rising to $V_{(OVP3)}$ test conditions description. 10
- Changed max value of $T_{SM3PWR(OFF)}$ to 500. 10

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS658629IZWSRQ1	ACTIVE	NFBGA	ZWS	169	1000	RoHS & Green	SNAGCU	Level-3-260C-168 HR	-40 to 85	TPS658629I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

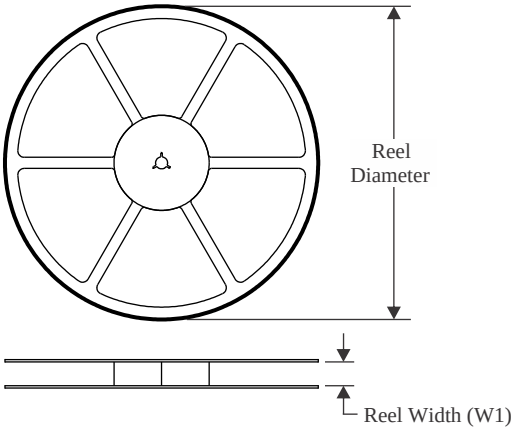
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

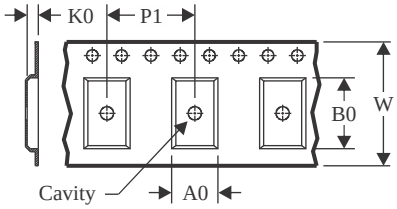
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

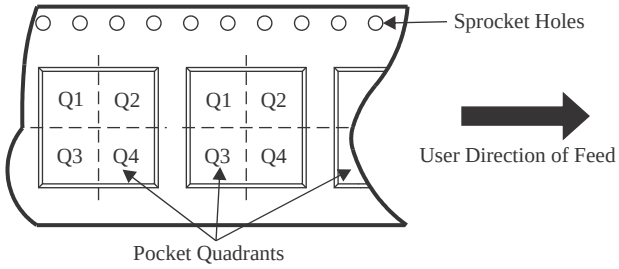


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

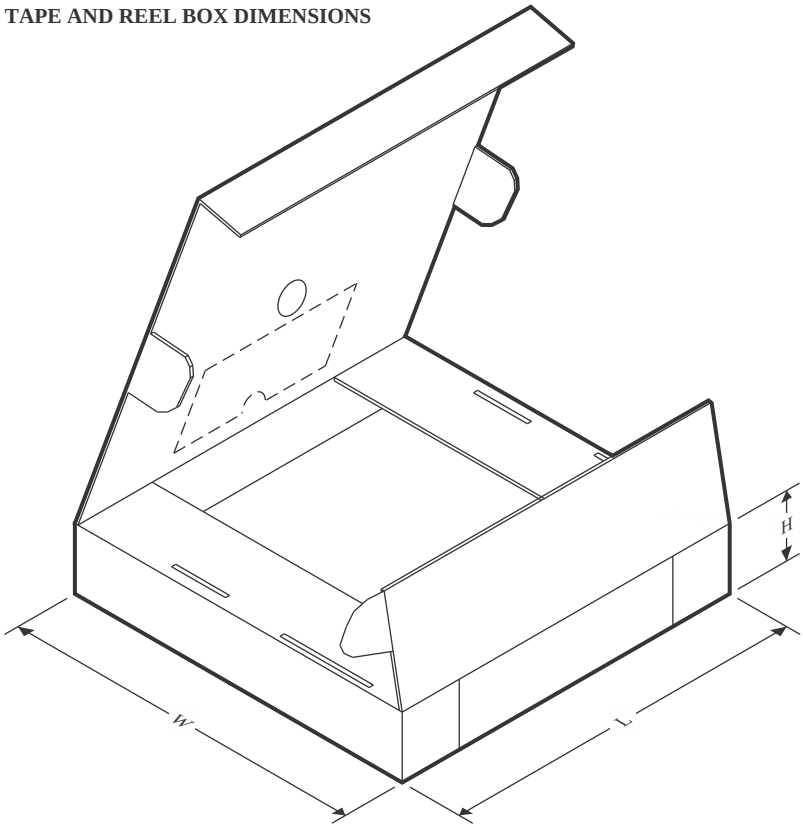
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS658629IZWSRQ1	NFBGA	ZWS	169	1000	330.0	24.4	12.35	12.35	2.3	16.0	24.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

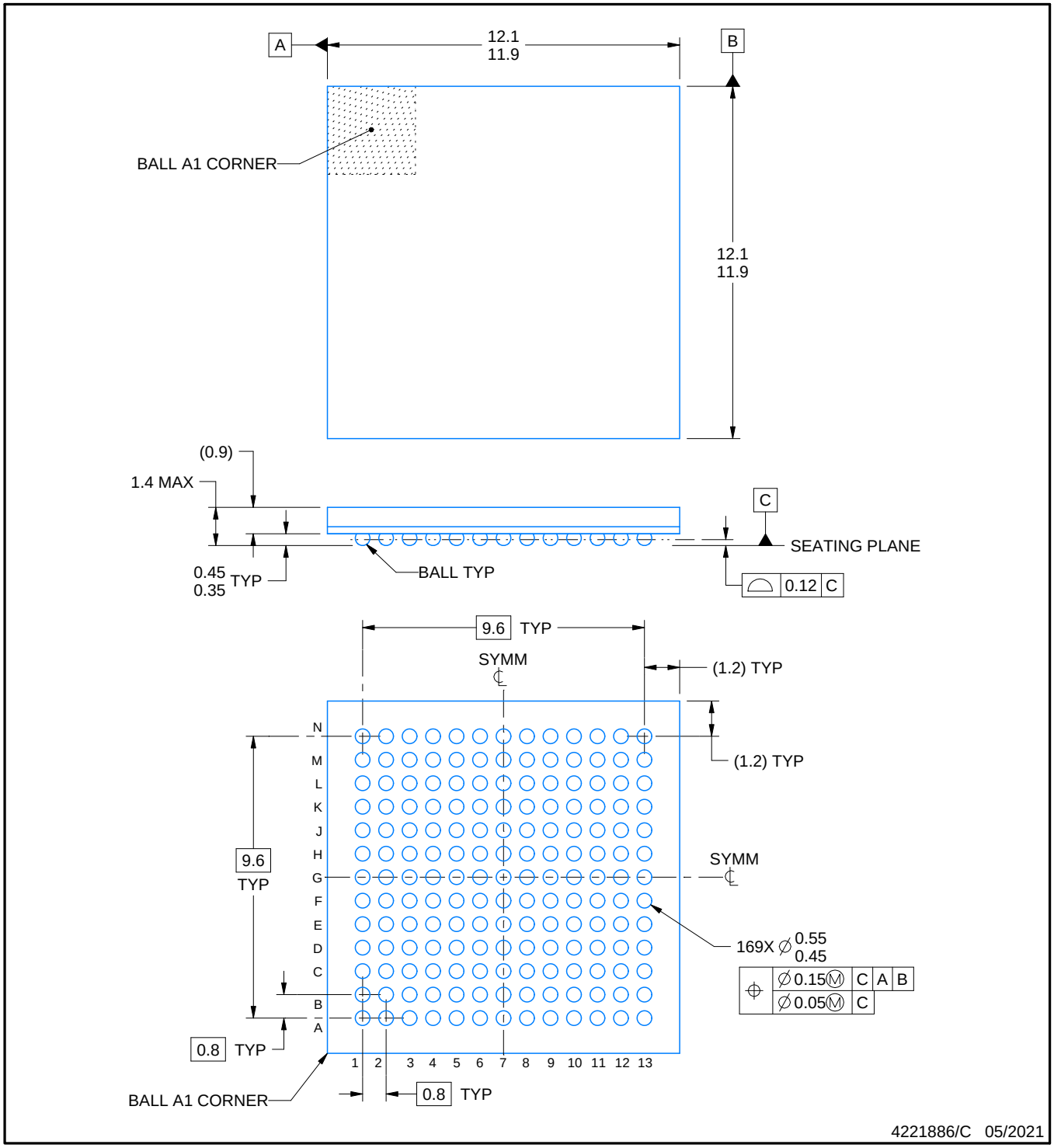
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS658629IZWSRQ1	NFBGA	ZWS	169	1000	336.6	336.6	41.3

PACKAGE OUTLINE

ZWS0169A

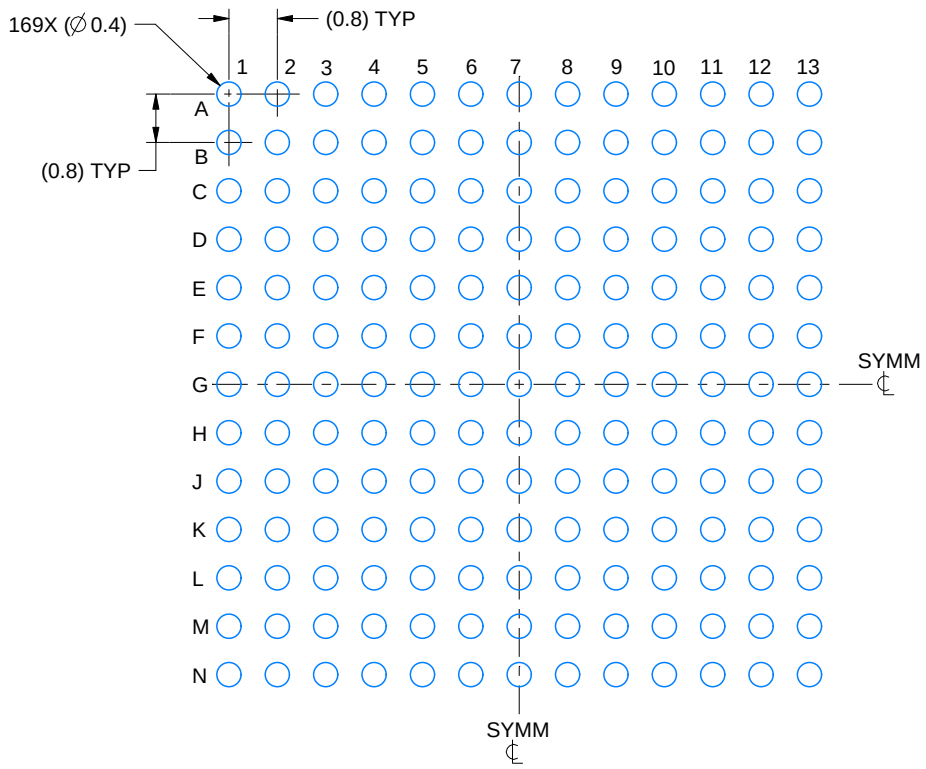
NFBGA - 1.4 mm max height

PLASTIC BALL GRID ARRAY

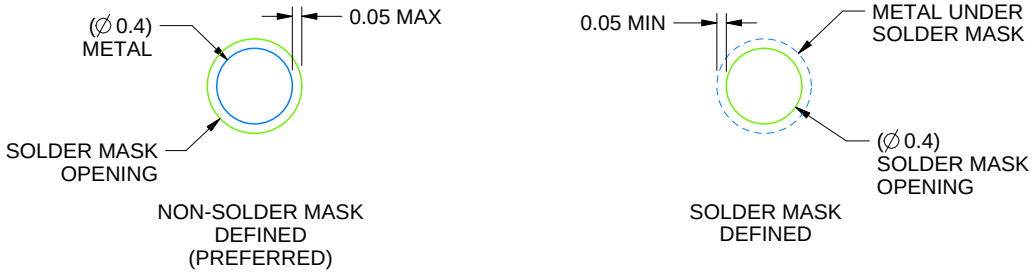


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS
NOT TO SCALE

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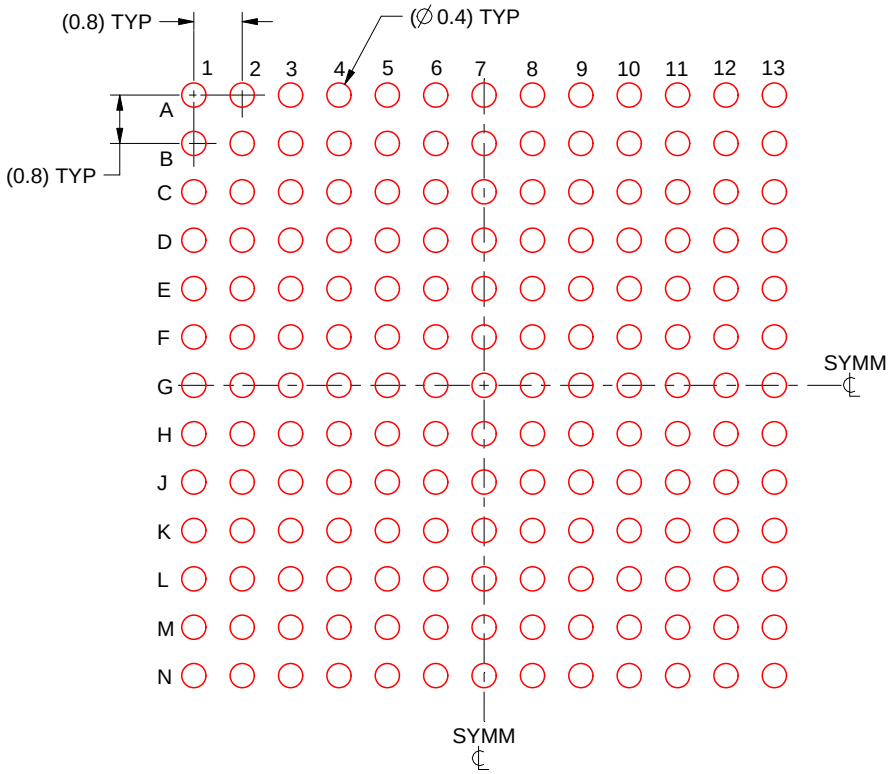
NOTES: (continued)

3. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For information, see Texas Instruments literature number SSZA002 (www.ti.com/lit/ssza002).



SOLDER PASTE EXAMPLE
BASED ON 0.15 mm THICK STENCIL
SCALE:8X

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NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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