

具有反向电流保护功能的 TPS737-Q1 1A 低压降稳压器

1 特性

- 符合汽车类应用要求
- 具有符合 AEC-Q100 标准的下列特性：
 - 器件温度等级 1: -40°C 至 125°C 环境温度范围
 - 器件 HBM ESD 分类等级 2
 - 器件 CDM ESD 分类等级 C4A
- 与 $1\mu\text{F}$ 或更大的陶瓷输出电容器一起工作时保持稳定
- 输入电压范围: 2.2V 至 5.5V
- 超低压降: 1A 为 130mV (典型值)
- 即使使用仅为 $1\mu\text{F}$ 的输出电容器, 也能实现出色的负载瞬态响应
- NMOS 拓扑可提供低反向漏电流
- 初始精度为 1%
- 整个线路、负载和温度范围内的精度达 3%
- 关断模式下静态电流小于 20nA (典型值)
- 通过热关断和电流限制实现故障保护
- 提供了多个输出电压版本

2 应用

- 适用于 DSP、FPGA、ASIC 和微处理器的负载点调节
- 适用于开关电源的后置稳压
- 便携式和电池供电类设备

3 说明

TPS737xx-Q1 线性低压降 (LDO) 稳压器系列在电压跟随器配置中使用了 NMOS 旁路元件。该拓扑结构对输出电容值和等效串联电阻 (ESR) 的敏感度相对较低, 从而实现多种负载配置。即使使用 $1\mu\text{F}$ 的小型陶瓷输出电容器, 也能实现出色的负载瞬态响应。NMOS 拓扑结构也可实现极低压降。

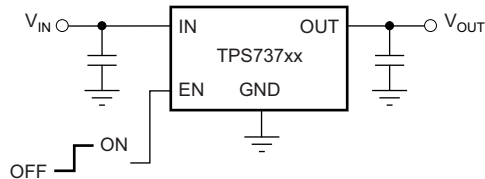
TPS737xx-Q1 系列利用先进的 BiCMOS 工艺实现高精度, 同时提供极低的压降和低接地引脚电流。未启用时的电流消耗低于 20nA, 适用于便携式应用。这些器件受到热关断和折返电流限制的保护。

器件信息(1)

器件型号	封装	封装尺寸 (标称值)
TPS737-Q1	VSON (8)	3.00mm x 3.00mm

(1) 要了解所有可用封装, 请参阅数据表末尾的可订购产品附录。

典型应用电路



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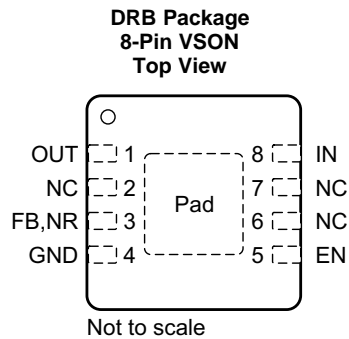
4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision A (July 2016) to Revision B	Page
• 已更改 更改了器件温度等级、AEC-Q100 “特性” 项目符号	1
• 已删除 删除了子项目符号（从“特性” 输出电压版本 项目符号中）	1

Changes from Original (December 2008) to Revision A	Page
• 已添加 添加了器件信息表、引脚配置和功能部分、规格部分、ESD 额定值表、建议运行条件表、热性能信息表、详细 说明 部分、应用和实施部分、电源建议部分、布局部分、器件和文档支持部分以及机械、封装和可订购信息部分	1
• 已删除 删除了订购信息表，请参阅数据表末尾的 POA.....	1

5 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	5	I	Driving the enable pin (EN) high turns on the regulator. Driving this pin low puts the regulator into shutdown mode. See Enable Pin and Shutdown for more details. EN must not be left floating and can be connected to IN if not used.
FB	3	I	Adjustable voltage version only. This is the input to the control loop error amplifier, and it is used to set the output voltage of the device.
GND	4, Pad	G	Ground
IN	8	I	Unregulated input supply
NR	3	—	Fixed voltage versions only. Connecting an external capacitor to this pin bypasses noise generated by the internal bandgap, reducing output noise to very low levels.
OUT	1	O	Regulator output. A 1- μ F or larger capacitor of any type is required for stability.
NC	2, 6, 7	—	No internal connection

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Input supply voltage		-0.3	6	V
Enable voltage		-0.3	6	V
Output voltage		-0.3	5.5	V
Input voltage	NR or FB pin	-0.3	6	V
Peak output current		Internally limited		
Output short-circuit duration		Indefinite		
Junction temperature range, T _J		-55	150	°C
Storage temperature, T _{stg}		-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002 ⁽¹⁾	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{IN}	Input supply voltage	2.2	5.5	V
I _{OUT}	Output current	0	1	A
T _J	Operating junction temperature	-40	125	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS737xx-Q1	UNIT
		DRB (VSON)	
		8 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	52.2	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	59.4	°C/W
R _{θJB}	Junction-to-board thermal resistance	19.3	°C/W
ψ _{JT}	Junction-to-top characterization parameter	2	°C/W
ψ _{JB}	Junction-to-board characterization parameter	19.3	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	11.8	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics application report](#).

6.5 Electrical Characteristics

over operating temperature range ($T_J = -40^\circ\text{C}$ to 125°C), $V_{IN} = (V_{OUT(nom)} + 1\text{ V})^{(1)}$, $I_{OUT} = 10\text{ mA}$, $V_{EN} = 2.2\text{ V}$, $C_{OUT} = 2.2\text{ }\mu\text{F}$ (unless otherwise noted). Typical values are at $T_J = 25^\circ\text{C}$.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
V_{IN}	Input voltage range ⁽¹⁾⁽²⁾		2.2		5.5	V	
V_{FB}	Internal reference (TPS73701)	$T_J = 25^\circ\text{C}$	1.192	1.2	1.216	V	
V_{OUT}	Output voltage range (TPS73701) ⁽³⁾		V_{FB}		$5.5 - V_{DO}$	V	
	Accuracy ⁽¹⁾⁽⁴⁾	Nominal	$T_J = 25^\circ\text{C}$	-1		1	%
			$5.36\text{ V} < V_{IN} < 5.5\text{ V}$, $V_{OUT} = 5.08\text{ V}$, $10\text{ mA} < I_{OUT} < 800\text{ mA}$, $-40^\circ\text{C} < T_J < 85^\circ\text{C}$, TPS73701		-2		
	Over V_{IN} , I_{OUT} , and temperature	$V_{OUT} + 0.5\text{ V} \leq V_{IN} \leq 5.5\text{ V}$, $10\text{ mA} \leq I_{OUT} \leq 1\text{ A}$		-3	± 0.5	3	
$\Delta V_{OUT}\% / \Delta V_{IN}$	Line regulation ⁽¹⁾	$V_{OUT(nom)} + 0.5\text{ V} \leq V_{IN} \leq 5.5\text{ V}$		0.01		%/V	
$\Delta V_{OUT}\% / \Delta I_{OUT}$	Load regulation	$1\text{ mA} \leq I_{OUT} \leq 1\text{ A}$		0.002		%/mA	
		$10\text{ mA} \leq I_{OUT} \leq 1\text{ A}$		0.0005			
V_{DO}	Dropout voltage ⁽⁵⁾ ($V_{IN} = V_{OUT(nom)} - 0.1\text{ V}$)	$I_{OUT} = 1\text{ A}$		130	500	mV	
$Z_O(\text{DO})$	Output impedance in dropout	$2.2\text{ V} \leq V_{IN} \leq V_{OUT} + V_{DO}$		0.25		Ω	
I_{CL}	Output current limit	$V_{OUT} = 0.9 \times V_{OUT(nom)}$	1.05	1.6	2.2	A	
I_{SC}	Short-circuit current	$V_{OUT} = 0\text{ V}$		450		mA	
I_{REV}	Reverse leakage current ⁽⁶⁾ ($-I_{IN}$)	$V_{EN} \leq 0.5\text{ V}$, $0\text{ V} \leq V_{IN} \leq V_{OUT}$		0.1		μA	
I_{GND}	GND pin current	$I_{OUT} = 10\text{ mA}$ (I_Q)		400		μA	
		$I_{OUT} = 1\text{ A}$		1300			
I_{SHDN}	Shutdown current (I_{GND})	$V_{EN} \leq 0.5\text{ V}$, $V_{OUT} \leq V_{IN} \leq 5.5\text{ V}$		20		nA	
I_{FB}	FB pin current (TPS73701)			0.1	0.6	μA	
PSRR	Power-supply rejection ratio (ripple rejection)	$f = 100\text{ Hz}$, $I_{OUT} = 1\text{ A}$		58		dB	
		$f = 10\text{ kHz}$, $I_{OUT} = 1\text{ A}$		37			
V_N	Output noise voltage BW = 10 Hz to 100 kHz	$C_{OUT} = 10\text{ }\mu\text{F}$		$27 \times V_{OUT}$		μV_{RMS}	
t_{STR}	Startup time	$V_{OUT} = 3\text{ V}$, $R_L = 30\text{ }\Omega$, $C_{OUT} = 1\text{ }\mu\text{F}$		600		μs	
$V_{EN(HI)}$	EN pin high (enabled)		1.7		V_{IN}	V	
$V_{EN(LO)}$	EN pin low (shutdown)		0		0.5	V	
$I_{EN(HI)}$	EN pin current (enabled)	$V_{EN} = 5.5\text{ V}$		20		nA	
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing		160		$^\circ\text{C}$	
		Reset, temperature decreasing		140			
T_J	Operating junction temperature		-40		125	$^\circ\text{C}$	

(1) Minimum $V_{IN} = V_{OUT} + V_{DO}$ or 2.2 V , whichever is greater.

(2) For $V_{OUT(nom)} < 1.6\text{ V}$, when $V_{IN} \leq 1.6\text{ V}$, the output locks to V_{IN} and may result in an overvoltage condition on the output. To avoid this situation, disable the device before powering down V_{IN} .

(3) TPS73701 is tested at $V_{OUT} = 1.2\text{ V}$.

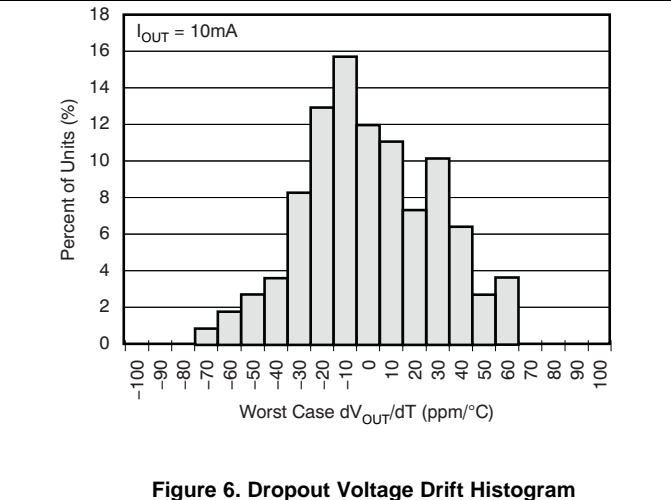
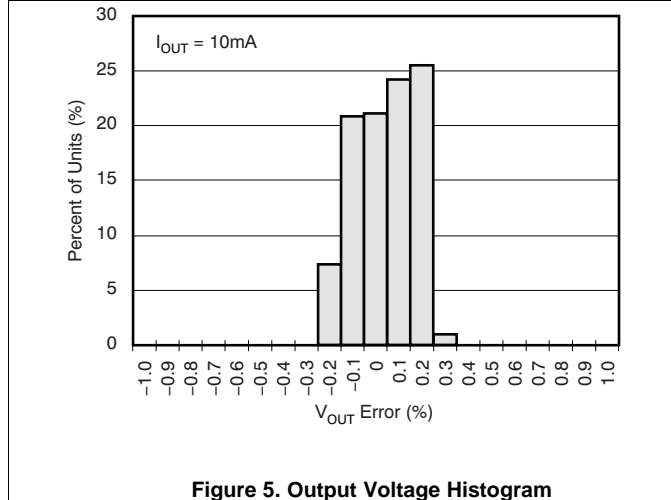
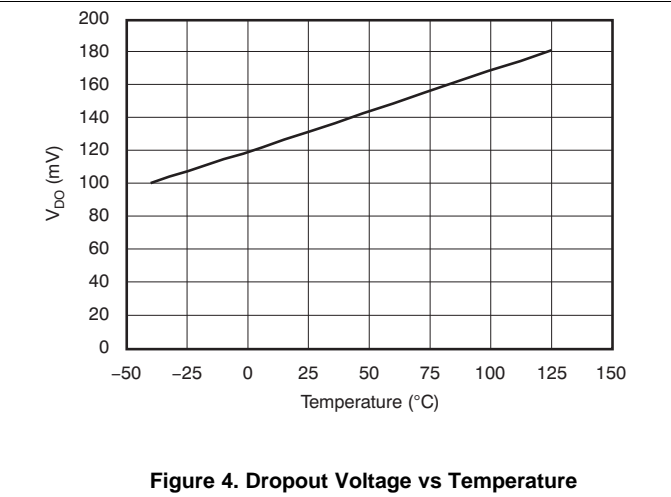
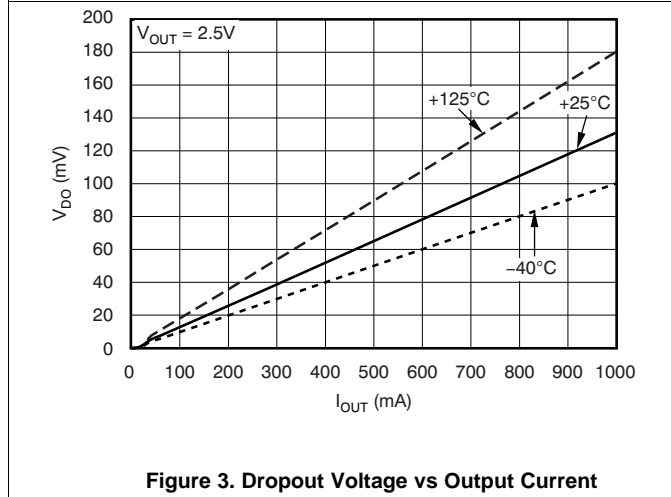
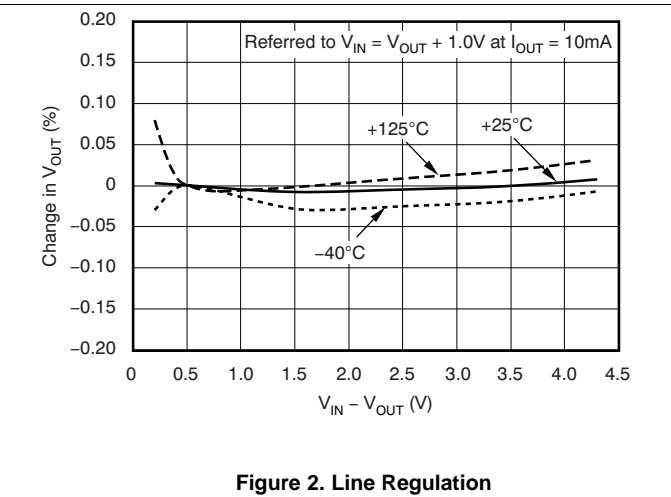
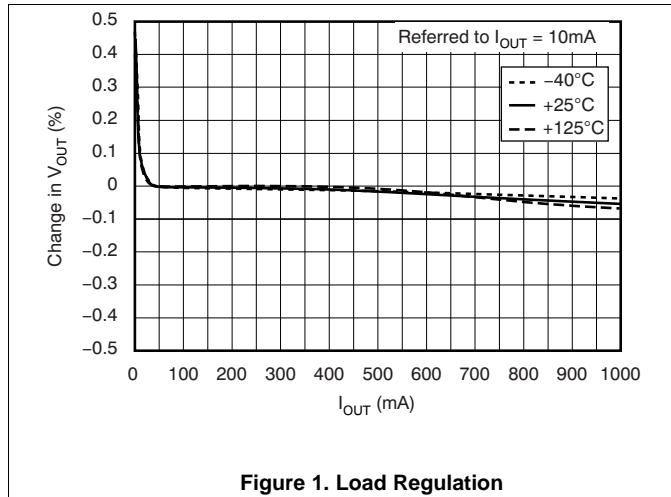
(4) Tolerance of external resistors not included in this specification.

(5) V_{DO} is not measured for fixed output versions with $V_{OUT(nom)} < 2.3\text{ V}$, because minimum $V_{IN} = 2.2\text{ V}$.

(6) Fixed-voltage versions only; see the [Reverse Current](#) section for more information.

6.6 Typical Characteristics

$T_J = 25^\circ\text{C}$, $V_{IN} = (V_{OUT(nom)} + 1\text{ V})$, $I_{OUT} = 10\text{ mA}$, $V_{EN} = 2.2\text{ V}$, $C_{OUT} = 2.2\text{ }\mu\text{F}$ (unless otherwise noted)



Typical Characteristics (continued)

$T_J = 25^\circ\text{C}$, $V_{IN} = (V_{OUT(nom)} + 1\text{ V})$, $I_{OUT} = 10\text{ mA}$, $V_{EN} = 2.2\text{ V}$, $C_{OUT} = 2.2\text{ }\mu\text{F}$ (unless otherwise noted)

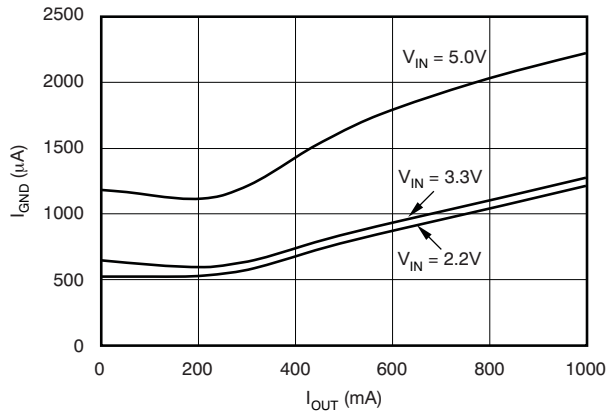


Figure 7. Ground Pin Current vs Output Current

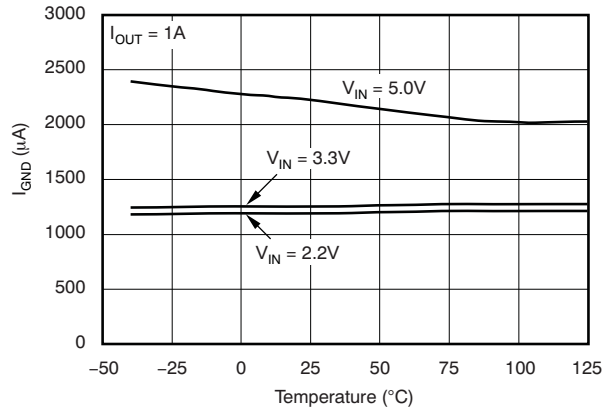


Figure 8. Ground Pin Current vs Temperature

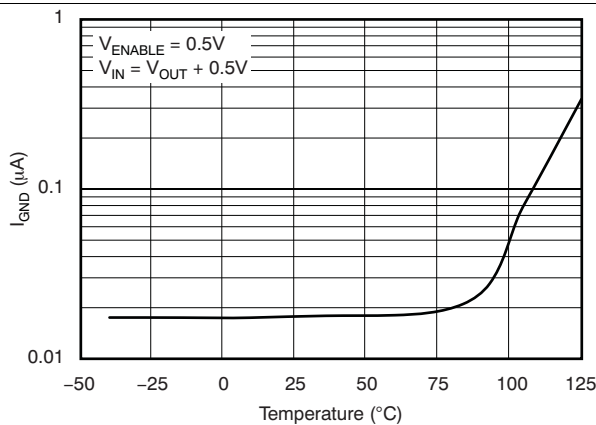


Figure 9. Ground Pin Current In Shutdown vs Temperature

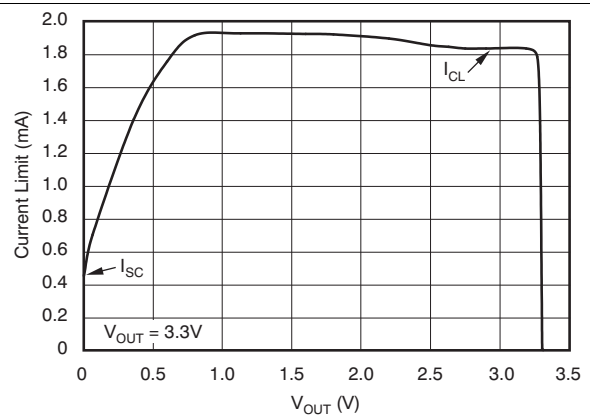


Figure 10. Current Limit vs V_{OUT} (Foldback)

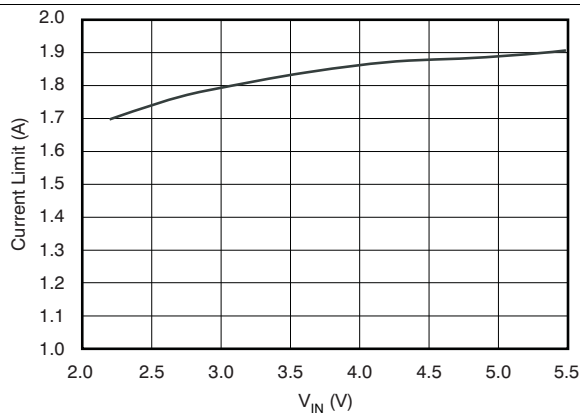


Figure 11. Current Limit vs V_{IN}

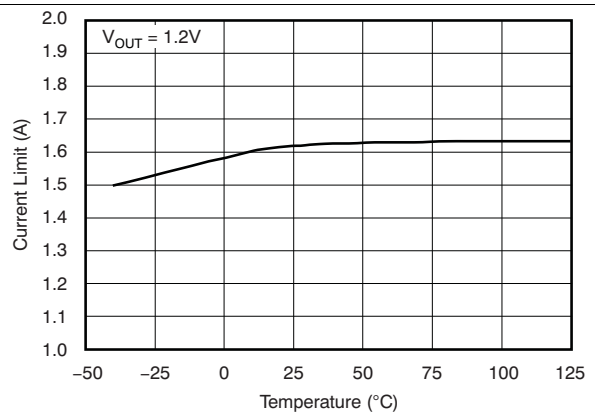


Figure 12. Current Limit vs Temperature

Typical Characteristics (continued)

$T_J = 25^\circ\text{C}$, $V_{IN} = (V_{OUT(nom)} + 1\text{ V})$, $I_{OUT} = 10\text{ mA}$, $V_{EN} = 2.2\text{ V}$, $C_{OUT} = 2.2\text{ }\mu\text{F}$ (unless otherwise noted)

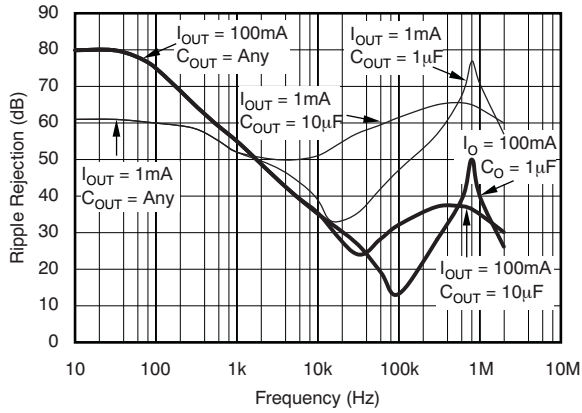


Figure 13. PSRR (Ripple Rejection) vs Frequency

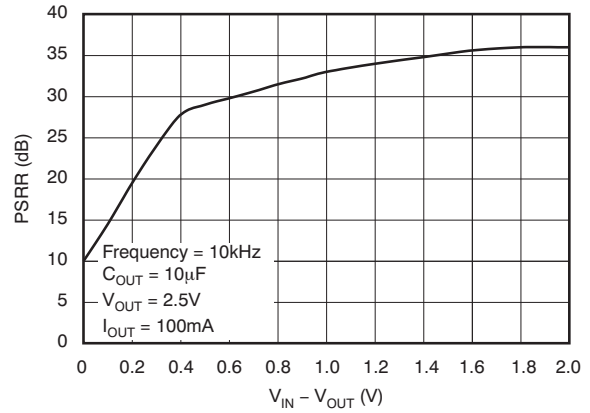


Figure 14. PSRR (Ripple Rejection) vs $V_{IN} - V_{OUT}$

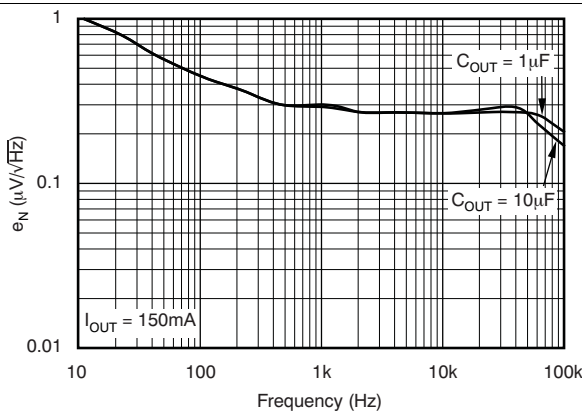


Figure 15. Noise Spectral Density

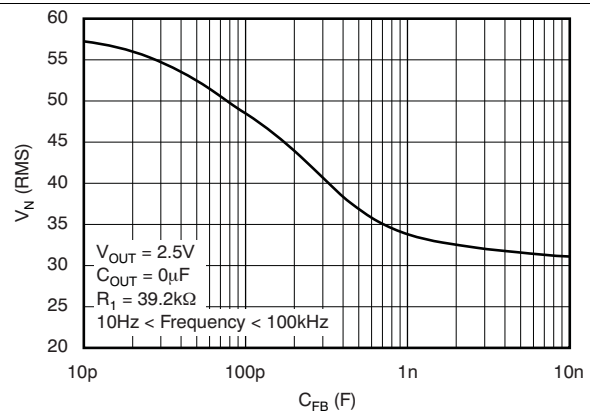


Figure 16. TPS73701 RMS Noise Voltage vs C_{FB}

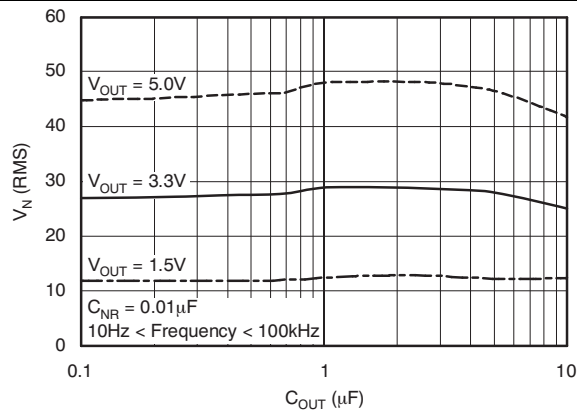


Figure 17. RMS Noise Voltage vs C_{OUT}

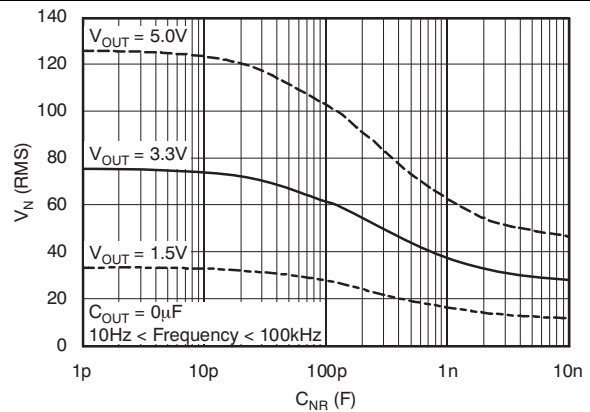
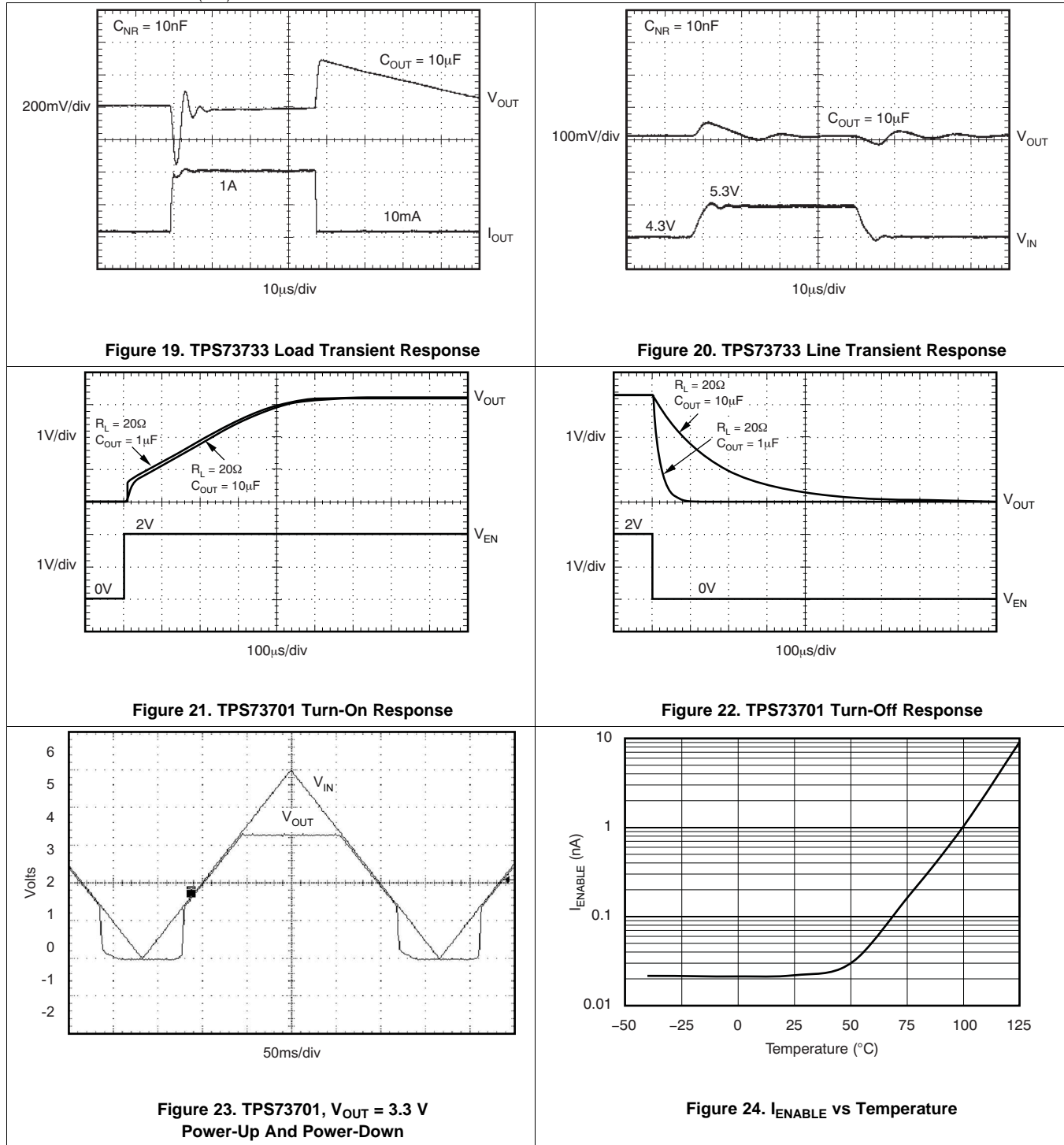


Figure 18. RMS Noise Voltage vs C_{NR}

Typical Characteristics (continued)

$T_J = 25^\circ\text{C}$, $V_{IN} = (V_{OUT(nom)} + 1\text{ V})$, $I_{OUT} = 10\text{ mA}$, $V_{EN} = 2.2\text{ V}$, $C_{OUT} = 2.2\text{ }\mu\text{F}$ (unless otherwise noted)



Typical Characteristics (continued)

$T_J = 25^\circ\text{C}$, $V_{IN} = (V_{OUT(nom)} + 1\text{ V})$, $I_{OUT} = 10\text{ mA}$, $V_{EN} = 2.2\text{ V}$, $C_{OUT} = 2.2\text{ }\mu\text{F}$ (unless otherwise noted)

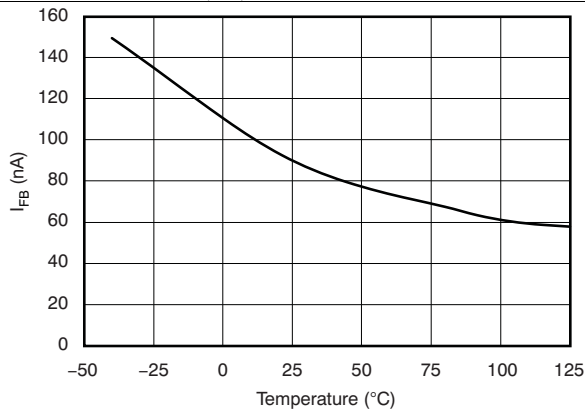


Figure 25. TPS73701 I_{FB} vs Temperature

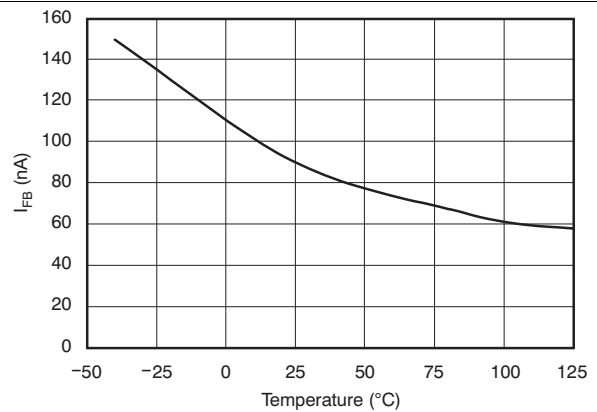


Figure 26. TPS73701 I_{FB} vs Temperature

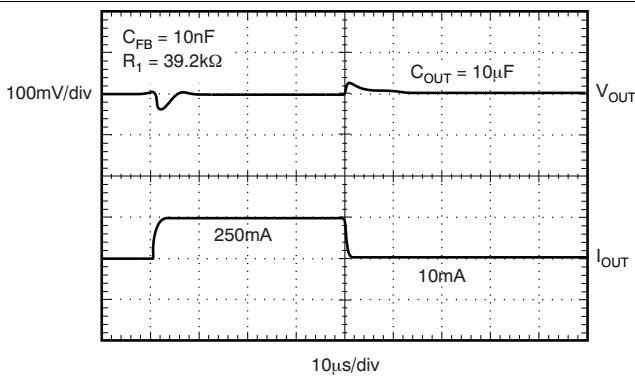


Figure 27. TPS73701 Load Transient, Adjustable Version

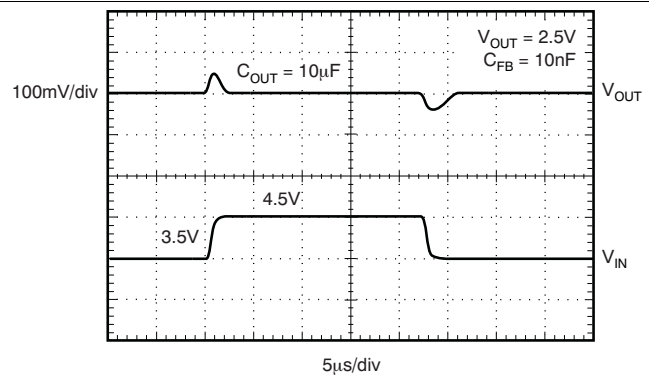


Figure 28. TPS73701 Line Transient, Adjustable Version

7 Detailed Description

7.1 Overview

The TPS737xx-Q1 belongs to a family of new generation LDO regulators that use an NMOS pass transistor to achieve ultra-low-dropout performance, reverse current blockage, and freedom from output capacitor constraints. These features combined with an enable input make the TPS737xx-Q1 ideal for portable applications. This regulator family offers a wide selection of fixed output voltage versions and an adjustable output version. All versions have thermal and over-current protection, including foldback current limit.

Table 1. Standard 1% Resistor Values for Common Output Voltages

V _{OUT}	R ₁	R ₂
1.2 V	Short	Open
1.5 V	23.2 kΩ	95.3 kΩ
1.8 V	28. kΩ	56.2 kΩ
2.5 V	39.2 kΩ	36.5 kΩ
2.8 V	44.2 kΩ	33.2 kΩ
3 V	46.4 kΩ	33.2 kΩ
3.3 V	52.3 kΩ	30.1 kΩ

7.2 Functional Block Diagrams

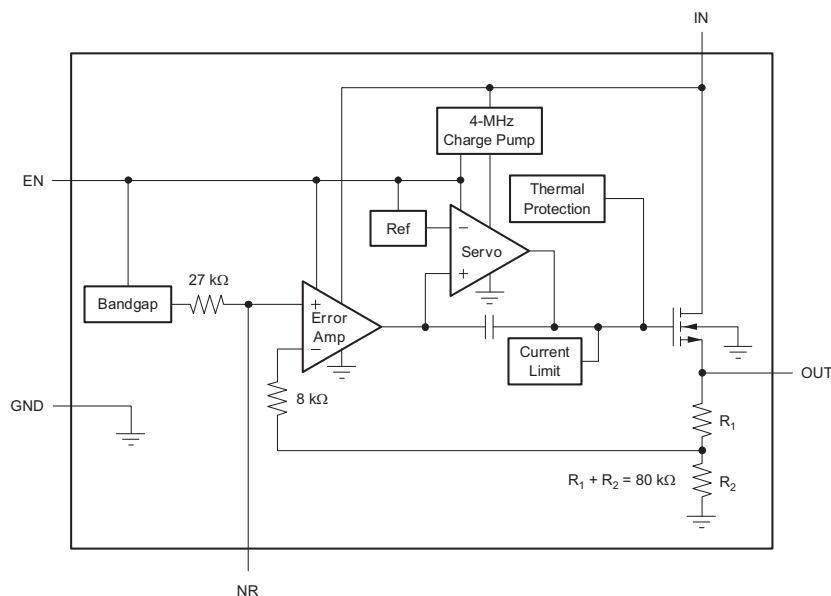
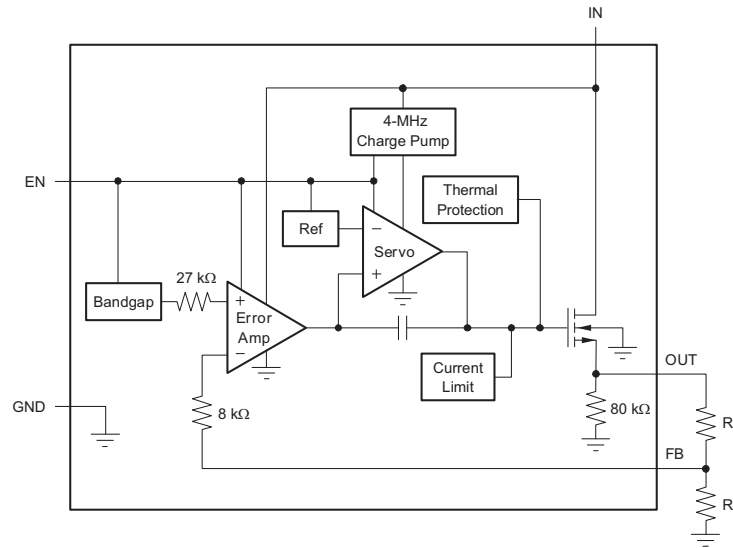


Figure 29. Fixed Voltage Version

Functional Block Diagrams (continued)


See [Table 1](#) for standard resistor values.

Figure 30. Adjustable Voltage Version

7.3 Feature Description

7.3.1 Output Noise

A precision bandgap reference is used to generate the internal reference voltage (V_{REF}). This reference is the dominant noise source within the TPS737xx-Q1 and it generates approximately $32 \mu V_{RMS}$ (10 Hz to 100 kHz) at the reference output (NR). The regulator control loop adds gain to the reference noise with the same gain as the reference voltage, so that the noise voltage of the regulator is approximately given by [Equation 1](#).

$$V_N = 32 \mu V_{RMS} \times \frac{(R_1 + R_2)}{R_2} = 32 \mu V_{RMS} \times \frac{V_{OUT}}{V_{REF}} \quad (1)$$

Because the value of V_{REF} is 1.2 V, this relationship reduces to:

$$V_N (\mu V_{RMS}) = 27 \left(\frac{\mu V_{RMS}}{V} \right) \times V_{OUT} (V) \quad (2)$$

for the case of no C_{NR} .

An internal 27-k Ω resistor in series with the noise reduction pin (NR) forms a low-pass filter for the voltage reference when an external noise reduction capacitor (C_{NR}) is connected from NR to ground. The total noise in the 10-Hz to 100-kHz bandwidth is reduced by a factor of approximately 3.2 for $C_{NR} = 10$ nF, giving the approximate relationship for $C_{NR} = 10$ nF in [Equation 3](#).

$$V_N (\mu V_{RMS}) = 8.5 \left(\frac{\mu V_{RMS}}{V} \right) \times V_{OUT} (V) \quad (3)$$

This noise reduction effect is shown in [Figure 18](#).

The TPS737xx-Q1 uses an internal charge pump to develop an internal supply voltage sufficient to drive the gate of the NMOS pass element above V_{OUT} . The charge pump generates approximately 250 μV of switching noise at approximately 4 MHz, however, charge-pump noise contribution is negligible at the output of the regulator for most values of I_{OUT} and C_{OUT} .

Feature Description (continued)

7.3.2 Internal Current Limit

The TPS737xx-Q1 internal current limit helps protect the regulator during fault conditions. Foldback current limit helps to protect the regulator from damage during output short-circuit conditions by reducing current limit when V_{OUT} drops below 0.5 V. See [Figure 10](#).

7.3.3 Enable Pin and Shutdown

The enable pin (EN) is active high and is compatible with standard TTL-CMOS levels. A V_{EN} below 0.5 V (maximum) turns the regulator off and drops the GND pin current to approximately 10 nA. When EN is used to shutdown the regulator, all charge is removed from the pass transistor gate, and the output ramps back up to a regulated V_{OUT} (see [Figure 21](#)).

When shutdown capability is not required, EN can be connected to V_{IN} . However, the pass gate may not be discharged using this configuration, and the pass transistor may be left on (enhanced) for a significant time after V_{IN} is removed. This scenario can result in reverse current flow (if the IN pin is low impedance) and faster ramp times upon power-up. In addition, for V_{IN} ramp times slower than a few milliseconds, the output may overshoot upon power-up.

7.3.4 Reverse Current

The NMOS pass element of the TPS737xx-Q1 provides inherent protection against current flow from the output of the regulator to the input when the gate of the pass device is pulled low. To ensure that all charge is removed from the gate of the pass element, the EN pin must be driven low before the input voltage is removed. If this is not done, the pass element may be left on because of stored charge on the gate.

After the EN pin is driven low, no bias voltage is required on any pin for reverse current blocking. Reverse current is specified as the current flowing out of the IN pin because of voltage applied on the OUT pin. There is additional current flowing into the OUT pin as a result of the 80-k Ω internal resistor divider to ground (see [Figure 29](#) and [Figure 30](#)).

For the TPS73701, reverse current may flow when V_{FB} is more than 1 V above V_{IN} .

7.3.5 Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 160°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage due to overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. Junction temperature must be limited to 125°C maximum for reliable operation. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. Thermal protection must trigger at least 35°C above the maximum expected ambient condition of your application for good reliability. This produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS737xx-Q1 is designed to protect against overload conditions. It was not intended to replace proper heatsinking. Continuously running the TPS737xx-Q1 into thermal shutdown degrades device reliability.

7.4 Device Functional Modes

Driving the EN pin over 1.7 V turns on the regulator. Driving the EN below 0.5 V causes the regulator to enter shutdown mode. In shutdown, the current consumption of the device is reduced to 20 nA (typical).

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS737xx-Q1 family of LDO regulators use an NMOS pass transistor to achieve ultra-low-dropout performance, reverse current blockage, and freedom from output capacitor constraints. These features, combined with low noise and an enable input, make the TPS737xx-Q1 ideal for portable applications.

8.2 Typical Application

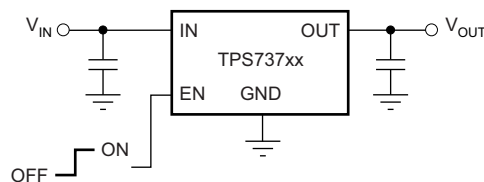


Figure 31. Typical Application Circuit For Fixed-Voltage Versions

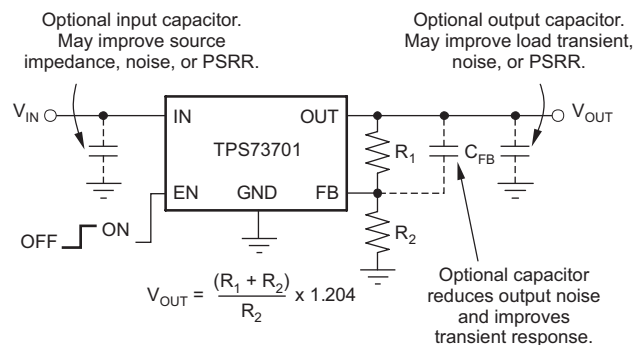


Figure 32. Typical Application Circuit For Adjustable-Voltage Version

8.2.1 Design Requirements

R_1 and R_2 can be calculated for any output voltage using the formula shown in [Figure 32](#). Sample resistor values for common output voltages are shown in [Table 1](#).

Make the parallel combination of R_1 and R_2 approximately equal to 19 k Ω for best accuracy. This 19 k Ω , in addition to the internal 8-k Ω resistor, presents the same impedance to the error amplifier as the 27-k Ω bandgap reference output. This impedance helps compensate for leakages into the error amplifier terminals.

The TPS73701 adjustable version does not have the NR pin available. However, connecting a feedback capacitor (C_{FB}) from the output to the feedback pin (FB) reduces output noise and improves load transient performance. This capacitor must be limited to 0.1 μ F.

Typical Application (continued)

8.2.2 Detailed Design Procedure

8.2.2.1 Input and Output Capacitor Requirements

Although an input capacitor is not required for stability, if input impedance is very low, it is good analog design practice to connect a 0.1- μF to 1- μF low equivalent series resistance (ESR) capacitor across the input supply near the regulator. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated or the device is located several inches from the power source.

The TPS737xx-Q1 requires a 1- μF output capacitor for stability. It is designed to be stable for all available types and values of capacitors. In applications where multiple low ESR capacitors are in parallel, ringing may occur when the product of C_{OUT} and total ESR drops below 50 n Ω . Total ESR includes all parasitic resistances, including capacitor ESR and board, socket, and solder joint resistance. In most applications, the sum of capacitor ESR and trace resistance meets this requirement.

8.2.2.2 Dropout Voltage

The TPS737xx-Q1 uses an NMOS pass transistor to achieve extremely low dropout. When $(V_{\text{IN}} - V_{\text{OUT}})$ is less than the dropout voltage (V_{DO}), the NMOS pass device is in its linear region of operation and the input-to-output resistance is the $R_{\text{DS(ON)}}$ of the NMOS pass element.

The TPS737xx-Q1 requires a larger voltage drop from V_{IN} to V_{OUT} to avoid degraded transient response for large step changes in load current. The boundary of this transient dropout region is approximately twice the DC dropout. Values of $V_{\text{IN}} - V_{\text{OUT}}$ above this line ensure normal transient response.

Operating in the transient dropout region can cause an increase in recovery time. The time required to recover from a load transient is a function of the magnitude of the change in load current rate, the rate of change in load current, and the available headroom (V_{IN} to V_{OUT} voltage drop). Under worst-case conditions (full-scale instantaneous load change with $(V_{\text{IN}} - V_{\text{OUT}})$ close to DC dropout levels), the TPS737xx-Q1 can take a couple of hundred microseconds to return to the specified regulation accuracy.

8.2.2.3 Transient Response

The low open-loop output impedance provided by the NMOS pass element in a voltage follower configuration allows operation without a 1- μF output capacitor. As with any regulator, the addition of additional capacitance from the OUT pin to ground reduces undershoot magnitude but increases its duration. In the adjustable version, the addition of a capacitor (C_{FB}) between the OUT pin and the FB pin also improves the transient response.

The TPS737xx-Q1 does not have active pulldown when the output is overvoltage. This architecture allows for applications that connect higher voltage sources, such as alternate power supplies, to be connected to the output. This architecture also results in an output overshoot of several percent if the load current quickly drops to zero when a capacitor is connected to the output. The duration of overshoot can be reduced by adding a load resistor. The overshoot decays at a rate determined by the output capacitor (C_{OUT}) and the internal and external load resistance. The rate of decay is given by [Equation 4](#) and [Equation 5](#).

(Fixed voltage version)

$$\frac{dV}{dT} = \frac{V_{\text{OUT}}}{C_{\text{OUT}} \times 80 \text{ k}\Omega \parallel R_{\text{LOAD}}} \quad (4)$$

(Adjustable voltage version)

$$\frac{dV}{dT} = \frac{V_{\text{OUT}}}{C_{\text{OUT}} \times 80 \text{ k}\Omega \parallel (R_1 + R_2) \parallel R_{\text{LOAD}}} \quad (5)$$

Typical Application (continued)

8.2.3 Application Curves

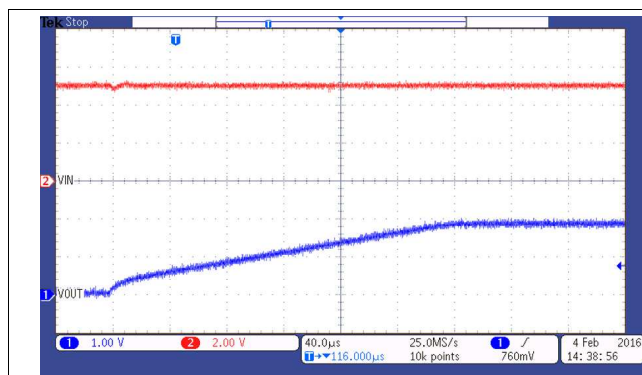


Figure 33. TPS737xx-Q1 Start-Up

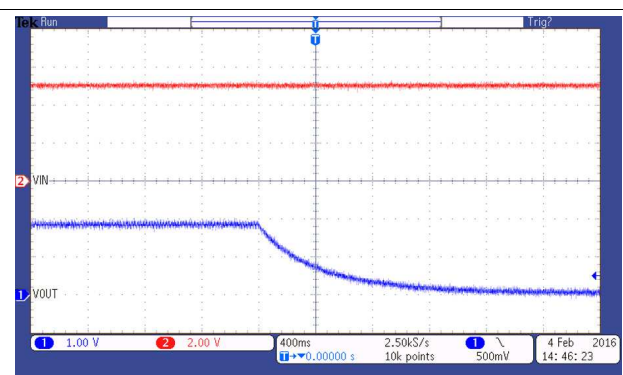


Figure 34. TPS737xx-Q1 Shutdown

9 Power Supply Recommendations

The device is designed to operate from an input voltage supply range from 2.2 V to 5.5 V. The input voltage range provides adequate headroom for the device to have a regulated output. This input supply must be well regulated. If the input supply is noisy, additional input capacitors with low ESR help improve the output noise performance.

10 Layout

10.1 Layout Guidelines

10.1.1 Improve PSRR and Noise Performance

TI recommends that the printed circuit board (PCB) be designed with separate ground planes for V_{IN} and V_{OUT} , with each ground plane connected only at the GND pin of the device, to improve AC performance such as PSRR, output noise, and transient response. In addition, the ground connection for the bypass capacitor must connect directly to the GND pin of the device.

10.1.2 Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the PCB layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for JEDEC low-K and high-K boards are shown in [Thermal Information](#). Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves the heatsink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation (P_D) is equal to the product of the output current multiplied by the voltage drop across the output pass element (V_{IN} to V_{OUT}). See [Equation 6](#).

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (6)$$

Power dissipation can be minimized by using the lowest possible input voltage necessary to assure the required output voltage.

10.2 Layout Example

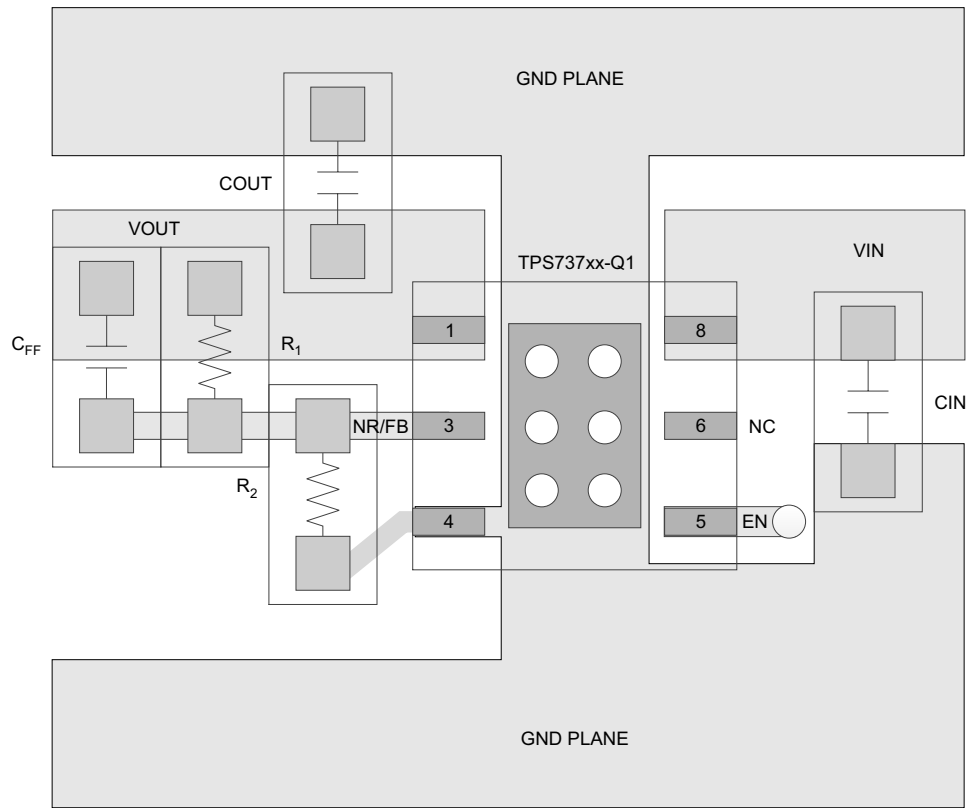


Figure 35. Layout Diagram

11 器件和文档支持

11.1 文档支持

11.1.1 相关文档

请参阅如下相关文档：

《[表面贴装器件的焊盘建议](#)》(SBFA015)

11.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。单击右上角的通知我进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.3 社区资源

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.4 商标

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11.5 静电放电警告



ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

12.1 封装

请参阅《[表面贴装器件的焊盘建议](#)》(SBFA015)，获取有关 TPS737xx-Q1 焊盘尺寸的建议。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS73719QDRBRQ1	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	719Q	Samples
TPS73733QDRBRQ1	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	733Q	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TPS737-Q1 :

- Catalog : [TPS737](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS73719QDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS73733QDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS73719QDRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TPS73733QDRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0

DRB 8

GENERIC PACKAGE VIEW

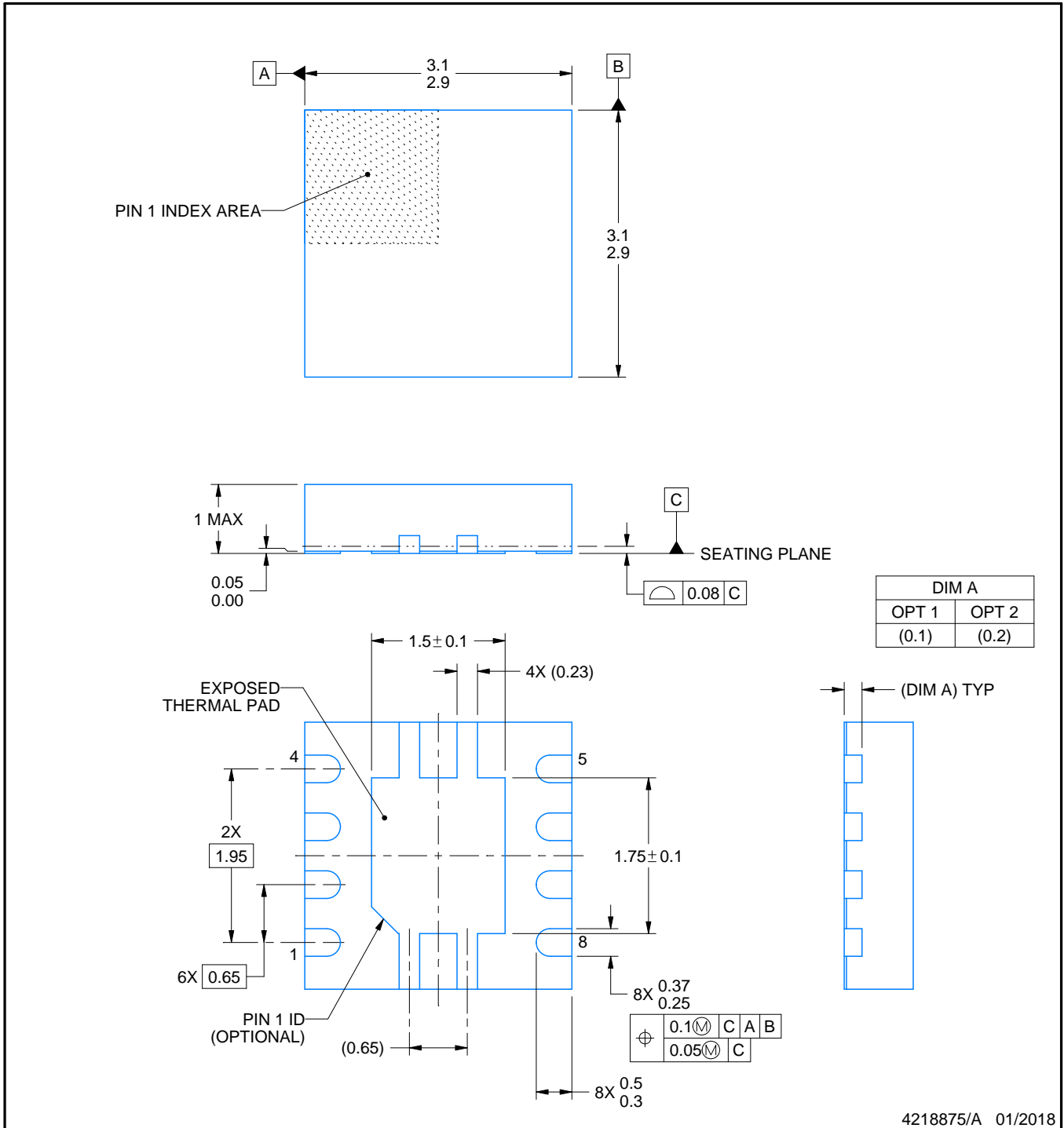
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4203482/L



4218875/A 01/2018

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

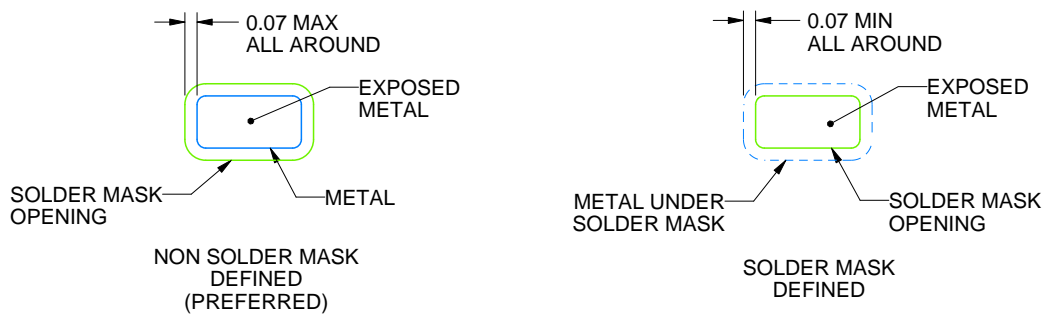
DRB0008A

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

4218875/A 01/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DRB0008A

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
84% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218875/A 01/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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