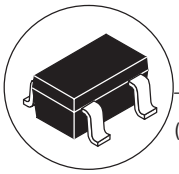
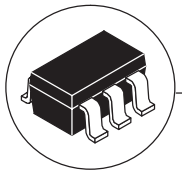




ULTRALOW NOISE, HIGH PSRR, FAST RF 100-mA LOW-DROPOUT LINEAR REGULATORS

FEATURES

- **Qualified for Automotive Applications**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)**
- **100-mA Low-Dropout Regulator With $\overline{EN}$**
- **Available in 1.8-V, 3.3-V, 4.7-V, and Adj.**
- **High PSRR (70 dB at 10 kHz)**
- **Ultralow Noise (15 μV_{RMS})**
- **Fast Start-Up Time (63 μs)**
- **Stable With Any 1-μF Ceramic Capacitor**
- **Excellent Load/Line Transient**
- **Very Low Dropout Voltage (38 mV at Full Load, TPS79147)**
- **5-Pin SOT23 (DBV) Package**
- **TPS792xx Provides EN Options**

APPLICATIONS

- **VCOs**
- **RF**
- **Bluetooth™, Wireless LAN**

DESCRIPTION

The TPS791xx family of low-dropout (LDO) low-power linear voltage regulators features high power supply rejection ratio (PSRR), ultralow noise, fast start-up, and excellent line and load transient responses in a small outline, SOT23, package. Each device in the family is stable with a small 1-μF ceramic capacitor on the output.

The family uses an advanced, proprietary BiCMOS fabrication process to yield extremely low dropout voltages (e.g., 38 mV at 100 mA, TPS79147). Each device achieves fast start-up times (approximately 63 μs with a 0.001 μF bypass capacitor) while consuming very low quiescent current (170 μA typical). Moreover, when the device is placed in standby mode, the supply current is reduced to less than 1 μA. The TPS79118 exhibits approximately 15 μV_{RMS} of output voltage noise with a 0.1 μF bypass capacitor.

Applications with analog components that are noise sensitive, such as portable RF electronics, benefit from the high PSRR and low noise features as well as the fast response time.

ORDERING INFORMATION

T_J	VOLTAGE	PACKAGE	PART NUMBER	SYMBOL
−40°C to 125°C	1.2 to 5.5 V	SOT23 (DBV)	TPS79101DBVRQ1(1)	PEU1
	1.8 V		TPS79118DBVRQ1(1)	PER1
	3.3 V		TPS79133DBVRQ1(1)	PES1
	4.7 V		TPS79147DBVRQ1(1)(2)	PET1

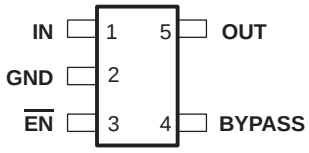
(1) The DBVR indicates tape and reel of 3000 parts.
(2) This part is Product Preview.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

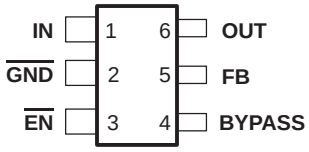
Bluetooth is a trademark owned by the Bluetooth SIG, Inc.

DBV PACKAGE
(TOP VIEW)



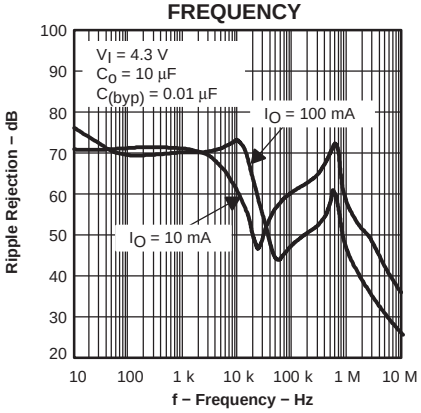
Fixed Option

DBV PACKAGE
(TOP VIEW)

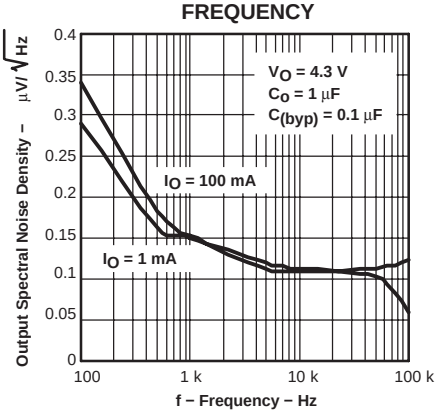


Adjustable Option

TPS79133
RIPPLE REJECTION
vs
FREQUENCY



TPS79133
OUTPUT SPECTRAL NOISE DENSITY
vs
FREQUENCY



ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

	TPS79101, TPS79118 TPS79133, TPS79147
Input voltage range(2)	−0.3 V to 6 V
Voltage range at $\overline{EN}$	−0.3 V to V_I + 0.3 V
Voltage on OUT	−0.3 V to 6 V
Peak output current	Internally limited
ESD rating, HBM	2 kV
ESD rating, CDM	500 V
Continuous total power dissipation	See Dissipation Rating Table
Operating virtual junction temperature range, T_J	−40°C to 150°C
Operating ambient temperature range, T_A	−40°C to 85°C
Storage temperature range, T_{stg}	−65°C to 150°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

PACKAGE DISSIPATION RATING

BOARD	PACKAGE	$R_{\theta JC}$	$R_{\theta JA}$	DERATING FACTOR ABOVE T_A = 25°C	$T_A \le 25°C$ POWER RATING	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
Low K(1)	DBV	63.75°C/W	256°C/W	3.906 mW/°C	391 mW	215 mW	156 mW
High K(2)	DBV	63.75°C/W	178.3°C/W	5.609 mW/°C	561 mW	308 mW	224 mW

(1) The JEDEC low-K (1s) board design used to derive this data was a 3-inch × 3-inch, two-layer board with 2-ounce copper traces on top of the board.
(2) The JEDEC high-K (2s2p) board design used to derive this data was a 3-inch × 3-inch, multilayer board with 1-ounce internal power and ground planes and 2-ounce copper traces on top and bottom of the board.

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Input voltage, V_I (1)	2.7		5.5	V
Continuous output current, I_O (2)	0		100	mA
Operating junction temperature, T_J	−40		125	°C

(1) To calculate the minimum input voltage for your maximum output current, use the following formula:
$V_I(min) = V_O(max) + V_{DO}$ (max load)
(2) Continuous output current and operating junction temperature are limited by internal protection circuitry, but it is not recommended that the device operate under conditions beyond those specified in this table for extended periods of time.

ELECTRICAL CHARACTERISTICS

over recommended operating free-air temperature range, (T_J = −40 to 125 °C), $V_I = V_{O(typ)}$ + 1 V, I_O = 1 mA, $\overline{EN}$ = 0 V, C_o = 10 µF, $C_{O(byp)}$= 0.01 µF (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Output voltage	TPS79101	T_J = 25°C, 1.22 V ≤ V_O ≤ 5.2 V			V_O		V
		0 µA< I_O < 100 mA(1), 1.22 V ≤ V_O ≤ 5.2 V		0.98 V_O		1.02 V_O	
	TPS79118	T_J = 25°C			1.8		
		0 µA < I_O < 100 mA, 2.8 V < V_I < 5.5 V		1.764		1.836	
	TPS79133	T_J = 25°C			3.3		
		0 µA < I_O < 100 mA, 4.3 V < V_I < 5.5 V		3.234		3.366	
	TPS79147	T_J = 25°C			4.7		
		0 µA < I_O < 100 mA, 5.2 V < V_I < 5.5 V		4.606		4.794	
Quiescent current (GND current)		0 µA < I_O < 100 mA, T_J = 25°C			170		µA
		0 µA < I_O < 100 mA				250	
Load regulation		0 µA < I_O < 100 mA, T_J = 25°C			5		mV
Output voltage line regulation ($\Delta V_O/V_O$)(2)		V_O + 1 V < V_I ≤ 5.5 V, T_J = 25°C			0.05		%/V
		V_O + 1 V < V_I ≤ 5.5 V				0.12	
Output noise voltage (TPS79118)		BW = 100 Hz to 100 kHz, I_O = 100 mA, T_J = 25°C	$C_{(byp)}$ = 0.001 µF		32		µV_{RMS}
			$C_{(byp)}$ = 0.0047 µF		17		
			$C_{(byp)}$ = 0.01 µF		16		
			$C_{(byp)}$ = 0.1 µF		15		
Time, start-up (TPS79133)		R_L = 33 Ω, C_o = 1 µF, T_J = 25°C	$C_{(byp)}$ = 0.001 µF		53		µs
			$C_{(byp)}$ = 0.0047 µF		67		
			$C_{(byp)}$ = 0.01 µF		98		
Output current limit		V_O = 0 V(1)		285		600	mA
UVLO threshold		V_{CC} rising		2.25		2.65	V
UVLO hysteresis		T_J = 25°C, V_{CC} rising			100		mV

(1) The minimum IN operating voltage is 2.7 V or $V_{O(typ)}$ + 1 V, whichever is greater. The maximum IN voltage is 5.5 V. The maximum output current is 100 mA.

(2) If V_O ≤ 1.8 V then V_{Imin} = 2.7 V, V_{Imax} = 5.5 V:

$$\text{Line regulation (mV)} = (\%/V) \times \frac{V_O\left(V_{Imax} - 2.7\ V\right)}{100} \times 1000$$

If V_O ≥ 2.5 V then $V_{Imin} = V_O$ + 1 V, V_{Imax} = 5.5 V:

$$\text{Line regulation (mV)} = (\%/V) \times \frac{V_O\left(V_{Imax} - \left(V_O + 1\ V\right)\right)}{100} \times 1000$$

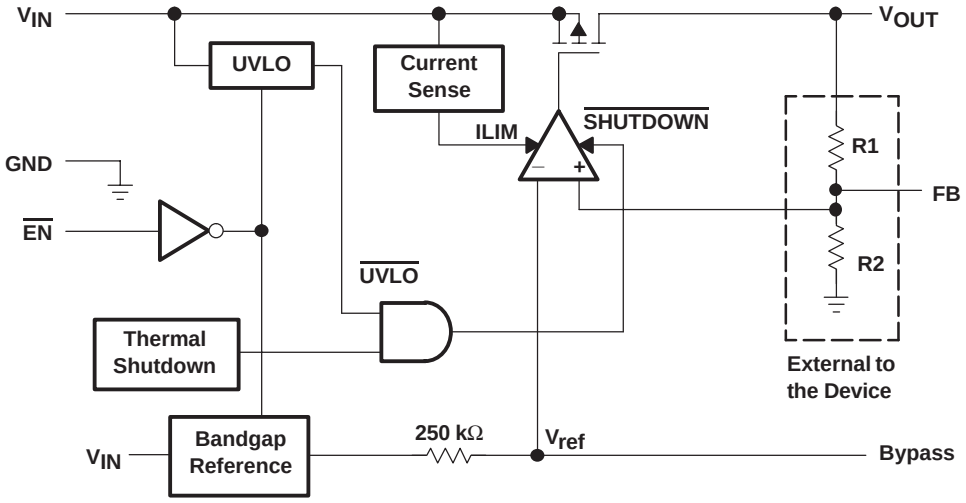
ELECTRICAL CHARACTERISTICS continued

over recommended operating free-air temperature range, (T_J = −40 to 125 °C), $V_I = V_{O(typ)}$ + 1 V, I_O = 1 mA, $\overline{EN}$ = 0 V, C_O = 10 µF, $C_{O(byp)}$= 0.01 µF (unless otherwise noted)

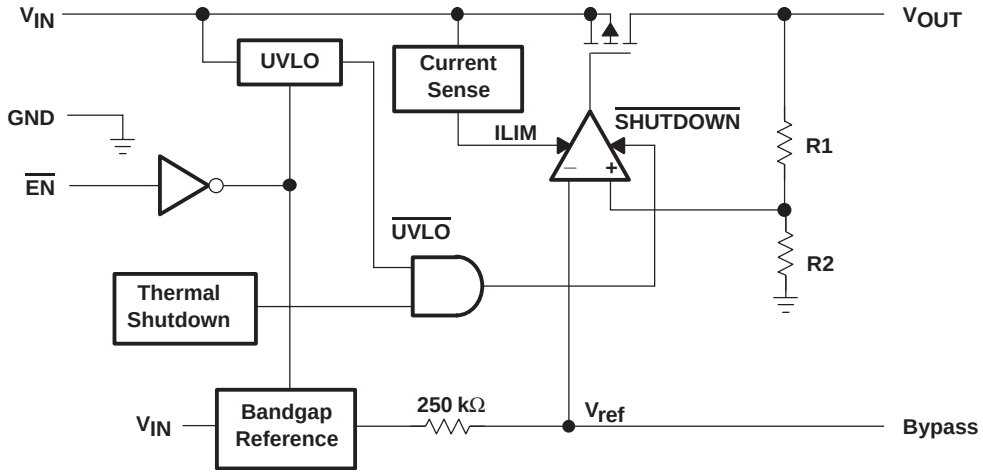
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Standby current		$\overline{EN}$ = V_I, 2.7 V < V_I < 5.5 V		0.07	1	µA
High level enable input voltage		2.7 V < V_I < 5.5 V	2			V
Low level enable input voltage		2.7 V < V_I < 5.5 V			0.7	V
Input current ($\overline{EN}$)		$\overline{EN}$ = V_I	−1		1	µA
Power supply ripple rejection	TPS79118	f = 100 Hz, T_J = 25°C, I_O = 10 mA		80		dB
		f = 100 Hz, T_J = 25°C, I_O = 100 mA		75		
		f = 10 kHz, T_J = 25°C, I_O = 100 mA		72		
		f = 100 kHz, T_J = 25°C, I_O = 100 mA		45		
	TPS79133	f = 100 Hz, T_J = 25°C, I_O = 10 mA		70		
		f = 100 Hz, T_J = 25°C, I_O = 100 mA		75		
		f = 10 kHz, T_J = 25°C, I_O = 100 mA		73		
		f = 100 kHz, T_J = 25°C, I_O = 100 mA		37		
Dropout voltage(1)	TPS79133	I_O = 100 mA, T_J = 25°C		50		mV
		I_O = 100 mA			90	
	TPS79147	I_O = 100 mA, T_J = 25°C		38		
		I_O = 100 mA			70	

(1) IN voltage equals V_O(typ) − 100 mV; The TPS79118 dropout voltage is limited by the input voltage range limitations.

FUNCTIONAL BLOCK DIAGRAM—ADJUSTABLE VERSION



FUNCTIONAL BLOCK DIAGRAM—FIXED VERSION



Terminal Functions

TERMINAL			I/O	DESCRIPTION
NAME	ADJ	FIXED		
BYPASS	4	4		An external bypass capacitor, connected to this terminal, in conjunction with an internal resistor, creates a low-pass filter to further reduce regulator noise.
$\overline{EN}$	3	3	I	The $\overline{EN}$ terminal is an input which enables or shuts down the device. When $\overline{EN}$ is a logic high, the device will be in shutdown mode. When $\overline{EN}$ is a logic low, the device will be enabled.
FB	5	N/A	I	This terminal is the feedback input voltage for the adjustable device.
GND	2	2		Regulator ground
IN	1	1	I	The IN terminal is the input to the device.
OUT	6	5	O	The OUT terminal is the regulated output of the device.

TYPICAL CHARACTERISTICS

TPS79118
OUTPUT VOLTAGE vs OUTPUT CURRENT

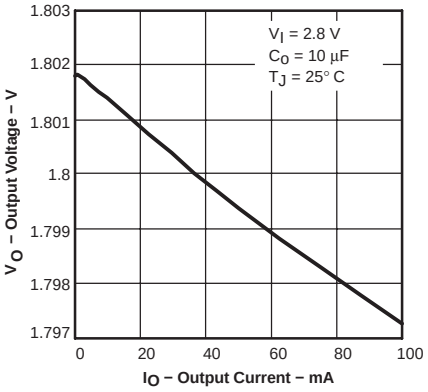


Figure 1

TPS79133
OUTPUT VOLTAGE vs OUTPUT CURRENT

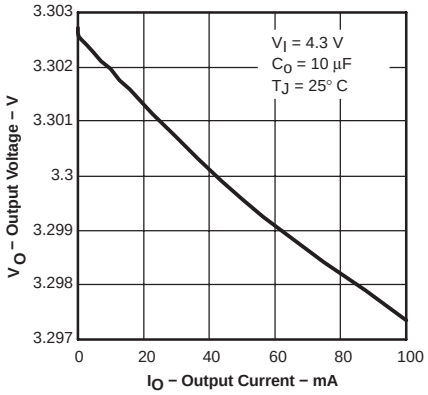


Figure 2

TPS79118
OUTPUT VOLTAGE vs JUNCTION TEMPERATURE

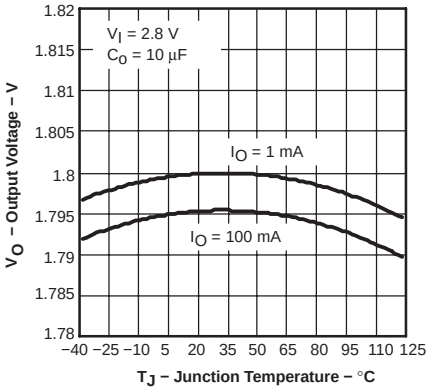


Figure 3

TPS79133
OUTPUT VOLTAGE vs JUNCTION TEMPERATURE

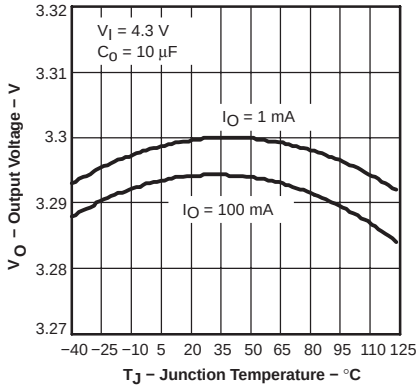


Figure 4

TPS79133
GROUND CURRENT vs JUNCTION TEMPERATURE

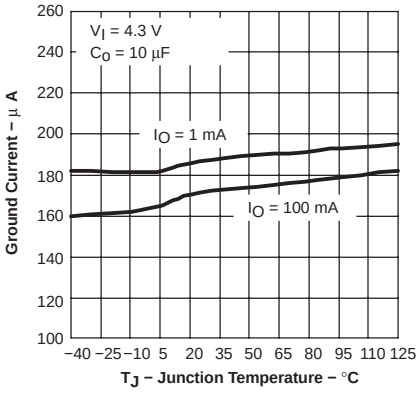


Figure 5

TPS79118
OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY

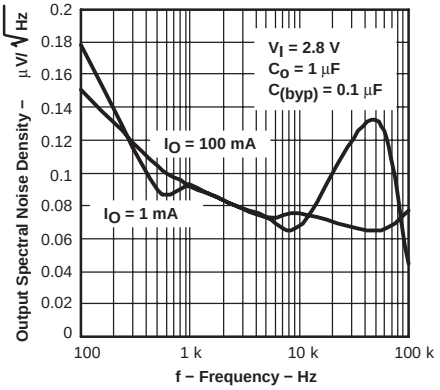


Figure 6

TPS79118
OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY

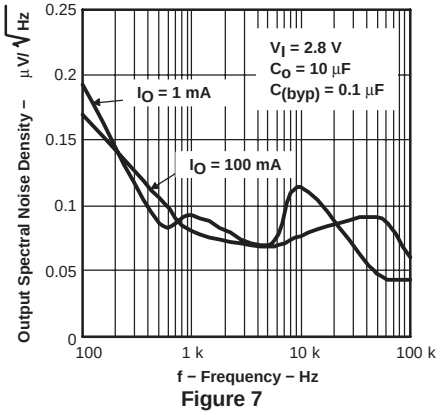


Figure 7

TPS79118
OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY

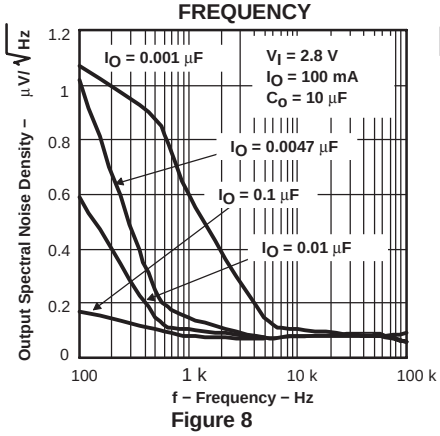


Figure 8

TPS79133
OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY

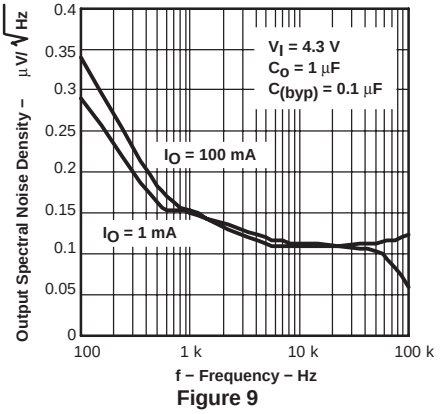


Figure 9

TYPICAL CHARACTERISTICS

TPS79133
OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY

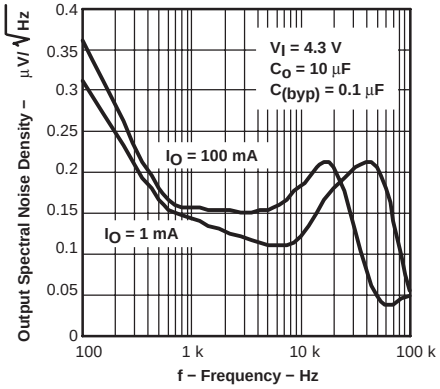


Figure 10

TPS79133
OUTPUT SPECTRAL NOISE DENSITY vs FREQUENCY

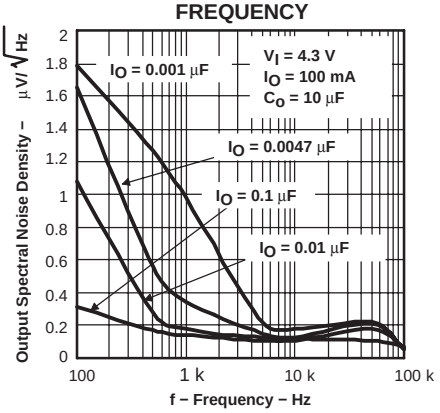


Figure 11

ROOT MEAN SQUARED OUTPUT NOISE vs BYPASS CAPACITANCE

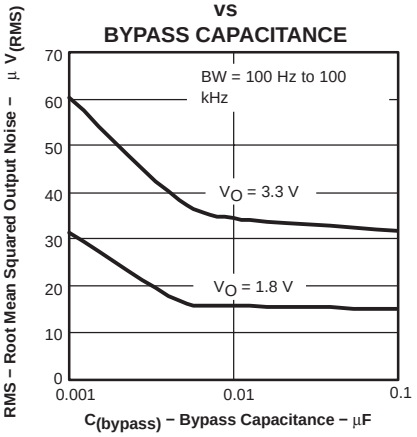


Figure 12

TPS79133
OUTPUT IMPEDANCE vs FREQUENCY

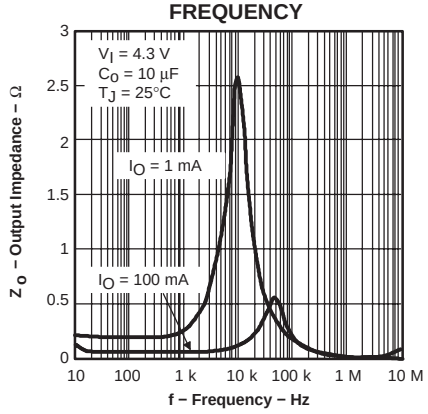


Figure 13

TPS79133
DROPOUT VOLTAGE vs JUNCTION TEMPERATURE

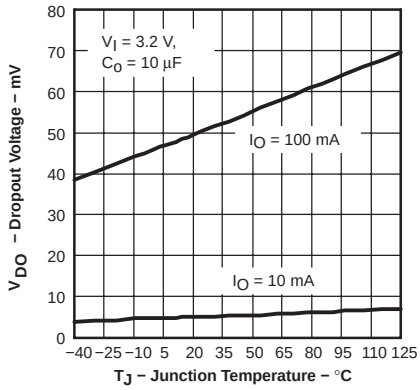


Figure 14

TPS792133
DROPOUT VOLTAGE vs OUTPUT CURRENT

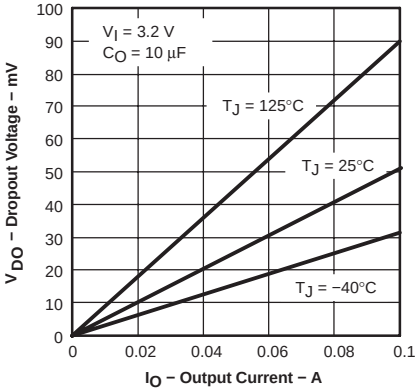


Figure 15

TPS79101
DROPOUT VOLTAGE vs INPUT VOLTAGE

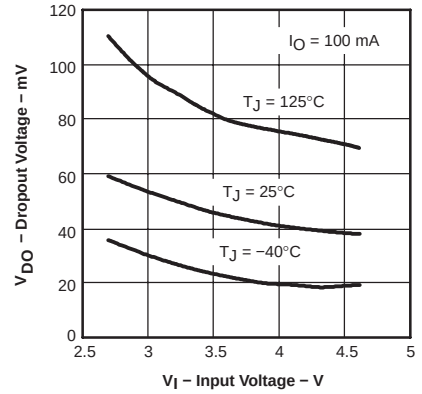


Figure 16

MINIMUM REQUIRED INPUT VOLTAGE vs OUTPUT VOLTAGE

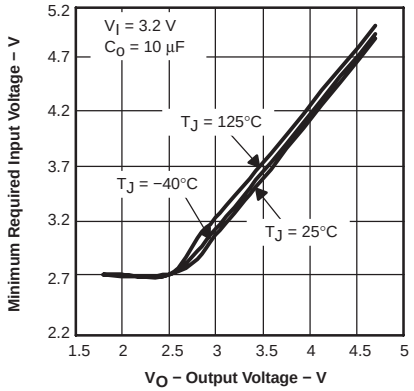


Figure 17

TPS79118
RIPPLE REJECTION vs FREQUENCY

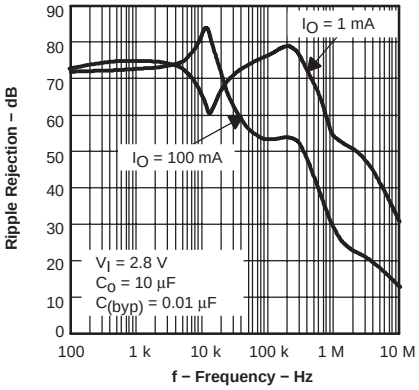


Figure 18

TYPICAL CHARACTERISTICS

TPS79118
RIPPLE REJECTION vs FREQUENCY

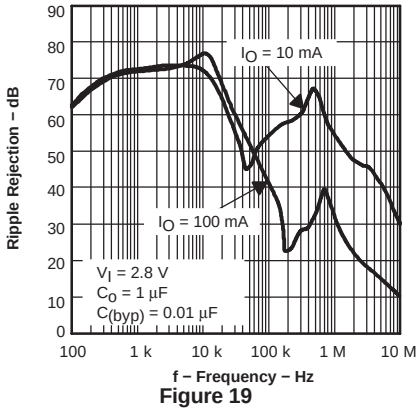


Figure 19

TPS79118
RIPPLE REJECTION vs FREQUENCY

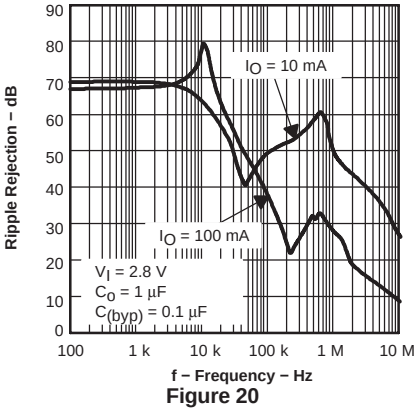


Figure 20

TPS79133
RIPPLE REJECTION vs FREQUENCY

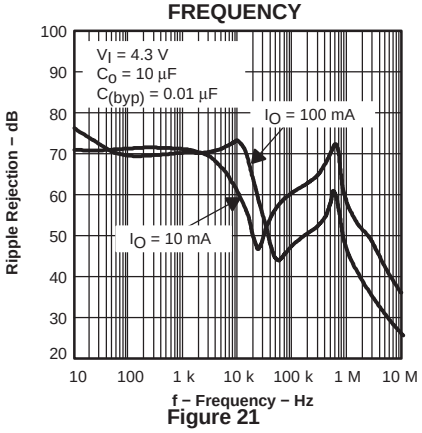


Figure 21

TPS79133
RIPPLE REJECTION vs FREQUENCY

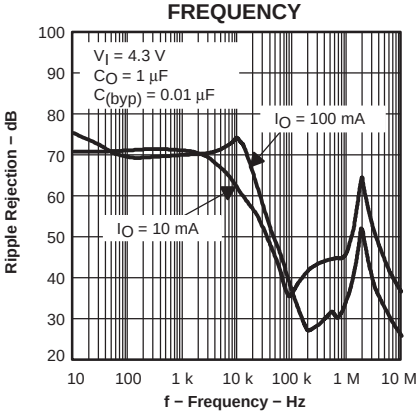


Figure 22

TPS79133
RIPPLE REJECTION vs FREQUENCY

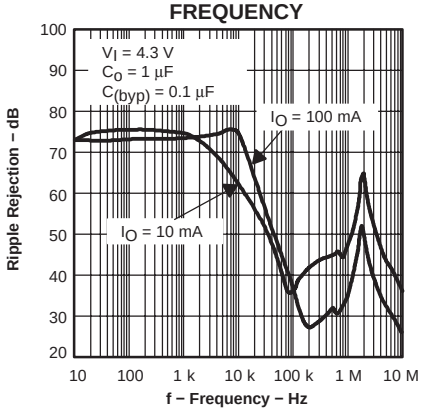


Figure 23

TPS79133
OUTPUT VOLTAGE, ENABLE VOLTAGE vs TIME (START-UP)

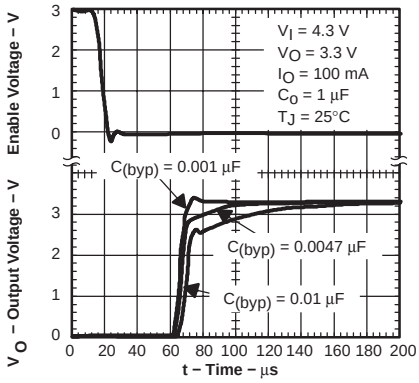


Figure 24

TPS79118
LINE TRANSIENT RESPONSE

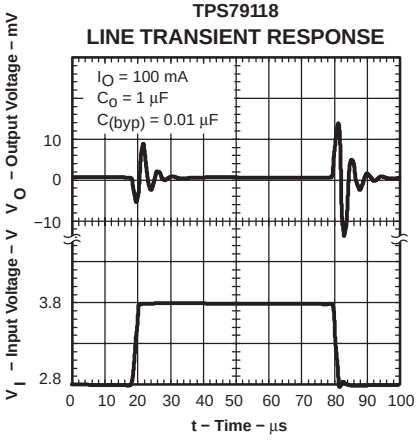


Figure 25

TPS79118
LOAD TRANSIENT RESPONSE

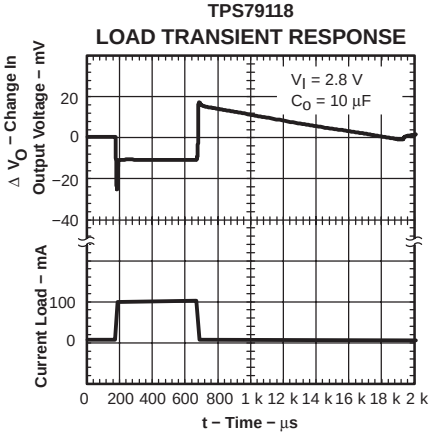


Figure 26

TPS79133
LINE TRANSIENT RESPONSE

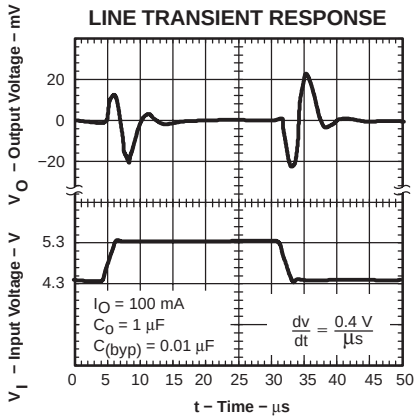


Figure 27

TYPICAL CHARACTERISTICS

TPS79133
LOAD TRANSIENT RESPONSE

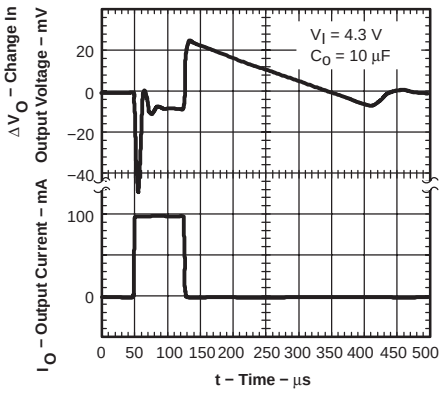


Figure 28

TPS79118
TYPICAL REGIONS OF STABILITY
EQUIVALENT SERIES RESISTANCE (ESR)
vs
OUTPUT CURRENT

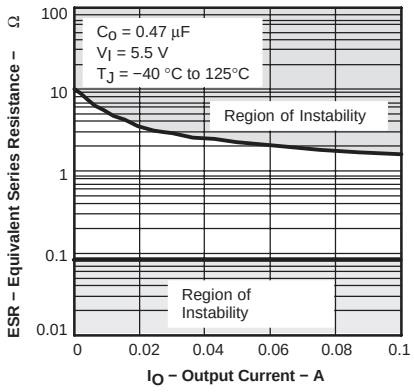


Figure 29

TPS79118
TYPICAL REGIONS OF STABILITY
EQUIVALENT SERIES RESISTANCE (ESR)
vs
OUTPUT CURRENT

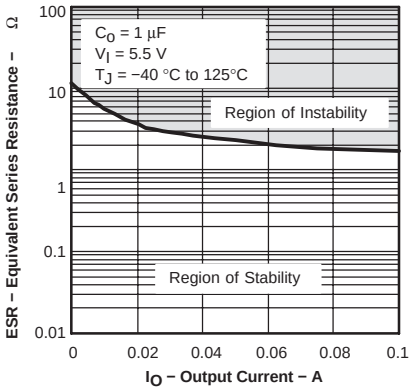


Figure 30

TPS79118
TYPICAL REGIONS OF STABILITY
EQUIVALENT SERIES RESISTANCE (ESR)
vs
OUTPUT CURRENT

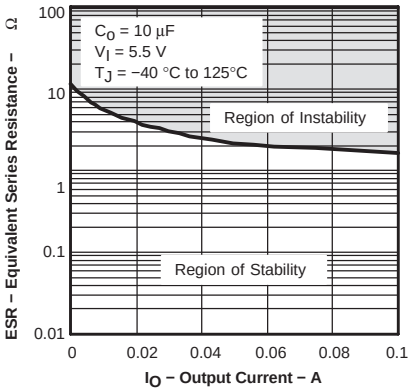


Figure 31

APPLICATION INFORMATION

The TPS791xx family of low-dropout (LDO) regulators have been optimized for use in noise-sensitive battery-operated equipment. The device features extremely low dropout voltages, high PSRR, ultralow output noise, low quiescent current (170 μA typically), and enable-input to reduce supply currents to less than 1 μA when the regulator is turned off.

A typical application circuit is shown in Figure 32.

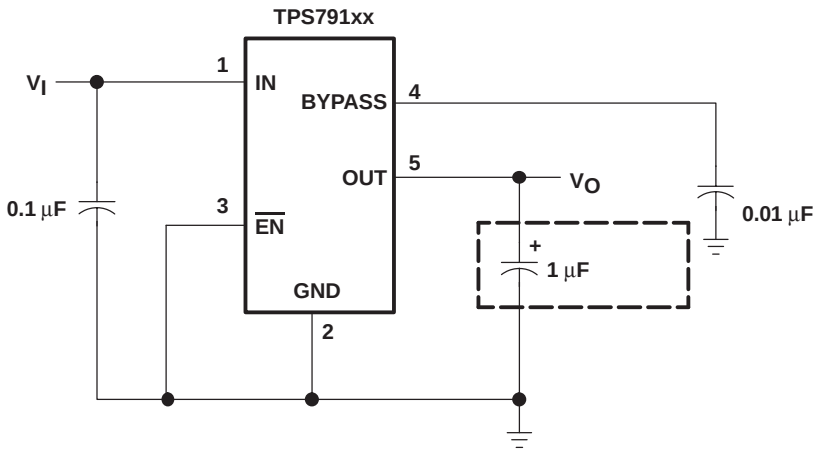


Figure 32. Typical Application Circuit

EXTERNAL CAPACITOR REQUIREMENTS

A 0.1-μF or larger ceramic input bypass capacitor, connected between IN and GND and located close to the TPS791xx, is required for stability and to improve transient response, noise rejection, and ripple rejection. A higher-value electrolytic input capacitor may be necessary if large, fast-rise-time load transients are anticipated and the device is located several inches from the power source.

Like all low dropout regulators, the TPS791xx requires an output capacitor connected between OUT and GND to stabilize the internal control loop. The minimum recommended capacitance is 1 μF. Any 1 μF or larger ceramic capacitor is suitable. The device is also stable with a 0.47 μF ceramic capacitor with at least 75 mΩ of ESR.

The internal voltage reference is a key source of noise in an LDO regulator. The TPS791xx has a BYPASS pin which is connected to the voltage reference through a 250-kΩ internal resistor. The 250-kΩ internal resistor, in conjunction with an external bypass capacitor connected to the BYPASS pin, creates a low pass filter to reduce the voltage reference noise and, therefore, the noise at the regulator output. In order for the regulator to operate properly, the current flow out of the BYPASS pin must be at a minimum because any leakage current creates an IR drop across the internal resistor thus creating an output error. Therefore, the bypass capacitor must have minimal leakage current.

For example, the TPS79118 exhibits approximately 15 μV_{RMS} of output voltage noise using a 0.1 μF ceramic bypass capacitor and a 1 μF ceramic output capacitor. Note that the output starts up slower as the bypass capacitance increases due to the RC time constant at the bypass pin that is created by the internal 250 kΩ resistor and external capacitor.

BOARD LAYOUT RECOMMENDATION TO IMPROVE PSRR AND NOISE PERFORMANCE

To improve ac measurements like PSRR, output noise, and transient response, it is recommended that the board be designed with separate ground planes for V_{IN} and V_{OUT}, with each ground plane connected only at the ground pin of the device. In addition, the ground connection for the bypass capacitor should connect directly to the ground pin of the device.

POWER DISSIPATION AND JUNCTION TEMPERATURE

Specified regulator operation is assured to a junction temperature of 125°C; the maximum junction temperature should be restricted to 125°C under normal operating conditions. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, P_D, which must be less than or equal to $P_{D(max)}$.

The maximum-power-dissipation limit is determined using the following equation:

$$P_{D(max)} = \frac{T_J max - T_A}{R_{\theta JA}} \quad (1)$$

Where:

$T_J max$ is the maximum allowable junction temperature.

$R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package, see the dissipation rating table.

T_A is the ambient temperature.

The regulator dissipation is calculated using:

$$P_D = \left(V_I - V_O\right) \times I_O \quad (2)$$

Power dissipation resulting from quiescent current is negligible. Excessive power dissipation triggers the thermal protection circuit.

PROGRAMMING THE TPS79101 ADJUSTABLE LDO REGULATOR

The output voltage of the TPS79101 adjustable regulator is programmed using an external resistor divider as shown in Figure 33. The output voltage is calculated using:

$$V_O = V_{ref} \times \left(1 + \frac{R1}{R2}\right) \quad (3)$$

Where:

V_{ref} = 1.2246 V typ (the internal reference voltage)

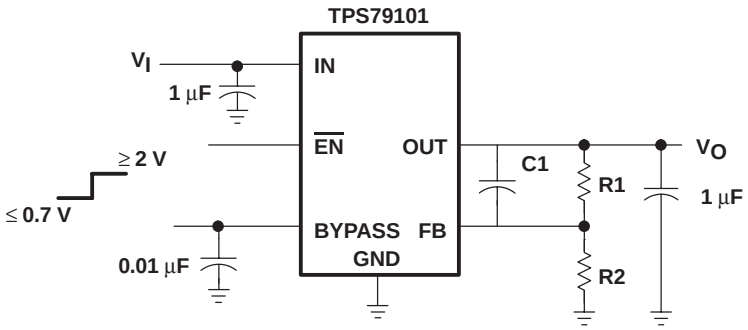
Resistors R1 and R2 should be chosen for approximately 50-μA divider current. Lower value resistors can be used for improved noise performance, but the solution consumes more power. Higher resistor values should be avoided as leakage current into/out of FB across R1/R2 creates an offset voltage that artificially increases/decreases the feedback voltage and thus erroneously decreases/increases V_O. The recommended design procedure is to choose R2 = 30.1 kΩ to set the divider current at 50 μA, C1 = 15 pF for stability, and then calculate R1 using:

$$R1 = \left(\frac{V_O}{V_{ref}} - 1\right) \times R2 \quad (4)$$

In order to improve the stability of the adjustable version, it is suggested that a small compensation capacitor be placed between OUT and FB. For voltages <1.8 V, the value of this capacitor should be 100 pF. For voltages >1.8 V, the approximate value of this capacitor can be calculated as:

$$C1 = \frac{(3 \times 10^{-7}) \times (R1 + R2)}{(R1 \times R2)} \quad (5)$$

The suggested value of this capacitor for several resistor ratios is shown in the table below. If this capacitor is not used (such as in a unity-gain configuration) or if an output voltage < 1.8 V is chosen, then the minimum recommended output capacitor is 2.2 μF instead of 1 μF.



OUTPUT VOLTAGE PROGRAMMING GUIDE

OUTPUT VOLTAGE	R1	R2	C1
2.5 V	31.6 kΩ	30.1 kΩ	22 pF
3.3 V	51 kΩ	30.1 kΩ	15 pF
3.6 V	59 kΩ	30.1 kΩ	15 pF

Figure 33. TPS79101 Adjustable LDO Regulator Programming

REGULATOR PROTECTION

The TPS791xx PMOS-pass transistor has a built-in back diode that conducts reverse current when the input voltage drops below the output voltage (e.g., during power down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage operation is anticipated, external limiting might be appropriate.

The TPS791xx features internal current limiting and thermal protection. During normal operation, the TPS791xx limits output current to approximately 400 mA. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package or the absolute maximum voltage ratings of the device. If the temperature of the device exceeds approximately 165°C, thermal-protection circuitry shuts it down. Once the device has cooled down to below approximately 140°C, regulator operation resumes.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS79101DBVRQ1	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PEU1	Samples
TPS79118DBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PER1	Samples
TPS79133DBVRG4Q1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PES1	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS791-Q1 :

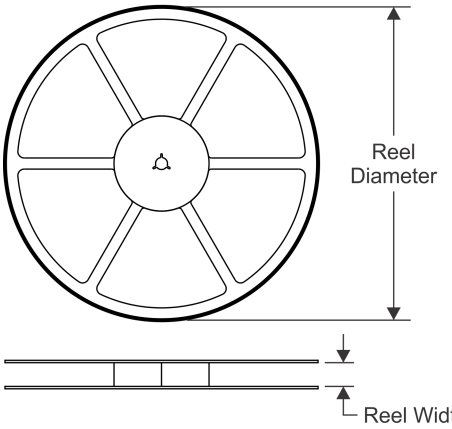
- Catalog : TPS791

NOTE: Qualified Version Definitions:

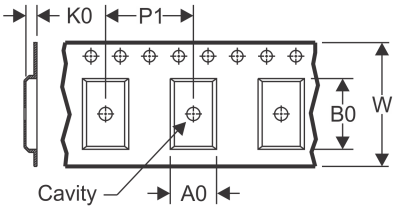
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

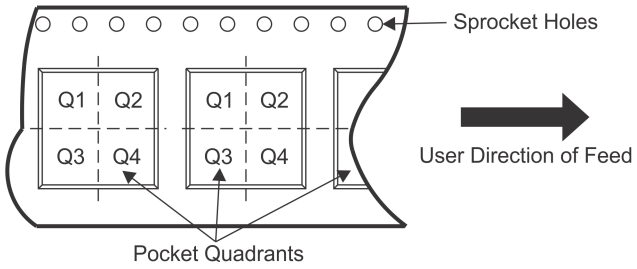


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

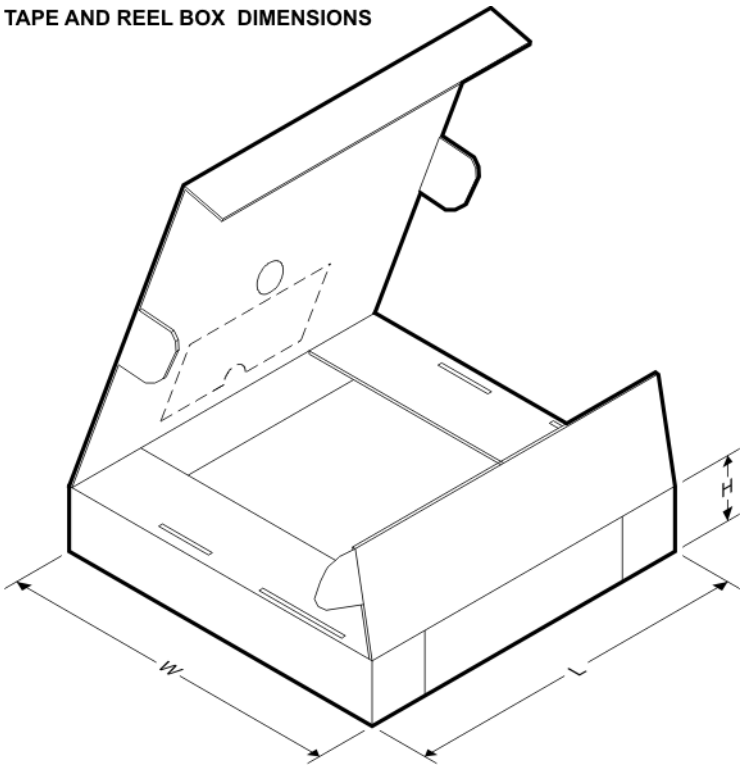
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS79101DBVRQ1	SOT-23	DBV	6	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS79118DBVRQ1	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3
TPS79133DBVRG4Q1	SOT-23	DBV	5	3000	180.0	9.0	3.15	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

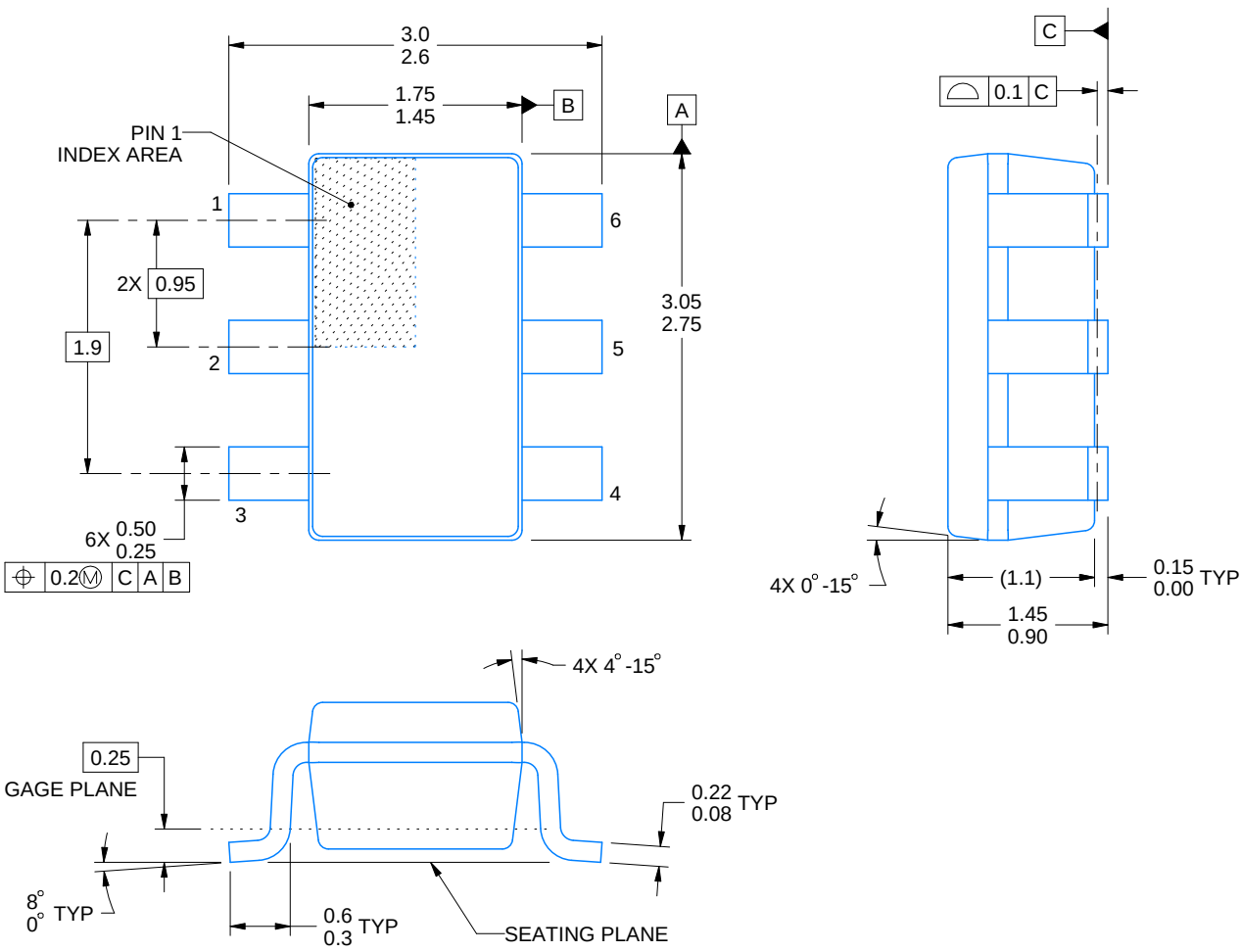
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS79101DBVRQ1	SOT-23	DBV	6	3000	182.0	182.0	20.0
TPS79118DBVRQ1	SOT-23	DBV	5	3000	182.0	182.0	20.0
TPS79133DBVRG4Q1	SOT-23	DBV	5	3000	182.0	182.0	20.0

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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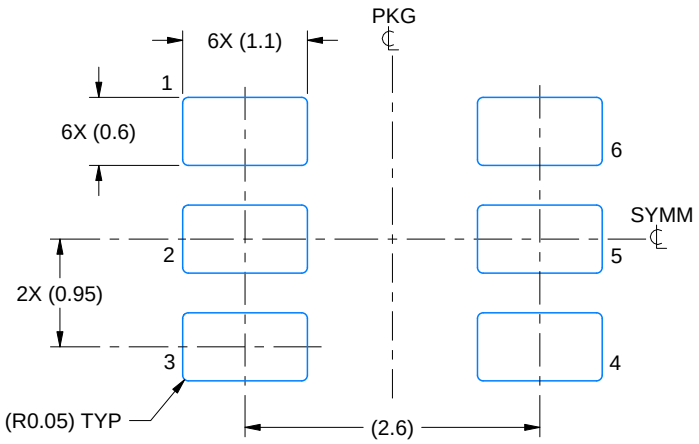
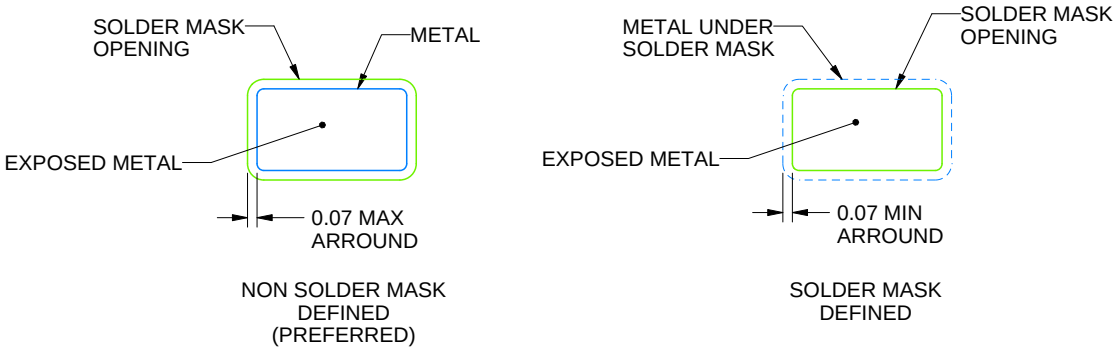
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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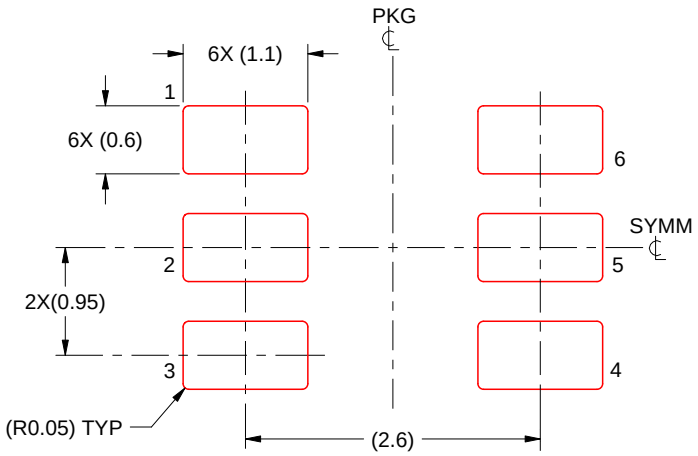
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

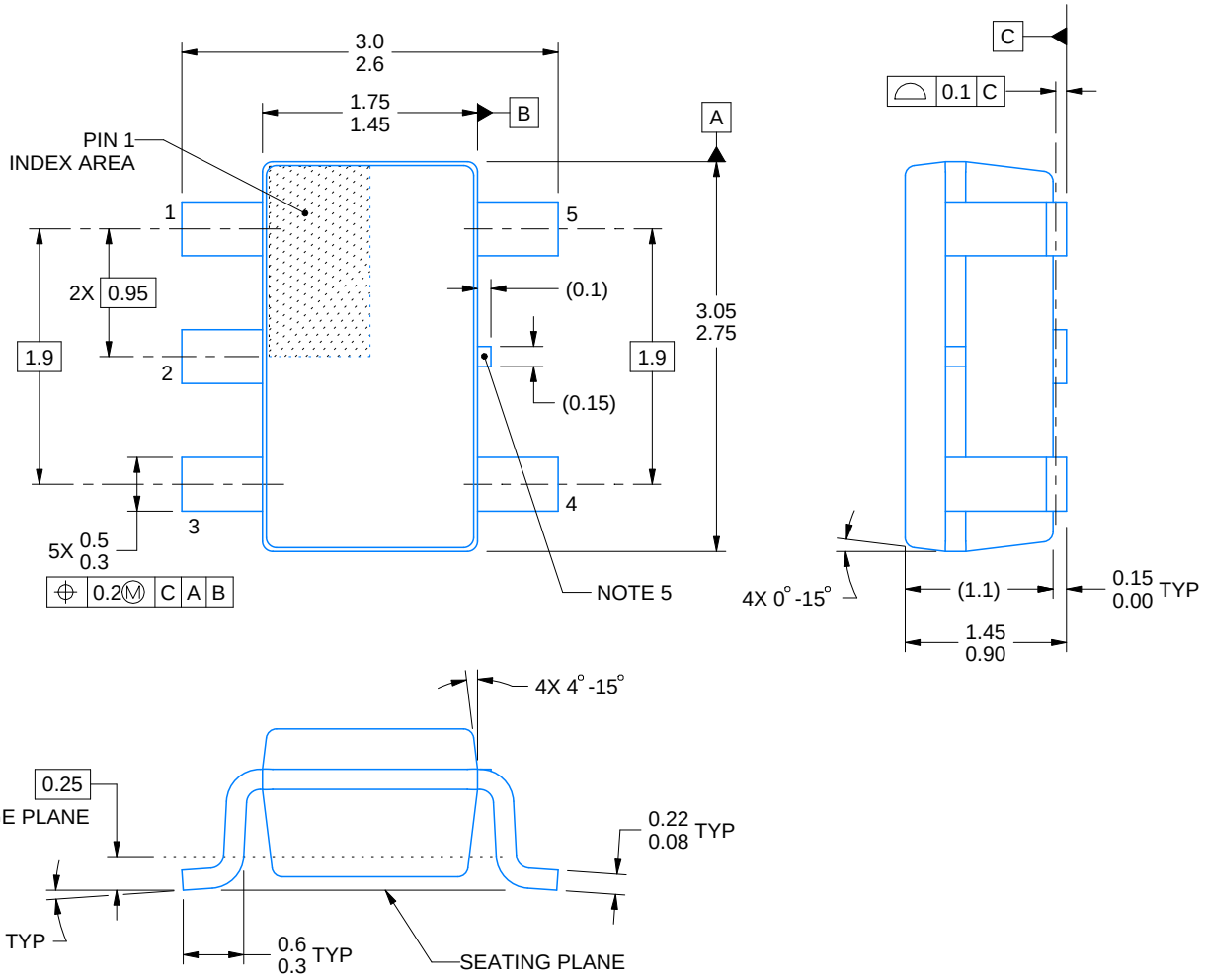
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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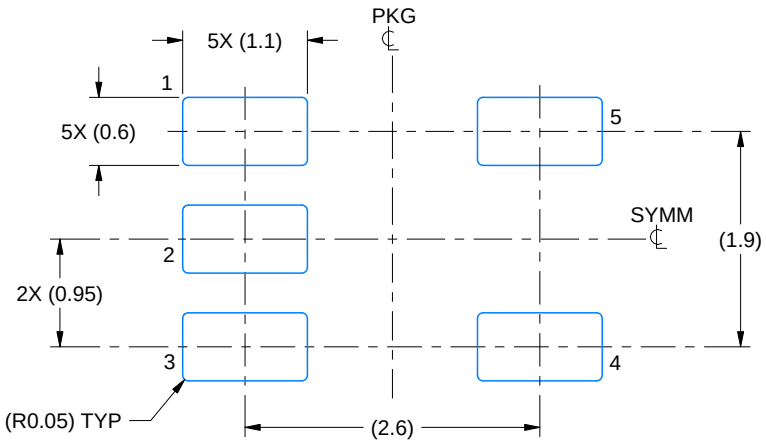
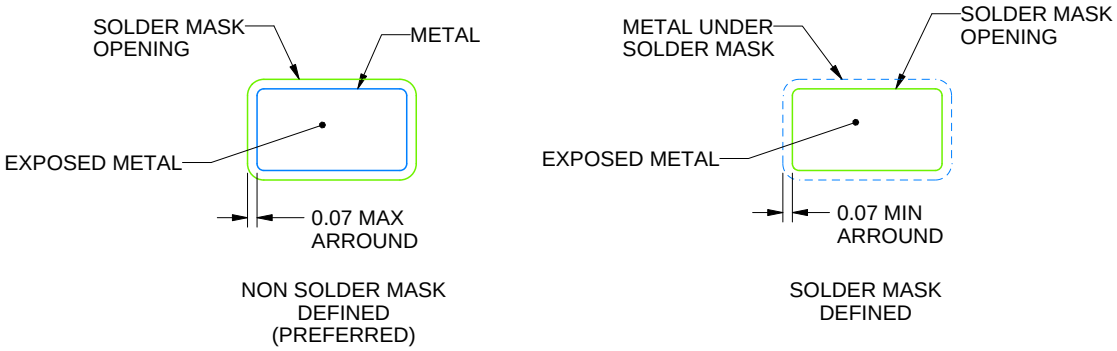
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
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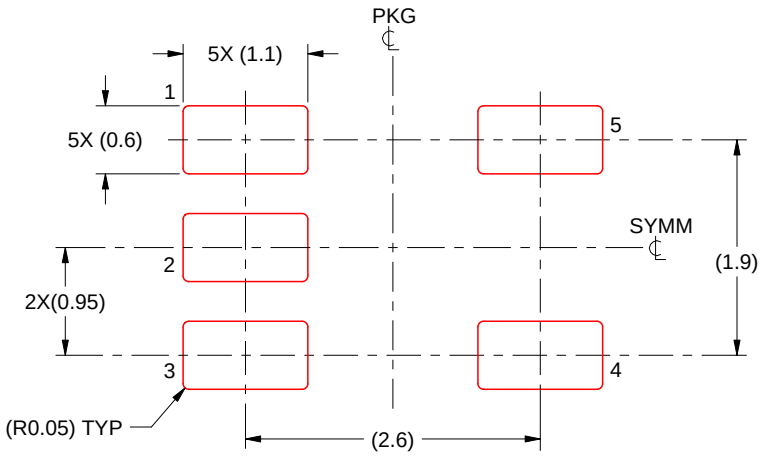

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K 08/2024

NOTES: (continued)

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9. Board assembly site may have different recommendations for stencil design.

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