

TPS7A4101 50V 输入电压、50mA 超高电压线性稳压器

1 特性

- 宽输入电压范围：7V 至 50V
- 准确度：
 - 标称：1%
 - 整个线路、负载和温度范围内：2.5%
- 低静态电流：25 μ A
- 关断时的静态电流：4.1 μ A
- 最大输出电流：50mA
- CMOS 逻辑电平兼容的使能引脚
- 可调节输出电压范围：约为 1.175V 至 48V
- 与陶瓷电容搭配工作时保持稳定：
 - 输入电容： $\geq 1\mu$ F
 - 输出电容： $\geq 4.7\mu$ F
- 压降电压：290mV
- 内置限流和热关断保护
- 封装：高导热性能 HVSSOP-8 PowerPAD™
- 工作温度范围：-40°C 至 125°C

2 应用

- 由工业用总线（具有高电压瞬态）供电的微处理器、微控制器
- 工业自动化
- 电信基础设施
- 汽车
- 发光二极管 (LED) 照明
- 偏置电源

3 说明

TPS7A4101 是一款能够耐受超高电压的线性稳压器，不仅融合了耐热增强型封装 (HVSSOP-8) 的优势，还能够承受高达 50V 的持续直流电压或瞬态输入电压。

TPS7A4101 在与任何高于 4.7 μ F 的输出电容以及高于 1 μ F 的输入电容搭配使用时，均可保持稳定（在一定的温度和容差范围内）。鉴于这款器件的封装 (HVSSOP-8) 小巧且可能使用的输出电容也较小，因此实现起来只需占用非常小的电路板空间。此外，TPS7A4101 还提供了一个与标准 CMOS 逻辑兼容的使能引脚 (EN)，用于支持低电流关断模式。

TPS7A4101 具有内部热关断和电流限制功能，以便在故障情况下保护系统。HVSSOP-8 封装的运行温度范围为 $T_J = -40^\circ\text{C}$ 至 125°C 。

此外，TPS7A4101 器件非常适合在电信和工业应用中通过中间电压轨生成低电压电源；该器件不但能够提供充分稳压的电压轨，而且能够承受超高的快速电压瞬变并在其间保持稳压状态。这些特性相当于一套更为简单且经济高效的电气浪涌保护电路，因此受到 PoE、偏置电源和 LED 照明等青睐。

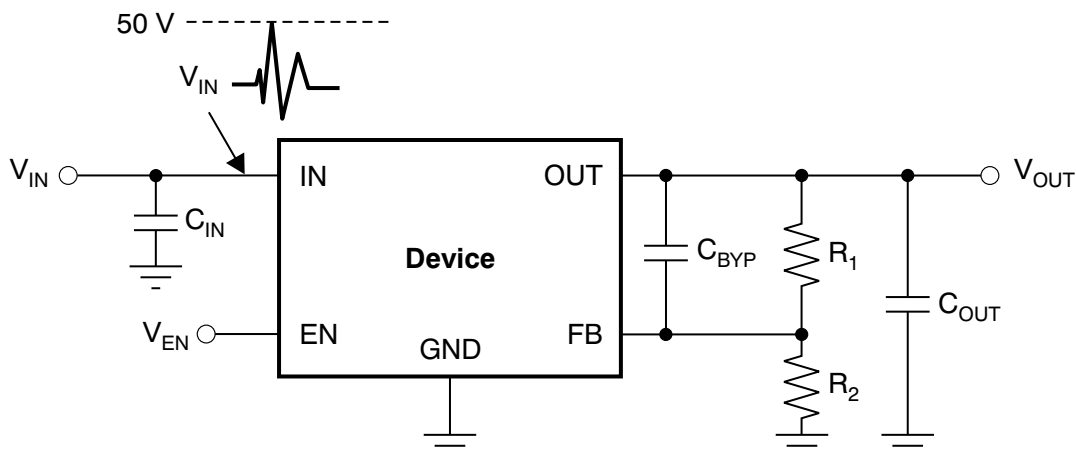
器件信息⁽¹⁾

器件型号	封装	封装尺寸 (标称值)
TPS7A4101	HVSSOP (8) ⁽²⁾	3.00mm × 3.00mm

(1) 如需了解所有可用封装，请参阅产品说明书末尾的可订购产品附录。

(2) HVSSOP 与 MSOP 相同。

典型应用图



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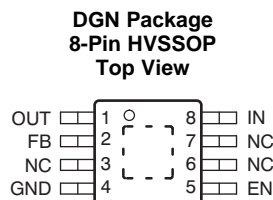
4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision A (August 2015) to Revision B	Page
• 已更改 通篇将 MSOP 更改为 HVSSOP	1
• Changed minimum specifications of –55 V to –60 V and changed maximum specifications of 55 V to 60 V in <i>Voltage</i> parameter of <i>Absolute Maximum Ratings</i> table	3
• Added parameter names to <i>Recommended Operating Conditions</i> table	4
• Deleted T_J parameter from <i>Electrical Characteristics</i> table	5
• Deleted <i>Dissipation Ratings</i> table	6
• Changed T_J value for disabled mode operating mode from 165 to 170°C	9

Changes from Original (December 2011) to Revision A	Page
• 已添加 <i>ESD</i> 额定值表，特性 说明 部分、器件功能模式、应用和实施 部分、电源建议 部分、布局 部分、器件和文档支持 部分以及机械、封装和可订购信息 部分。	1
• Changed maximum <i>Recommended Operation Conditions</i> values for VIN, VOUT, and VEN.	4

5 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
OUT	1	O	Regulator output. A capacitor greater than 4.7 μ F must be tied from this pin to ground to assure stability.
FB	2	I	This pin is the input to the control-loop error amplifier. This pin is used to set the output voltage of the device.
NC	3, 6, 7	—	Not internally connected. This pin must either be left open or tied to GND.
GND	4	—	Ground
EN	5	I	This pin turns the regulator on or off. If $V_{EN} \geq V_{EN_HI}$ the regulator is enabled. If $V_{EN} \leq V_{EN_LO}$, the regulator is disabled. If not used, the EN pin can be connected to IN. Make sure that $V_{EN} \leq V_{IN}$ at all times.
IN	8	I	Input supply
PowerPAD	—	—	Solder to printed-circuit-board (PCB) to enhance thermal performance. The PowerPAD is internally connected to GND. Although the PowerPAD can be left floating, TI highly recommends connecting the PowerPAD to the GND plane.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
Voltage	IN pin to GND pin	–0.3	60	V
	OUT pin to GND pin	–0.3	60	
	OUT pin to IN pin	–60	0.3	
	FB pin to GND pin	–0.3	2	
	FB pin to IN pin	–60	0.3	
	EN pin to IN pin	–60	0.3	
	EN pin to GND pin	–0.3	60	
Current	Peak output	Internally limited		
Temperature	Operating junction, T_J	–40	125	°C
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	\pm 2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	\pm 500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	7		50	V
V_{OUT}	Output voltage	1.161		48	V
V_{EN}	Enable pin voltage	0		50	V
I_{OUT}	Output current	0		50	mA

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPS7A4101	UNIT
		DGN (HVSSOP)	
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	66.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	54.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	38.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	37.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	15.5	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics application report](#).

6.5 Electrical Characteristics

at $T_J = -40^\circ\text{C}$ to 125°C , $V_{IN} = V_{OUT(NOM)} + 2\text{ V}$ or $V_{IN} = 7\text{ V}$ (whichever is greater), $V_{EN} = V_{IN}$, $I_{OUT} = 100\ \mu\text{A}$, $C_{IN} = 1\ \mu\text{F}$, $C_{OUT} = 4.7\ \mu\text{F}$, and FB tied to OUT (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range		7		50	V
V_{REF}	Internal reference	$T_J = 25^\circ\text{C}$, $V_{FB} = V_{REF}$, $V_{IN} = 9\text{ V}$, $I_{OUT} = 25\text{ mA}$	1.161	1.173	1.185	V
V_{OUT}	Output voltage range ⁽¹⁾	$V_{IN} \geq V_{OUT(NOM)} + 2\text{ V}$	V_{REF}		48	V
	Nominal accuracy	$T_J = 25^\circ\text{C}$, $V_{IN} = 9\text{ V}$, $I_{OUT} = 25\text{ mA}$	-1		1	% V_{OUT}
	Overall accuracy	$V_{OUT(NOM)} + 2\text{ V} \leq V_{IN} \leq 24\text{ V}$ ⁽²⁾ $100\ \mu\text{A} \leq I_{OUT} \leq 50\text{ mA}$	-2.5		2.5	% V_{OUT}
$\Delta V_{O(\Delta VI)}$	Line regulation	$7\text{ V} \leq V_{IN} \leq 50\text{ V}$		0.03		% V_{OUT}
$\Delta V_{O(\Delta VL)}$	Load regulation	$100\ \mu\text{A} \leq I_{OUT} \leq 50\text{ mA}$		0.31		% V_{OUT}
V_{DO}	Dropout voltage	$V_{IN} = 17\text{ V}$, $V_{OUT(NOM)} = 18\text{ V}$, $I_{OUT} = 20\text{ mA}$		290		mV
		$V_{IN} = 17\text{ V}$, $V_{OUT(NOM)} = 18\text{ V}$, $I_{OUT} = 50\text{ mA}$		0.78	1.3	V
I_{LIM}	Current limit	$V_{OUT} = 90\% V_{OUT(NOM)}$, $V_{IN} = 7\text{ V}$, $T_J \leq 85^\circ\text{C}$	51	117	200	mA
		$V_{OUT} = 90\% V_{OUT(NOM)}$, $V_{IN} = 9\text{ V}$	51	128	200	
I_{GND}	Ground current	$7\text{ V} \leq V_{IN} \leq 50\text{ V}$, $I_{OUT} = 0\text{ mA}$		25	65	μA
		$I_{OUT} = 50\text{ mA}$		25		
I_{SHDN}	Shutdown supply current	$V_{EN} = 0.4\text{ V}$		4.1	20	μA
I_{FB}	Feedback current ⁽³⁾		-0.1	0.01	0.1	μA
I_{EN}	Enable current	$7\text{ V} \leq V_{IN} \leq 50\text{ V}$, $V_{IN} = V_{EN}$		0.02	1	μA
V_{EN_HI}	Enable high-level voltage		1.5		V_{IN}	V
V_{EN_LO}	Enable low-level voltage		0		0.4	V
V_{NOISE}	Output noise voltage	$V_{IN} = 12\text{ V}$, $V_{OUT(NOM)} = V_{REF}$, $C_{OUT} = 10\ \mu\text{F}$, $BW = 10\text{ Hz to }100\text{ kHz}$		58		μV_{RMS}
		$V_{IN} = 12\text{ V}$, $V_{OUT(NOM)} = 5\text{ V}$, $C_{OUT} = 10\ \mu\text{F}$, C_{BYP} ⁽⁴⁾ = 10 nF , $BW = 10\text{ Hz to }100\text{ kHz}$		73		
PSRR	Power-supply rejection ratio	$V_{IN} = 12\text{ V}$, $V_{OUT(NOM)} = 5\text{ V}$, $C_{OUT} = 10\ \mu\text{F}$, C_{BYP} ⁽⁴⁾ = 10 nF , $f = 100\text{ Hz}$		65		dB
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing		170		$^\circ\text{C}$
		Reset, temperature decreasing		150		

- (1) To ensure stability at no-load conditions, a current from the feedback resistive network greater than or equal to $10\ \mu\text{A}$ is required.
- (2) Maximum input voltage is limited to 24 V because of the package power dissipation limitations at full load ($P \approx (V_{IN} - V_{OUT}) \times I_{OUT} = (24\text{ V} - V_{REF}) \times 50\text{ mA} \approx 1.14\text{ W}$). The device is capable of sourcing a maximum current of 50 mA at higher input voltages as long as the power dissipated is within the thermal limits of the package plus any external heatsinking.
- (3) $I_{FB} > 0$ flows out of the device.
- (4) C_{BYP} refers to a bypass capacitor connected to the FB and OUT pins.

6.6 Typical Characteristics

at $T_J = -40^\circ\text{C}$ to 125°C , $V_{IN} = V_{OUT(NOM)} + 2\text{ V}$ or $V_{IN} = 9\text{ V}$ (whichever is greater), $V_{EN} = V_{IN}$, $I_{OUT} = 100\ \mu\text{A}$, $C_{IN} = 1\ \mu\text{F}$, $C_{OUT} = 4.7\ \mu\text{F}$, and FB tied to OUT (unless otherwise noted)

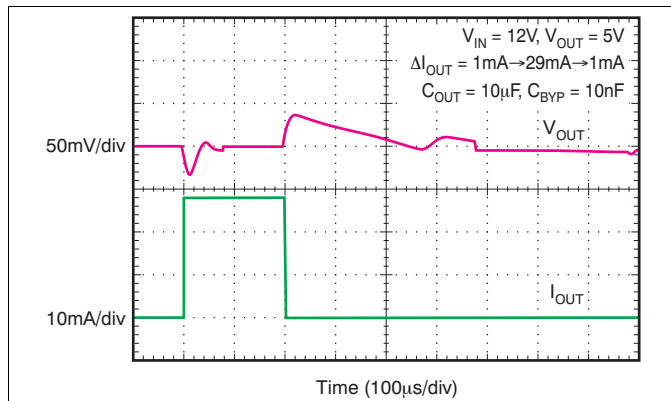


Figure 1. Load Transient Response

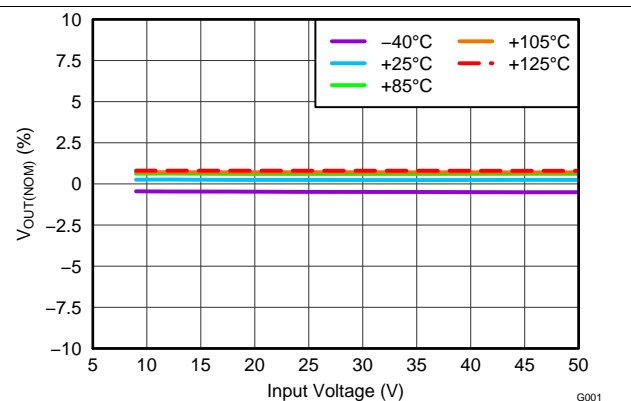


Figure 2. Line Regulation

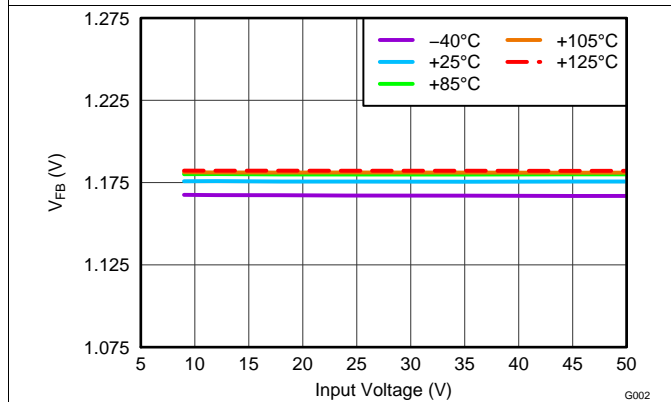


Figure 3. Feedback Voltage

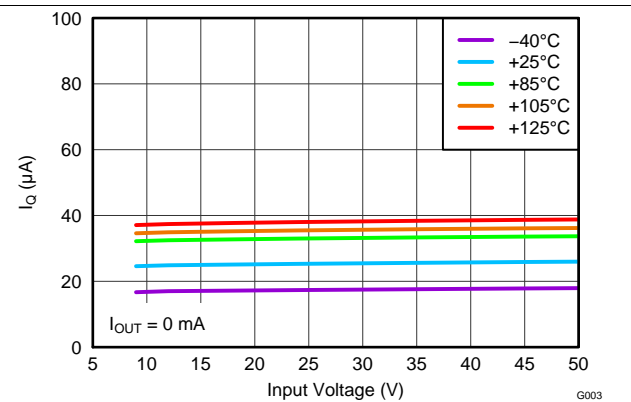


Figure 4. Quiescent Current vs Input Voltage

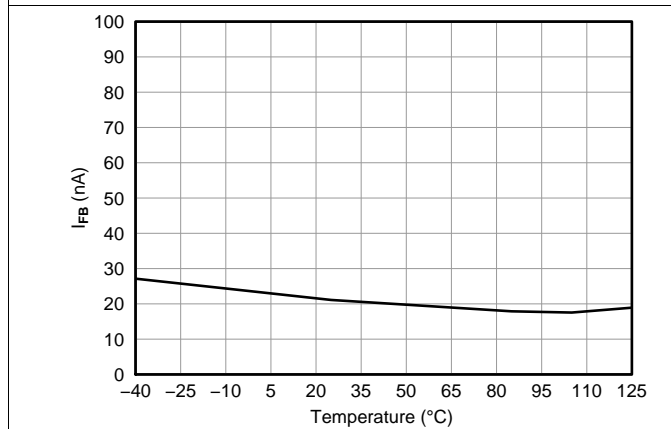


Figure 5. Feedback Current

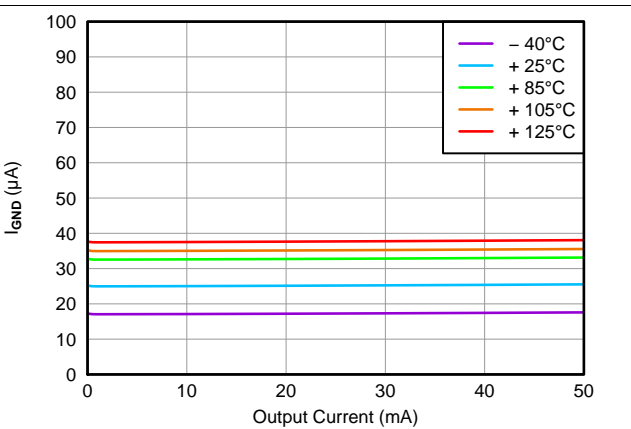


Figure 6. Ground Current

Typical Characteristics (continued)

at $T_J = -40^{\circ}\text{C}$ to 125°C , $V_{IN} = V_{OUT(NOM)} + 2\text{ V}$ or $V_{IN} = 9\text{ V}$ (whichever is greater), $V_{EN} = V_{IN}$, $I_{OUT} = 100\ \mu\text{A}$, $C_{IN} = 1\ \mu\text{F}$, $C_{OUT} = 4.7\ \mu\text{F}$, and FB tied to OUT (unless otherwise noted)

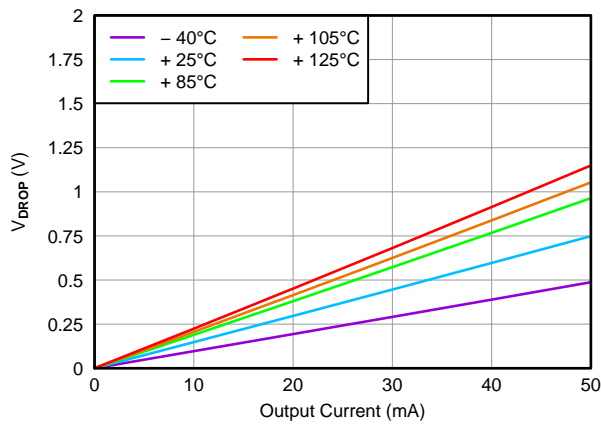


Figure 7. Dropout Voltage

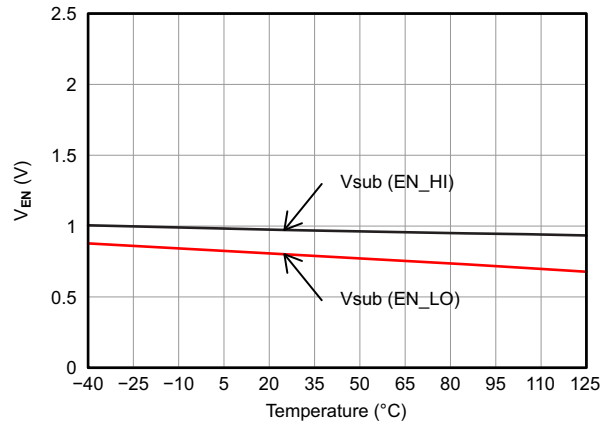


Figure 8. Enable Threshold Voltage

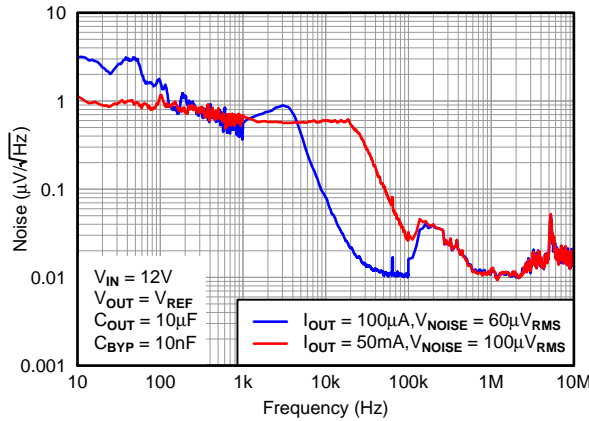


Figure 9. Output Spectral Noise Density

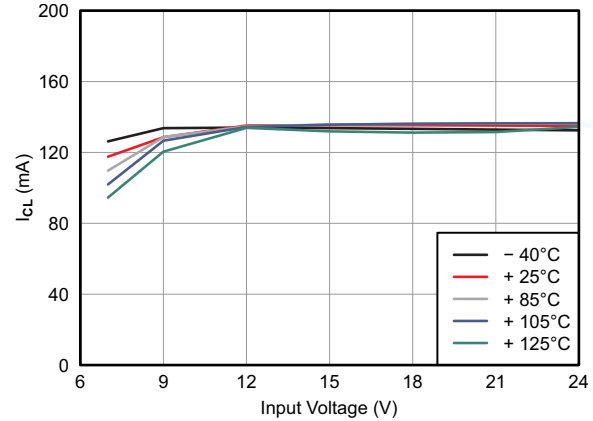


Figure 10. Current Limit

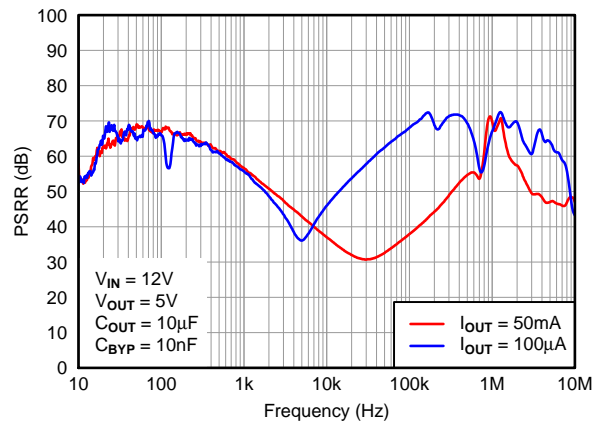


Figure 11. Power-Supply Rejection Ratio

7 Detailed Description

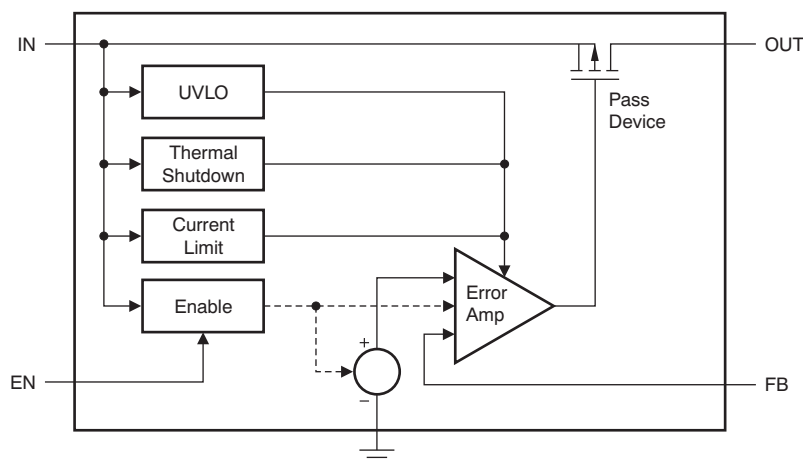
7.1 Overview

The TPS7A4101 belongs to a family of linear regulators that use an innovative BiCMOS process technology to achieve very high maximum input and output voltages.

This process not only allows the TPS7A4101 to maintain regulation during very fast high-voltage transients up to 50 V, but this process also allows the TPS7A4101 to regulate from a continuous high-voltage input rail. Unlike other regulators created using bipolar technology, the TPS7A4101 ground current is also constant over its output current range, resulting in increased efficiency and lower power consumption.

These features, combined with a high thermal performance HVSSOP-8 PowerPAD package, make this device ideal for industrial and telecom applications.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Enable Pin Operation

The TPS7A4101 provides an enable pin (EN) feature that turns on the regulator when $V_{EN} > 1.5\text{ V}$.

7.3.2 Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 170°C, allowing the device to cool. When the junction temperature cools to approximately 150°C, the output circuitry is enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, thus providing protection from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, limit junction temperature to a maximum of 125°C. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, trigger thermal protection at least 35°C above the maximum expected ambient condition of your particular application. This configuration produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS7A4101 is designed to protect against overload conditions. The protection circuitry is not intended to replace proper heatsinking. Continuously running the device into thermal shutdown degrades device reliability.

7.4 Device Functional Modes

7.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage is at least as high as $V_{IN(min)}$.
- The input voltage is greater than the nominal output voltage added to the dropout voltage.
- The enable voltage has previously exceeded the enable rising threshold voltage and has not decreased below the enable falling threshold.
- The output current is less than the current limit.
- The device junction temperature is less than the maximum specified junction temperature.

7.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode of operation, the output voltage is the same as the input voltage minus the dropout voltage. The transient performance of the device is significantly degraded because the pass device (as a bipolar junction transistor, or BJT) is in saturation and no longer controls the current through the LDO. Line or load transients in dropout can result in large output voltage deviations.

7.4.3 Disabled

The device is disabled under the following conditions:

- The enable voltage is less than the enable falling threshold voltage or has not yet exceeded the enable rising threshold.
- The device junction temperature is greater than the thermal shutdown temperature.

Table 1 lists the conditions that lead to the different modes of operation.

Table 1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	V_{EN}	I_{OUT}	T_J
Normal mode	$V_{IN} > V_{OUT(nom)} + V_{DO}$ and $V_{IN} > V_{IN(min)}$	$V_{EN} > V_{EN_HI}$	$I_{OUT} < I_{LIM}$	$T_J < 125^{\circ}C$
Dropout mode	$V_{IN(min)} < V_{IN} < V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{EN_HI}$	—	$T_J < 125^{\circ}C$
Disabled mode (any true condition disables the device)	—	$V_{EN} < V_{EN_LO}$	—	$T_J > 170^{\circ}C$

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Adjustable Operation

The TPS7A4101 has an output voltage range of approximately 1.175 V to 48 V. The nominal output voltage of the device is set by two external resistors, as shown in [Figure 12](#).

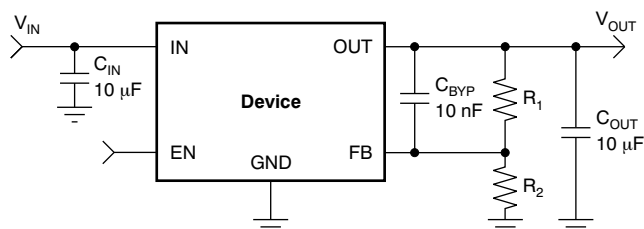


Figure 12. Adjustable Operation for Maximum AC Performance

R_1 and R_2 can be calculated for any output voltage range using the formula shown in [Equation 1](#). To ensure stability under no-load conditions, this resistive network must provide a current greater than or equal to 10 μ A.

$$R_1 = R_2 \left(\frac{V_{OUT}}{V_{REF}} - 1 \right), \text{ where } \frac{V_{OUT}}{R_1 + R_2} \geq 10 \mu\text{A} \quad (1)$$

If greater voltage accuracy is required, take into account the output voltage offset contributions because of the feedback pin current and use 0.1% tolerance resistors.

8.1.2 Transient Voltage Protection

One of the primary applications of the TPS7A4101 is to provide transient voltage protection to sensitive circuitry that may be damaged in the presence of high-voltage spikes.

This transient voltage protection can be more cost-effective and compact compared to topologies that use a transient voltage suppression (TVS) block.

8.2 Typical Application

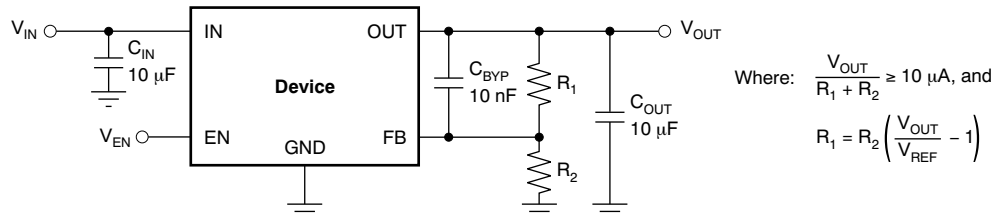


Figure 13. Example Circuit to Maximize Transient Performance

8.2.1 Design Requirements

For this design example, use the following parameters listed in Table 2.

Table 2. Design Parameters

PARAMETER	VALUE
V_{IN}	12 V, with 50 V surge tolerance
V_{OUT}	5 V (ideal), 4.981 V (actual)
I_{OUT}	28 mA
Accuracy	5 %
R1, R2	162 k Ω , 49.9 k Ω

8.2.2 Detailed Design Procedure

The maximum value of total feedback resistance can be calculated to be 500 k Ω . Equation 1 was used to calculate R1 and R2, and standard 1% resistors were selected to keep the accuracy within the 5% allocation. 10- μF ceramic input and output capacitors were selected, along with a 10-nF bypass capacitor for optimal AC performance.

8.2.2.1 Capacitor Recommendations

Low equivalent series resistance (ESR) capacitors should be used for the input, output, and bypass capacitors. Ceramic capacitors with X7R and X5R dielectrics are preferred. These dielectrics offer more stable characteristics. Ceramic X7R capacitors offer improved over-temperature performance, while ceramic X5R capacitors are the most cost-effective and are available in higher values.

High ESR capacitors may degrade PSRR.

8.2.2.2 Input and Output Capacitor Requirements

The TPS7A4101 high voltage linear regulator achieves stability with a minimum output capacitance of 4.7 μF and input capacitance of 1 μF ; however, TI highly recommends using 10- μF output and input capacitors to maximize AC performance.

8.2.2.3 Bypass Capacitor Requirements

Although a bypass capacitor (C_{BYP}) is not needed to achieve stability, TI highly recommends using a 10-nF bypass capacitor to maximize AC performance (including line transient, noise and PSRR).

8.2.2.4 Maximum AC Performance

To maximize line transient, noise, and PSRR performance, TI recommends including 10- μF (or higher) input and output capacitors, and a 10-nF bypass capacitor; see Figure 12. The solution shown delivers minimum noise levels of 58 μV_{RMS} and power-supply rejection levels above 36 dB from 10 Hz to 10 MHz.

8.2.2.5 Transient Response

As with any regulator, increasing the size of the output capacitor reduces over/undershoot magnitude but increases duration of the transient response.

The presence of the C_{BYP} capacitor may greatly improve the TPS7A4101 line transient response, as noted in [Figure 1](#).

8.2.3 Application Curve

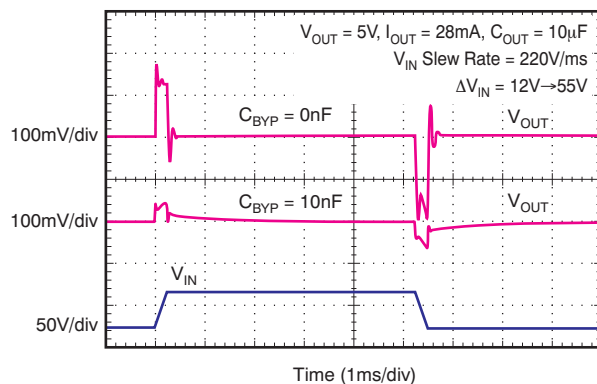


Figure 14. Line Transient Response vs C_{BYP}

9 Power Supply Recommendations

The input supply for the LDO should not exceed its recommended operating conditions (7 V to 50 V). The input voltage should provide adequate headroom for the device to have a regulated output. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance. The input and output supplies should also be bypassed with 10- μF capacitors located near the input and output pins. There should be no other components located between these capacitors and the pins.

10 Layout

10.1 Layout Guidelines

To improve AC performance such as PSRR, output noise, and transient response, TI recommends designing the board with separate ground planes for IN and OUT, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the output capacitor should connect directly to the GND pin of the device.

Equivalent series inductance (ESL) and ESR must be minimized to maximize performance and ensure stability. Every capacitor (C_{IN} , C_{OUT} , C_{BYP}) must be placed as close as possible to the device and on the same side of the PCB as the regulator itself.

Do not place any of the capacitors on the opposite side of the PCB from where the regulator is installed. The use of vias and long traces is strongly discouraged because they may impact system performance negatively and even cause instability.

If possible, and to ensure the maximum performance denoted in this product data sheet, use the same layout pattern used for TPS7A4101 evaluation board, available at www.ti.com.

10.1.1 Thermal Considerations

Thermal protection disables the output when the junction temperature rises to approximately 170°C, allowing the device to cool. When the junction temperature cools to approximately 150°C, the output circuitry is enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, thus providing protection from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to a maximum of 125°C. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least 35°C above the maximum expected ambient condition of the particular application. This configuration produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS7A4101 has been designed to protect against overload conditions. This circuitry is not intended to replace proper heatsinking. Continuously running the TPS7A4101 into thermal shutdown degrades device reliability.

10.1.2 Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the PCB layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for JEDEC low- and high-K boards are given in the [Thermal Information](#) table. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat dissipating layers also improves the heatsink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation (P_D) is equal to the product of the output current times the voltage drop across the output pass element, as shown in [Equation 2](#):

$$P_D = (V_{IN} - V_{OUT}) I_{OUT} \quad (2)$$

10.1.3 Package Mounting

Solder pad footprint recommendations for the TPS7A4101 are available at the end of this document and at www.ti.com.

10.2 Layout Example

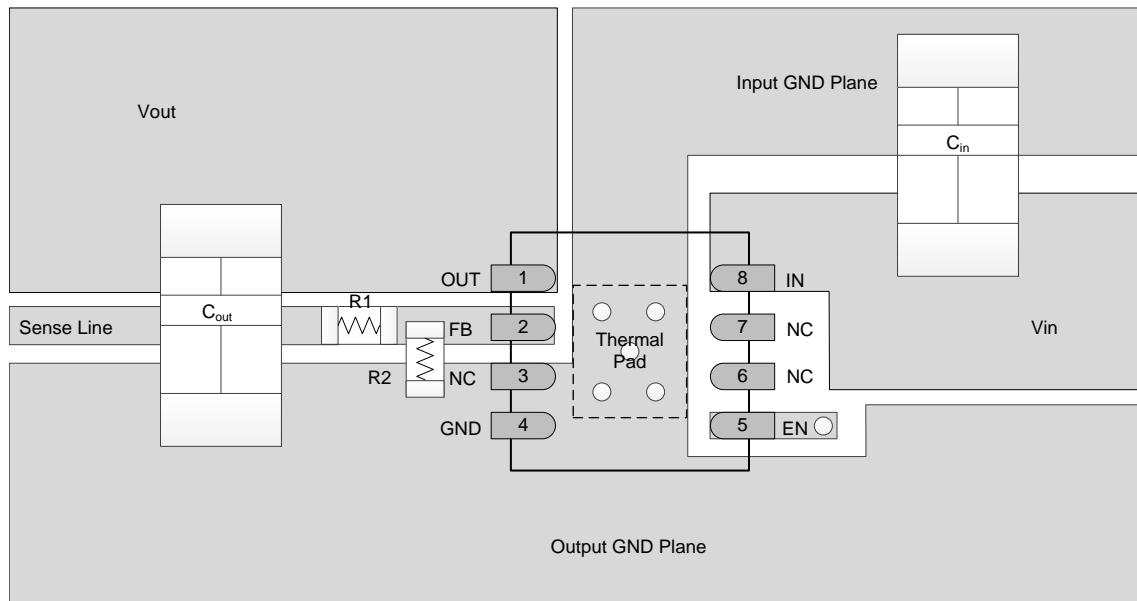


Figure 15. Recommended Layout Example

11 器件和文档支持

11.1 接收文档更新通知

要接收文档更新通知，请导航至 TI.com.cn 上的器件产品文件夹。单击右上角的通知我进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

11.2 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

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设计支持 *TI 参考设计支持* 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

11.3 商标

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11.4 静电放电警告



ESD 可能会损坏该集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理措施和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

11.5 术语表

SLYZ022 — *TI 术语表*。

这份术语表列出并解释术语、缩写和定义。

12 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知，且不会对此文档进行修订。如需获取此数据表的浏览器版本，请查阅左侧的导航栏。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS7A4101DGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	SBB	Samples
TPS7A4101DGNT	ACTIVE	HVSSOP	DGN	8	250	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	SBB	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A4101DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
TPS7A4101DGNT	HVSSOP	DGN	8	250	180.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A4101DGNR	HVSSOP	DGN	8	2500	346.0	346.0	35.0
TPS7A4101DGNT	HVSSOP	DGN	8	250	200.0	183.0	25.0

GENERIC PACKAGE VIEW

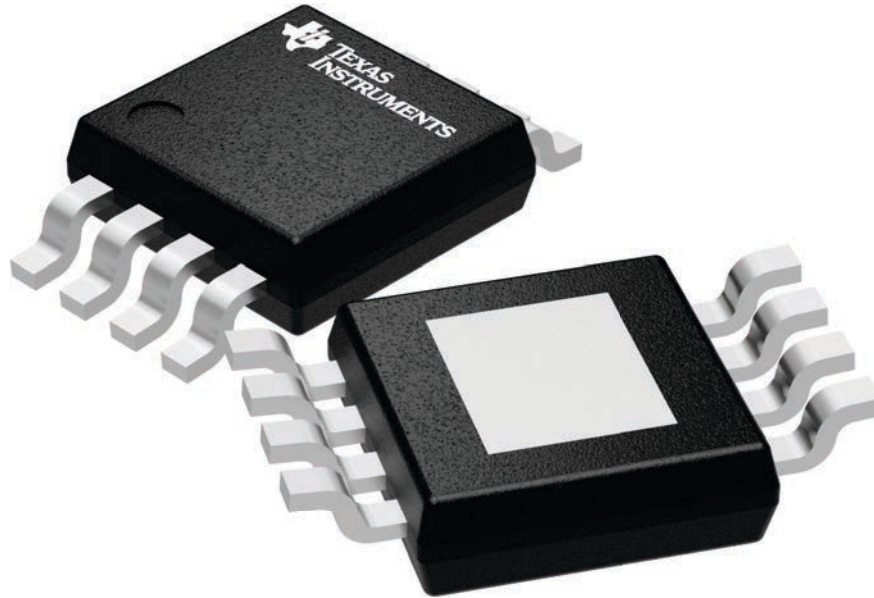
DGN 8

PowerPAD VSSOP - 1.1 mm max height

3 x 3, 0.65 mm pitch

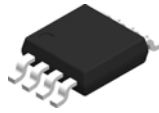
SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225482/A

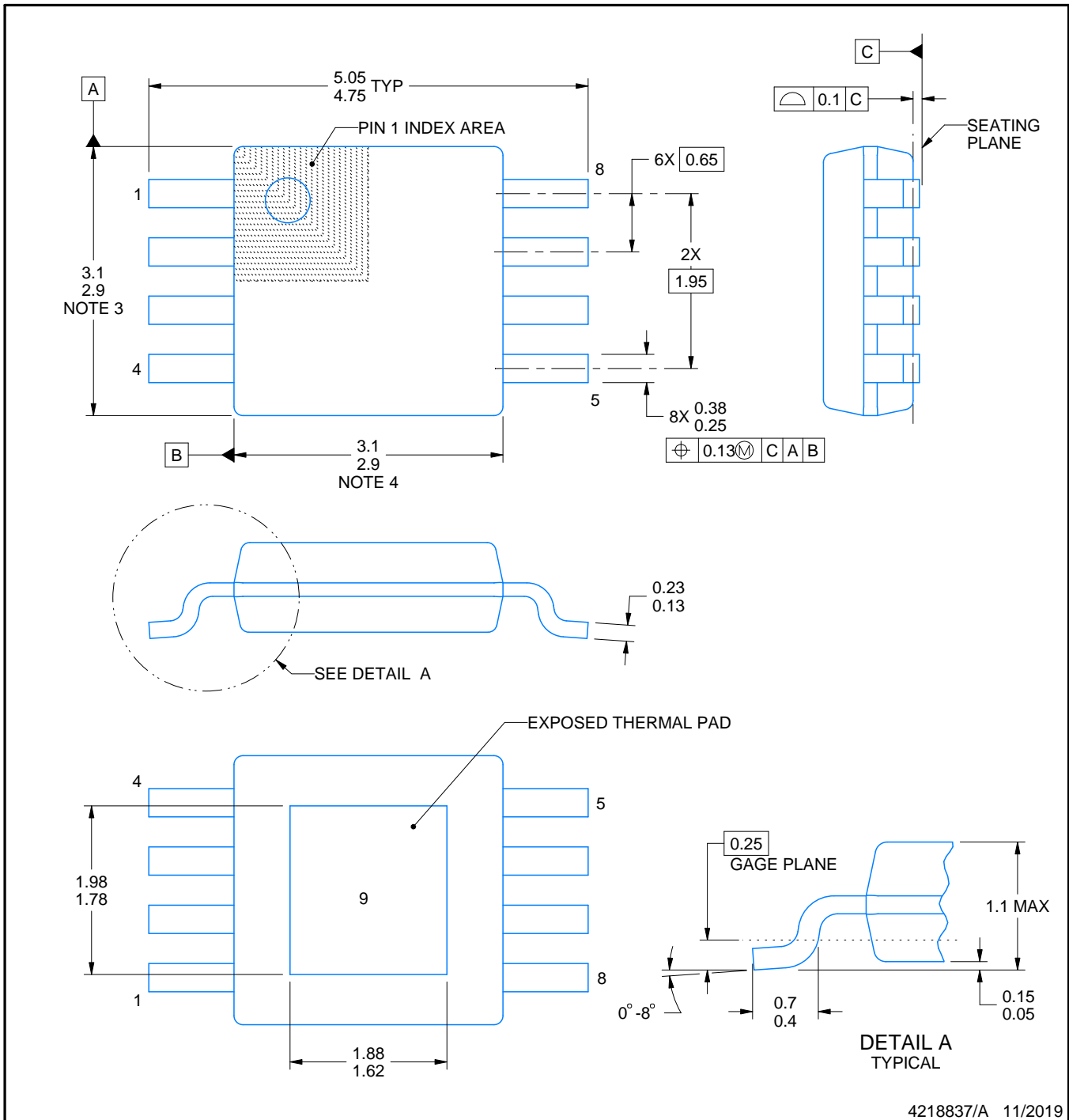
DGN0008B



PACKAGE OUTLINE

PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



4218837/A 11/2019

PowerPAD is a trademark of Texas Instruments.

NOTES:

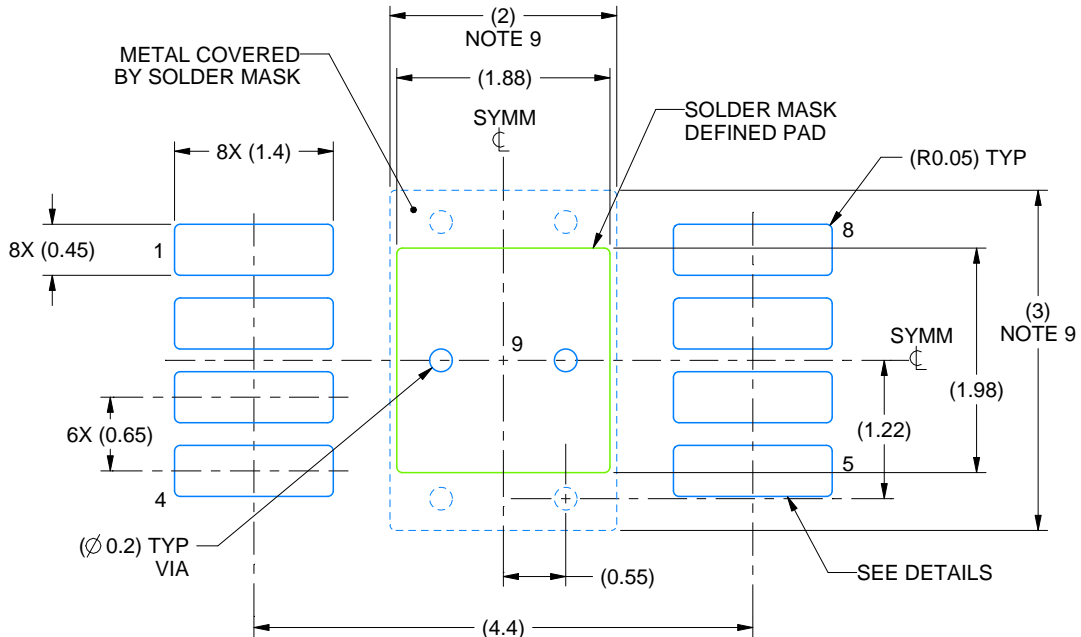
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

EXAMPLE BOARD LAYOUT

DGN0008B

PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X



SOLDER MASK DETAILS

4218837/A 11/2019

NOTES: (continued)

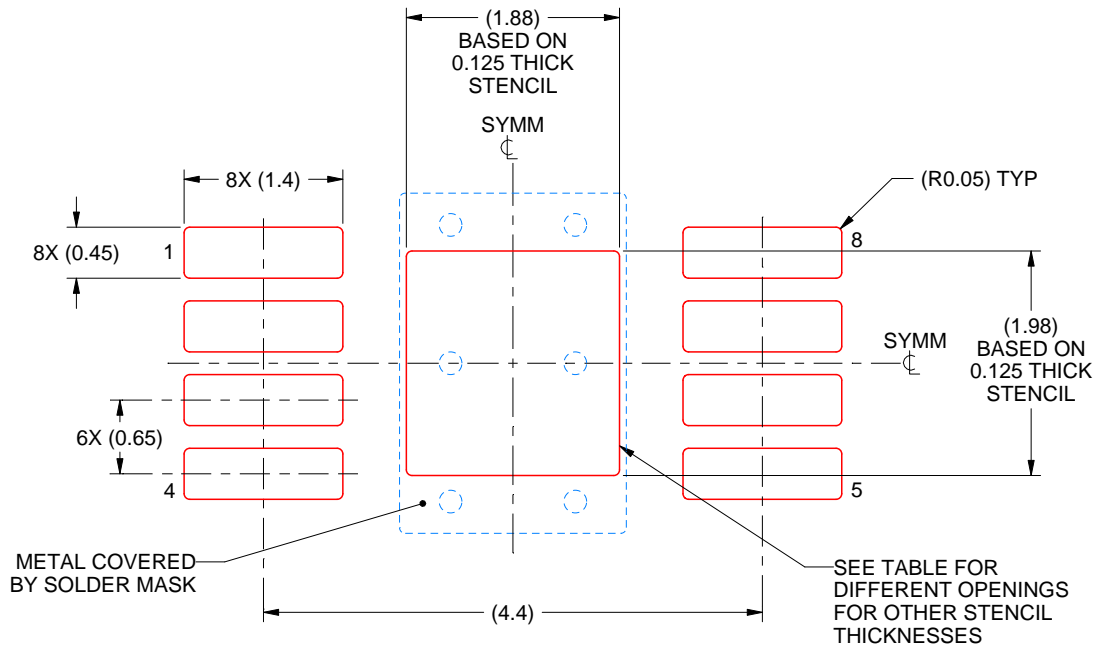
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

DGN0008B

PowerPAD™ VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.10 X 2.21
0.125	1.88 X 1.98 (SHOWN)
0.15	1.72 X 1.81
0.175	1.59 X 1.67

4218837/A 11/2019

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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