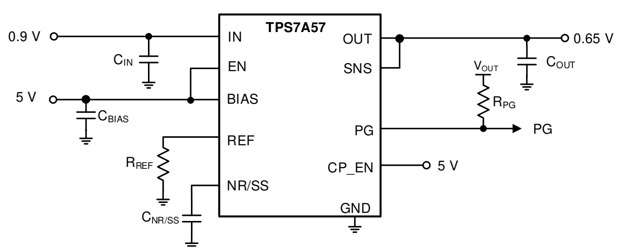
TPS7A57 5A、低 V_{IN} (0.7V)、低噪声 (2.1µV_{RMS})、高精度 (1%)、超低压降 (LDO) 稳压器

1 特性

- 输入电压范围：
  - 无偏置：1.1V 至 6.0V
  - 有偏置：0.7V 至 6.0V
- 输出电压噪声：2.45μV_{RMS}
- 整个线路、负载和温度范围内为 1%（最高）精度
- 低压降：75mV (5A)
- 电源抑制比 (5A)：
  - 1kHz 时为 100dB
  - 10kHz 时为 78dB
  - 100kHz 时为 60dB
  - 在 1MHz 时为 36dB
- 出色负载瞬态响应：
  - ±2mV，负载阶跃为 100mA 至 5A
- 可调输出电压范围：0.5V 至 5.2V
- 可调软启动浪涌控制
- BIAS 电源轨：
  - 内部电荷泵或 3V 至 11V 外部电源轨
  - 可禁用内部电荷泵
- 开漏电源正常状态 (PG) 输出
- 封装：3mm × 3mm 16 引脚 WQFN
  - EVM $R_{\theta JA}$：21.9°C/W

2 应用

- 宏远程无线电单元 (RRU)
- 室外回程单元
- 有源天线系统 mMIMO (AAS)
- 超声波扫描仪
- 实验室和现场仪表
- 传感器、成像和雷达



典型应用电路

3 说明

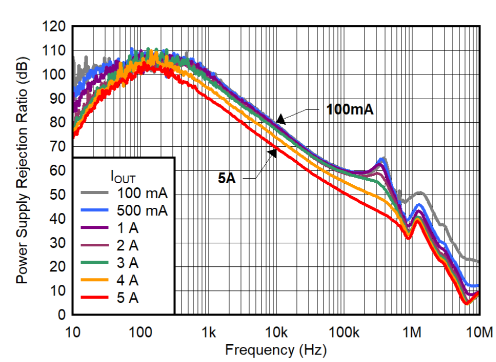
TPS7A57 是一款低噪声 (2.45µV_{RMS})、低压降线性稳压器 (LDO)，可提供 5A 电流，压降仅为 75mV（独立于输出电压）。该器件的输出电压可通过一个外部电阻进行调节，范围为 0.5V 至 5.2V。TPS7A57 集低噪声、高 PSRR（1MHz 时为 36dB）和高输出电流能力等特性一体，专为雷达电源、通信和成像应用中的噪声敏感型组件（例如射频放大器、雷达传感器、SERDES 和模拟芯片组）供电而设计。

需要以低输入和低输出 (LILO) 电压运行的数字负载（例如应用特定集成电路 (ASIC)、现场可编程门阵列 (FPGA) 和数字信号处理器 (DSP)）还能够从出色精度（在负载、线路和温度范围内可达 1%）、遥感功能、出色的瞬态性能和软启动功能中受益，以提供出色的系统性能。凭借多功能性、高性能和小尺寸解决方案，该 LDO 成为模数转换器 (ADC)、数模转换器 (DAC) 和成像传感器等高电流模拟负载以及串行器/解串器 (SerDes)、FPGA 和 DSP 等数字负载的理想选择。

封装信息(1)

器件型号	封装	封装尺寸（标称值）
TPS7A57	WQFN (16)	3.00mm × 3.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。



5A、1.2V_{IN}、0.9V_{OUT} PSRR，已启用 CP

内容

4 Revision History

注：以前版本的页码可能与当前版本的页码不同

DATE	REVISION	NOTES
July 2022	*	Initial release

5 Pin Configuration and Functions

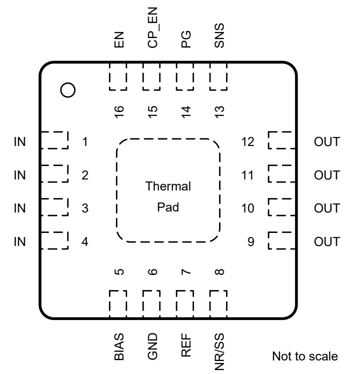


图 5-1. RTE Package, 16-Pin WQFN (Top View)

Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
BIAS	5	I	BIAS supply voltage pin. See the *Charge Pump Enable and BIAS Rail* section for additional information.
CP_EN	15	I	Charge pump enable pin. See the *Charge Pump Enable and BIAS Rail* section for additional information.
EN	16	I	Enable pin. See the *Precision Enable and UVLO* section for additional information.
GND	6	GND	Ground pin. See the *Layout Guidelines* section for additional information.
IN	1, 2, 3, 4	I	Input supply voltage pin. See the *Input and Output Capacitor Requirements (C_{IN} and C_{OUT})* section for more details.
NR/SS	8	I/O	Noise-reduction pin. See the *Programmable Soft-Start (NR/SS Pin)* and *Soft-Start, Noise Reduction (NR/SS Pin), and Power-Good (PG Pin)* sections for additional information.
OUT	9, 10, 11, 12	O	Regulated output pin. See the *Output Voltage Setting and Regulation* and *Input and Output Capacitor Requirements (C_{IN} and C_{OUT})* sections for more details.
PG	14	O	Open-drain, power-good indicator pin for the low-dropout regulator (LDO) output voltage. See the *Power-Good Pin (PG Pin)* section for additional information.
REF	7	I/O	Reference pin. See the *Output Voltage Setting and Regulation* section for additional information.
SNS	13	I	Output sense pin. See the *Output Voltage Setting and Regulation* section for additional information.
Thermal Pad	—	GND	Connect the pad to GND for best possible thermal performance. See the *Layout* section for more information.

(1) I = input, O = output, I/O = input or output, G = ground.

6 Specifications

6.1 Absolute Maximum Ratings

over operating junction temperature range and all voltages with respect to GND (unless otherwise noted)[1]

		MIN	MAX	UNIT
Voltage	BIAS	–0.3	11.2	V
	IN, PG, EN, CP_EN	–0.3	6.5	
	REF, NR/SS, SNS	–0.3	6	
	OUT	–0.3	V_{IN} + 0.3 [2]	
Current	OUT	Internally limited		A
	PG (sink current into the device)		5	mA
Temperature	Operating junction, T_J	–40	150	°C
	Storage, T_{stg}	–55	150	

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The absolute maximum rating is V_{IN} + 0.3 V or 6.0 V, whichever is smaller.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101[2]	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safemanufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safemanufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V_{IN}	Input supply voltage range	0.7		6	V
V_{REF}	Reference voltage range	0.5		5.3	V
V_{OUT}	Output voltage range	0.5		5.2	V
V_{BIAS}	Bias voltage range	3		11	V
I_{OUT}	Output current	0		5	A
C_{IN}	Input capacitor	4.7	10	1000	µF
C_{OUT}	Output capacitor (1)	22	22	3000	µF
C_{OUT_ESL}	Output capacitor ESR	2		20	mΩ
Z_{OUT_ESL}	Total impedance ESL	0.2		1	nH
C_{BIAS}	Bias pin capacitor	0	1	100	µF
$C_{NR/SS}$	Noise-reduction capacitor	0.1	4.7	10	µF
R_{PG}	Power-good pull-up resistance	10		100	kΩ
T_J	Junction temperature	–40		125	°C

(1) Effective output capacitance of 15 µF minimum required for stability

6.4 Thermal Information

THERMAL METRIC (1)		TPS7A57 RTE (WQFN) (2) 16 PINS	TPS7A57 RTE (WQFN) (3) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	40.3	21.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	39.3	–	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	14	–	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.5	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	14.0	11.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.8	–	°C/W

(1) For more information about traditional and new thermal metrics, see the Using New Thermal Metric application report.
(2) Evaluated using JEDEC standard (2s2p).
(3) Evaluated using EVM.

6.5 Electrical Characteristics

over operating temperature range (T_J = –40 °C to +125 °C), $V_{IN(NOM)} = V_{OUT(NOM)} + 0.4$ V, V_{CP_EN} = 1.8 V, V_{BIAS} = 0 V, I_{OUT} = 0 A, V_{EN} = 1.8 V, C_{IN} = 10 µF, C_{OUT} = 22 µF, C_{BIAS} = 0 nF, $C_{NR/SS}$ = 100 nF, SNS pin shorted to OUT pin, and PG pin pulled up to V_{IN} with 100 kΩ (unless otherwise noted); typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{UVLO(IN)}$	Input supply UVLO with BIAS	V_{IN} rising, V_{CP_EN} = 1.8 V (3 V ≤ V_{BIAS} ≤ 11 V) and V_{CP_EN} = 0 V (V_{OUT} + 3.2 V ≤ V_{BIAS} ≤ 11 V)		0.67	0.7	V
$V_{HYS(UVLO\_IN)}$	Input supply UVLO hysteresis with BIAS	V_{CP_EN} = 1.8 V (3 V ≤ V_{BIAS} ≤ 11 V) and V_{CP_EN} = 0 V (V_{OUT} + 3.2 V ≤ V_{BIAS} ≤ 11 V)		50		mV
$V_{UVLO(IN)}$	Input supply UVLO without BIAS	V_{IN} rising, V_{CP_EN} = 1.8 V		1.07	1.1	V
$V_{HYS(UVLO\_IN)}$	Input supply UVLO hysteresis without BIAS	V_{CP_EN} = 1.8 V		50		mV
$V_{UVLO(BIAS)} - V_{REF}$	BIAS UVLO relative to V_{REF} without CP	V_{BIAS} rising, V_{CP_EN} = 0 V, 1.4 V ≤ V_{REF} ≤ 5.2 V		2.1	2.95	V
$V_{HYS(UVLO\_BIAS - REF)}$	BIAS UVLO relative to V_{REF} hysteresis without CP	V_{CP_EN} = 0 V, 1.4 V ≤ V_{REF} ≤ 5.2 V		240		mV
$V_{UVLO(BIAS)}$	BIAS UVLO with CP	V_{BIAS} rising, V_{CP_EN} = 1.8 V, 0.7 V ≤ V_{IN} < 1.1 V		2.8	2.95	V
$V_{HYS(UVLO\_BIAS)}$	BIAS UVLO hysteresis with CP	V_{CP_EN} = 1.8 V, 0.7 V ≤ V_{IN} < 1.1 V		115		mV
$I_{NR/SS}$	NR/SS fast start-up charging current	$V_{NR/SS}$ = GND, V_{IN} = 1.1 V		0.2		mA
V_{OUT}	Output voltage accuracy [1]	0.5 V ≤ V_{OUT} ≤ 5.2 V, 0 A ≤ I_{OUT} ≤ 5 A, V_{CP_EN} = 0 V, V_{OUT} + 3.2 V ≤ V_{BIAS} ≤ 11 V; 0.7 V ≤ V_{IN} ≤ 6 V [2], V_{CP_EN} = 1.8 V, 3 V ≤ V_{BIAS} ≤ 11 V, 0.7 V ≤ V_{IN} ≤ 6 V [2], V_{CP_EN} = 1.8 V, no BIAS, 1.1 V ≤ V_{IN} ≤ 6 V	–1		1	%
I_{REF}	REF current pin	V_{IN} = 1.1 V, V_{CP_EN} = 1.8 V, V_{OUT} = 0.5 V, I_{LOAD} = 0 A, V_{BIAS} = 0 V		50		µA
		V_{CP_EN} = 0 V (CP disabled), 0.7 V ≤ V_{IN} ≤ 6 V [1] [2], 0.5 V ≤ V_{OUT} ≤ 5.2 V, V_{OUT} + 3.2 V ≤ V_{BIAS} ≤ 11 V, 0 A ≤ I_{OUT} ≤ 5 A	–1		1	%
		V_{CP_EN} = 1.8 V (CP enabled, V_{BIAS} = 0 V), 1.1 V ≤ V_{IN} ≤ 6 V [1], 0.5 V ≤ V_{OUT} ≤ 5.2 V, 0 A ≤ I_{OUT} ≤ 5 A [2]	–1		1	%
		V_{CP_EN} = 1.8 V (CP enabled), 0.7 V ≤ V_{IN} ≤ 6 V [1], 0.5 V ≤ V_{OUT} ≤ 5.2 V, 3 V ≤ V_{BIAS} ≤ 11 V, 0 A ≤ I_{OUT} ≤ 5 A	–1		1	%
V_{OS}	Output offset voltage ($V_{NR/SS} - V_{OUT}$)	V_{IN} = 0.7 V, V_{OUT} = 0.5 V, I_{OUT} = 0 A, V_{CP_EN} = 1.8 V, 3 V ≤ V_{BIAS} ≤ 11 V, V_{CP_EN} = 0 V, V_{OUT} + 3.2 V ≤ V_{BIAS} ≤ 11 V	–1		1	mV
		0.7 V ≤ V_{IN} ≤ 6 V [1] [2], 0.5 V ≤ V_{OUT} ≤ 5.2 V, V_{CP_EN} = 1.8 V, 3 V ≤ V_{BIAS} ≤ 11 V, 0 A ≤ I_{OUT} ≤ 5 A	–2		2	mV
		1.1 V ≤ V_{IN} ≤ 6.0 V [1] [2], 0.5 V ≤ V_{OUT} ≤ 5.2 V, V_{CP_EN} = 1.8 V, V_{BIAS} = 0 V, 0 A ≤ I_{OUT} ≤ 5 A	–2		2	mV
		0.7 V ≤ V_{IN} ≤ 6 V [1] [2], 0.5 V ≤ V_{OUT} ≤ 5.2 V, V_{CP_EN} = 0 V, V_{OUT} + 3.2 V ≤ V_{BIAS} ≤ 11 V, 0 A ≤ I_{OUT} ≤ 5 A	–2		2	mV
$\Delta I_{REF(\Delta VBIAS)}$	Line regulation: ΔI_{REF}	V_{OUT} + 3.2 V ≤ V_{BIAS} ≤ 11 V, V_{IN} = 0.7V, V_{OUT} = 0.5 V, V_{CP_EN} = 0 V, I_{OUT} = 0 A		0.15		nA/V
$\Delta V_{OS(\Delta VBIAS)}$	Line regulation: ΔV_{OS}	V_{OUT} + 3.2 V ≤ V_{BIAS} ≤ 11 V, V_{IN} = 0.7 V, V_{OUT} = 0.5 V, V_{CP_EN} = 0 V, I_{OUT} = 0 A		0.06		µV/V
$\Delta I_{REF(\Delta VIN)}$	Line regulation: ΔI_{REF}	1.1 V ≤ V_{IN} ≤ 6 V, V_{OUT} = 0.5 V, V_{CP_EN} = 1.8 V, I_{OUT} = 0 A, V_{BIAS} = 0 V		0.03		nA/V
$\Delta V_{OS(\Delta VIN)}$	Line regulation: ΔV_{OS}	1.1 V ≤ V_{IN} ≤ 6 V, V_{OUT} = 0.5 V, V_{CP_EN} = 1.8 V, I_{OUT} = 0 A, V_{BIAS} = 0 V		0.01		µV/V

6.5 Electrical Characteristics (continued)

over operating temperature range (T_J = –40 °C to +125 °C), $V_{IN(NOM)} = V_{OUT(NOM)} + 0.4$ V, V_{CP_EN} = 1.8 V, V_{BIAS} = 0 V, I_{OUT} = 0 A, V_{EN} = 1.8 V, C_{IN} = 10 µF, C_{OUT} = 22 µF, C_{BIAS} = 0 nF, $C_{NR/SS}$ = 100 nF, SNS pin shorted to OUT pin, and PG pin pulled up to V_{IN} with 100 kΩ (unless otherwise noted); typical values are at T_J = 25°C

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\Delta V_{OS(\Delta IOUT)}$	Load regulation: ΔV_{OS}	V_{IN} = 0.7 V, V_{OUT} = 0.5 V, V_{CP_EN} = 0 V, 0 A ≤ I_{OUT} ≤ 5 A, V_{OUT} + 3.2 V ≤ V_{BIAS} ≤ 11 V		5		µV/A
		V_{OUT} = 5.2 V, V_{CP_EN} = 1.8 V, 0 A ≤ I_{OUT} ≤ 5 A, V_{BIAS} = 0 V		175		
	Change in I_{REF} vs V_{REF}	0.5 V ≤ V_{REF} ≤ 5.2 V, V_{IN} = 6 V, I_{OUT} = 0 A, V_{CP_EN} = 1.8 V, V_{BIAS} = 0 V		4.4		nA
	Change in V_{OS} vs V_{REF}			0.25		mV
V_{DO}	Dropout voltage [(3)]	1.1 V ≤ V_{IN} ≤ 5.3 V, I_{OUT} = 5 A, V_{CP_EN} = 1.8 V, –40°C ≤ T_J ≤ +125°C		75	110	mV
		1.1 V ≤ V_{IN} ≤ 5.3 V, I_{OUT} = 5 A, V_{CP_EN} = 1.8 V, –40°C ≤ T_J ≤ +85°C			100	
		0.7 V ≤ V_{IN} ≤ 1.1 V, I_{OUT} = 5 A, V_{CP_EN} = 1.8 V, V_{BIAS} = 3 V, –40°C ≤ T_J ≤ +125°C		75	110	
		0.7 V ≤ V_{IN} ≤ 1.1 V, I_{OUT} = 5 A, V_{CP_EN} = 1.8 V, V_{BIAS} = 3 V, –40 °C ≤ T_J ≤ +85 °C			100	
		0.7 V ≤ V_{IN} ≤ 5.3 V, I_{OUT} = 5 A, V_{CP_EN} = 0 V, V_{BIAS} = V_{IN} + 3.2 V, –40°C ≤ T_J ≤ +125°C		75	110	
		0.7 V ≤ V_{IN} ≤ 5.3 V, I_{OUT} = 5 A, V_{CP_EN} = 0 V, V_{BIAS} = V_{IN} + 3.2 V, –40°C ≤ T_J ≤ +85°C			100	
I_{LIM}	Output current limit	V_{OUT} forced at 0.9 × $V_{OUT(NOM)}$, $V_{OUT(NOM)}$ = 5.2 V, V_{IN} = $V_{OUT(NOM)}$ + 400 mV, V_{CP_EN} = 0 V, V_{BIAS} = V_{OUT} + 3.2 V	5.2	6.0	6.7	A
I_{SC}	Short circuit current limit	R_{LOAD} = 10 mΩ, under foldback operation		4		A
I_{BIAS}	BIAS pin current	V_{IN} = 6 V, I_{OUT} = 0 A, V_{CP_EN} = 0 V, V_{BIAS} = V_{OUT} + 3.2 V, V_{OUT} = 5.2 V	1	1.5	2	mA
		V_{IN} = 0.7 V, I_{OUT} = 5 A, V_{OUT} = 0.5 V, V_{CP_EN} = 1.8 V, 3.0 V ≤ V_{BIAS} ≤ 11 V	8	11	15	
I_{GND}	GND pin current	V_{IN} = 6 V, I_{OUT} = 0 A, V_{CP_EN} = 0 V, V_{BIAS} = V_{OUT} + 3.2 V, V_{OUT} = 5.2 V	3.5	5	6.5	mA
		V_{IN} = 5.6 V, I_{OUT} = 5 A, V_{OUT} = 5.2 V, V_{CP_EN} = 1.8 V, V_{BIAS} = 0 V		16.5		
		V_{IN} = 1.1 V, I_{OUT} = 5 A, V_{OUT} = 0.5 V, V_{CP_EN} = 1.8 V, V_{BIAS} = 0 V	12	17.5	24	
		V_{IN} = 0.7 V, I_{OUT} = 5 A, V_{OUT} = 0.5 V, V_{CP_EN} = 1.8 V, 3 V ≤ V_{BIAS} ≤ 11 V	11	16.5	23	
		V_{IN} = 0.7 V, I_{OUT} = 5 A, V_{OUT} = 0.5 V, V_{CP_EN} = 0 V, V_{OUT} + 3.2 V ≤ V_{BIAS} ≤ 11 V	5	7	9	
I_{SDN}	Shutdown GND pin current	PG = (open), V_{IN} = 6 V, V_{EN} = 0.4 V, V_{CP_EN} = 1.8 V, V_{BIAS} = 0 V		100	300	µA
		PG = (open), V_{IN} = 6 V, V_{EN} = 0.4 V, V_{CP_EN} = 0.4 V, V_{BIAS} = 11 V		150	450	
I_{EN}	EN pin current	V_{IN} = 6 V, 0 V ≤ V_{EN} ≤ 6 V, V_{CP_EN} = 1.8 V, V_{BIAS} = 0 V	-5		5	µA
$V_{IH(EN)}$	EN trip point rising (turn-on)	V_{IN} = 1.1 V (V_{CP_EN} = 1.8 V) or V_{BIAS} ≥ 3 V (V_{CP_EN} = 0 V)	0.62	0.65	0.68	V
$V_{HYS(EN)}$	EN trip point hysteresis	V_{IN} = 1.1 V (V_{CP_EN} = 1.8 V) or V_{BIAS} ≥ 3 V (V_{CP_EN} = 0 V)		40		mV
I_{CP_EN}	CP_EN pin current	V_{IN} = 6.0 V, 0 V ≤ V_{CP_EN} ≤ 6 V	–5		5	µA
$V_{IH(CP\_EN)}$	CP_EN trip point rising (turn-on)	1.1 V ≤ V_{IN} ≤ 6 V, V_{EN} = 1.8 V, V_{BIAS} = 0 V, 0.7 V ≤ V_{IN} ≤ 1.1 V, V_{EN} = 1.8 V, V_{BIAS} = 3 V	0.57	0.6	0.63	V
$V_{HYS(CP\_EN)}$	CP_EN trip point hysteresis	1.1 V ≤ V_{IN} ≤ 6 V, V_{EN} = 1.8 V, V_{BIAS} = 0 V, 0.7 V ≤ V_{IN} ≤ 1.1 V, V_{EN} = 1.8 V, V_{BIAS} = 3 V		56		mV

6.5 Electrical Characteristics (continued)

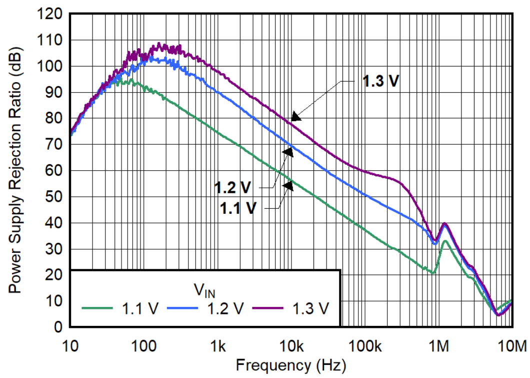
over operating temperature range (T_J = –40 °C to +125 °C), $V_{IN(NOM)}$ = $V_{OUT(NOM)}$ + 0.4 V, V_{CP_EN} = 1.8 V, V_{BIAS} = 0 V, I_{OUT} = 0 A, V_{EN} = 1.8 V, C_{IN} = 10 µF, C_{OUT} = 22 µF, C_{BIAS} = 0 nF, $C_{NR/SS}$ = 100 nF, SNS pin shorted to OUT pin, and PG pin pulled up to V_{IN} with 100 kΩ (unless otherwise noted); typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{IT(PG)}$	PG pin threshold	For PG transitioning low with falling V_{OUT}, V_{IN} = 1.1 V, V_{BIAS} = 0 V, V_{CP_EN} = 1.8 V, V_{OUT} < $V_{IT(PG)}$, I_{PG} = –1 mA (current into device)	87	90	93	%
$V_{HYS(PG)}$	PG pin hysteresis	V_{IN} = 1.1 V, V_{BIAS} = 0 V, V_{CP_EN} = 1.8 V, V_{OUT} < $V_{IT(PG)}$, I_{PG} = –1 mA (current into device)		2		%
$V_{OL(PG)}$	PG pin low-level output voltage	V_{IN} = 1.1 V, V_{BIAS} = 0 V, V_{CP_EN} = 1.8 V, V_{OUT} < $V_{IT(PG)}$, I_{PG} = –1 mA (current into device)			0.4	V
$I_{LKG(PG)}$	PG pin leakage current	V_{PG} = 6 V, V_{OUT} > $V_{IT(PG)}$, V_{IN} = 1.1 V, V_{BIAS} = 0 V, V_{CP_EN} = 1.8 V			1	µA
PSRR	Power-supply ripple rejection	f = 1 MHz, V_{IN} = 0.8 V, $V_{OUT(NOM)}$ = 0.5 V, V_{CP_EN} = 0 V, V_{BIAS} = V_{OUT} + 3.2 V, I_{OUT} = 5 A, $C_{NR/SS}$ = 4.7 µF		40		dB
		f = 1 MHz, V_{IN} = 0.9 V, $V_{OUT(NOM)}$ = 0.5 V, V_{CP_EN} = 0 V, V_{BIAS} = V_{OUT} + 3.2 V, I_{OUT} = 5 A, $C_{NR/SS}$ = 4.7 µF		40		
		f = 1 MHz, V_{IN} = 5.3 V, $V_{OUT(NOM)}$ = 5 V, V_{CP_EN} = 1.8 V, V_{BIAS} = 0 V, I_{OUT} = 5 A, $C_{NR/SS}$ = 4.7 µF		40		
		f = 1 MHz, V_{IN} = 5.4 V, $V_{OUT(NOM)}$ = 5 V, , V_{CP_EN} = 1.8 V, V_{BIAS} = 0 V, I_{OUT} = 5 A, $C_{NR/SS}$ = 4.7 µF		36		
V_n	Output noise voltage	BW = 10 Hz to 100 kHz, 0.7V ≤ V_{IN} ≤ 6 V, 0.5 V ≤ V_{OUT} ≤ 5.2 V, I_{OUT} = 5 A, $C_{NR/SS}$ = 4.7 µF, V_{CP_EN} = 0 V, V_{BIAS} = V_{OUT} + 3.2 V		2.49		$µV_{RMS}$
		BW = 10 Hz to 100 kHz, 1.1 V ≤ V_{IN} ≤ 6 V, 0.5 V ≤ V_{OUT} ≤ 5.2 V, I_{OUT} = 5 A, $C_{NR/SS}$ = 4.7 µF, V_{CP_EN} = 1.8 V, V_{BIAS} = 0 V		2.49		
	Noise spectral density	f = 100 Hz, 0.7 V ≤ V_{IN} ≤ 6 V, 0.5 V ≤ V_{OUT} ≤ 5.2 V, I_{OUT} = 5 A, $C_{NR/SS}$ = 4.7 µF, V_{CP_EN} = 0 V, V_{BIAS} = V_{OUT} + 3.2 V		20		nV/√Hz
		f = 1 kHz, 0.7 V ≤ V_{IN} ≤ 6 V, 0.5 V ≤ V_{OUT} ≤ 5.2 V, I_{OUT} = 5 A, $C_{NR/SS}$ = 4.7 µF, V_{CP_EN} = 0 V, V_{BIAS} = V_{OUT} + 3.2 V		9		
		f = 10 kHz, 0.7 V ≤ V_{IN} ≤ 6 V, 0.5 V ≤ V_{OUT} ≤ 5.2 V, I_{OUT} = 5 A, $C_{NR/SS}$ = 4.7 µF, V_{CP_EN} = 0 V, V_{BIAS} = V_{OUT} + 3.2 V		6		
R_{DIS}	Output pin active discharge resistance	V_{IN} = 1.1 V, V_{CP_EN} = 1.8 V, V_{BIAS} = 0 V, V_{EN} = 0 V		110		Ω
R_{NR/SS_DIS}	NR/SS pin active discharge resistance	V_{IN} = 1.1 V, V_{CP_EN} = 1.8 V, V_{BIAS} = 0 V, V_{EN} = 0 V		100		Ω
$T_{SD(shutdown)}$	Thermal shutdown temperature	Shutdown, temperature increasing		165		°C
$T_{SD(reset)}$	Thermal shutdown reset temperature	Reset, temperature decreasing		150		°C

(1) Max power dissipation of 2 W.
(2) Limited by pulse max power dissipation. For 0 mA ≤ I_{OUT} ≤ 2.5 A, V_{IN} = 6 V, 0 mA ≤ I_{OUT} ≤ 5 A, V_{IN} = 5.6 V.
(3) V_{REF} = V_{IN}, V_{SNS} = 97% × V_{REF}.

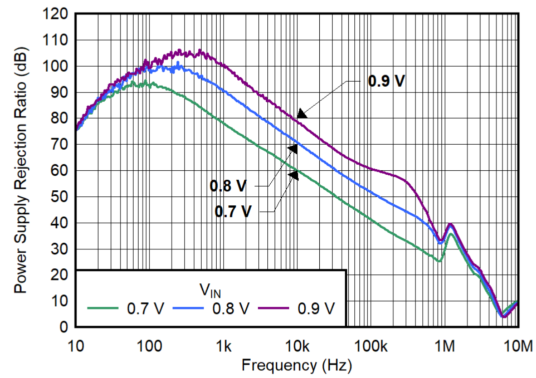
6.6 Typical Characteristics

V_{IN} = $V_{OUT(NOM)}$ + 0.4 V, V_{EN} = 1.8 V, V_{CP_EN} = 1.8 V, C_{IN} = 10 μF, $C_{NR/SS}$ = 4.7 μF, C_{OUT} = 22 μF, C_{BIAS} = 0 nF, SNS pin shorted to OUT pin, and PG pin pulled up to V_{IN} with 100 kΩ (unless otherwise noted); typical values are at T_J = 25°C



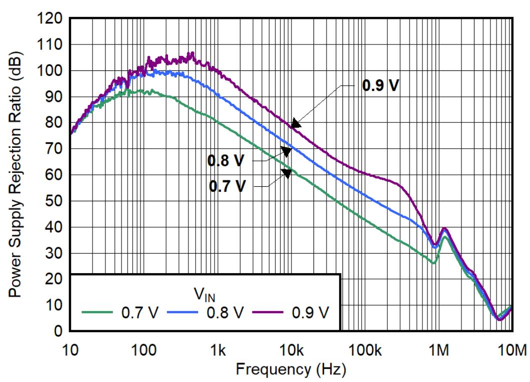
$C_{NR/SS}$ = C_{IN} = 4.7 μF, C_{OUT} = 22 μF, V_{CP_EN} = V_{IN}, V_{OUT} = 0.9 V, V_{BIAS} = 0 V, I_{OUT} = 5 A

图 6-1. PSRR vs Frequency and V_{IN} for CP Enabled, No Bias



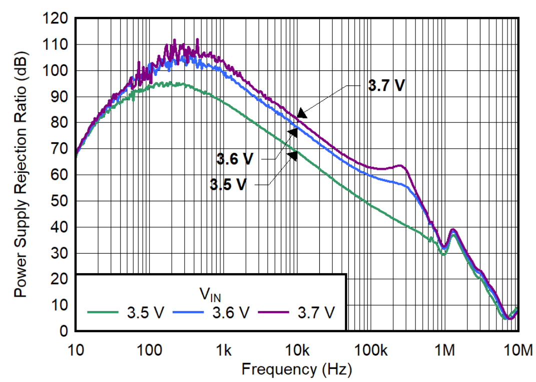
$C_{NR/SS}$ = C_{IN} = 4.7 μF, C_{OUT} = 22 μF, V_{CP_EN} = V_{IN}, V_{OUT} = 0.5 V, V_{BIAS} = 3 V, I_{OUT} = 5 A

图 6-2. PSRR vs Frequency and V_{IN} for CP Enabled, Minimum Bias



$C_{NR/SS}$ = C_{IN} = 4.7 μF, C_{OUT} = 22 μF, V_{CP_EN} = 0 V, V_{OUT} = 0.5 V, V_{BIAS} = 11 V, I_{OUT} = 5 A

图 6-3. PSRR vs Frequency and V_{IN} for CP Disabled, Maximum Bias

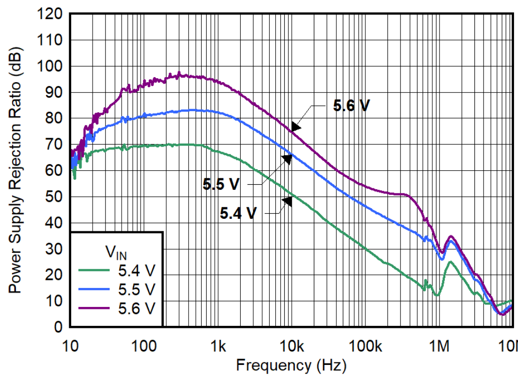


$C_{NR/SS}$ = C_{IN} = 4.7 μF, C_{OUT} = 22 μF, V_{CP_EN} = 0 V, V_{OUT} = 3.3 V, V_{BIAS} = 6.5 V, I_{OUT} = 5 A

图 6-4. PSRR vs Frequency and V_{IN} for CP Disabled, Minimum Bias

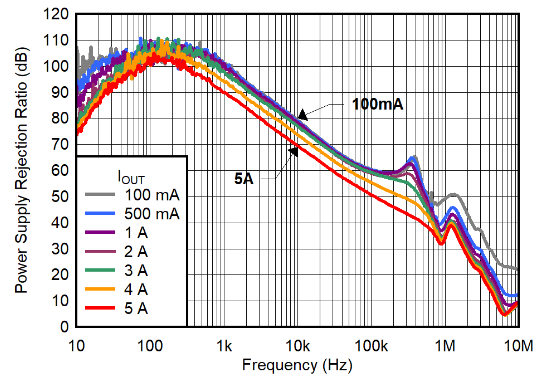
6.6 Typical Characteristics (continued)

$V_{IN} = V_{OUT(NOM)} + 0.4$ V, $V_{EN} = 1.8$ V, $V_{CP\_EN} = 1.8$ V, $C_{IN} = 10$ µF, $C_{NR/SS} = 4.7$ µF, $C_{OUT} = 22$ µF, $C_{BIAS} = 0$ nF, SNS pin shorted to OUT pin, and PG pin pulled up to V_{IN} with 100 kΩ (unless otherwise noted); typical values are at $T_J = 25°C$



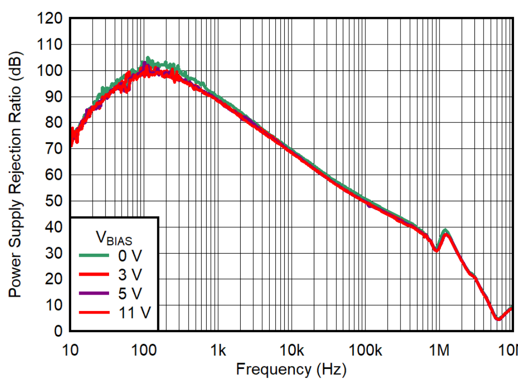
$C_{NR/SS} = C_{IN} = 4.7$ µF, $C_{OUT} = 22$ µF, $V_{CP\_EN} = 0$ V, $V_{OUT} = 5.2$ V, $V_{BIAS} = 11$ V, $I_{OUT} = 5$ A

图 6-5. PSRR vs Frequency and V_{IN} for CP Disabled, Maximum Bias



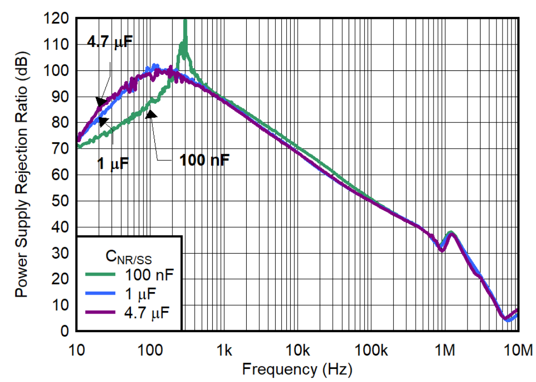
$C_{NR/SS} = C_{IN} = 4.7$ µF, $C_{OUT} = 22$ µF, $V_{CP\_EN} = 0$ V, $V_{IN} = 1.2$ V, $V_{OUT} = 0.9$ V, $V_{BIAS} = 0$ V, $I_{OUT} = 5$ A

图 6-6. PSRR vs Frequency and I_{OUT} for CP Enabled, No Bias



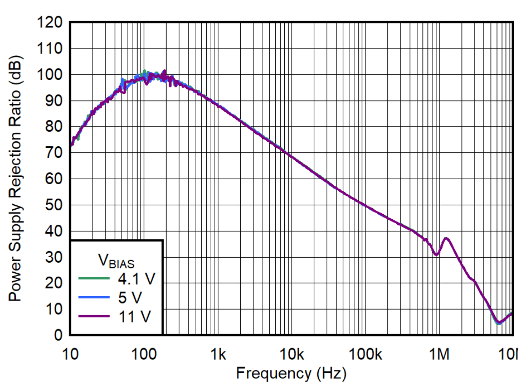
$C_{NR/SS} = C_{IN} = 4.7$ µF, $C_{OUT} = 22$ µF, $V_{CP\_EN} = 0$ V, $V_{IN} = 1.2$ V, $V_{OUT} = 0.9$ V, $I_{OUT} = 5$ A

图 6-7. PSRR vs Frequency and V_{BIAS} for CP Enabled



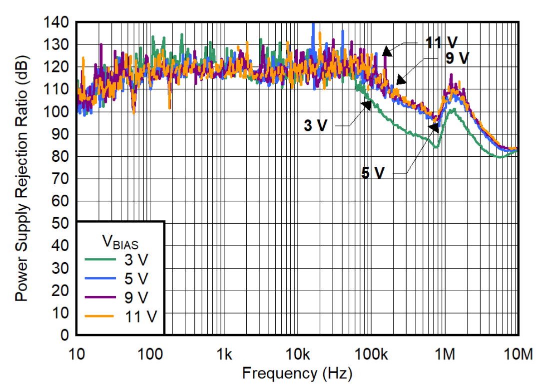
$C_{IN} = 4.7$ µF, $C_{OUT} = 22$ µF, $V_{CP\_EN} = 0$ V, $V_{IN} = 1.2$ V, $V_{OUT} = 0.9$ V, $V_{BIAS} = 11$ V, $I_{OUT} = 5$ A

图 6-8. PSRR vs Frequency and $C_{NR/SS}$ for CP Disabled



$C_{NR/SS} = C_{IN} = 4.7$ µF, $C_{OUT} = 22$ µF, $V_{CP\_EN} = 0$ V, $V_{IN} = 1.2$ V, $V_{OUT} = 0.9$ V, $I_{OUT} = 5$ A

图 6-9. PSRR vs Frequency and V_{BIAS} for CP Disabled

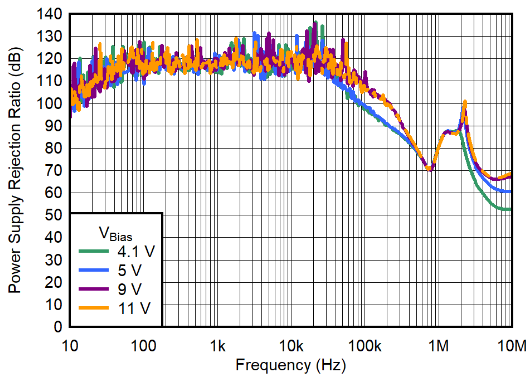


$C_{NR/SS} = C_{IN} = 4.7$ µF, $C_{OUT} = 22$ µF, $V_{CP\_EN} = 1.8$ V, $V_{IN} = 0.8$ V, $V_{OUT} = 0.5$ V, $I_{OUT} = 5$ A

图 6-10. BIAS PSRR vs Frequency and V_{BIAS} for CP Enabled, V_{IN} = 0.8 V

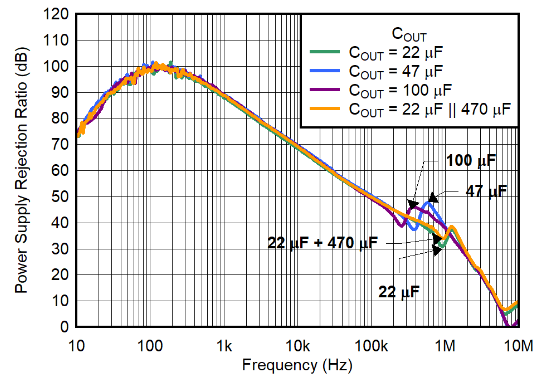
6.6 Typical Characteristics (continued)

V_{IN} = $V_{OUT(NOM)}$ + 0.4 V, V_{EN} = 1.8 V, V_{CP_EN} = 1.8 V, C_{IN} = 10 μF, $C_{NR/SS}$ = 4.7 μF, C_{OUT} = 22 μF, C_{BIAS} = 0 nF, SNS pin shorted to OUT pin, and PG pin pulled up to V_{IN} with 100 kΩ (unless otherwise noted); typical values are at T_J = 25°C



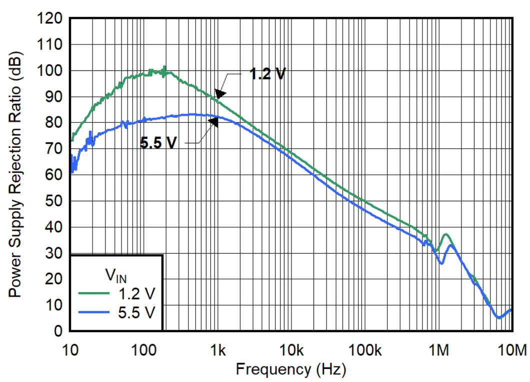
$C_{NR/SS}$ = C_{IN} = 4.7 μF, C_{OUT} = 22 μF, V_{CP_EN} = 0 V, V_{IN} = 1.2 V, V_{OUT} = 0.9 V, I_{OUT} = 5 A

图 6-11. BIAS PSRR vs Frequency and V_{BIAS} for CP Disabled, V_{IN} = 1.2 V



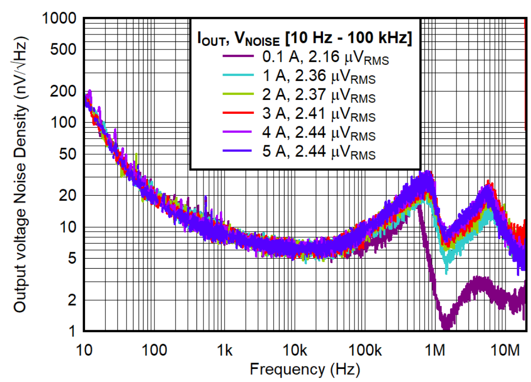
$C_{NR/SS}$ = C_{IN} = 4.7 μF, V_{CP_EN} = 0 V, V_{IN} = 1.2 V, V_{OUT} = 0.9 V, V_{BIAS} = 11 V, I_{OUT} = 5 A

图 6-12. PSRR vs Frequency and C_{OUT}



$C_{NR/SS}$ = C_{IN} = 4.7 μF, C_{OUT} = 22 μF, V_{CP_EN} = 0 V, V_{OUT} = V_{IN} – 300 mV, V_{BIAS} = 11 V, I_{OUT} = 5 A

图 6-13. PSRR vs Frequency and V_{IN}

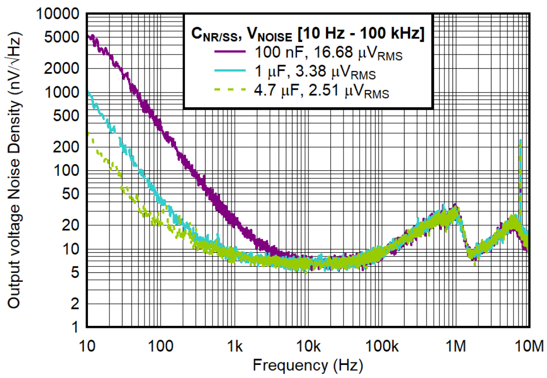


$C_{NR/SS}$ = C_{IN} = 4.7 μF, C_{OUT} = 22 μF, V_{CP_EN} = V_{IN}, V_{IN} = 0.8 V, V_{OUT} = 0.5 V, V_{BIAS} = 3.7 V

图 6-14. Output Voltage Noise Density vs Frequency and I_{OUT} for CP Enabled

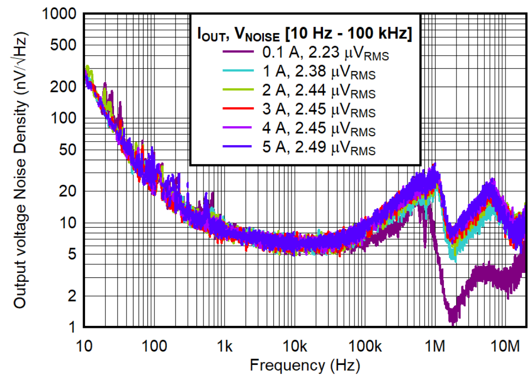
6.6 Typical Characteristics (continued)

$V_{IN} = V_{OUT(NOM)} + 0.4$ V, $V_{EN} = 1.8$ V, $V_{CP\_EN} = 1.8$ V, $C_{IN} = 10$ µF, $C_{NR/SS} = 4.7$ µF, $C_{OUT} = 22$ µF, $C_{BIAS} = 0$ nF, SNS pin shorted to OUT pin, and PG pin pulled up to V_{IN} with 100 kΩ (unless otherwise noted); typical values are at $T_J = 25°C$



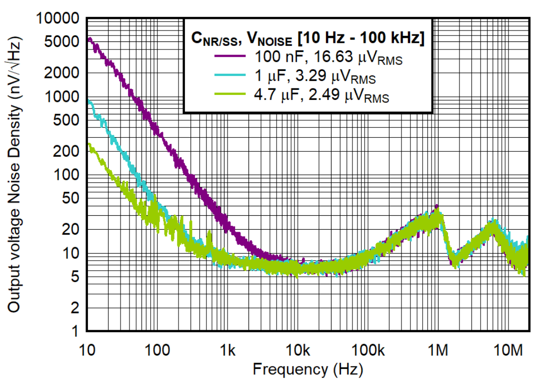
$C_{IN} = 4.7$ µF, $C_{OUT} = 22$ µF, $V_{CP\_EN} = V_{IN}$, $V_{IN} = 5.3$ V, $V_{OUT} = 5$ V, $I_{OUT} = 5$ A

图 6-15. Output Voltage Noise Density vs Frequency and $C_{NR/SS}$ for CP Enabled



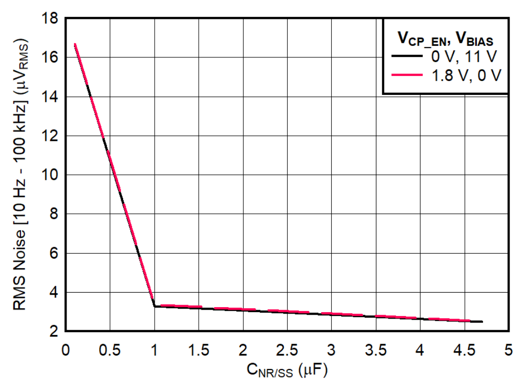
$C_{NR/SS} = C_{IN} = 4.7$ µF, $C_{OUT} = 22$ µF, $V_{IN} = 5.3$ V, $V_{OUT} = 5$ V, $V_{BIAS} = 11$ V, $I_{OUT} = 5$ A

图 6-16. Output Voltage Noise Density vs Frequency and I_{OUT} for CP Disabled



$C_{IN} = 4.7$ µF, $C_{OUT} = 22$ µF, $V_{IN} = 5.3$ V, $V_{OUT} = 5$ V, $V_{BIAS} = 11$ V

图 6-17. Output Voltage Noise Density vs Frequency and $C_{NR/SS}$ for CP Disabled

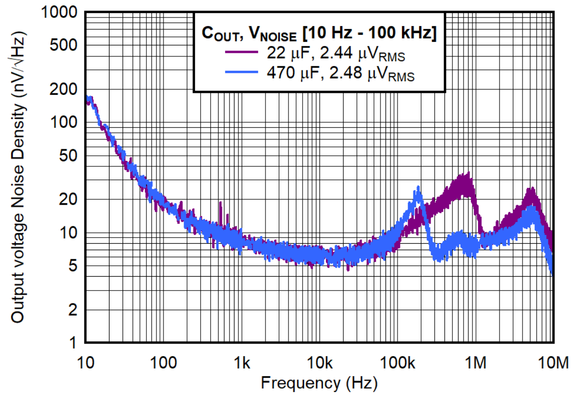


$C_{NR/SS} = C_{IN} = 4.7$ µF, $V_{IN} = 5.3$ V, $V_{OUT} = 5$ V

图 6-18. RMS Noise vs $C_{NR/SS}$

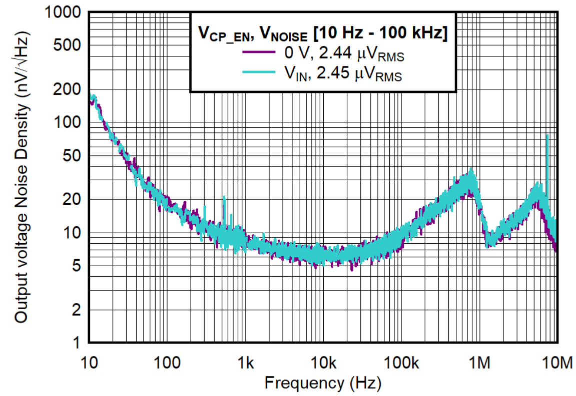
6.6 Typical Characteristics (continued)

$V_{IN} = V_{OUT(NOM)} + 0.4$ V, $V_{EN} = 1.8$ V, $V_{CP\_EN} = 1.8$ V, $C_{IN} = 10$ µF, $C_{NR/SS} = 4.7$ µF, $C_{OUT} = 22$ µF, $C_{BIAS} = 0$ nF, SNS pin shorted to OUT pin, and PG pin pulled up to V_{IN} with 100 kΩ (unless otherwise noted); typical values are at $T_J = 25°C$



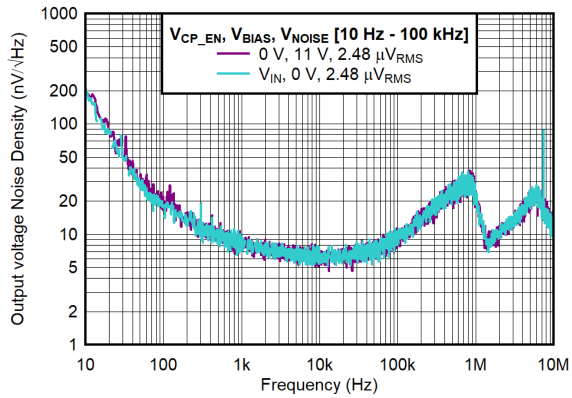
$C_{NR/SS} = C_{IN} = 4.7$ µF, CP_EN = GND, $V_{IN} = 0.8$ V, $V_{OUT} = 0.5$ V, $V_{BIAS} = 3.7$ V

图 6-19. Output Voltage Noise Density vs Frequency and C_{OUT}



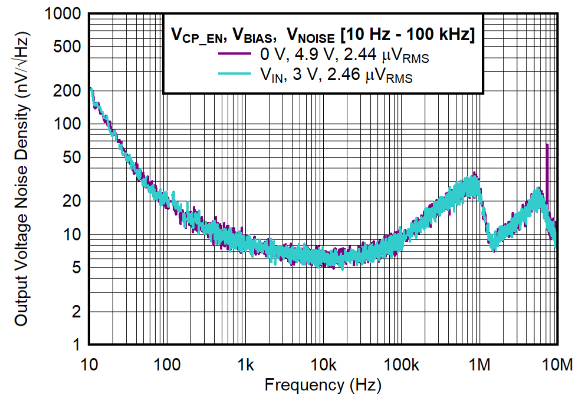
$C_{NR/SS} = C_{IN} = 4.7$ µF, $C_{OUT} = 22$ µF, $V_{IN} = 0.8$ V, $V_{BIAS} = 3.7$ V, $I_{OUT} = 5$ A

图 6-20. Output Voltage Noise Density vs Frequency and V_{CP_EN} for $V_{OUT} = 0.5$ V



$C_{NR/SS} = C_{IN} = 4.7$ µF, $C_{OUT} = 22$ µF, $V_{IN} = 1.2$ V, $I_{OUT} = 5$ A

图 6-21. Output Voltage Noise Density vs Frequency and V_{CP_EN} for $V_{OUT} = 0.9$ V

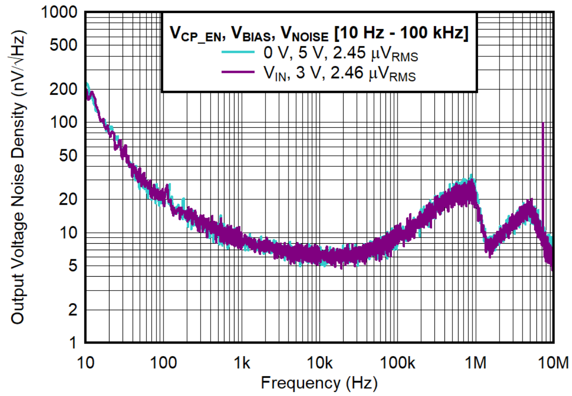


$C_{NR/SS} = C_{IN} = 4.7$ µF, $C_{OUT} = 22$ µF, $V_{IN} = 1.5$ V, $I_{OUT} = 5$ A

图 6-22. Output Voltage Noise Density vs Frequency and V_{CP_EN} for $V_{OUT} = 1.2$ V

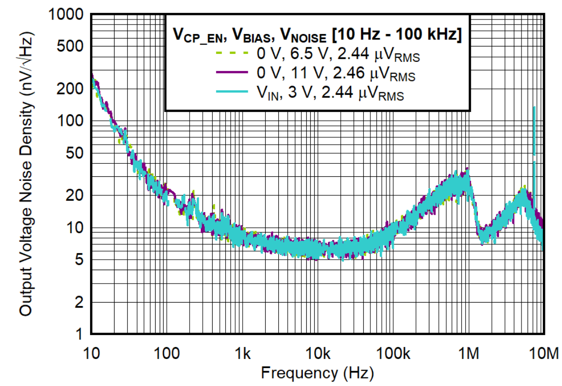
6.6 Typical Characteristics (continued)

V_{IN} = $V_{OUT(NOM)}$ + 0.4 V, V_{EN} = 1.8 V, V_{CP_EN} = 1.8 V, C_{IN} = 10 µF, $C_{NR/SS}$ = 4.7 µF, C_{OUT} = 22 µF, C_{BIAS} = 0 nF, SNS pin shorted to OUT pin, and PG pin pulled up to V_{IN} with 100 kΩ (unless otherwise noted); typical values are at T_J = 25°C



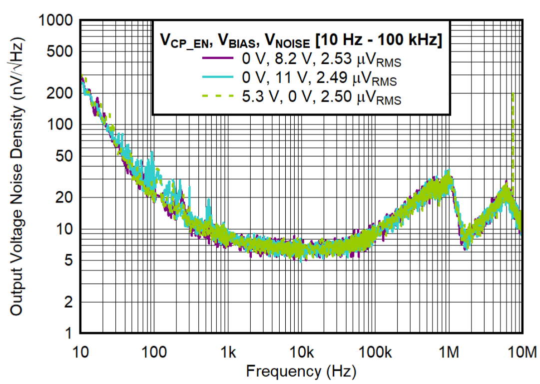
$C_{NR/SS}$ = C_{IN} = 4.7 µF, C_{OUT} = 22 µF, V_{IN} = 2.1 V, I_{OUT} = 5 A

图 6-23. Output Voltage Noise Density vs Frequency and V_{CP_EN} for V_{OUT} = 1.8 V



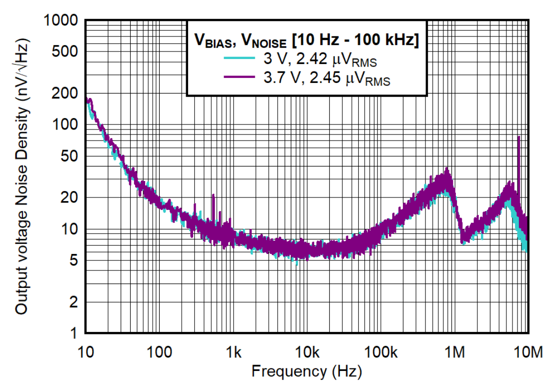
$C_{NR/SS}$ = C_{IN} = 4.7 µF, C_{OUT} = 22 µF, V_{IN} = 3.6 V, I_{OUT} = 5 A

图 6-24. Output Voltage Noise Density vs Frequency and V_{CP_EN} for V_{OUT} = 3.3 V



$C_{NR/SS}$ = C_{IN} = 4.7 µF, C_{OUT} = 22 µF, V_{IN} = 5.3 V, I_{OUT} = 5 A

图 6-25. Output Voltage Noise Density vs Frequency and V_{CP_EN} for V_{OUT} = 5 V

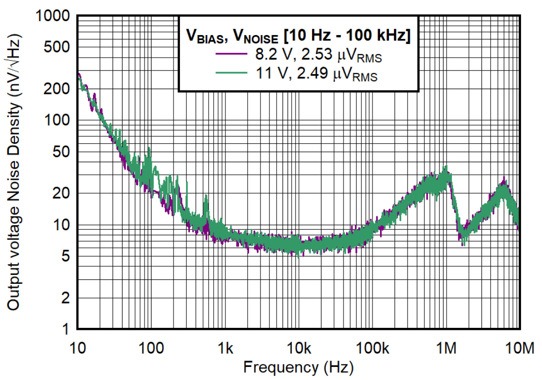


$C_{NR/SS}$ = C_{IN} = 4.7 µF, V_{CP_EN} = V_{IN}, C_{OUT} = 22 µF, V_{IN} = 0.8 V, I_{OUT} = 5 A

图 6-26. Output Voltage Noise Density vs Frequency and V_{BIAS} for V_{OUT} = 0.5 V, CP Enabled

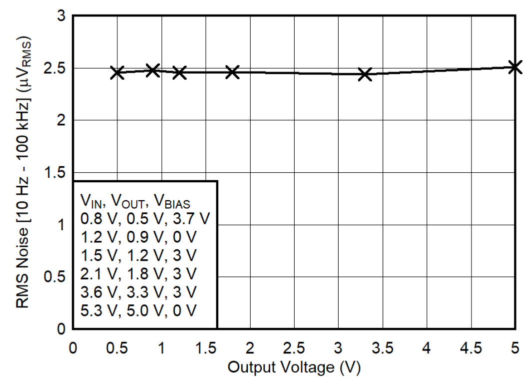
6.6 Typical Characteristics (continued)

$V_{IN} = V_{OUT(NOM)} + 0.4$ V, $V_{EN} = 1.8$ V, $V_{CP\_EN} = 1.8$ V, $C_{IN} = 10$ µF, $C_{NR/SS} = 4.7$ µF, $C_{OUT} = 22$ µF, $C_{BIAS} = 0$ nF, SNS pin shorted to OUT pin, and PG pin pulled up to V_{IN} with 100 kΩ (unless otherwise noted); typical values are at $T_J = 25°C$



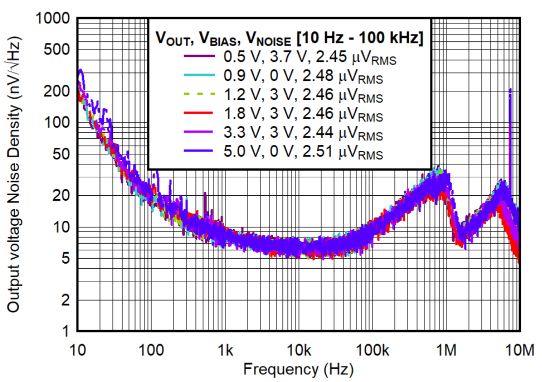
$C_{NR/SS} = C_{IN} = 4.7$ µF, $V_{CP\_EN} = 0$ V, $C_{OUT} = 22$ µF, $V_{IN} = 5.3$ V, $I_{OUT} = 5$ A

图 6-27. Output Voltage Noise Density vs Frequency and V_{BIAS} for V_{OUT} = 5 V, CP Disabled



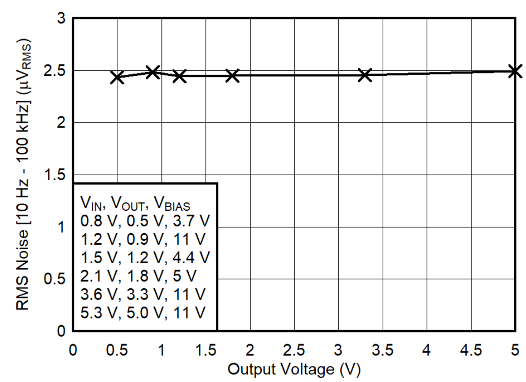
$C_{NR/SS} = C_{IN} = 4.7$ µF, $V_{CP\_EN} = 1.8$ V, $C_{OUT} = 22$ µF, $I_{OUT} = 5$ A

图 6-28. RMS Noise vs V_{OUT} for CP Enabled



$C_{NR/SS} = C_{IN} = 4.7$ µF, $V_{CP\_EN} = 1.8$ V, $C_{OUT} = 22$ µF, $V_{IN} = V_{OUT} + 0.3$ V, $I_{OUT} = 5$ A

图 6-29. Output Voltage Noise Density vs Frequency and V_{OUT} for CP Enabled

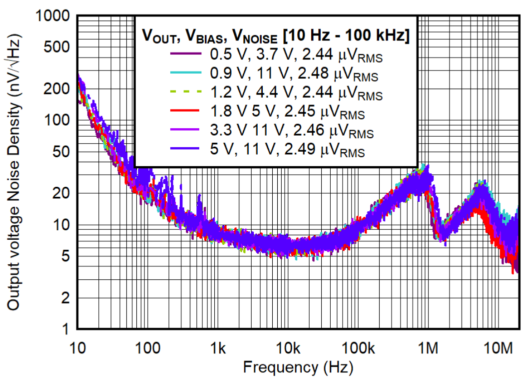


$C_{NR/SS} = C_{IN} = 4.7$ µF, $V_{CP\_EN} = 0$ V, $C_{OUT} = 22$ µF, $I_{OUT} = 5$ A

图 6-30. RMS Noise vs V_{OUT} for CP Disabled

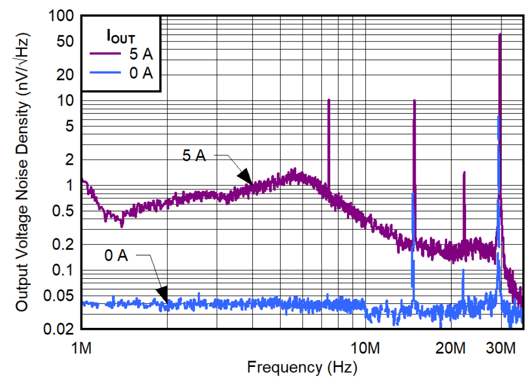
6.6 Typical Characteristics (continued)

$V_{IN} = V_{OUT(NOM)} + 0.4$ V, $V_{EN} = 1.8$ V, $V_{CP\_EN} = 1.8$ V, $C_{IN} = 10$ µF, $C_{NR/SS} = 4.7$ µF, $C_{OUT} = 22$ µF, $C_{BIAS} = 0$ nF, SNS pin shorted to OUT pin, and PG pin pulled up to V_{IN} with 100 kΩ (unless otherwise noted); typical values are at $T_J = 25°C$



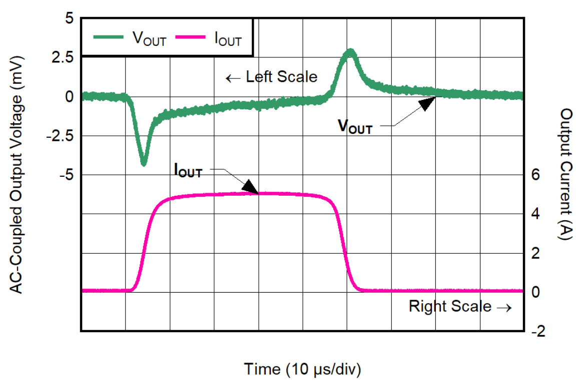
$C_{NR/SS} = C_{IN} = 4.7$ µF, $V_{CP\_EN} = 0$ V, $C_{OUT} = 22$ µF, $V_{IN} = V_{OUT} + 0.3$ V, $I_{OUT} = 5$ A

图 6-31. Output Voltage Noise Density vs Frequency and V_{OUT} for CP Disabled



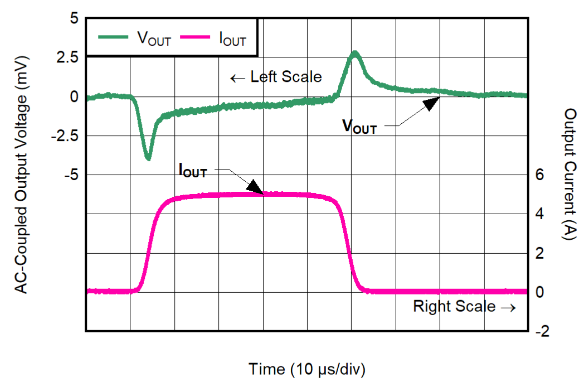
$C_{NR/SS} = C_{IN} = 4.7$ µF, $C_{OUT} = 22$ µF, $V_{IN} = V_{OUT} + 0.3$ V, $V_{CP\_EN} = V_{IN}$, $V_{BIAS} = 0$ V, $V_{OUT} = 5$ V

图 6-32. Charge Pump Output Voltage Noise Density vs Frequency and I_{OUT}



$C_{NR/SS} = C_{IN} = 4.7$ µF, $C_{OUT} = 22$ µF, $V_{CP\_EN} = 1.8$ V, $V_{BIAS} = 3$ V, $V_{IN} = 0.8$ V, SR = 1 A/µs

图 6-33. Load Transient for $V_{OUT} = 0.5$ V, $I_{OUT} = 100$ mA to 5 A, CP Enabled

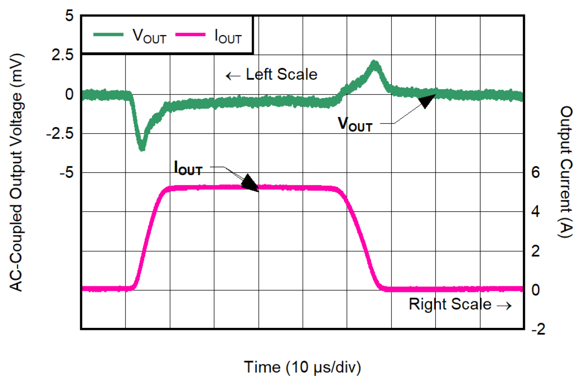


$C_{NR/SS} = C_{IN} = 4.7$ µF, $C_{OUT} = 22$ µF, $V_{CP\_EN} = 1.8$ V, $V_{BIAS} = 0$ V, $V_{IN} = 1.1$ V, SR = 1 A/µs

图 6-34. Load Transient for $V_{OUT} = 0.5$ V, $I_{OUT} = 100$ mA to 5 A, CP Enabled

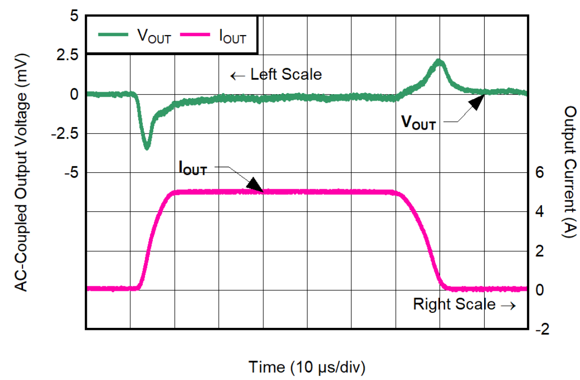
6.6 Typical Characteristics (continued)

V_{IN} = $V_{OUT(NOM)}$ + 0.4 V, V_{EN} = 1.8 V, V_{CP_EN} = 1.8 V, C_{IN} = 10 µF, $C_{NR/SS}$ = 4.7 µF, C_{OUT} = 22 µF, C_{BIAS} = 0 nF, SNS pin shorted to OUT pin, and PG pin pulled up to V_{IN} with 100 kΩ (unless otherwise noted); typical values are at T_J = 25°C



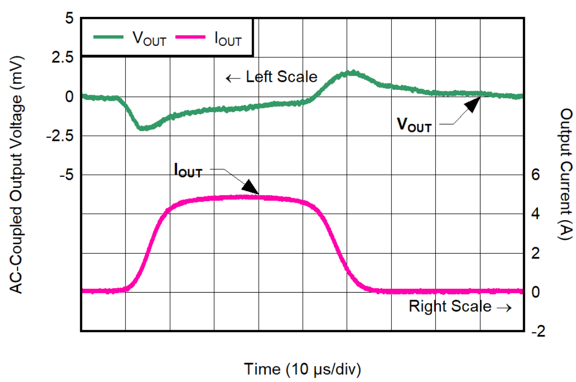
$C_{NR/SS}$ = C_{IN} = 4.7 µF, C_{OUT} = 22 µF, V_{CP_EN} = 1.8 V, V_{BIAS} = 0 V, V_{IN} = 3.6 V, SR = 1 A/µs

图 6-35. Load Transient for V_{OUT} = 3.3 V, I_{OUT} = 100 mA to 5 A, CP Enabled



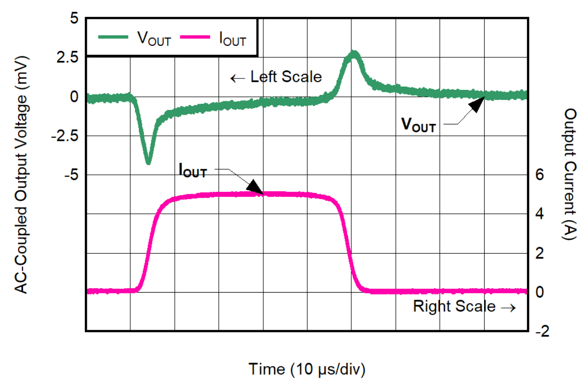
$C_{NR/SS}$ = C_{IN} = 4.7 µF, C_{OUT} = 22 µF, V_{CP_EN} = 1.8 V, V_{BIAS} = 0 V, V_{IN} = 5.5 V, SR = 1 A/µs

图 6-36. Load Transient for V_{OUT} = 5.2 V, I_{OUT} = 100 mA to 5 A, CP Enabled



$C_{NR/SS}$ = C_{IN} = 4.7 µF, C_{OUT} = 22 µF, V_{CP_EN} = 0 V, V_{BIAS} = 3.7 V, V_{IN} = 0.8 V

图 6-37. Load Transient for V_{OUT} = 0.5 V, I_{OUT} = 100 mA to 5 A, CP Disabled, SR = 0.5 A/µs

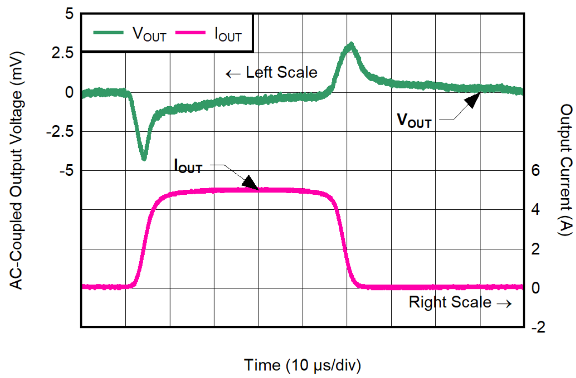


$C_{NR/SS}$ = C_{IN} = 4.7 µF, C_{OUT} = 22 µF, V_{CP_EN} = 0 V, V_{BIAS} = 3.7 V, V_{IN} = 0.8 V

图 6-38. Load Transient for V_{OUT} = 0.5 V, I_{OUT} = 100 mA to 5 A, CP Disabled, SR = 1 A/µs

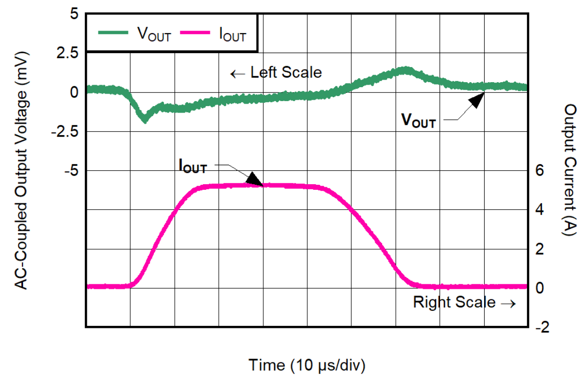
6.6 Typical Characteristics (continued)

V_{IN} = $V_{OUT(NOM)}$ + 0.4 V, V_{EN} = 1.8 V, V_{CP_EN} = 1.8 V, C_{IN} = 10 μF, $C_{NR/SS}$ = 4.7 μF, C_{OUT} = 22 μF, C_{BIAS} = 0 nF, SNS pin shorted to OUT pin, and PG pin pulled up to V_{IN} with 100 kΩ (unless otherwise noted); typical values are at T_J = 25°C



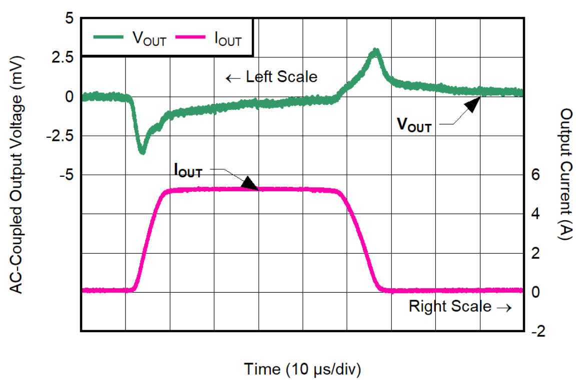
$C_{NR/SS}$ = C_{IN} = 4.7 μF, C_{OUT} = 22 μF, V_{CP_EN} = 0 V, V_{BIAS} = 11 V, V_{IN} = 0.8 V

图 6-39. Load Transient for V_{OUT} = 0.5 V, I_{OUT} = 100 mA to 5 A, CP Disabled, SR = 1 A/μs, V_{BIAS} = 11 V



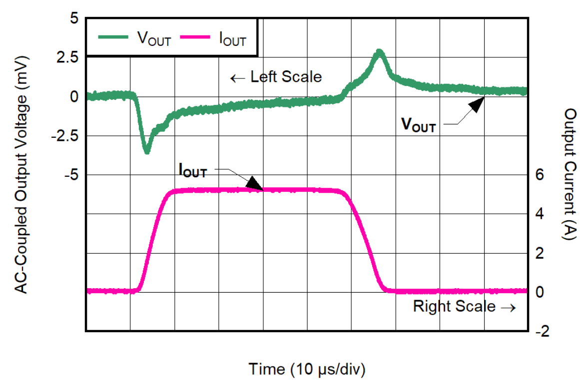
$C_{NR/SS}$ = C_{IN} = 4.7 μF, C_{OUT} = 22 μF, V_{CP_EN} = 0 V, V_{BIAS} = 6.5 V, V_{IN} = 3.6 V

图 6-40. Load Transient for V_{OUT} = 3.3 V, I_{OUT} = 100 mA to 5 A, CP Disabled, SR = 0.5 A/μs, V_{BIAS} = 6.5 V



$C_{NR/SS}$ = C_{IN} = 4.7 μF, C_{OUT} = 22 μF, V_{CP_EN} = 0 V, V_{BIAS} = 6.5 V, V_{IN} = 3.6 V

图 6-41. Load Transient for V_{OUT} = 3.3 V, I_{OUT} = 100 mA to 5 A, CP Disabled, SR = 1 A/μs, V_{BIAS} = 6.5 V

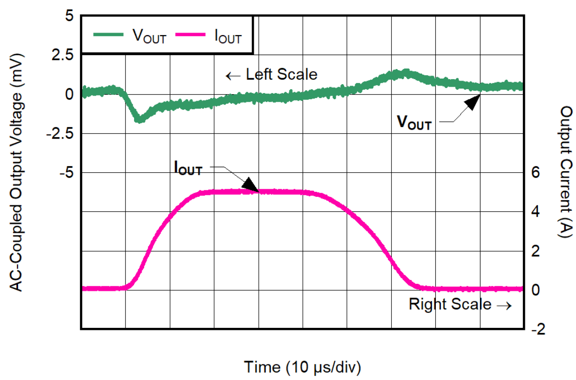


$C_{NR/SS}$ = C_{IN} = 4.7 μF, C_{OUT} = 22 μF, V_{CP_EN} = 0 V, V_{BIAS} = 11 V, V_{IN} = 3.6 V

图 6-42. Load Transient for V_{OUT} = 3.3 V, I_{OUT} = 100 mA to 5 A, CP Disabled, SR = 1 A/μs, V_{BIAS} = 11 V

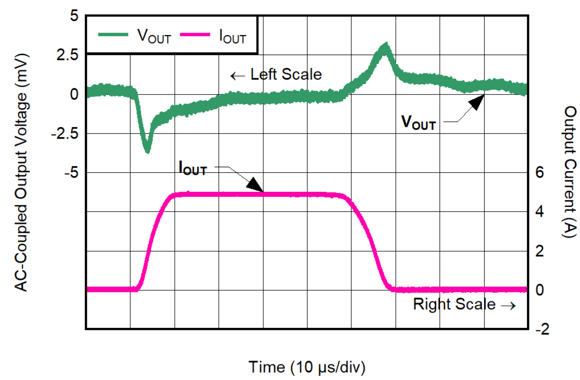
6.6 Typical Characteristics (continued)

$V_{IN} = V_{OUT(NOM)} + 0.4$ V, $V_{EN} = 1.8$ V, $V_{CP\_EN} = 1.8$ V, $C_{IN} = 10$ µF, $C_{NR/SS} = 4.7$ µF, $C_{OUT} = 22$ µF, $C_{BIAS} = 0$ nF, SNS pin shorted to OUT pin, and PG pin pulled up to V_{IN} with 100 kΩ (unless otherwise noted); typical values are at $T_J = 25°C$



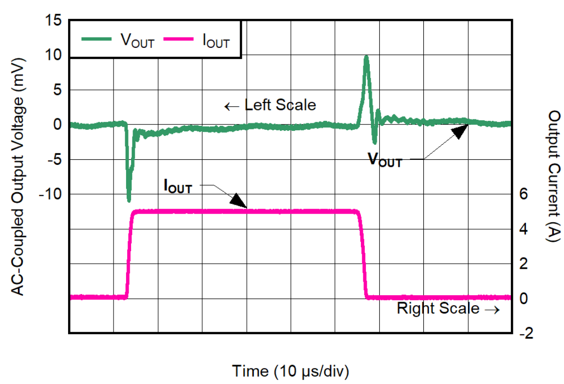
$C_{NR/SS} = C_{IN} = 4.7$ µF, $C_{OUT} = 22$ µF, $V_{CP\_EN} = 0$ V, $V_{BIAS} = 8.4$ V, $V_{IN} = 5.5$ V

图 6-43. Load Transient for $V_{OUT} = 5.2$ V, $I_{OUT} = 100$ mA to 5 A, CP Disabled, SR = 0.5 A/µs, $V_{BIAS} = 8.4$ V



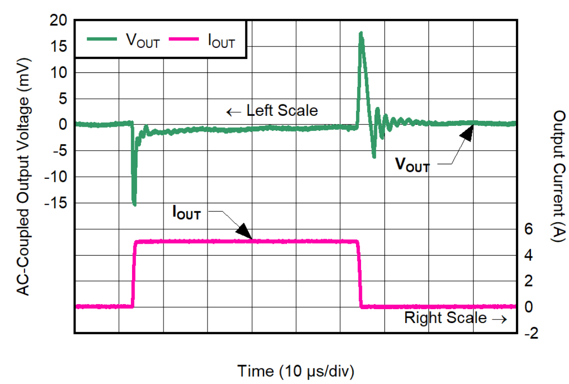
$C_{NR/SS} = C_{IN} = 4.7$ µF, $C_{OUT} = 22$ µF, $V_{CP\_EN} = 0$ V, $V_{BIAS} = 8.4$ V, $V_{IN} = 5.5$ V

图 6-44. Load Transient for $V_{OUT} = 5.2$ V, $I_{OUT} = 100$ mA to 5 A, CP Disabled, SR = 1 A/µs, $V_{BIAS} = 8.4$ V



$C_{NR/SS} = C_{IN} = 4.7$ µF, $C_{OUT} = 22$ µF, $V_{CP\_EN} = 0$ V, $V_{BIAS} = 8.4$ V, $V_{IN} = 5.5$ V

图 6-45. Load Transient for $V_{OUT} = 5.2$ V, $I_{OUT} = 100$ mA to 5 A, CP Disabled, SR = 5 A/µs, $V_{BIAS} = 8.4$ V

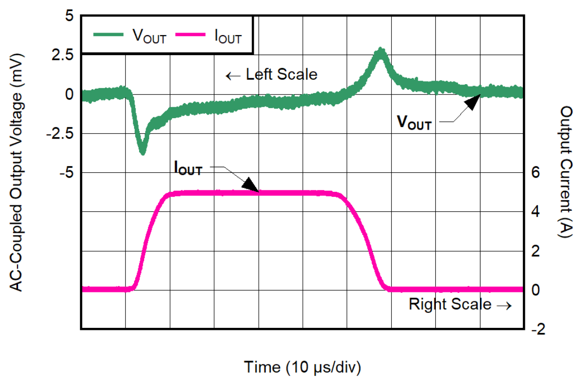


$C_{NR/SS} = C_{IN} = 4.7$ µF, $C_{OUT} = 22$ µF, $V_{CP\_EN} = 0$ V, $V_{BIAS} = 8.4$ V, $V_{IN} = 5.5$ V

图 6-46. Load Transient for $V_{OUT} = 5.2$ V, $I_{OUT} = 100$ mA to 5 A, CP Disabled, SR = 10 A/µs, $V_{BIAS} = 8.4$ V

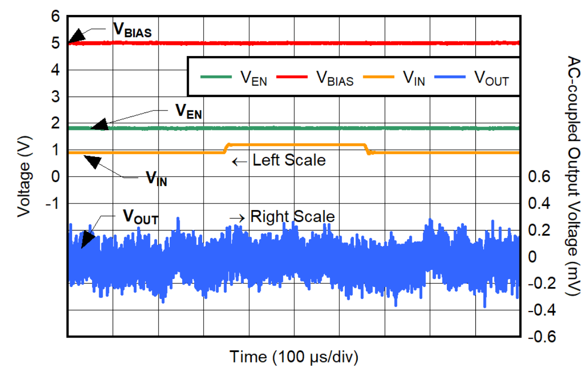
6.6 Typical Characteristics (continued)

$V_{IN} = V_{OUT(NOM)} + 0.4$ V, $V_{EN} = 1.8$ V, $V_{CP\_EN} = 1.8$ V, $C_{IN} = 10$ µF, $C_{NR/SS} = 4.7$ µF, $C_{OUT} = 22$ µF, $C_{BIAS} = 0$ nF, SNS pin shorted to OUT pin, and PG pin pulled up to V_{IN} with 100 kΩ (unless otherwise noted); typical values are at $T_J = 25°C$



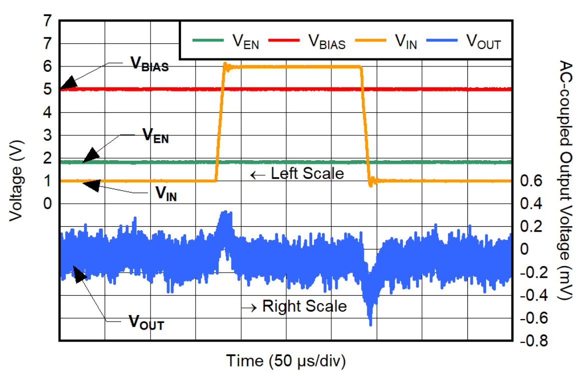
$C_{NR/SS} = C_{IN} = 4.7$ µF, $C_{OUT} = 22$ µF, $V_{CP\_EN} = 0$ V, $V_{BIAS} = 11$ V, $V_{IN} = 5.5$ V

图 6-47. Load Transient for $V_{OUT} = 5.2$ V, $I_{OUT} = 100$ mA to 5 A, CP Disabled, SR = 1 A/µs, $V_{BIAS} = 11$ V



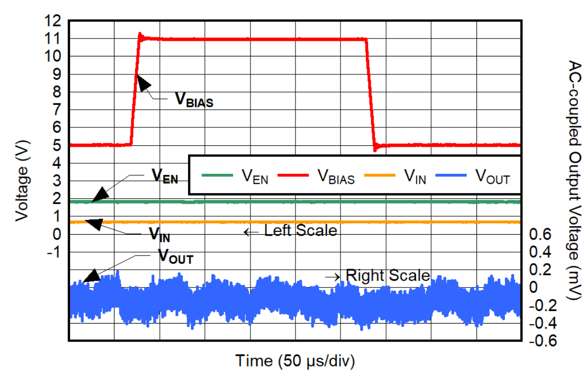
$C_{NR/SS} = C_{IN} = 4.7$ µF, $C_{OUT} = 22$ µF, $V_{CP\_EN} = 0$ V, $V_{BIAS} = 5$ V, $V_{OUT} = 0.5$ V, $I_{OUT} = 100$ mA, SR = 1 V/µs

图 6-48. IN Line Transient for $V_{IN} = 0.9$ V to 1.2 V



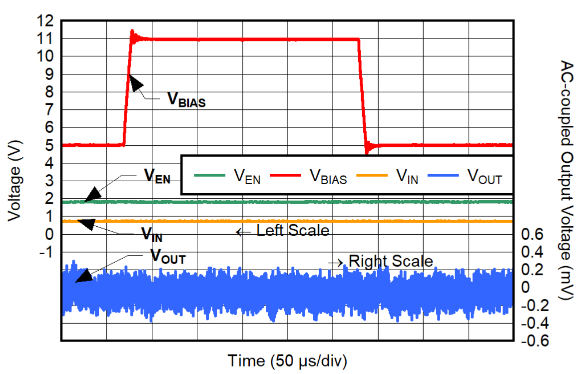
$C_{NR/SS} = C_{IN} = 4.7$ µF, $C_{OUT} = 22$ µF, $V_{CP\_EN} = 0$ V, $V_{BIAS} = 5$ V, $V_{OUT} = 0.5$ V, $I_{OUT} = 100$ mA, SR = 1 V/µs

图 6-49. IN Line Transient for $V_{IN} = 0.9$ V to 6 V



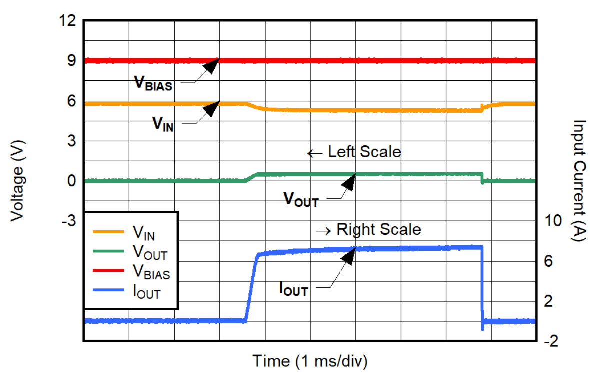
$C_{NR/SS} = C_{IN} = 4.7$ µF, $C_{OUT} = 22$ µF, $V_{CP\_EN} = 0$ V, $V_{IN} = 0.8$ V, $V_{OUT} = 0.5$ V, SR = 1 V/µs

图 6-50. BIAS Line Transient for $V_{IN} = 0.9$ V to 6 V, $I_{OUT} = 100$ mA



$C_{NR/SS} = C_{IN} = 4.7$ µF, $C_{OUT} = 22$ µF, $V_{CP\_EN} = 0$ V, $V_{IN} = 0.8$ V, $V_{OUT} = 0.5$ V, SR = 1 V/µs

图 6-51. BIAS Line Transient for $V_{IN} = 0.9$ V to 6 V, $I_{OUT} = 5$ A

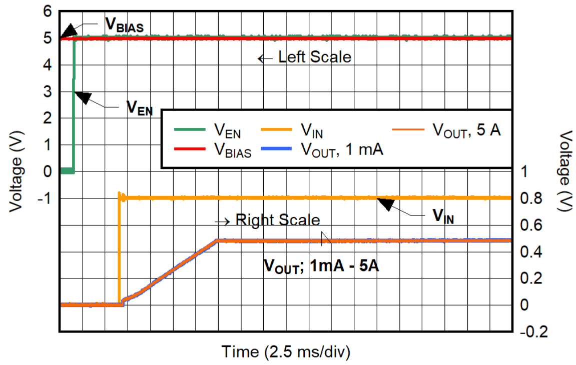


$C_{NR/SS} = C_{IN} = 4.7$ µF, $C_{OUT} = 22$ µF, $V_{CP\_EN} = 0$ V, $V_{BIAS} = 9$ V, $V_{IN} = 5.5$ V, $V_{OUT(nom)} = 5.2$ V

图 6-52. Start-Up Under Current Limit

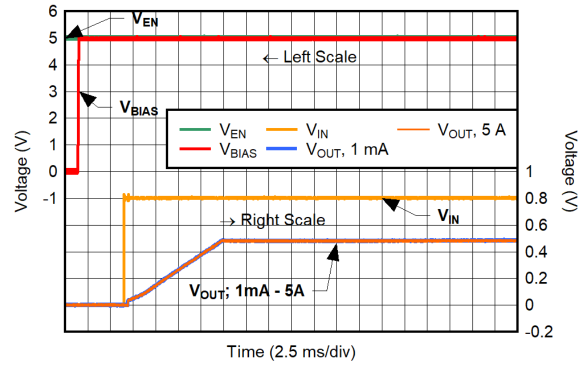
6.6 Typical Characteristics (continued)

$V_{IN} = V_{OUT(NOM)} + 0.4$ V, $V_{EN} = 1.8$ V, $V_{CP\_EN} = 1.8$ V, $C_{IN} = 10$ µF, $C_{NR/SS} = 4.7$ µF, $C_{OUT} = 22$ µF, $C_{BIAS} = 0$ nF, SNS pin shorted to OUT pin, and PG pin pulled up to V_{IN} with 100 kΩ (unless otherwise noted); typical values are at $T_J = 25°C$



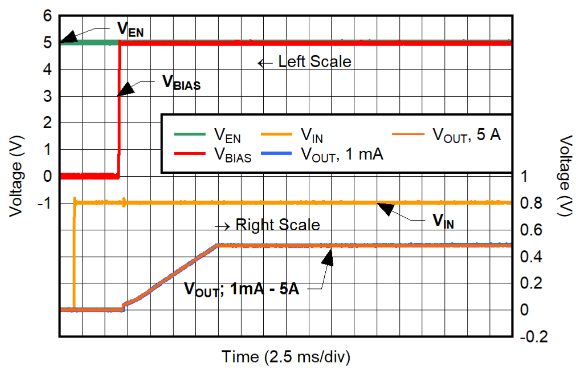
$C_{NR/SS} = C_{IN} = 4.7$ µF, $C_{OUT} = 22$ µF, $V_{CP\_EN} = 0$ V, $V_{BIAS} = 5$ V, $V_{IN} = 0.8$ V, $V_{OUT} = 0.5$ V

图 6-53. Start-Up for BIAS-EN-IN Rail Sequence for CP Disabled



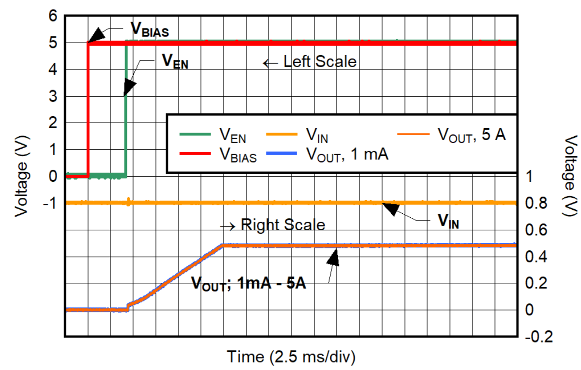
$C_{NR/SS} = C_{IN} = 4.7$ µF, $C_{OUT} = 22$ µF, $V_{CP\_EN} = 0$ V, $V_{BIAS} = 5$ V, $V_{IN} = 0.8$ V, $V_{OUT} = 0.5$ V

图 6-54. Start-Up for EN-BIAS-IN Rail Sequence for CP Disabled



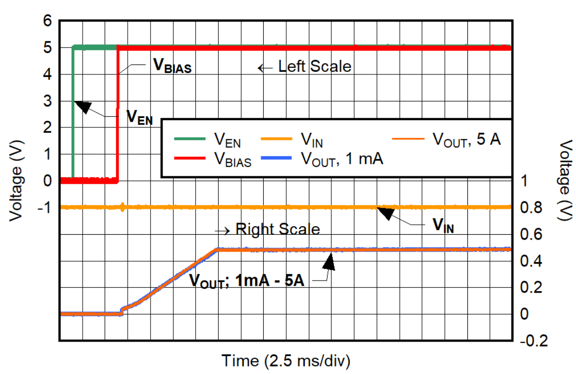
$C_{NR/SS} = C_{IN} = 4.7$ µF, $C_{OUT} = 22$ µF, $V_{CP\_EN} = 0$ V, $V_{BIAS} = 5$ V, $V_{IN} = 0.8$ V, $V_{OUT} = 0.5$ V

图 6-55. Start-Up for EN-IN-BIAS Rail Sequence for CP Disabled



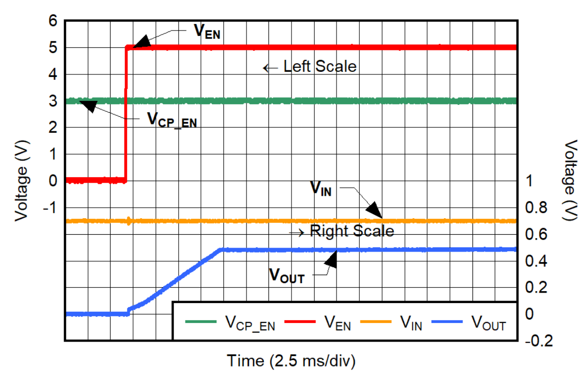
$C_{NR/SS} = C_{IN} = 4.7$ µF, $C_{OUT} = 22$ µF, $V_{CP\_EN} = 0$ V, $V_{BIAS} = 5$ V, $V_{IN} = 0.8$ V, $V_{OUT} = 0.5$ V

图 6-56. Start-Up for IN-BIAS-EN Rail Sequence for CP Disabled



$C_{NR/SS} = C_{IN} = 4.7$ µF, $C_{OUT} = 22$ µF, $V_{CP\_EN} = 0$ V, $V_{BIAS} = 5$ V, $V_{IN} = 0.8$ V, $V_{OUT} = 0.5$ V

图 6-57. Start-Up for IN-EN-BIAS Rail Sequence for CP Disabled

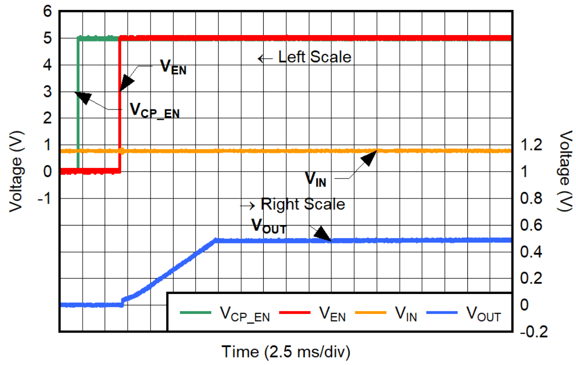


$C_{NR/SS} = C_{IN} = 4.7$ µF, $C_{OUT} = 22$ µF, $V_{CP\_EN} = 3$ V, $V_{BIAS} = 5$ V, $V_{IN} = 0.7$ V, $V_{OUT} = 0.5$ V, $I_{OUT} = 5$ A

图 6-58. Start-Up for CP_EN-BIAS-IN Rail Sequence for CP Enabled

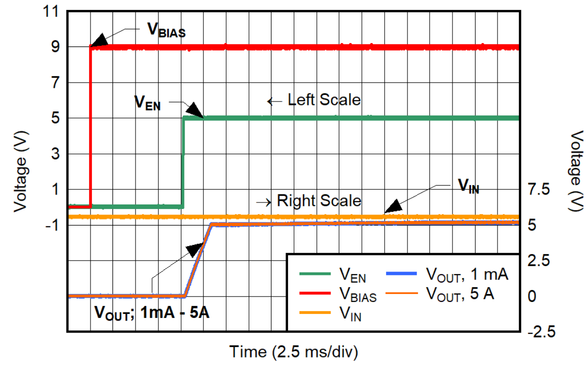
6.6 Typical Characteristics (continued)

$V_{IN} = V_{OUT(NOM)} + 0.4$ V, $V_{EN} = 1.8$ V, $V_{CP\_EN} = 1.8$ V, $C_{IN} = 10$ µF, $C_{NR/SS} = 4.7$ µF, $C_{OUT} = 22$ µF, $C_{BIAS} = 0$ nF, SNS pin shorted to OUT pin, and PG pin pulled up to V_{IN} with 100 kΩ (unless otherwise noted); typical values are at $T_J = 25°C$



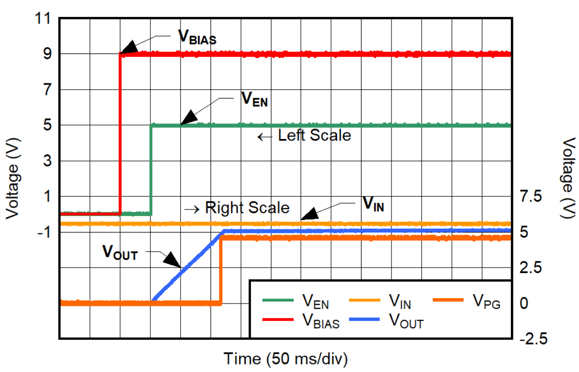
$C_{NR/SS} = C_{IN} = 4.7$ µF, $C_{OUT} = 22$ µF, $V_{CP\_EN} = 3$ V, $V_{BIAS} = 5$ V, $V_{IN} = 0.7$ V, $V_{OUT} = 0.5$ V, $I_{OUT} = 5$ A

图 6-59. Start-Up for IN-CP_EN-EN Rail Sequence for CP Enabled



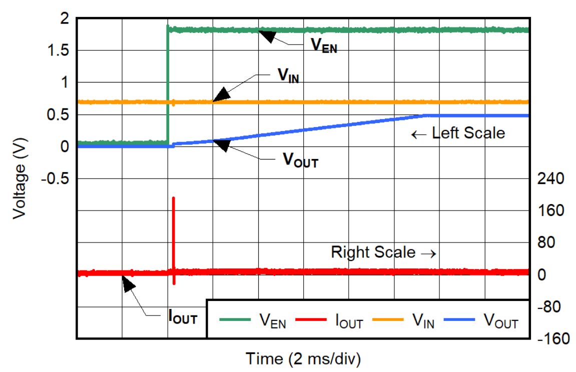
$C_{NR/SS} = 100$ nF, $C_{IN} = 4.7$ µF, $C_{OUT} = 22$ µF, $V_{CP\_EN} = 3$ V, $V_{BIAS} = 9$ V, $V_{IN} = 5.6$ V, $V_{OUT} = 5.2$ V

图 6-60. Start-Up for IN-BIAS-EN Rail Sequence for CP Disabled, $V_{OUT} = 5.2$ V, $C_{NR/SS} = 100$ nF



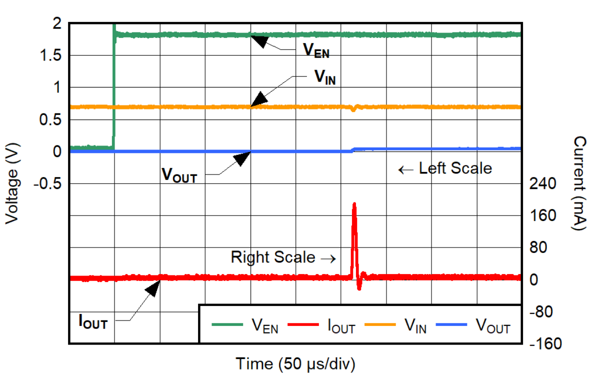
$C_{NR/SS} = C_{IN} = 4.7$ µF, $C_{OUT} = 22$ µF, $V_{CP\_EN} = 3$ V, $V_{BIAS} = 9$ V, $V_{IN} = 5.6$ V, $V_{OUT} = 5.2$ V, $I_{OUT} = 5$ A

图 6-61. Start-Up for IN-BIAS-EN-PG Rail Sequence for CP Disabled, $V_{OUT} = 5.2$ V, $C_{NR/SS} = 4.7$ µF



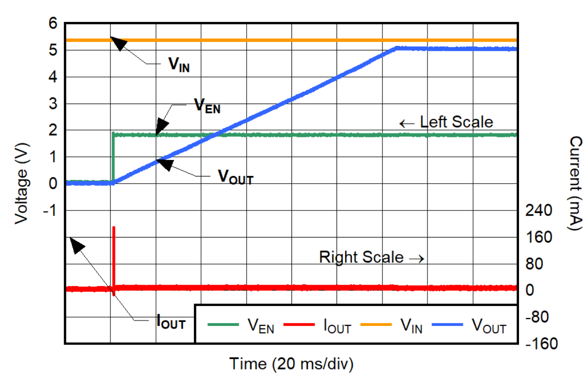
$C_{NR/SS} = C_{IN} = 4.7$ µF, $C_{OUT} = 22$ µF, $V_{CP\_EN} = 0$ V, $V_{BIAS} = 5$ V, $V_{IN} = 0.7$ V, $V_{OUT} = 0.5$ V

图 6-62. Inrush Current for CP Disabled, $V_{OUT} = 0.5$ V



$C_{NR/SS} = C_{IN} = 4.7$ µF, $C_{OUT} = 22$ µF, $V_{CP\_EN} = 0$ V, $V_{BIAS} = 5$ V, $V_{IN} = 0.7$ V, $V_{OUT} = 0.5$ V

图 6-63. Inrush Current for CP Disabled, $V_{OUT} = 0.5$ V, First 500 µs

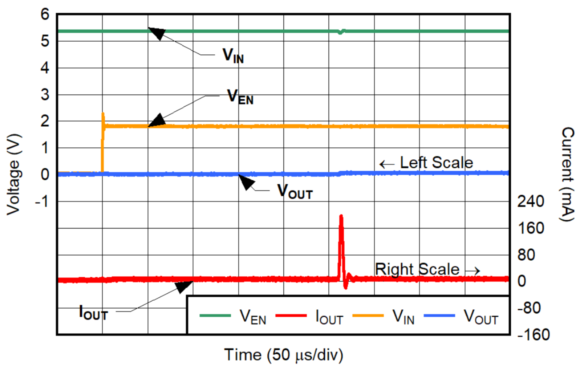


$C_{NR/SS} = C_{IN} = 4.7$ µF, $C_{OUT} = 22$ µF, $V_{CP\_EN} = 0$ V, $V_{BIAS} = 9$ V, $V_{IN} = 5.5$ V, $V_{OUT} = 5.2$ V

图 6-64. Inrush Current for CP Disabled, $V_{OUT} = 5.2$ V

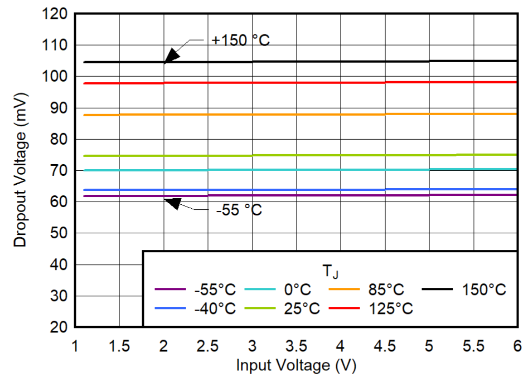
6.6 Typical Characteristics (continued)

V_{IN} = $V_{OUT(NOM)}$ + 0.4 V, V_{EN} = 1.8 V, V_{CP_EN} = 1.8 V, C_{IN} = 10 μF, $C_{NR/SS}$ = 4.7 μF, C_{OUT} = 22 μF, C_{BIAS} = 0 nF, SNS pin shorted to OUT pin, and PG pin pulled up to V_{IN} with 100 kΩ (unless otherwise noted); typical values are at T_J = 25°C



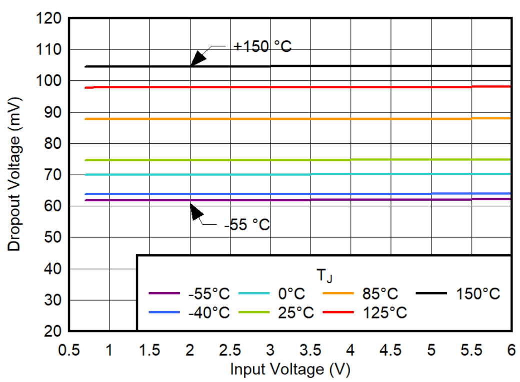
$C_{NR/SS}$ = C_{IN} = 4.7 μF, C_{OUT} = 22 μF, V_{CP_EN} = 0 V, V_{BIAS} = 9 V, V_{IN} = 5.5 V, V_{OUT} = 5.2 V

图 6-65. Inrush Current for CP Disabled, V_{OUT} = 5.2 V, First 500 μs



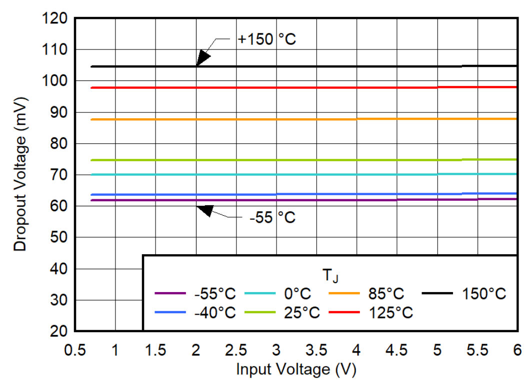
$C_{NR/SS}$ = C_{IN} = 4.7 μF, C_{OUT} = 22 μF, V_{CP_EN} = 1.8 V, V_{BIAS} = 0 V, I_{OUT} = 5 A

图 6-66. Dropout Voltage vs V_{IN} for CP Enabled, No Bias Rail



$C_{NR/SS}$ = C_{IN} = 4.7 μF, C_{OUT} = 22 μF, V_{CP_EN} = 1.8 V, I_{OUT} = 5 A

图 6-67. Dropout Voltage vs V_{IN} for CP Enabled, V_{BIAS} = 3 V

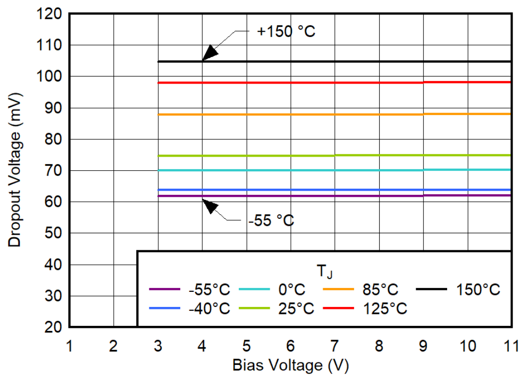


$C_{NR/SS}$ = C_{IN} = 4.7 μF, C_{OUT} = 22 μF, V_{CP_EN} = 1.8 V, I_{OUT} = 5 A

图 6-68. Dropout Voltage vs V_{IN} for CP Enabled, V_{BIAS} = V_{IN} + 3.2 V

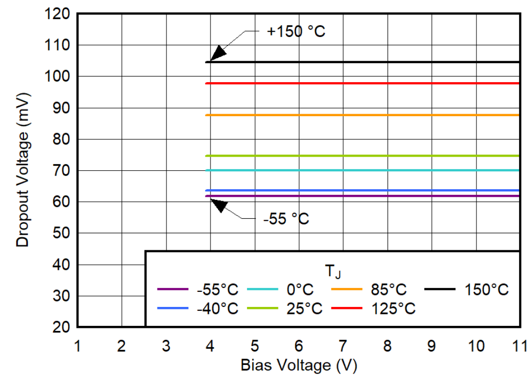
6.6 Typical Characteristics (continued)

V_{IN} = $V_{OUT(NOM)}$ + 0.4 V, V_{EN} = 1.8 V, V_{CP_EN} = 1.8 V, C_{IN} = 10 µF, $C_{NR/SS}$ = 4.7 µF, C_{OUT} = 22 µF, C_{BIAS} = 0 nF, SNS pin shorted to OUT pin, and PG pin pulled up to V_{IN} with 100 kΩ (unless otherwise noted); typical values are at T_J = 25°C



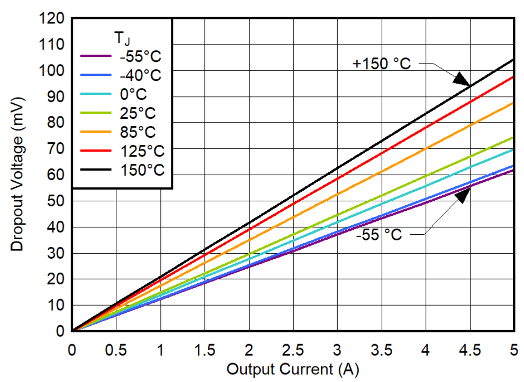
$C_{NR/SS}$ = C_{IN} = 4.7 µF, C_{OUT} = 22 µF, V_{CP_EN} = 1.8 V, I_{OUT} = 5 A

图 6-69. Dropout Voltage vs V_{BIAS} for CP Enabled, V_{IN} = 0.7 V



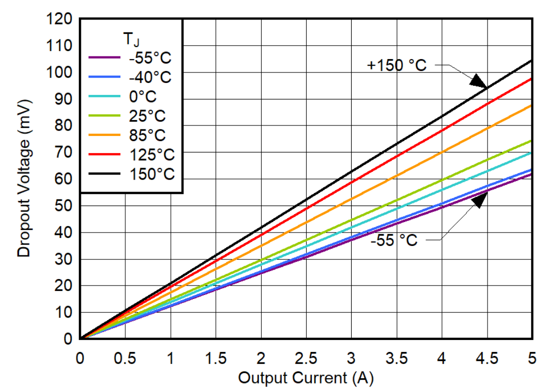
$C_{NR/SS}$ = C_{IN} = 4.7 µF, C_{OUT} = 22 µF, V_{CP_EN} = 0 V, I_{OUT} = 5 A

图 6-70. Dropout Voltage vs V_{BIAS} for CP Disabled, V_{IN} = 0.7 V



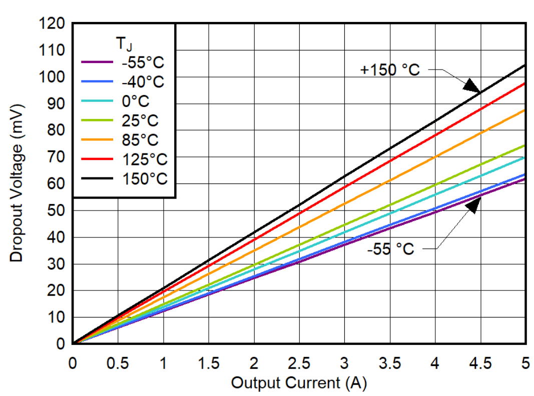
$C_{NR/SS}$ = C_{IN} = 4.7 µF, C_{OUT} = 22 µF, V_{CP_EN} = 0 V

图 6-71. Dropout Voltage vs I_{OUT} for CP Disabled, V_{IN} = 0.7 V, V_{BIAS} = 3.9 V



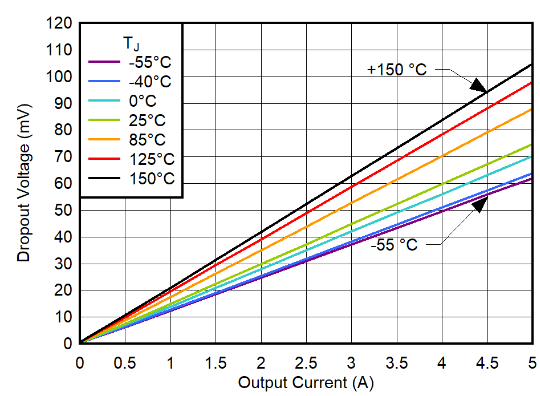
$C_{NR/SS}$ = C_{IN} = 4.7 µF, C_{OUT} = 22 µF, V_{CP_EN} = 1.8 V

图 6-72. Dropout Voltage vs I_{OUT} for CP Enabled, V_{IN} = 0.7 V, V_{BIAS} = 3 V



$C_{NR/SS}$ = C_{IN} = 4.7 µF, C_{OUT} = 22 µF, V_{CP_EN} = 1.8 V, V_{BIAS} = 0 V

图 6-73. Dropout Voltage vs I_{OUT} for CP Enabled, V_{IN} = 1.1 V, No Bias

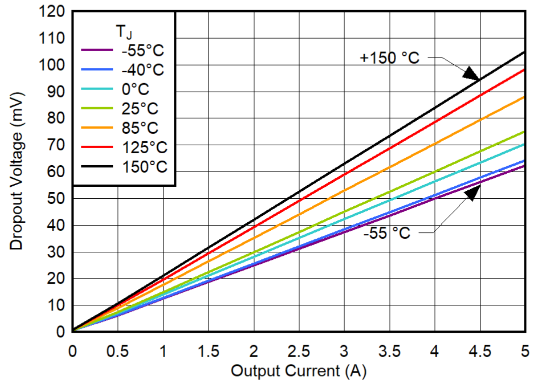


$C_{NR/SS}$ = C_{IN} = 4.7 µF, C_{OUT} = 22 µF, V_{CP_EN} = 1.8 V, V_{BIAS} = 0 V

图 6-74. Dropout Voltage vs I_{OUT} for CP Enabled, V_{IN} = 5.3 V, No Bias

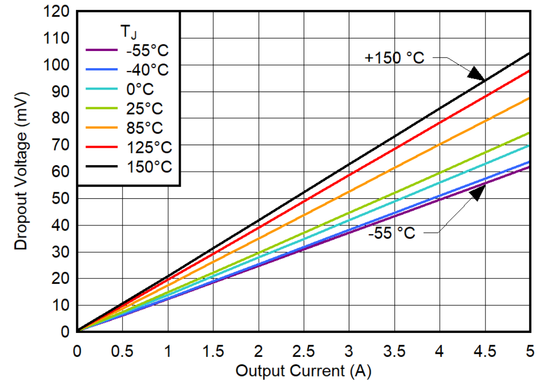
6.6 Typical Characteristics (continued)

$V_{IN} = V_{OUT(NOM)}$ + 0.4 V, V_{EN} = 1.8 V, V_{CP_EN} = 1.8 V, C_{IN} = 10 µF, $C_{NR/SS}$ = 4.7 µF, C_{OUT} = 22 µF, C_{BIAS} = 0 nF, SNS pin shorted to OUT pin, and PG pin pulled up to V_{IN} with 100 kΩ (unless otherwise noted); typical values are at T_J = 25°C



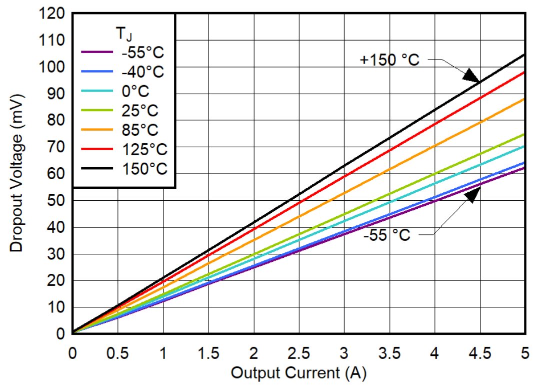
$C_{NR/SS} = C_{IN}$ = 4.7 µF, C_{OUT} = 22 µF, V_{CP_EN} = 1.8 V, V_{BIAS} = 0 V

图 6-75. Dropout Voltage vs I_{OUT} for CP Enabled, V_{IN} = 6 V, No Bias



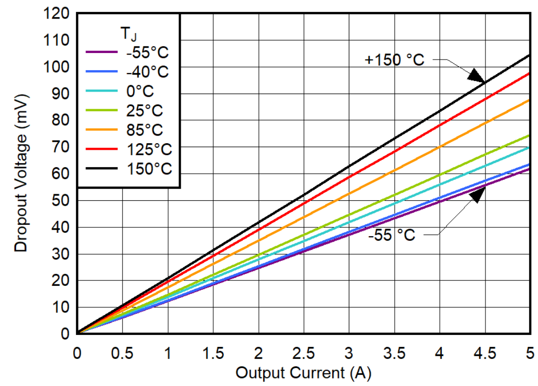
$C_{NR/SS} = C_{IN}$ = 4.7 µF, C_{OUT} = 22 µF, V_{CP_EN} = 1.8 V

图 6-76. Dropout Voltage vs I_{OUT} for CP Enabled, V_{IN} = 5.3 V, V_{BIAS} = 3 V



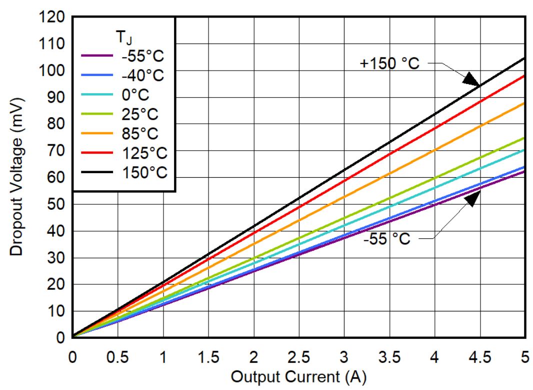
$C_{NR/SS} = C_{IN}$ = 4.7 µF, C_{OUT} = 22 µF, V_{CP_EN} = 1.8 V

图 6-77. Dropout Voltage vs I_{OUT} for CP Enabled, V_{IN} = 6 V, V_{BIAS} = 3 V



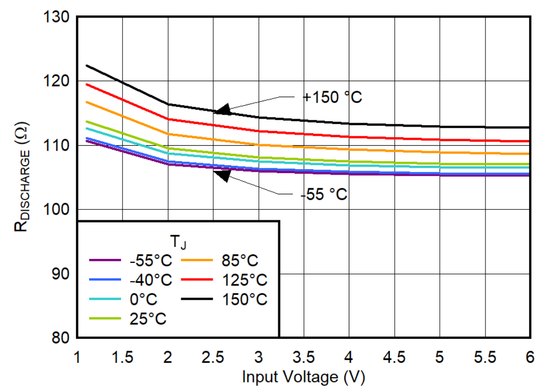
$C_{NR/SS} = C_{IN}$ = 4.7 µF, C_{OUT} = 22 µF, V_{CP_EN} = 0 V

图 6-78. Dropout Voltage vs I_{OUT} for CP Disabled, V_{IN} = 5.3 V, V_{BIAS} = 9.2 V



$C_{NR/SS} = C_{IN}$ = 4.7 µF, C_{OUT} = 22 µF, V_{CP_EN} = 0 V

图 6-79. Dropout Voltage vs I_{OUT} for CP Disabled, V_{IN} = 6 V, V_{BIAS} = 9.2 V

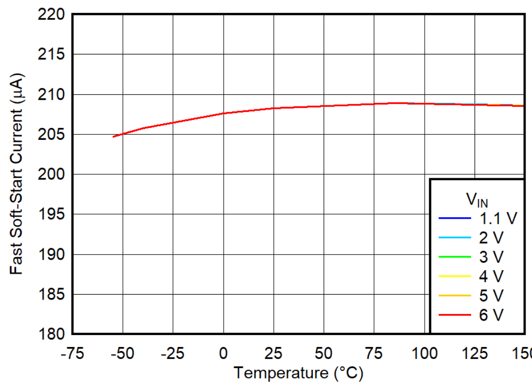


$C_{NR/SS} = C_{IN}$ = 4.7 µF, C_{OUT} = 22 µF, V_{CP_EN} = 1.8 V

图 6-80. Output Discharge Resistor vs V_{IN}

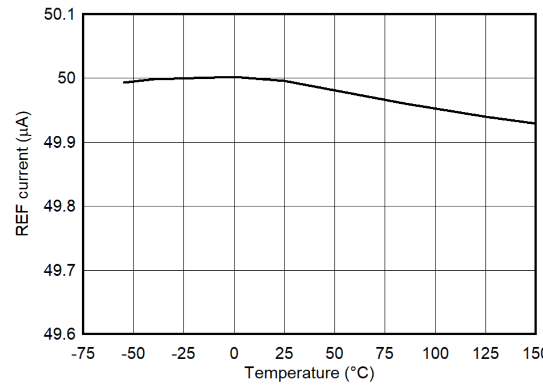
6.6 Typical Characteristics (continued)

$V_{IN} = V_{OUT(NOM)} + 0.4$ V, V_{EN} = 1.8 V, V_{CP_EN} = 1.8 V, C_{IN} = 10 µF, $C_{NR/SS}$ = 4.7 µF, C_{OUT} = 22 µF, C_{BIAS} = 0 nF, SNS pin shorted to OUT pin, and PG pin pulled up to V_{IN} with 100 kΩ (unless otherwise noted); typical values are at T_J = 25°C



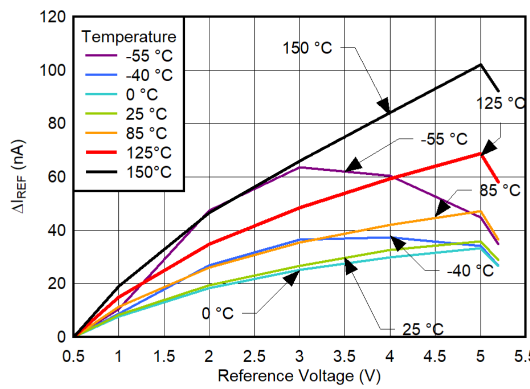
$C_{NR/SS} = C_{IN}$ = 4.7 µF, C_{OUT} = 22 µF, V_{CP_EN} = 0 V, V_{BIAS} = 0 V

图 6-81. Fast Soft-Start Current vs Temperature and V_{IN}



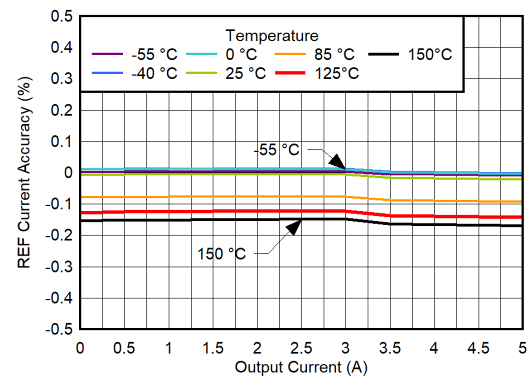
$C_{NR/SS} = C_{IN}$ = 4.7 µF, C_{OUT} = 22 µF, V_{CP_EN} = 1.8 V, V_{BIAS} = 0 V, V_{IN} = 1.1 V

图 6-82. Reference Current vs Temperature



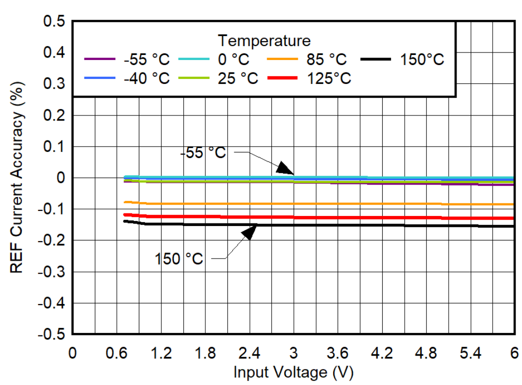
$C_{NR/SS} = C_{IN}$ = 4.7 µF, C_{OUT} = 22 µF, V_{CP_EN} = 1.8 V, V_{BIAS} = 0 V, V_{IN} = 6 V, I_{OUT} = 0 A

图 6-83. Change in Reference Current vs V_{REF}



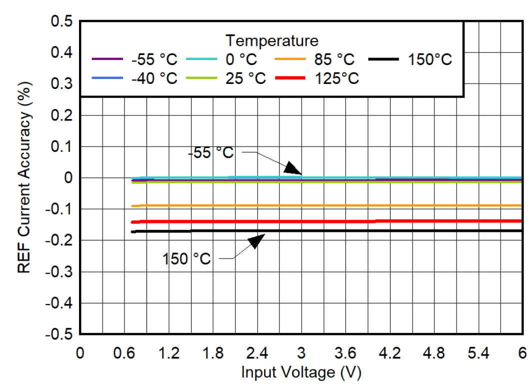
$C_{NR/SS} = C_{IN}$ = 4.7 µF, C_{OUT} = 22 µF, V_{CP_EN} = 1.8 V, V_{BIAS} = 0 V, V_{IN} = 1.1 V, V_{OUT} = 0.5 V

图 6-84. Reference Current Accuracy vs I_{OUT}



$C_{NR/SS} = C_{IN}$ = 4.7 µF, C_{OUT} = 22 µF, V_{CP_EN} = 1.8 V, V_{BIAS} = 3 V, V_{OUT} = 0.5 V

图 6-85. Reference Current Accuracy vs V_{IN} for CP Enabled

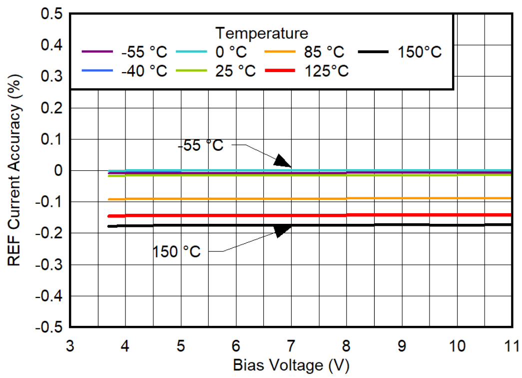


$C_{NR/SS} = C_{IN}$ = 4.7 µF, C_{OUT} = 22 µF, V_{CP_EN} = 0 V, V_{BIAS} = 3.7 V, V_{OUT} = 0.5 V

图 6-86. Reference Current Accuracy vs V_{IN} for CP Disabled

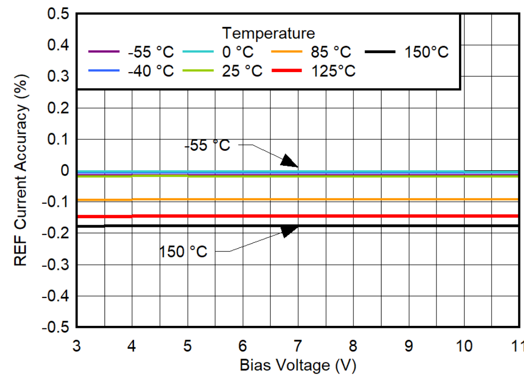
6.6 Typical Characteristics (continued)

$V_{IN} = V_{OUT(NOM)} + 0.4$ V, $V_{EN} = 1.8$ V, $V_{CP\_EN} = 1.8$ V, $C_{IN} = 10$ μF, $C_{NR/SS} = 4.7$ μF, $C_{OUT} = 22$ μF, $C_{BIAS} = 0$ nF, SNS pin shorted to OUT pin, and PG pin pulled up to V_{IN} with 100 kΩ (unless otherwise noted); typical values are at $T_J = 25°C$



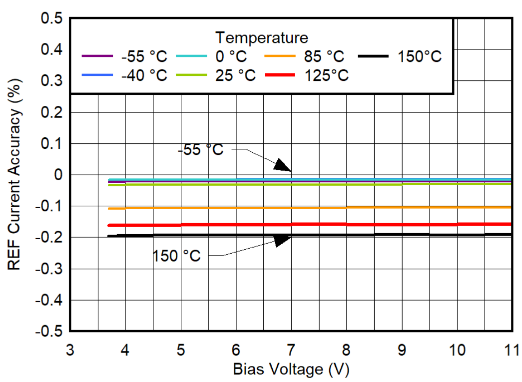
$C_{NR/SS} = C_{IN} = 4.7$ μF, $C_{OUT} = 22$ μF, $V_{CP\_EN} = 0$ V, $V_{IN} = 0.7$ V, $V_{OUT} = 0.5$ V

图 6-87. Reference Current Accuracy vs V_{BIAS} for CP Disabled, $I_{OUT} = 0$ A



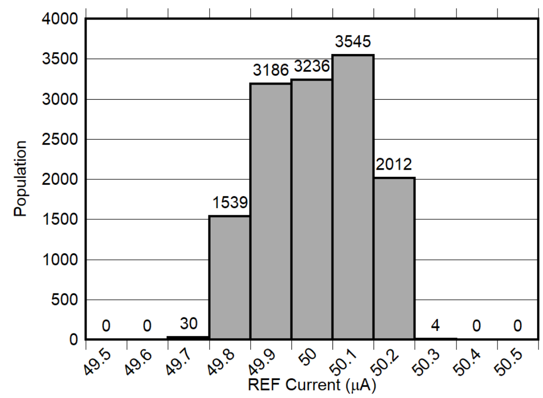
$C_{NR/SS} = C_{IN} = 4.7$ μF, $C_{OUT} = 22$ μF, $V_{CP\_EN} = 1.8$ V, $V_{IN} = 0.7$ V, $V_{OUT} = 0.5$ V

图 6-88. Reference Current Accuracy vs V_{BIAS} for CP Enabled, $I_{OUT} = 0$ A



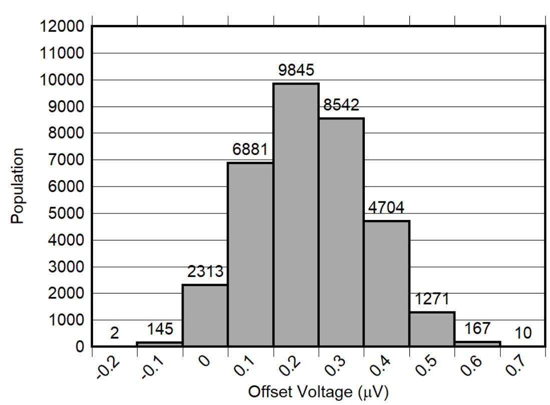
$C_{NR/SS} = C_{IN} = 4.7$ μF, $C_{OUT} = 22$ μF, $V_{CP\_EN} = 0$ V, $V_{IN} = 0.7$ V, $V_{OUT} = 0.5$ V

图 6-89. Reference Current Accuracy vs V_{BIAS} for CP Disabled, $I_{OUT} = 5$ A



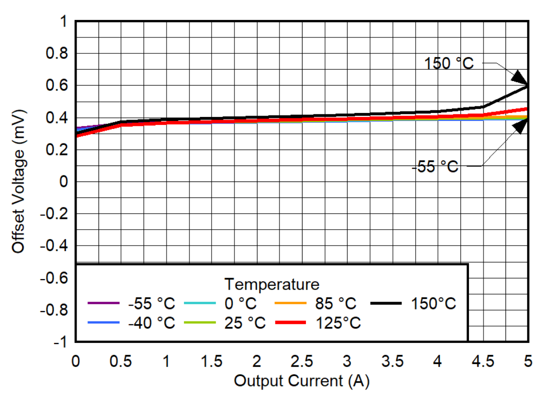
$C_{NR/SS} = C_{IN} = 4.7$ μF, $C_{OUT} = 22$ μF

图 6-90. I_{REF} Distribution



$C_{NR/SS} = C_{IN} = 4.7$ μF, $C_{OUT} = 22$ μF

图 6-91. V_{OS} Distribution

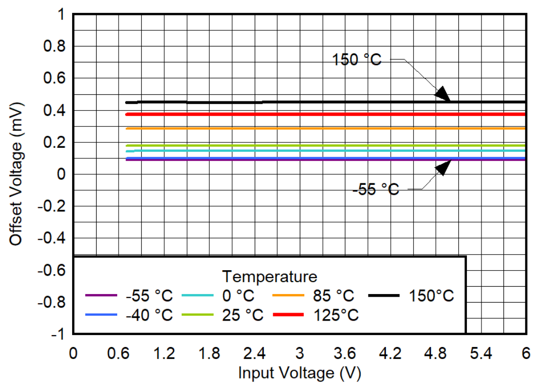


$C_{NR/SS} = C_{IN} = 4.7$ μF, $C_{OUT} = 22$ μF, $V_{CP\_EN} = 1.8$ V, $V_{IN} = 5.5$ V, $V_{OUT} = 5.2$ V

图 6-92. Offset Voltage vs I_{OUT}

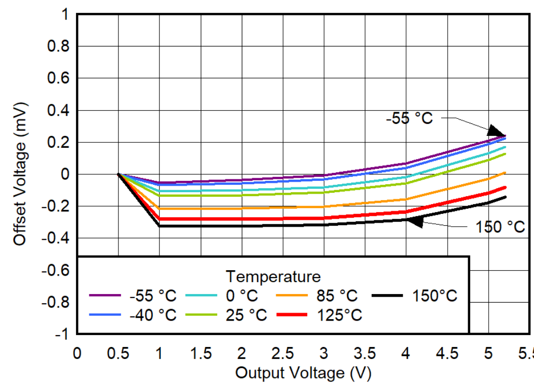
6.6 Typical Characteristics (continued)

V_{IN} = $V_{OUT(NOM)}$ + 0.4 V, V_{EN} = 1.8 V, V_{CP_EN} = 1.8 V, C_{IN} = 10 μF, $C_{NR/SS}$ = 4.7 μF, C_{OUT} = 22 μF, C_{BIAS} = 0 nF, SNS pin shorted to OUT pin, and PG pin pulled up to V_{IN} with 100 kΩ (unless otherwise noted); typical values are at T_J = 25°C



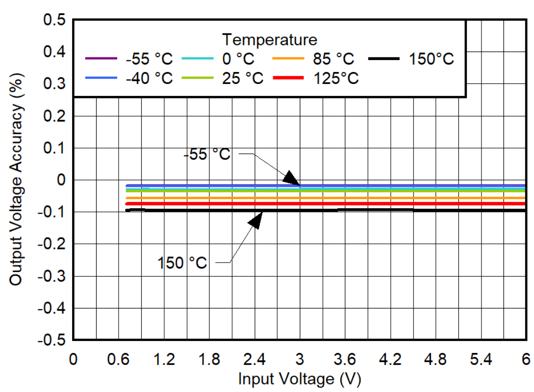
$C_{NR/SS}$ = C_{IN} = 4.7 μF, C_{OUT} = 22 μF, V_{CP_EN} = 0 V, V_{BIAS} = 3.7 V, V_{OUT} = 0.5 V, I_{OUT} = 0 A

图 6-93. Offset Voltage vs V_{IN}



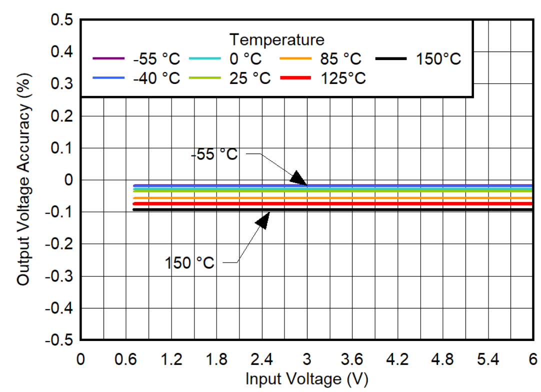
$C_{NR/SS}$ = C_{IN} = 4.7 μF, C_{OUT} = 22 μF, V_{CP_EN} = 0 V, V_{BIAS} = 0 V, V_{IN} = 6 V, I_{OUT} = 0 A

图 6-94. Offset Voltage vs V_{OUT}



$C_{NR/SS}$ = C_{IN} = 4.7 μF, C_{OUT} = 22 μF, V_{CP_EN} = 0 V, V_{BIAS} = 11 V, V_{OUT} = 0.5 V, I_{OUT} = 0 A

图 6-95. Output Voltage Accuracy vs V_{IN} for V_{BIAS} = 11 V, CP Disabled

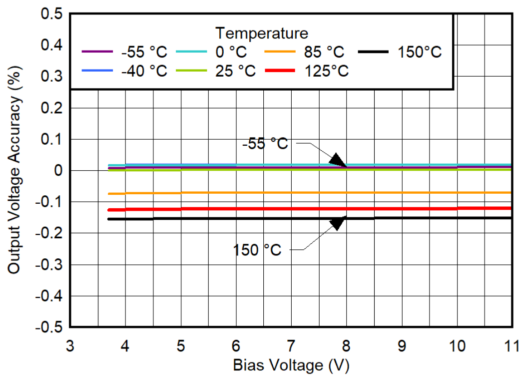


$C_{NR/SS}$ = C_{IN} = 4.7 μF, C_{OUT} = 22 μF, V_{CP_EN} = 0 V, V_{BIAS} = 3.7 V, V_{OUT} = 0.5 V, I_{OUT} = 0 A

图 6-96. Output Voltage Accuracy vs V_{IN} for V_{BIAS} = 3.7 V, CP Disabled

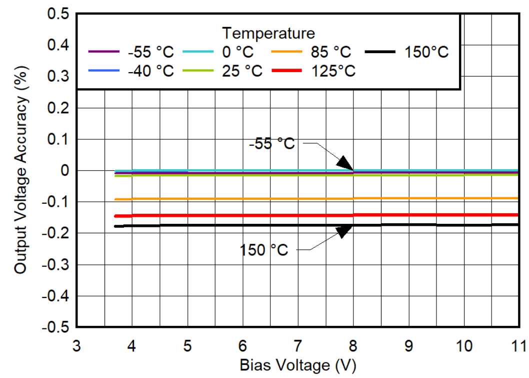
6.6 Typical Characteristics (continued)

$V_{IN} = V_{OUT(NOM)}$ + 0.4 V, V_{EN} = 1.8 V, V_{CP_EN} = 1.8 V, C_{IN} = 10 µF, $C_{NR/SS}$ = 4.7 µF, C_{OUT} = 22 µF, C_{BIAS} = 0 nF, SNS pin shorted to OUT pin, and PG pin pulled up to V_{IN} with 100 kΩ (unless otherwise noted); typical values are at T_J = 25°C



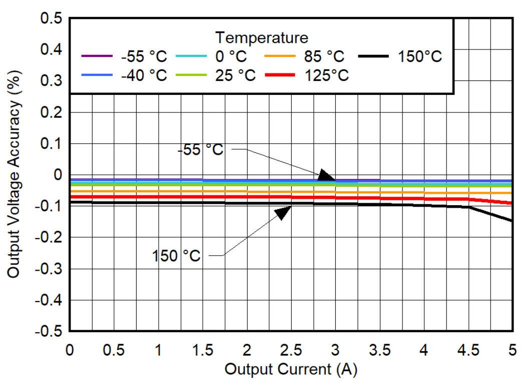
$C_{NR/SS} = C_{IN}$ = 4.7 µF, C_{OUT} = 22 µF, V_{CP_EN} = 0 V, V_{IN} = 6 V, V_{OUT} = 0.5 V, I_{OUT} = 0 A

图 6-97. Output Voltage Accuracy vs V_{BIAS} for V_{IN} = 6 V, CP Disabled



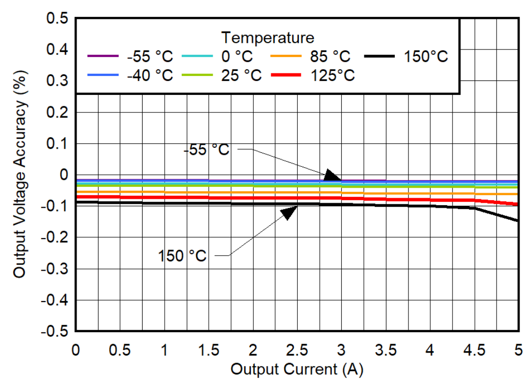
$C_{NR/SS} = C_{IN}$ = 4.7 µF, C_{OUT} = 22 µF, V_{CP_EN} = 0 V, V_{IN} = 0.7 V, V_{OUT} = 0.5 V, I_{OUT} = 0 A

图 6-98. Output Voltage Accuracy vs V_{BIAS} for V_{IN} = 0.7 V, CP Disabled



$C_{NR/SS} = C_{IN}$ = 4.7 µF, C_{OUT} = 22 µF, V_{CP_EN} = 0 V, V_{BIAS} = 11 V, V_{IN} = 0.7 V, V_{OUT} = 0.5 V, I_{OUT} = 0 A

图 6-99. Output Voltage Accuracy vs I_{OUT} for V_{BIAS} = 11 V, CP Disabled

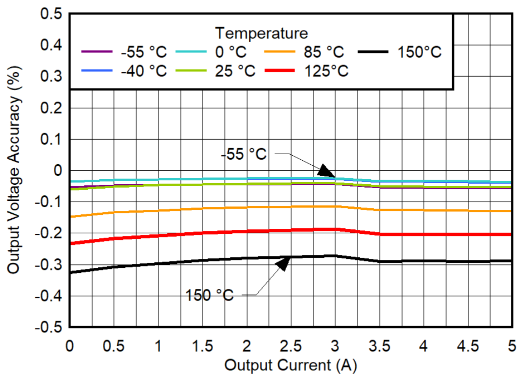


$C_{NR/SS} = C_{IN}$ = 4.7 µF, C_{OUT} = 22 µF, V_{CP_EN} = 0 V, V_{BIAS} = 11 V, V_{IN} = 0.7 V, V_{OUT} = 0.5 V, I_{OUT} = 0 A

图 6-100. Output Voltage Accuracy vs I_{OUT} for V_{BIAS} = 3.7 V, CP Disabled

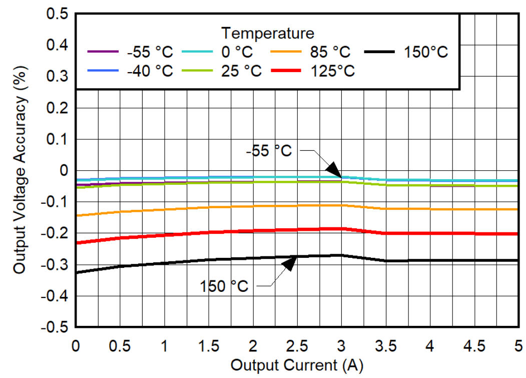
6.6 Typical Characteristics (continued)

$V_{IN} = V_{OUT(NOM)} + 0.4$ V, $V_{EN} = 1.8$ V, $V_{CP\_EN} = 1.8$ V, $C_{IN} = 10$ µF, $C_{NR/SS} = 4.7$ µF, $C_{OUT} = 22$ µF, $C_{BIAS} = 0$ nF, SNS pin shorted to OUT pin, and PG pin pulled up to V_{IN} with 100 kΩ (unless otherwise noted); typical values are at $T_J = 25°C$



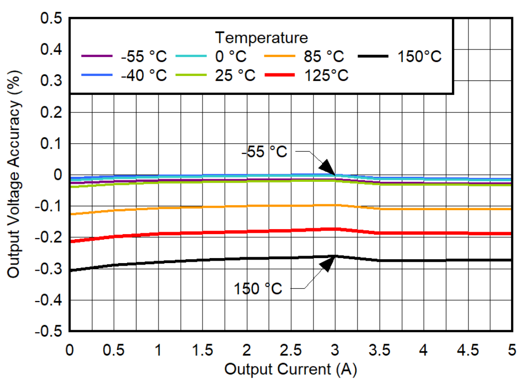
$C_{NR/SS} = C_{IN} = 4.7$ µF, $C_{OUT} = 22$ µF, $V_{CP\_EN} = 0$ V, $V_{BIAS} = 11$ V, $V_{IN} = 6$ V, $V_{OUT} = 5.2$ V, $I_{OUT} = 0$ A

图 6-101. Output Voltage Accuracy vs I_{OUT} for $V_{IN} = 6$ V, $V_{BIAS} = 11$ V, CP Disabled



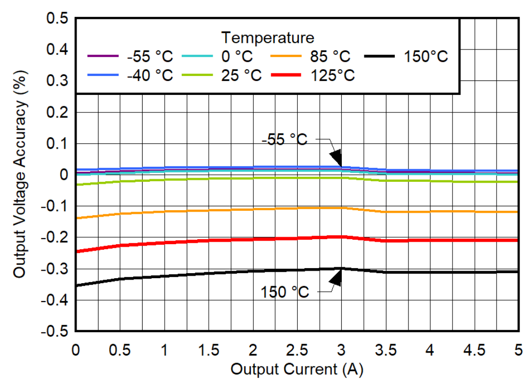
$C_{NR/SS} = C_{IN} = 4.7$ µF, $C_{OUT} = 22$ µF, $V_{CP\_EN} = 0$ V, $V_{BIAS} = 8.4$ V, $V_{IN} = 6$ V, $V_{OUT} = 5.2$ V, $I_{OUT} = 0$ A

图 6-102. Output Voltage Accuracy vs I_{OUT} for $V_{IN} = 6$ V, $V_{BIAS} = 8.4$ V, CP Disabled



$C_{NR/SS} = C_{IN} = 4.7$ µF, $C_{OUT} = 22$ µF, $V_{CP\_EN} = 0$ V, $V_{BIAS} = 11$ V, $V_{IN} = 5.6$ V, $V_{OUT} = 5.2$ V, $I_{OUT} = 0$ A

图 6-103. Output Voltage Accuracy vs I_{OUT} for $V_{IN} = 5.6$ V, $V_{BIAS} = 11$ V, CP Disabled

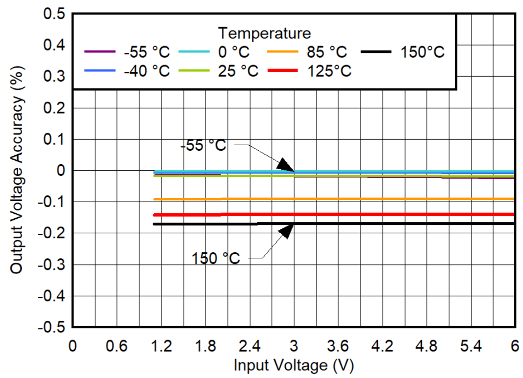


$C_{NR/SS} = C_{IN} = 4.7$ µF, $C_{OUT} = 22$ µF, $V_{CP\_EN} = 0$ V, $V_{BIAS} = 8.4$ V, $V_{IN} = 5.6$ V, $V_{OUT} = 5.2$ V, $I_{OUT} = 0$ A

图 6-104. Output Voltage Accuracy vs I_{OUT} for $V_{IN} = 5.6$ V, $V_{BIAS} = 8.4$ V, CP Disabled

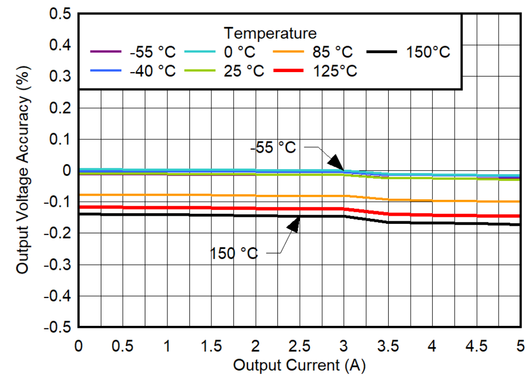
6.6 Typical Characteristics (continued)

$V_{IN} = V_{OUT(NOM)} + 0.4$ V, $V_{EN} = 1.8$ V, $V_{CP\_EN} = 1.8$ V, $C_{IN} = 10$ µF, $C_{NR/SS} = 4.7$ µF, $C_{OUT} = 22$ µF, $C_{BIAS} = 0$ nF, SNS pin shorted to OUT pin, and PG pin pulled up to V_{IN} with 100 kΩ (unless otherwise noted); typical values are at $T_J = 25$°C



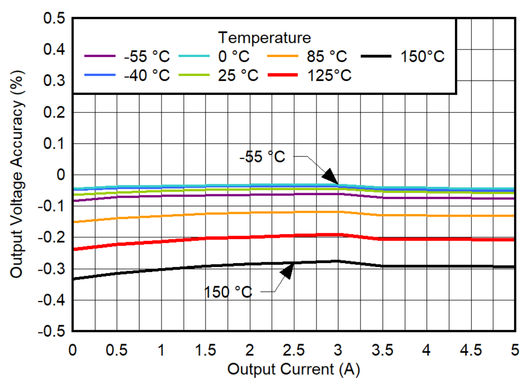
$C_{NR/SS} = C_{IN} = 4.7$ µF, $C_{OUT} = 22$ µF, $V_{CP\_EN} = 1.8$ V, $V_{BIAS} = 0$ V, $V_{IN} = 0.7$ V, $V_{OUT} = 0.5$ V, $I_{OUT} = 0$ A

图 6-105. Output Voltage Accuracy vs V_{IN} for CP Enabled



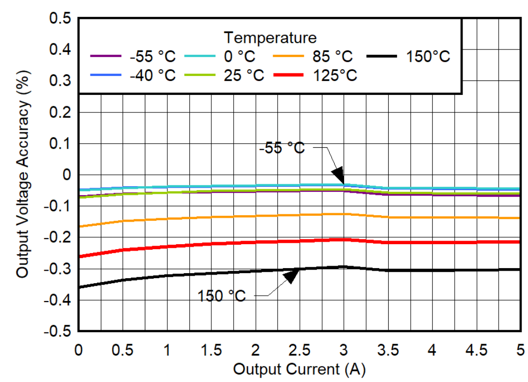
$C_{NR/SS} = C_{IN} = 4.7$ µF, $C_{OUT} = 22$ µF, $V_{CP\_EN} = 1.8$ V, $V_{BIAS} = 0$ V, $V_{IN} = 1.1$ V, $V_{OUT} = 0.5$ V

图 6-106. Output Voltage Accuracy vs I_{OUT} for $V_{IN} = 1.1$ V, CP Enabled



$C_{NR/SS} = C_{IN} = 4.7$ µF, $C_{OUT} = 22$ µF, $V_{CP\_EN} = 1.8$ V, $V_{BIAS} = 0$ V, $V_{IN} = 6$ V, $V_{OUT} = 5.2$ V

图 6-107. Output Voltage Accuracy vs I_{OUT} for $V_{IN} = 6$ V, CP Enabled

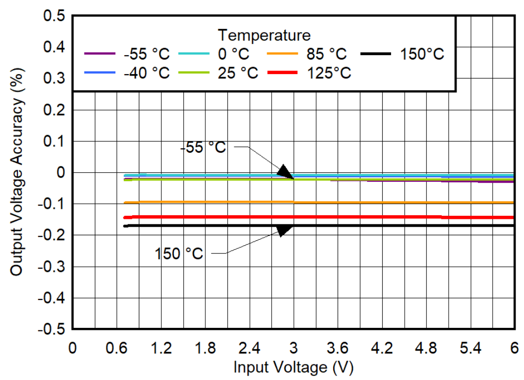


$C_{NR/SS} = C_{IN} = 4.7$ µF, $C_{OUT} = 22$ µF, $V_{CP\_EN} = 1.8$ V, $V_{BIAS} = 0$ V, $V_{IN} = 5.6$ V, $V_{OUT} = 5.2$ V

图 6-108. Output Voltage Accuracy vs I_{OUT} for $V_{IN} = 5.6$ V, CP Enabled

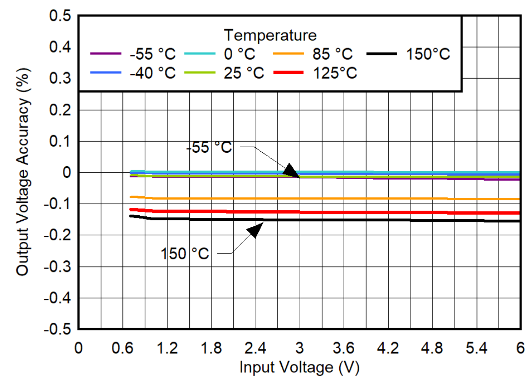
6.6 Typical Characteristics (continued)

$V_{IN} = V_{OUT(NOM)} + 0.4$ V, $V_{EN} = 1.8$ V, $V_{CP\_EN} = 1.8$ V, $C_{IN} = 10$ μF, $C_{NR/SS} = 4.7$ μF, $C_{OUT} = 22$ μF, $C_{BIAS} = 0$ nF, SNS pin shorted to OUT pin, and PG pin pulled up to V_{IN} with 100 kΩ (unless otherwise noted); typical values are at $T_J = 25°C$



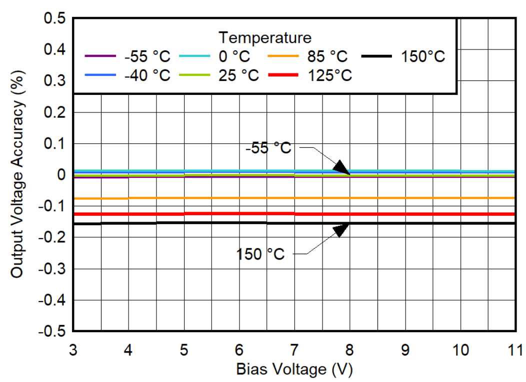
$C_{NR/SS} = C_{IN} = 4.7$ μF, $C_{OUT} = 22$ μF, $V_{CP\_EN} = 1.8$ V, $V_{BIAS} = 11$ V, $V_{OUT} = 0.5$ V, $I_{OUT} = 0$ A

图 6-109. Output Voltage Accuracy vs V_{IN} for V_{BIAS} = 11 V, CP Enabled



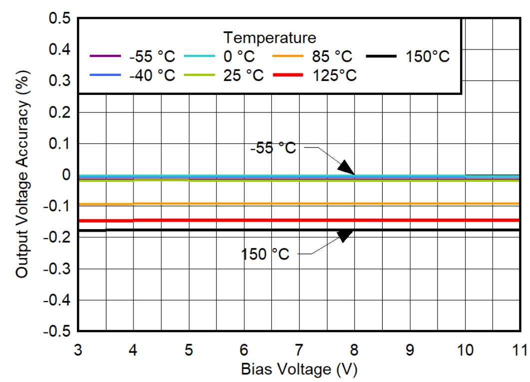
$C_{NR/SS} = C_{IN} = 4.7$ μF, $C_{OUT} = 22$ μF, $V_{CP\_EN} = 1.8$ V, $V_{BIAS} = 3$ V, $V_{OUT} = 0.5$ V, $I_{OUT} = 0$ A

图 6-110. Output Voltage Accuracy vs V_{IN} for V_{BIAS} = 3 V, CP Enabled



$C_{NR/SS} = C_{IN} = 4.7$ μF, $C_{OUT} = 22$ μF, $V_{CP\_EN} = 1.8$ V, $V_{IN} = 6$ V, $V_{OUT} = 0.5$ V, $I_{OUT} = 0$ A

图 6-111. Output Voltage Accuracy vs V_{BIAS} for V_{IN} = 6 V, CP Enabled

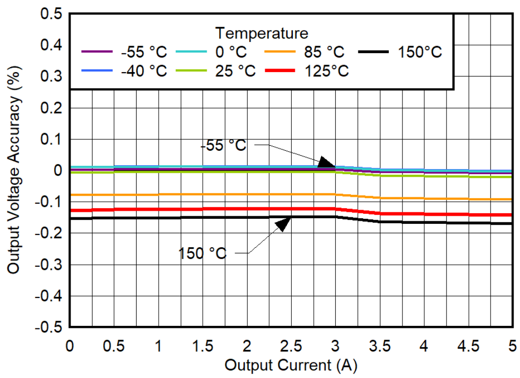


$C_{NR/SS} = C_{IN} = 4.7$ μF, $C_{OUT} = 22$ μF, $V_{CP\_EN} = 1.8$ V, $V_{IN} = 0.7$ V, $V_{OUT} = 0.5$ V, $I_{OUT} = 0$ A

图 6-112. Output Voltage Accuracy vs V_{BIAS} for V_{IN} = 0.7 V, CP Enabled

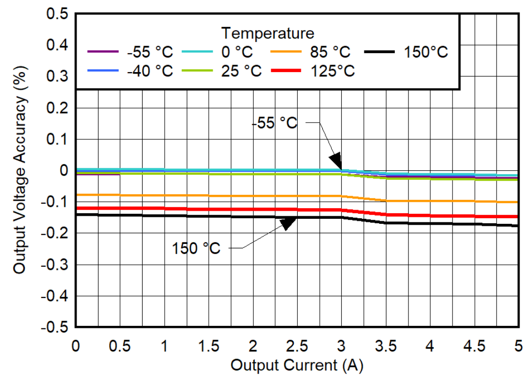
6.6 Typical Characteristics (continued)

$V_{IN} = V_{OUT(NOM)} + 0.4$ V, $V_{EN} = 1.8$ V, $V_{CP\_EN} = 1.8$ V, $C_{IN} = 10$ μF, $C_{NR/SS} = 4.7$ μF, $C_{OUT} = 22$ μF, $C_{BIAS} = 0$ nF, SNS pin shorted to OUT pin, and PG pin pulled up to V_{IN} with 100 kΩ (unless otherwise noted); typical values are at $T_J = 25°C$



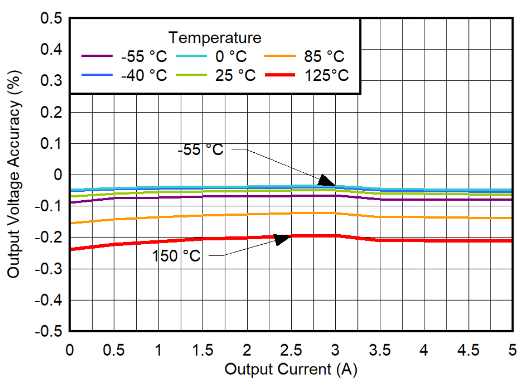
$C_{NR/SS} = C_{IN} = 4.7$ μF, $C_{OUT} = 22$ μF, $V_{CP\_EN} = 1.8$ V, $V_{BIAS} = 11$ V, $V_{IN} = 0.7$ V, $V_{OUT} = 0.5$ V

图 6-113. Output Voltage Accuracy vs I_{OUT} for $V_{OUT} = 0.5$ V, $V_{BIAS} = 11$ V, CP Enabled



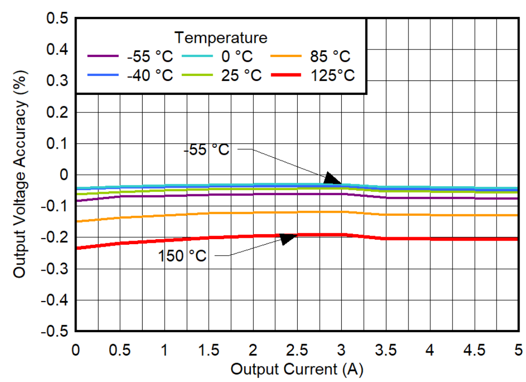
$C_{NR/SS} = C_{IN} = 4.7$ μF, $C_{OUT} = 22$ μF, $V_{CP\_EN} = 1.8$ V, $V_{BIAS} = 11$ V, $V_{IN} = 0.7$ V, $V_{OUT} = 0.5$ V

图 6-114. Output Voltage Accuracy vs I_{OUT} for $V_{OUT} = 0.5$ V, $V_{BIAS} = 3$ V, CP Enabled



$C_{NR/SS} = C_{IN} = 4.7$ μF, $C_{OUT} = 22$ μF, $V_{CP\_EN} = 1.8$ V, $V_{BIAS} = 11$ V, $V_{IN} = 6$ V, $V_{OUT} = 5.2$ V

图 6-115. Output Voltage Accuracy vs I_{OUT} for $V_{IN} = 6$ V, $V_{BIAS} = 11$ V, CP Enabled

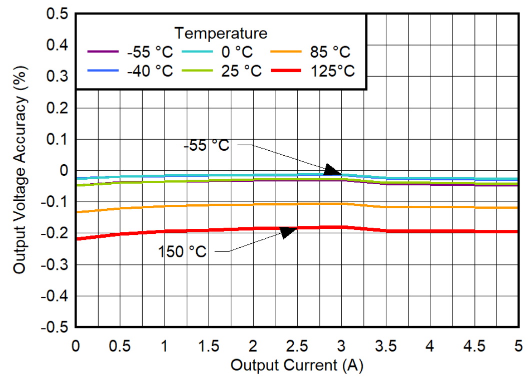


$C_{NR/SS} = C_{IN} = 4.7$ μF, $C_{OUT} = 22$ μF, $V_{CP\_EN} = 1.8$ V, $V_{BIAS} = 3$ V, $V_{IN} = 6$ V, $V_{OUT} = 5.2$ V

图 6-116. Output Voltage Accuracy vs I_{OUT} for $V_{IN} = 6$ V, $V_{BIAS} = 3$ V, CP Enabled

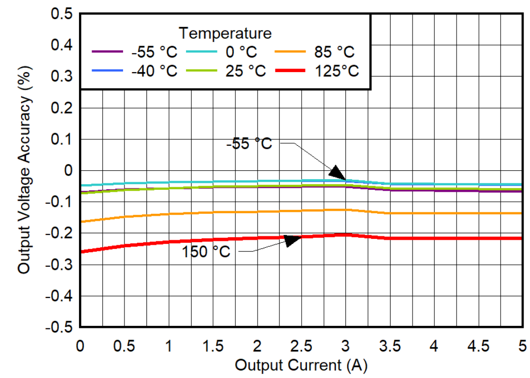
6.6 Typical Characteristics (continued)

V_{IN} = $V_{OUT(NOM)}$ + 0.4 V, V_{EN} = 1.8 V, V_{CP_EN} = 1.8 V, C_{IN} = 10 µF, $C_{NR/SS}$ = 4.7 µF, C_{OUT} = 22 µF, C_{BIAS} = 0 nF, SNS pin shorted to OUT pin, and PG pin pulled up to V_{IN} with 100 kΩ (unless otherwise noted); typical values are at T_J = 25°C



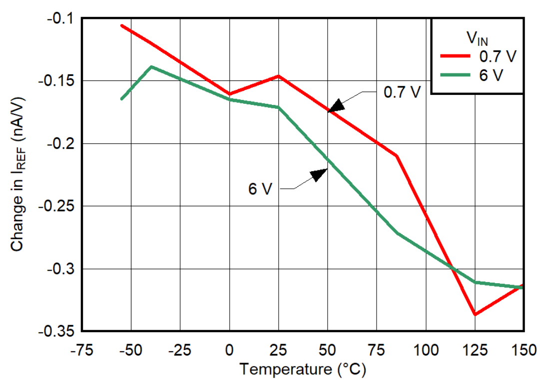
$C_{NR/SS}$ = C_{IN} = 4.7 µF, C_{OUT} = 22 µF, V_{CP_EN} = 1.8 V, V_{BIAS} = 11 V, V_{IN} = 5.6 V, V_{OUT} = 5.2 V

图 6-117. Output Voltage Accuracy vs I_{OUT} for V_{IN} = 5.6 V, V_{BIAS} = 11 V, CP Enabled



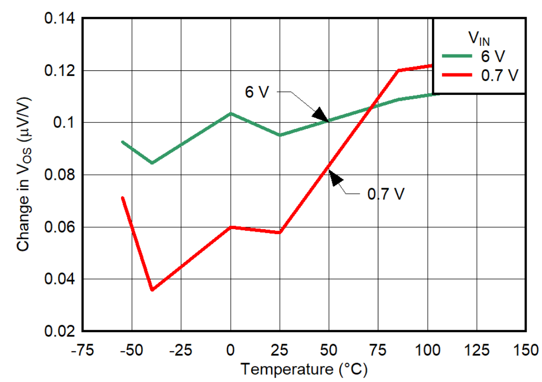
$C_{NR/SS}$ = C_{IN} = 4.7 µF, C_{OUT} = 22 µF, V_{CP_EN} = 1.8 V, V_{BIAS} = 3 V, V_{IN} = 5.6 V, V_{OUT} = 5.2 V

图 6-118. Output Voltage Accuracy vs I_{OUT} for V_{IN} = 5.6 V, V_{BIAS} = 3 V, CP Enabled



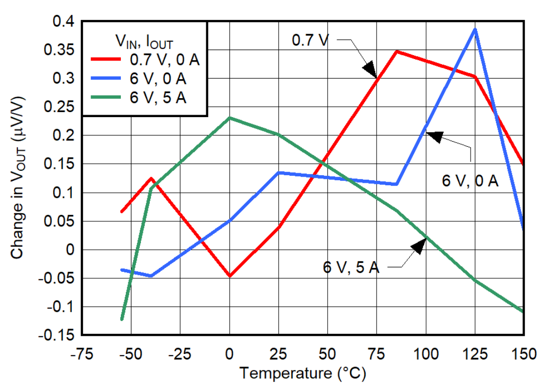
$C_{NR/SS}$ = C_{IN} = 4.7 µF, C_{OUT} = 22 µF, V_{CP_EN} = 0 V, V_{BIAS} = 3.7 V to 11 V, V_{OUT} = 0.5 V

图 6-119. I_{REF} BIAS Rail Line Regulation



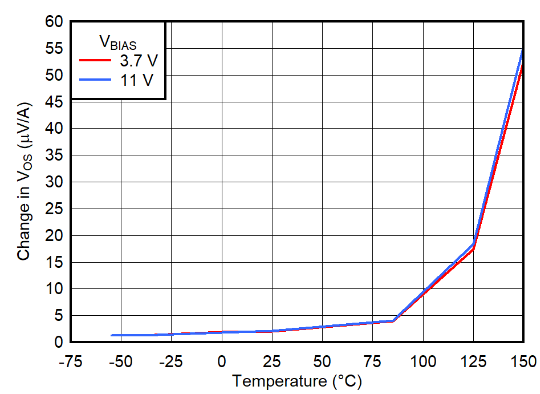
$C_{NR/SS}$ = C_{IN} = 4.7 µF, C_{OUT} = 22 µF, V_{CP_EN} = 0 V, V_{BIAS} = 3.7 V to 11 V, V_{OUT} = 0.5 V

图 6-120. V_{OS} BIAS Rail Line Regulation



$C_{NR/SS}$ = C_{IN} = 4.7 µF, C_{OUT} = 22 µF, V_{CP_EN} = 0 V, V_{BIAS} = 3.7 V to 11 V, V_{OUT} = 0.5 V

图 6-121. V_{OUT} BIAS Rail Line Regulation

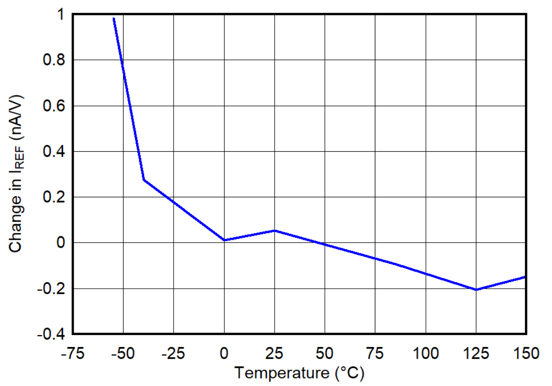


$C_{NR/SS}$ = C_{IN} = 4.7 µF, C_{OUT} = 22 µF, V_{CP_EN} = 0 V, V_{IN} = 0.7 V, V_{OUT} = 0.5 V

图 6-122. V_{OS} Load Regulation

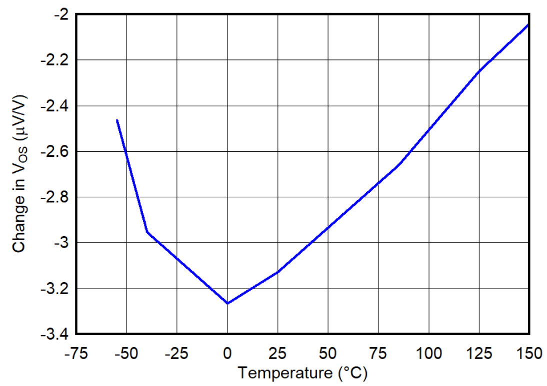
6.6 Typical Characteristics (continued)

$V_{IN} = V_{OUT(NOM)} + 0.4$ V, $V_{EN} = 1.8$ V, $V_{CP\_EN} = 1.8$ V, $C_{IN} = 10$ μF, $C_{NR/SS} = 4.7$ μF, $C_{OUT} = 22$ μF, $C_{BIAS} = 0$ nF, SNS pin shorted to OUT pin, and PG pin pulled up to V_{IN} with 100 kΩ (unless otherwise noted); typical values are at $T_J = 25°C$



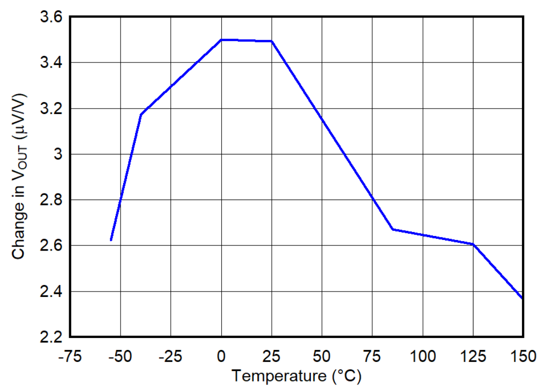
$C_{NR/SS} = C_{IN} = 4.7$ μF, $C_{OUT} = 22$ μF, $V_{CP\_EN} = 1.8$ V, $V_{IN} = 1.1$ V to 6 V, $V_{OUT} = 0.5$ V, $I_{OUT} = 0$ A

图 6-123. I_{REF} IN Rail Line Regulation



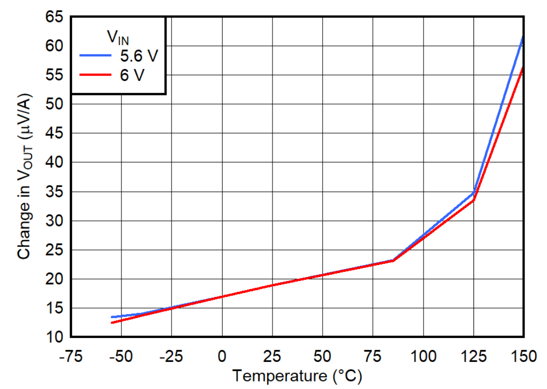
$C_{NR/SS} = C_{IN} = 4.7$ μF, $C_{OUT} = 22$ μF, $V_{CP\_EN} = 1.8$ V, $V_{IN} = 1.1$ V to 6 V, $V_{OUT} = 0.5$ V, $I_{OUT} = 0$ A

图 6-124. V_{OS} IN Rail Line Regulation



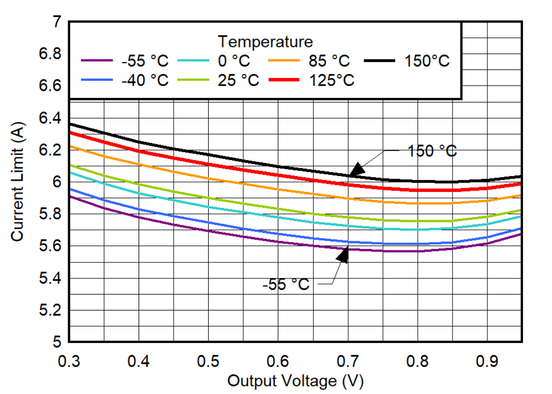
$C_{NR/SS} = C_{IN} = 4.7$ μF, $C_{OUT} = 22$ μF, $V_{CP\_EN} = 1.8$ V, $V_{IN} = 1.1$ V to 6 V, $V_{OUT} = 0.5$ V, $I_{OUT} = 0$ A

图 6-125. V_{OUT} IN Rail Line Regulation



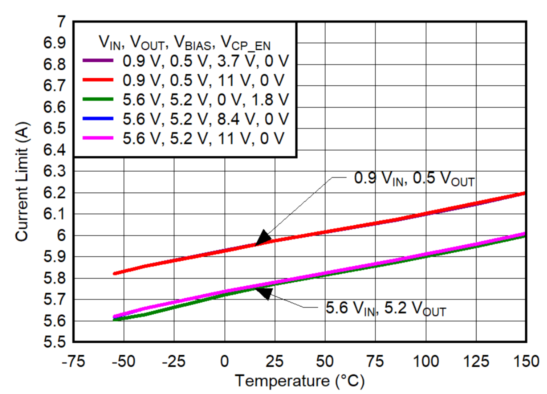
$C_{NR/SS} = C_{IN} = 4.7$ μF, $C_{OUT} = 22$ μF, $V_{CP\_EN} = 1.8$ V, $V_{BIAS} = 0$ V, $V_{OUT} = 5.2$ V, $I_{OUT} = 0$ A to 5 A

图 6-126. V_{OUT} Load Regulation



$C_{NR/SS} = C_{IN} = 4.7$ μF, $C_{OUT} = 22$ μF, $V_{CP\_EN} = 0$ V, $V_{BIAS} = 8.4$ V, $V_{IN} = 5.6$ V, $V_{OUT(nom)} = 5.2$ V

图 6-127. I_{LIMIT} vs V_{OUT}

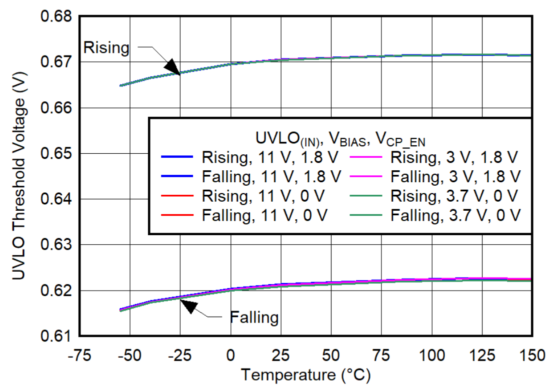


$C_{NR/SS} = C_{IN} = 4.7$ μF, $C_{OUT} = 22$ μF

图 6-128. I_{LIMIT} vs Temperature

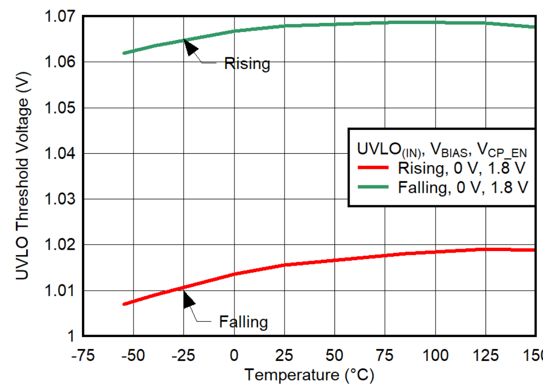
6.6 Typical Characteristics (continued)

$V_{IN} = V_{OUT(NOM)} + 0.4$ V, $V_{EN} = 1.8$ V, $V_{CP\_EN} = 1.8$ V, $C_{IN} = 10$ µF, $C_{NR/SS} = 4.7$ µF, $C_{OUT} = 22$ µF, $C_{BIAS} = 0$ nF, SNS pin shorted to OUT pin, and PG pin pulled up to V_{IN} with 100 kΩ (unless otherwise noted); typical values are at $T_J = 25°C$



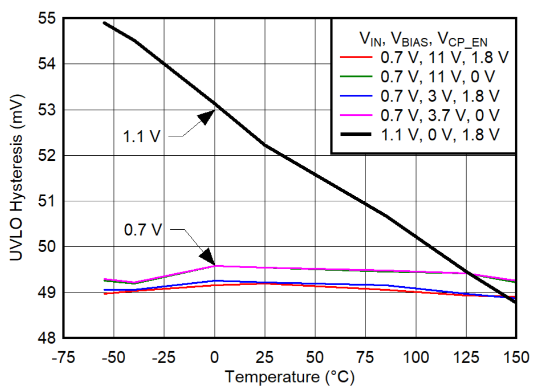
$C_{NR/SS} = C_{IN} = 4.7$ µF, $C_{OUT} = 22$ µF, $V_{OUT} = 0.5$ V

图 6-129. UVLO$_{IN}$ Threshold vs Temperature With BIAS Rail



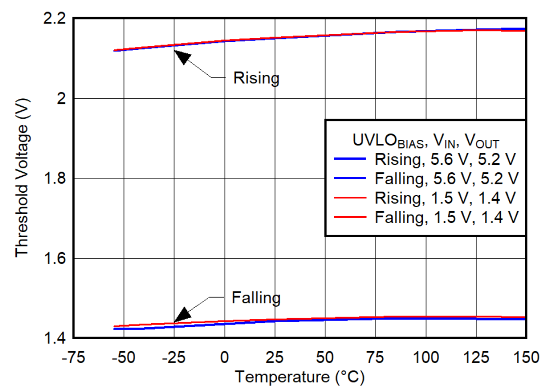
$C_{NR/SS} = C_{IN} = 4.7$ µF, $C_{OUT} = 22$ µF, $V_{OUT} = 0.5$ V

图 6-130. UVLO$_{IN}$ Threshold vs Temperature Without BIAS Rail



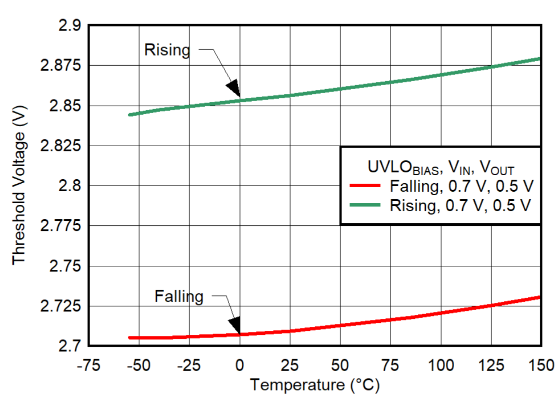
$C_{NR/SS} = C_{IN} = 4.7$ µF, $C_{OUT} = 22$ µF, $V_{OUT} = 0.5$ V

图 6-131. UVLO$_{IN}$ Hysteresis vs Temperature



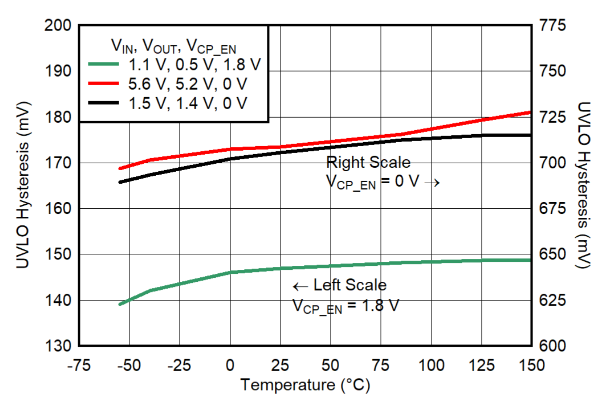
$C_{NR/SS} = C_{IN} = 4.7$ µF, $C_{OUT} = 22$ µF

图 6-132. UVLO$_{BIAS}$ Threshold vs Temperature for CP Disabled



$C_{NR/SS} = C_{IN} = 4.7$ µF, $C_{OUT} = 22$ µF

图 6-133. UVLO$_{BIAS}$ Threshold vs Temperature for CP Enabled

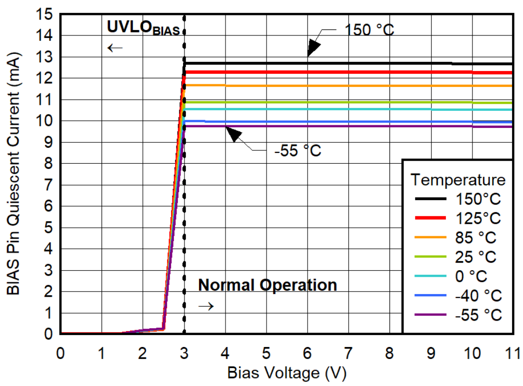


$C_{NR/SS} = C_{IN} = 4.7$ µF, $C_{OUT} = 22$ µF, $V_{OUT} = 0.5$ V

图 6-134. UVLO$_{IN}$ Hysteresis vs Temperature

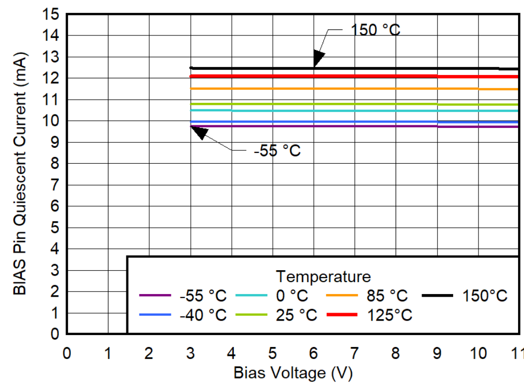
6.6 Typical Characteristics (continued)

$V_{IN} = V_{OUT(NOM)} + 0.4$ V, $V_{EN} = 1.8$ V, $V_{CP\_EN} = 1.8$ V, $C_{IN} = 10$ μF, $C_{NR/SS} = 4.7$ μF, $C_{OUT} = 22$ μF, $C_{BIAS} = 0$ nF, SNS pin shorted to OUT pin, and PG pin pulled up to V_{IN} with 100 kΩ (unless otherwise noted); typical values are at $T_J = 25°C$



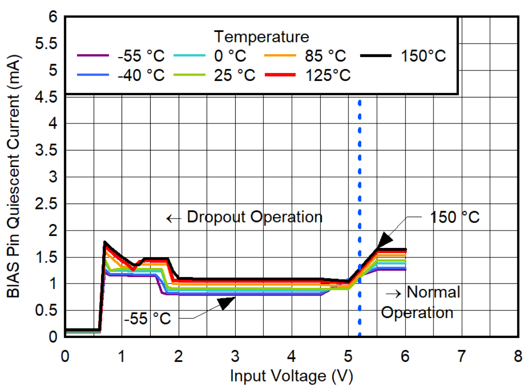
$C_{NR/SS} = C_{IN} = 4.7$ μF, $C_{OUT} = 22$ μF

图 6-135. BIAS Pin Quiescent Current vs V_{BIAS} for $V_{OUT} = 0.5$ V, CP Enabled, $I_{OUT} = 0$ A



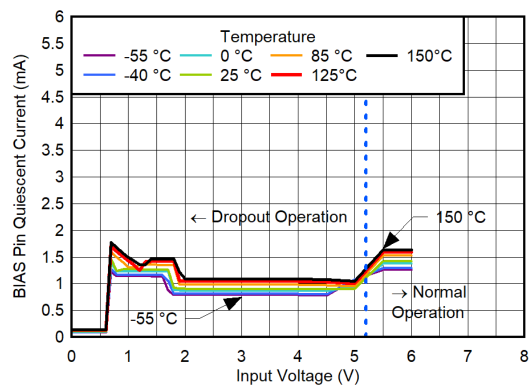
$C_{NR/SS} = C_{IN} = 4.7$ μF, $C_{OUT} = 22$ μF

图 6-136. BIAS Pin Quiescent Current vs V_{BIAS} for $V_{OUT} = 0.5$ V, CP Enabled, $I_{OUT} = 5$ A



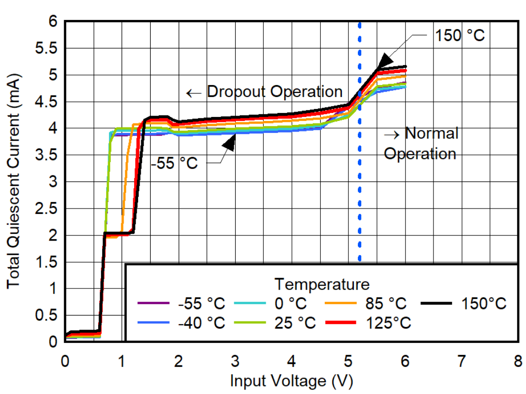
$C_{NR/SS} = C_{IN} = 4.7$ μF, $C_{OUT} = 22$ μF

图 6-137. BIAS Pin Quiescent Current vs V_{IN} for $V_{OUT} = 5.2$ V, $V_{BIAS} = 11$ V, CP Disabled



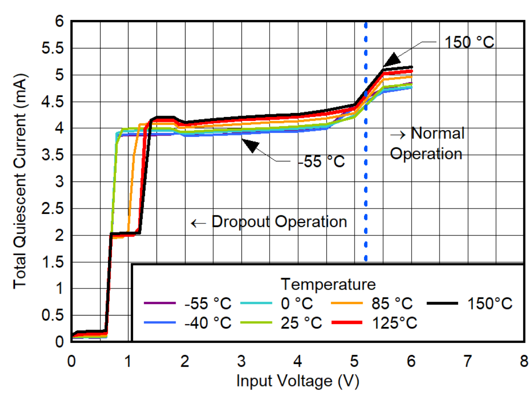
$C_{NR/SS} = C_{IN} = 4.7$ μF, $C_{OUT} = 22$ μF

图 6-138. BIAS Pin Quiescent Current vs V_{IN} for $V_{OUT} = 5.2$ V, $V_{BIAS} = 8.4$ V, CP Disabled



$C_{NR/SS} = C_{IN} = 4.7$ μF, $C_{OUT} = 22$ μF

图 6-139. Total BIAS Pin Quiescent Current vs V_{IN} for $V_{OUT} = 5.2$ V, $V_{BIAS} = 11$ V, CP Disabled

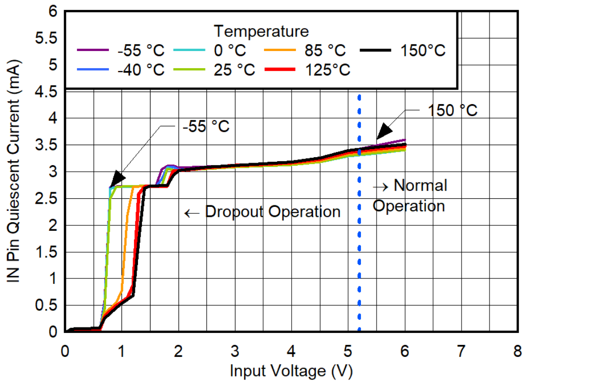


$C_{NR/SS} = C_{IN} = 4.7$ μF, $C_{OUT} = 22$ μF

图 6-140. Total Quiescent Current vs V_{IN} for $V_{OUT} = 5.2$ V, $V_{BIAS} = 8.4$ V, CP Disabled

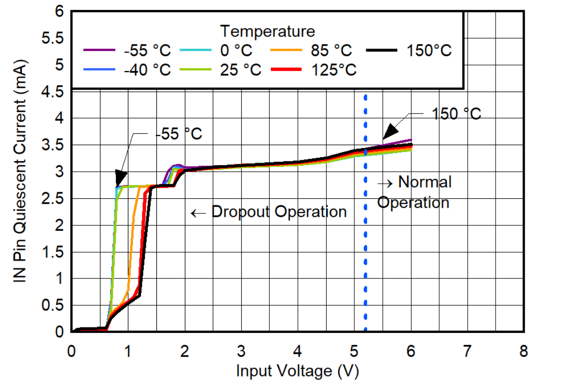
6.6 Typical Characteristics (continued)

V_{IN} = $V_{OUT(NOM)}$ + 0.4 V, V_{EN} = 1.8 V, V_{CP_EN} = 1.8 V, C_{IN} = 10 μF, $C_{NR/SS}$ = 4.7 μF, C_{OUT} = 22 μF, C_{BIAS} = 0 nF, SNS pin shorted to OUT pin, and PG pin pulled up to V_{IN} with 100 kΩ (unless otherwise noted); typical values are at T_J = 25°C



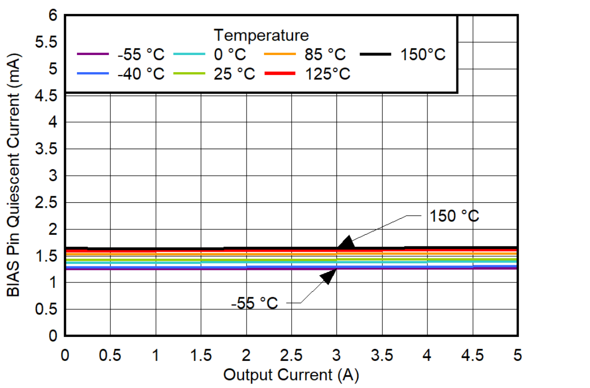
$C_{NR/SS}$ = C_{IN} = 4.7 μF, C_{OUT} = 22 μF

图 6-141. IN Pin Quiescent Current vs V_{IN} for V_{OUT} = 5.2 V, V_{BIAS} = 11 V, CP Disabled



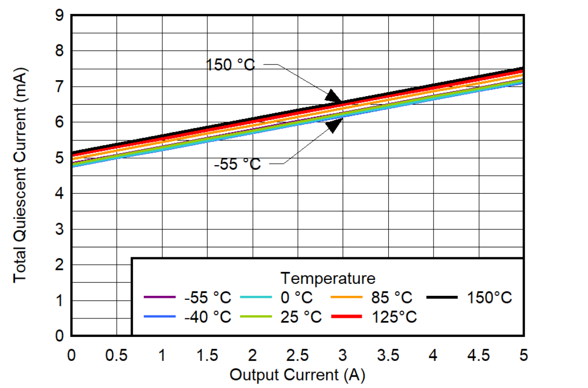
$C_{NR/SS}$ = C_{IN} = 4.7 μF, C_{OUT} = 22 μF

图 6-142. IN Pin Quiescent Current vs V_{IN} for V_{OUT} = 5.2 V, V_{BIAS} = 8.4 V, CP Disabled



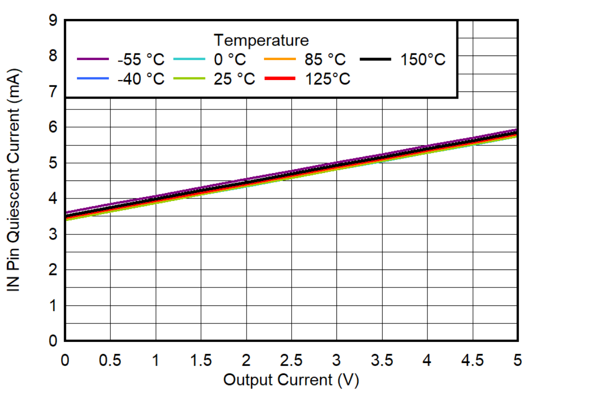
$C_{NR/SS}$ = C_{IN} = 4.7 μF, C_{OUT} = 22 μF, V_{IN} = 6 V

图 6-143. BIAS Pin Quiescent Current vs I_{OUT} for V_{OUT} = 5.2 V, V_{BIAS} = 11 V, CP Disabled



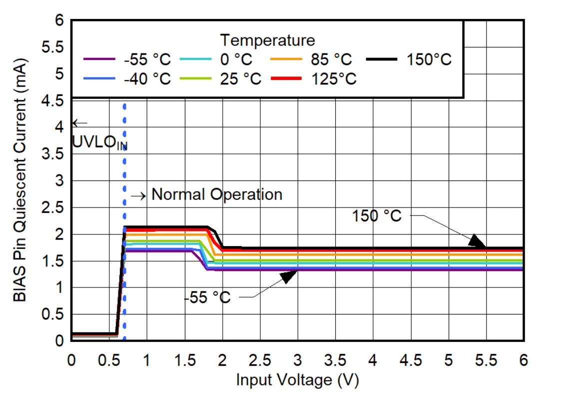
$C_{NR/SS}$ = C_{IN} = 4.7 μF, C_{OUT} = 22 μF, V_{IN} = 6 V

图 6-144. Total Quiescent Current vs I_{OUT} for V_{OUT} = 5.2 V, V_{BIAS} = 11 V, CP Disabled



$C_{NR/SS}$ = C_{IN} = 4.7 μF, C_{OUT} = 22 μF, V_{IN} = 6 V

图 6-145. IN Pin Quiescent Current vs I_{OUT} for V_{OUT} = 5.2 V, V_{BIAS} = 11 V, CP Disabled

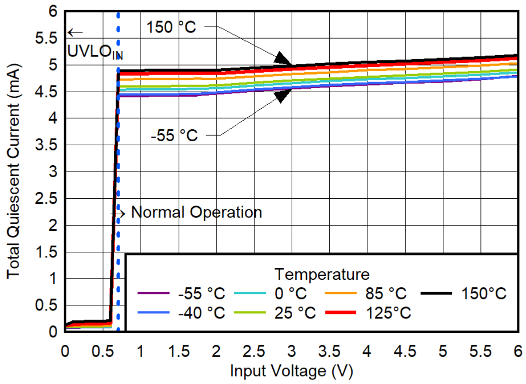


$C_{NR/SS}$ = C_{IN} = 4.7 μF, C_{OUT} = 22 μF

图 6-146. BIAS Pin Current vs V_{IN} for V_{OUT} = 0.5 V, V_{BIAS} = 11 V, CP Disabled

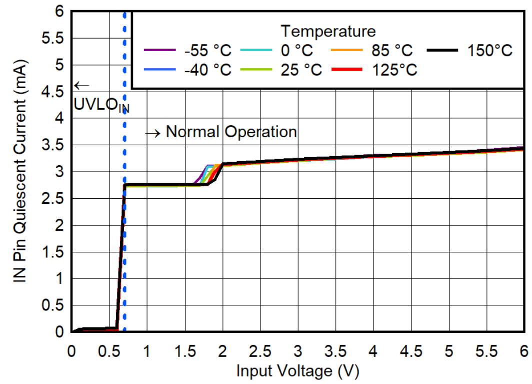
6.6 Typical Characteristics (continued)

$V_{IN} = V_{OUT(NOM)} + 0.4$ V, $V_{EN} = 1.8$ V, $V_{CP\_EN} = 1.8$ V, $C_{IN} = 10$ µF, $C_{NR/SS} = 4.7$ µF, $C_{OUT} = 22$ µF, $C_{BIAS} = 0$ nF, SNS pin shorted to OUT pin, and PG pin pulled up to V_{IN} with 100 kΩ (unless otherwise noted); typical values are at $T_J = 25°C$



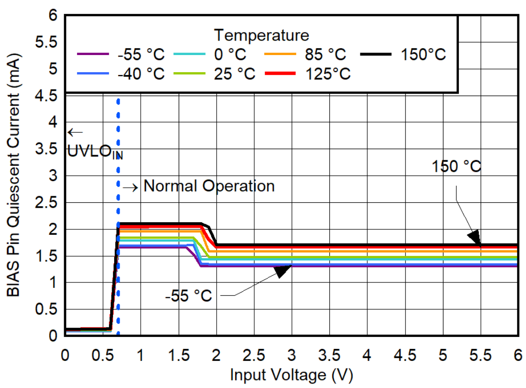
$C_{NR/SS} = C_{IN} = 4.7$ µF, $C_{OUT} = 22$ µF

图 6-147. Total Quiescent Current vs V_{IN} for V_{OUT} = 0.5 V, V_{BIAS} = 11 V, CP Disabled



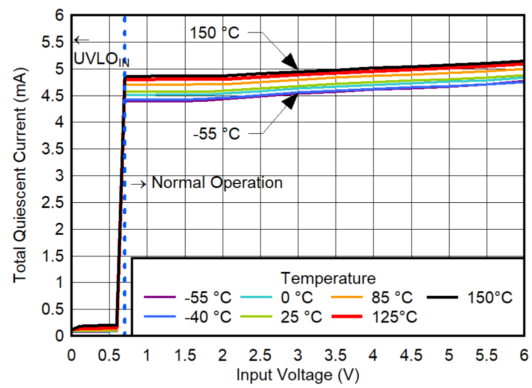
$C_{NR/SS} = C_{IN} = 4.7$ µF, $C_{OUT} = 22$ µF

图 6-148. IN Pin Quiescent Current vs V_{IN} for V_{OUT} = 0.5 V, V_{BIAS} = 11 V, CP Disabled



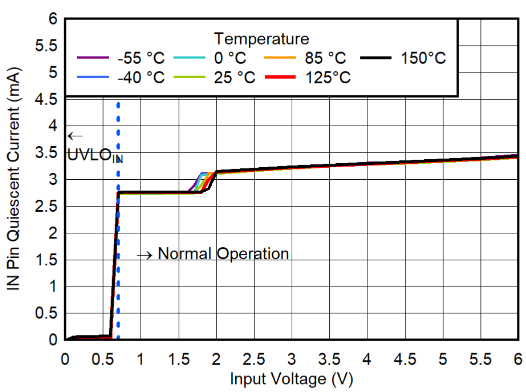
$C_{NR/SS} = C_{IN} = 4.7$ µF, $C_{OUT} = 22$ µF

图 6-149. BIAS Pin Quiescent Current vs V_{IN} for V_{OUT} = 0.5 V, V_{BIAS} = 3.7 V, CP Disabled



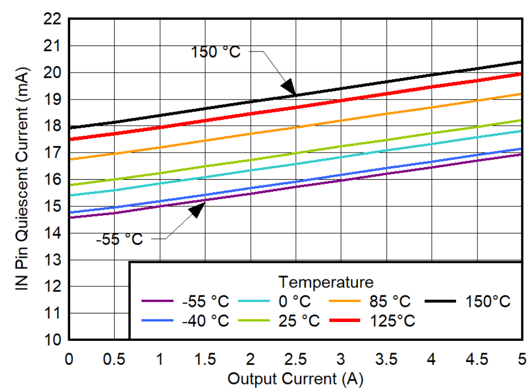
$C_{NR/SS} = C_{IN} = 4.7$ µF, $C_{OUT} = 22$ µF

图 6-150. Total Pin Quiescent Current vs V_{IN} for V_{OUT} = 0.5 V, V_{BIAS} = 3.7 V, CP Disabled



$C_{NR/SS} = C_{IN} = 4.7$ µF, $C_{OUT} = 22$ µF

图 6-151. IN Pin Quiescent Current vs V_{IN} for V_{OUT} = 0.5 V, V_{BIAS} = 3.7 V, CP Disabled

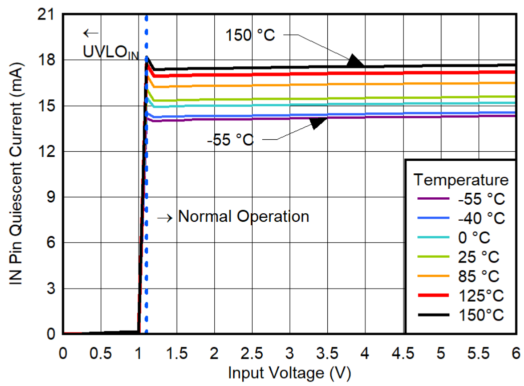


$C_{NR/SS} = C_{IN} = 4.7$ µF, $C_{OUT} = 22$ µF, $V_{IN} = 6$ V

图 6-152. IN Pin Quiescent Current vs I_{OUT} for V_{OUT} = 5.2 V, CP Enabled

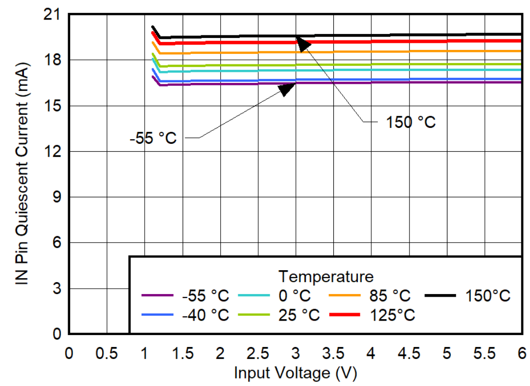
6.6 Typical Characteristics (continued)

$V_{IN} = V_{OUT(NOM)} + 0.4$ V, $V_{EN} = 1.8$ V, $V_{CP\_EN} = 1.8$ V, $C_{IN} = 10$ µF, $C_{NR/SS} = 4.7$ µF, $C_{OUT} = 22$ µF, $C_{BIAS} = 0$ nF, SNS pin shorted to OUT pin, and PG pin pulled up to V_{IN} with 100 kΩ (unless otherwise noted); typical values are at $T_J = 25°C$



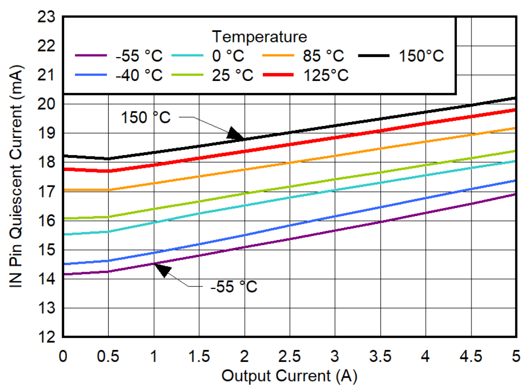
$C_{NR/SS} = C_{IN} = 4.7$ µF, $C_{OUT} = 22$ µF

图 6-153. BIAS Pin Quiescent Current vs V_{IN} for $V_{OUT} = 0.5$ V, No BIAS, CP Enabled, $I_{OUT} = 0$ A



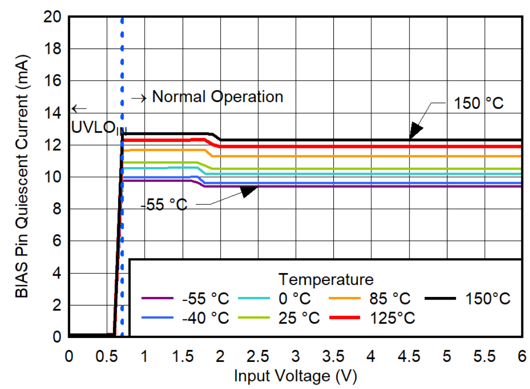
$C_{NR/SS} = C_{IN} = 4.7$ µF, $C_{OUT} = 22$ µF

图 6-154. BIAS Pin Quiescent Current vs V_{IN} for $V_{OUT} = 0.5$ V, No BIAS, CP Enabled, $I_{OUT} = 5$ A



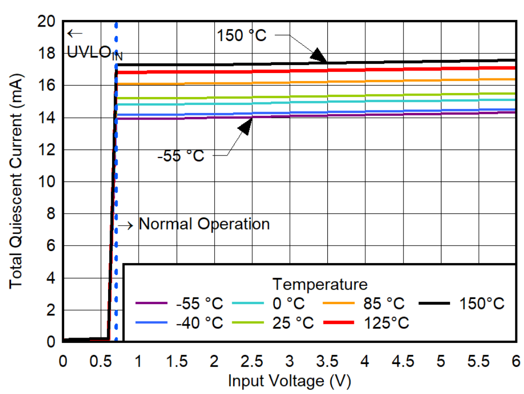
$C_{NR/SS} = C_{IN} = 4.7$ µF, $C_{OUT} = 22$ µF, $V_{IN} = 1.1$ V

图 6-155. IN Pin Quiescent Current vs I_{OUT} for $V_{OUT} = 0.5$ V, No BIAS, CP Enabled, $I_{OUT} = 0$ A



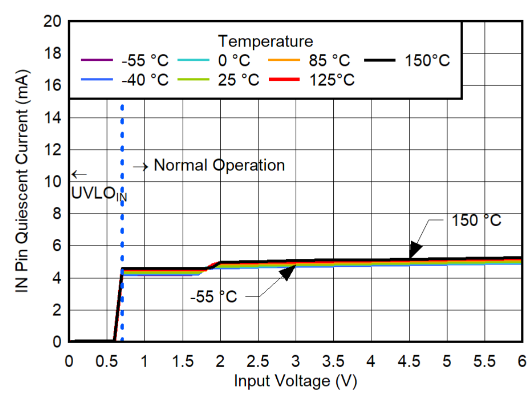
$C_{NR/SS} = C_{IN} = 4.7$ µF, $C_{OUT} = 22$ µF

图 6-156. BIAS Pin Quiescent Current vs V_{IN} for $V_{OUT} = 0.5$ V, $V_{BIAS} = 3$ V, CP Enabled, $I_{OUT} = 0$ A



$C_{NR/SS} = C_{IN} = 4.7$ µF, $C_{OUT} = 22$ µF

图 6-157. Total Quiescent Current vs V_{IN} for $V_{OUT} = 0.5$ V, $V_{BIAS} = 3$ V, CP Enabled, $I_{OUT} = 0$ A

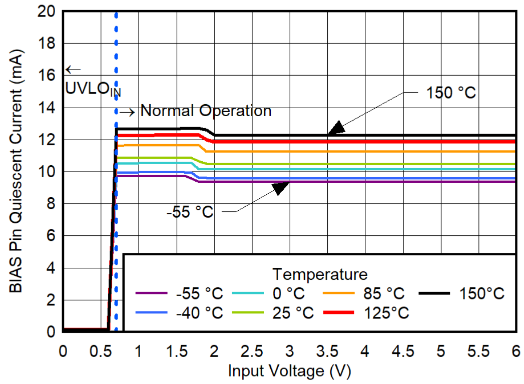


$C_{NR/SS} = C_{IN} = 4.7$ µF, $C_{OUT} = 22$ µF

图 6-158. IN Pin Quiescent Current vs V_{IN} for $V_{OUT} = 0.5$ V, $V_{BIAS} = 3$ V, CP Enabled, $I_{OUT} = 0$ A

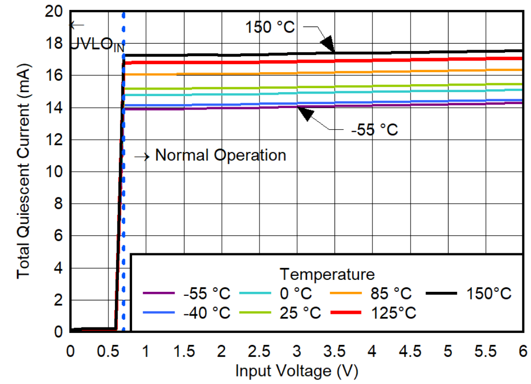
6.6 Typical Characteristics (continued)

$V_{IN} = V_{OUT(NOM)} + 0.4$ V, $V_{EN} = 1.8$ V, $V_{CP\_EN} = 1.8$ V, $C_{IN} = 10$ µF, $C_{NR/SS} = 4.7$ µF, $C_{OUT} = 22$ µF, $C_{BIAS} = 0$ nF, SNS pin shorted to OUT pin, and PG pin pulled up to V_{IN} with 100 kΩ (unless otherwise noted); typical values are at $T_J = 25°C$



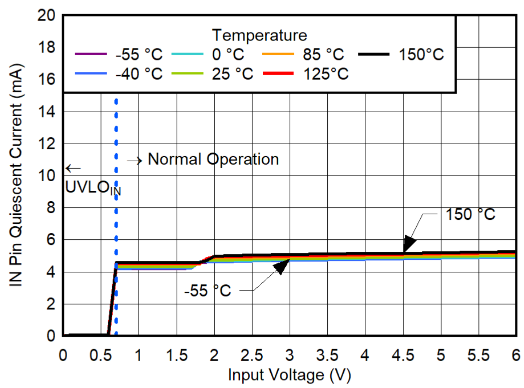
$C_{NR/SS} = C_{IN} = 4.7$ µF, $C_{OUT} = 22$ µF

图 6-159. BIAS Pin Quiescent Current vs V_{IN} for $V_{OUT} = 0.5$ V, $V_{BIAS} = 11$ V, CP Enabled, $I_{OUT} = 0$ A



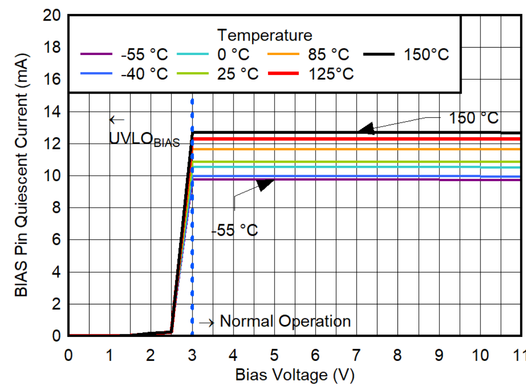
$C_{NR/SS} = C_{IN} = 4.7$ µF, $C_{OUT} = 22$ µF

图 6-160. Total Quiescent Current vs V_{IN} for $V_{OUT} = 0.5$ V, $V_{BIAS} = 11$ V, CP Enabled, $I_{OUT} = 0$ A



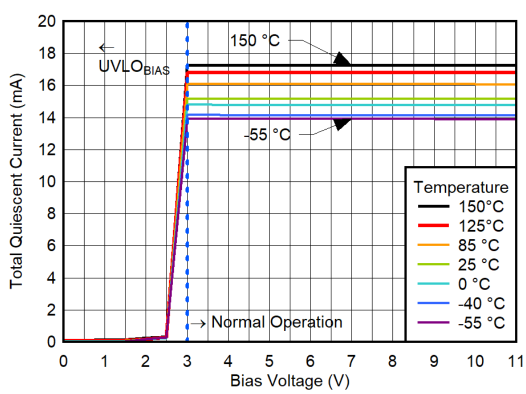
$C_{NR/SS} = C_{IN} = 4.7$ µF, $C_{OUT} = 22$ µF

图 6-161. IN Pin Quiescent Current vs V_{IN} for $V_{OUT} = 0.5$ V, $V_{BIAS} = 11$ V, CP Enabled, $I_{OUT} = 0$ A



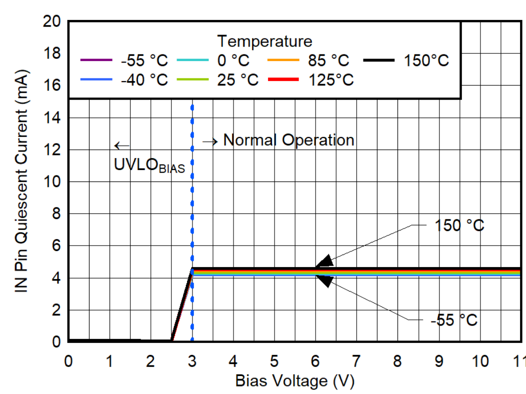
$C_{NR/SS} = C_{IN} = 4.7$ µF, $C_{OUT} = 22$ µF

图 6-162. BIAS Pin Quiescent Current vs V_{BIAS} for $V_{OUT} = 0.5$ V, $V_{IN} = 0.7$ V, CP Enabled, $I_{OUT} = 0$ A



$C_{NR/SS} = C_{IN} = 4.7$ µF, $C_{OUT} = 22$ µF

图 6-163. Total Quiescent Current vs V_{BIAS} for $V_{OUT} = 0.5$ V, $V_{IN} = 0.7$ V, CP Enabled, $I_{OUT} = 0$ A

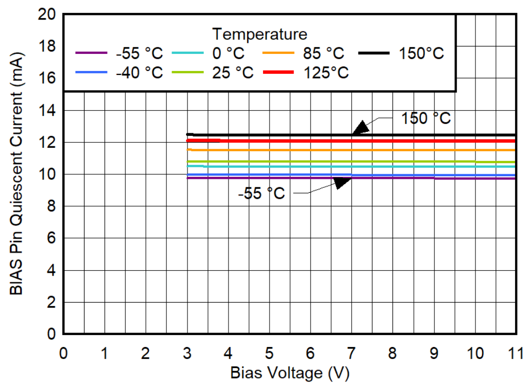


$C_{NR/SS} = C_{IN} = 4.7$ µF, $C_{OUT} = 22$ µF

图 6-164. IN Pin Quiescent Current vs V_{BIAS} for $V_{OUT} = 0.5$ V, $V_{IN} = 0.7$ V, CP Enabled, $I_{OUT} = 0$ A

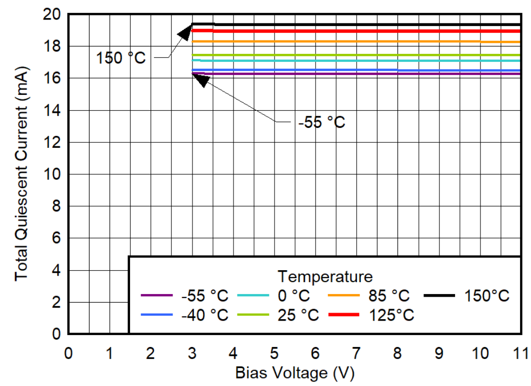
6.6 Typical Characteristics (continued)

V_{IN} = $V_{OUT(NOM)}$ + 0.4 V, V_{EN} = 1.8 V, V_{CP_EN} = 1.8 V, C_{IN} = 10 μF, $C_{NR/SS}$ = 4.7 μF, C_{OUT} = 22 μF, C_{BIAS} = 0 nF, SNS pin shorted to OUT pin, and PG pin pulled up to V_{IN} with 100 kΩ (unless otherwise noted); typical values are at T_J = 25°C



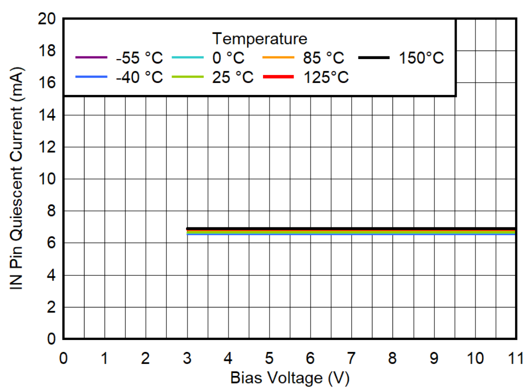
$C_{NR/SS}$ = C_{IN} = 4.7 μF, C_{OUT} = 22 μF

图 6-165. BIAS Pin Quiescent Current vs V_{BIAS} for V_{OUT} = 0.5 V, V_{IN} = 0.7 V, CP Enabled, I_{OUT} = 5 A



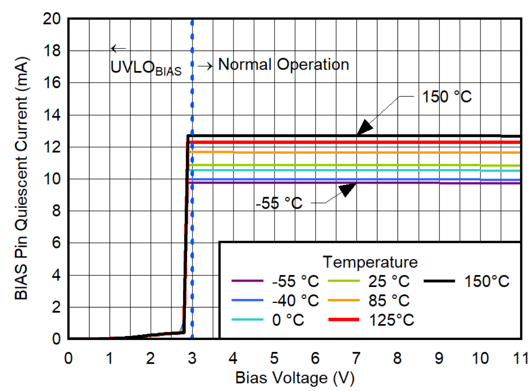
$C_{NR/SS}$ = C_{IN} = 4.7 μF, C_{OUT} = 22 μF

图 6-166. Total Quiescent Current vs V_{BIAS} for V_{OUT} = 0.5 V, V_{IN} = 0.7 V, CP Enabled, I_{OUT} = 5 A



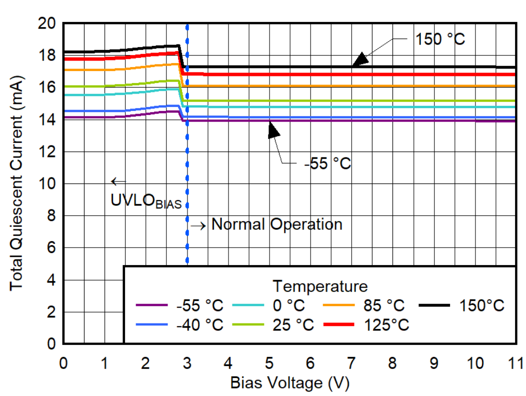
$C_{NR/SS}$ = C_{IN} = 4.7 μF, C_{OUT} = 22 μF

图 6-167. IN Pin Quiescent Current vs V_{BIAS} for V_{OUT} = 0.5 V, V_{IN} = 0.7 V, CP Enabled, I_{OUT} = 5 A



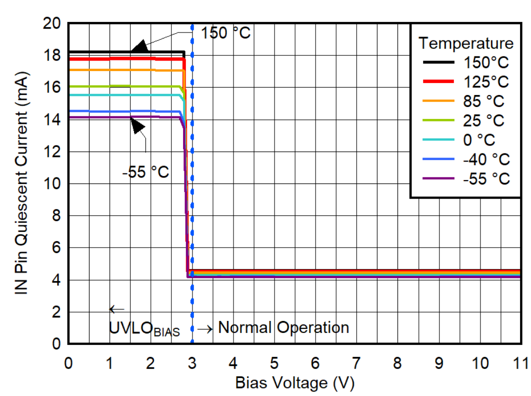
$C_{NR/SS}$ = C_{IN} = 4.7 μF, C_{OUT} = 22 μF

图 6-168. BIAS Pin Quiescent Current vs V_{BIAS} for V_{OUT} = 0.5 V, V_{IN} = 1.1 V, CP Enabled, I_{OUT} = 0 A



$C_{NR/SS}$ = C_{IN} = 4.7 μF, C_{OUT} = 22 μF

图 6-169. Total Quiescent Current vs V_{BIAS} for V_{OUT} = 0.5 V, V_{IN} = 1.1 V, CP Enabled, I_{OUT} = 0 A

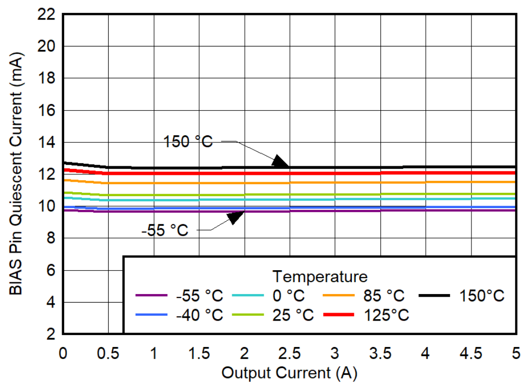


$C_{NR/SS}$ = C_{IN} = 4.7 μF, C_{OUT} = 22 μF

图 6-170. IN Pin Quiescent Current vs Bias Voltage for V_{OUT} = 0.5 V, V_{IN} = 1.1 V, CP Enabled, I_{OUT} = 0 A

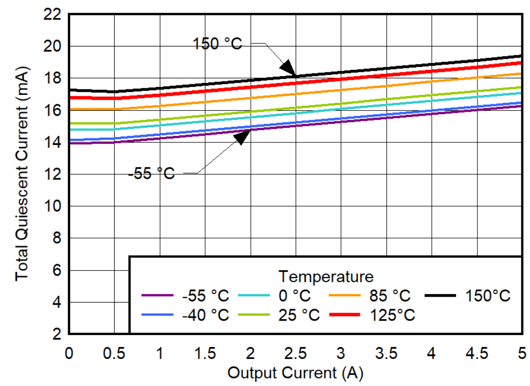
6.6 Typical Characteristics (continued)

V_{IN} = $V_{OUT(NOM)}$ + 0.4 V, V_{EN} = 1.8 V, V_{CP_EN} = 1.8 V, C_{IN} = 10 µF, $C_{NR/SS}$ = 4.7 µF, C_{OUT} = 22 µF, C_{BIAS} = 0 nF, SNS pin shorted to OUT pin, and PG pin pulled up to V_{IN} with 100 kΩ (unless otherwise noted); typical values are at T_J = 25°C



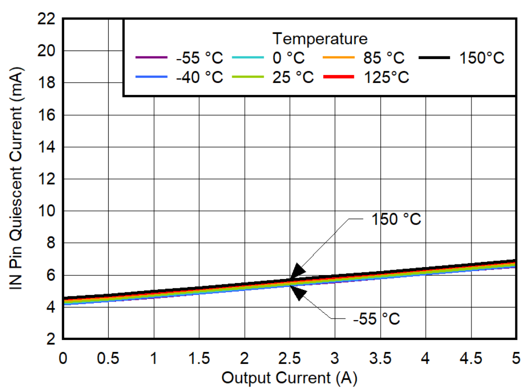
$C_{NR/SS}$ = C_{IN} = 4.7 µF, C_{OUT} = 22 µF

图 6-171. BIAS Pin Quiescent Current vs I_{OUT} for V_{OUT} = 0.5 V, V_{IN} = 0.7 V, V_{BIAS} = 3.7 V, CP Enabled, I_{OUT} = 0 A



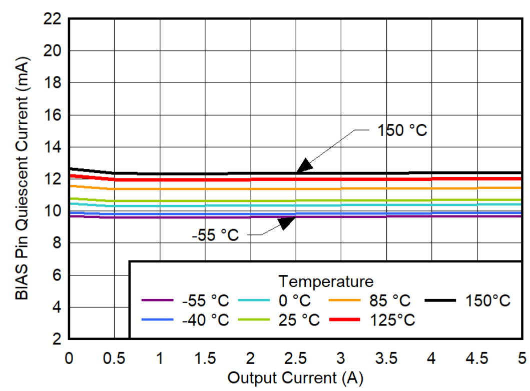
$C_{NR/SS}$ = C_{IN} = 4.7 µF, C_{OUT} = 22 µF

图 6-172. Total Quiescent Current vs I_{OUT} for V_{OUT} = 0.5 V, V_{IN} = 0.7 V, V_{BIAS} = 3.7 V, CP Enabled, I_{OUT} = 0 A



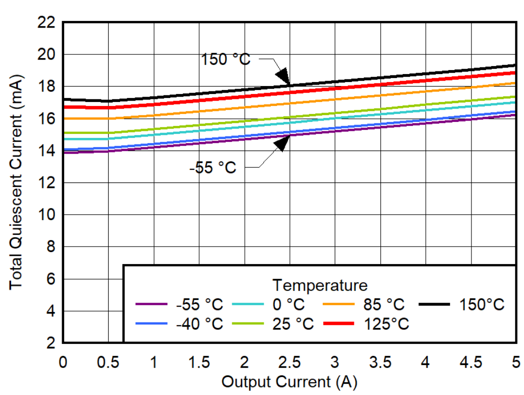
$C_{NR/SS}$ = C_{IN} = 4.7 µF, C_{OUT} = 22 µF

图 6-173. IN Pin Quiescent Current vs I_{OUT} for V_{OUT} = 0.5 V, V_{IN} = 0.7 V, V_{BIAS} = 3.7 V, CP Enabled, I_{OUT} = 0 A



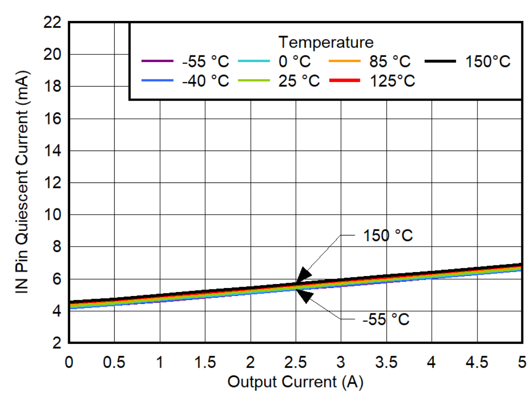
$C_{NR/SS}$ = C_{IN} = 4.7 µF, C_{OUT} = 22 µF

图 6-174. BIAS Pin Quiescent Current vs I_{OUT} for V_{OUT} = 0.5 V, V_{IN} = 0.7 V, V_{BIAS} = 11 V, CP Enabled, I_{OUT} = 0 A



$C_{NR/SS}$ = C_{IN} = 4.7 µF, C_{OUT} = 22 µF

图 6-175. Total Quiescent Current vs I_{OUT} for V_{OUT} = 0.5 V, V_{IN} = 0.7 V, V_{BIAS} = 11 V, CP Enabled, I_{OUT} = 0 A

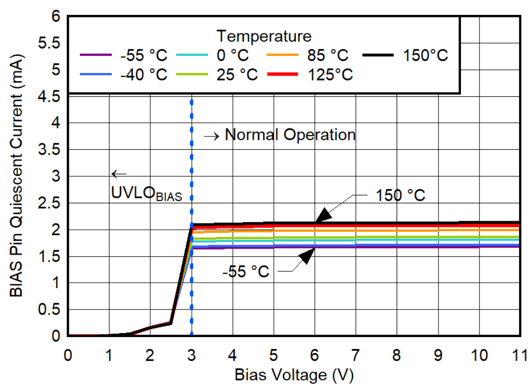


$C_{NR/SS}$ = C_{IN} = 4.7 µF, C_{OUT} = 22 µF

图 6-176. IN Pin Quiescent Current vs I_{OUT} for V_{OUT} = 0.5 V, V_{IN} = 0.7 V, V_{BIAS} = 11 V, CP Enabled, I_{OUT} = 0 A

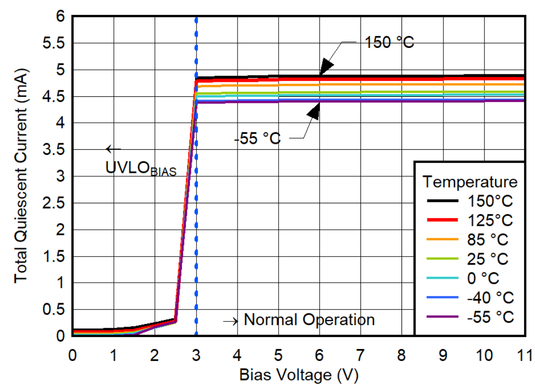
6.6 Typical Characteristics (continued)

V_{IN} = $V_{OUT(NOM)}$ + 0.4 V, V_{EN} = 1.8 V, V_{CP_EN} = 1.8 V, C_{IN} = 10 μF, $C_{NR/SS}$ = 4.7 μF, C_{OUT} = 22 μF, C_{BIAS} = 0 nF, SNS pin shorted to OUT pin, and PG pin pulled up to V_{IN} with 100 kΩ (unless otherwise noted); typical values are at T_J = 25°C



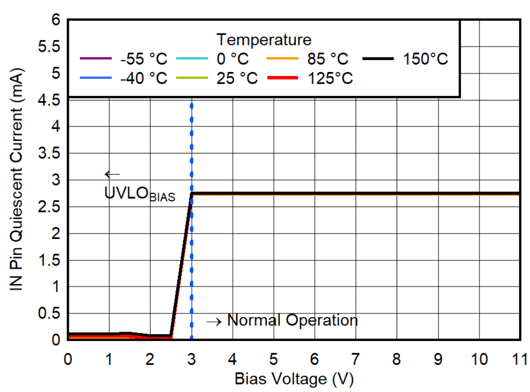
$C_{NR/SS}$ = C_{IN} = 4.7 μF, C_{OUT} = 22 μF

图 6-177. BIAS Pin Quiescent Current vs V_{BIAS} for V_{OUT} = 0.5 V, V_{IN} = 0.7 V, CP Disabled, I_{OUT} = 0 A



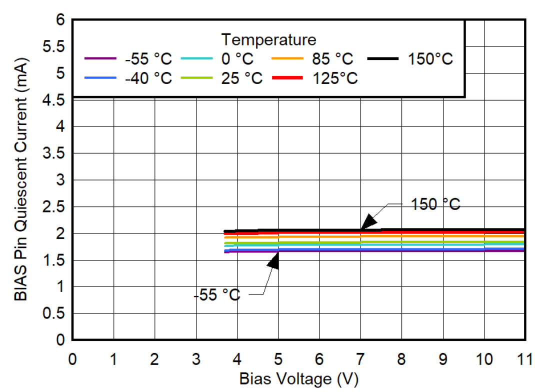
$C_{NR/SS}$ = C_{IN} = 4.7 μF, C_{OUT} = 22 μF

图 6-178. Total Quiescent Current vs V_{BIAS} for V_{OUT} = 0.5 V, V_{IN} = 0.7 V, CP Disabled, I_{OUT} = 0 A



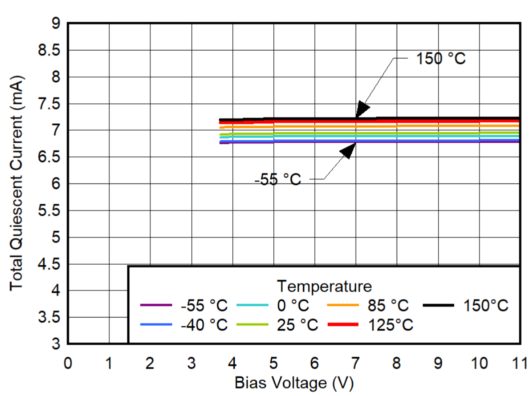
$C_{NR/SS}$ = C_{IN} = 4.7 μF, C_{OUT} = 22 μF

图 6-179. IN Pin Quiescent Current vs V_{BIAS} for V_{OUT} = 0.5 V, V_{IN} = 0.7 V, CP Disabled, I_{OUT} = 0 A



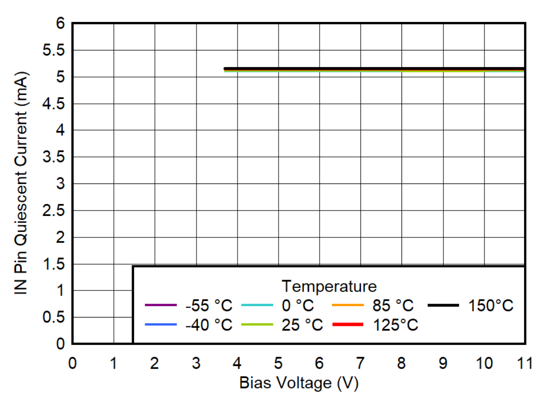
$C_{NR/SS}$ = C_{IN} = 4.7 μF, C_{OUT} = 22 μF

图 6-180. BIAS Pin Quiescent Current vs V_{BIAS} for V_{OUT} = 0.5 V, V_{IN} = 0.7 V, CP Disabled, I_{OUT} = 5 A



$C_{NR/SS}$ = C_{IN} = 4.7 μF, C_{OUT} = 22 μF

图 6-181. Total Quiescent Current vs V_{BIAS} for V_{OUT} = 0.5 V, V_{IN} = 0.7 V, CP Disabled, I_{OUT} = 5 A

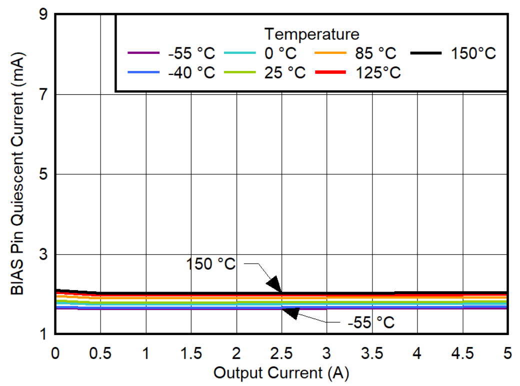


$C_{NR/SS}$ = C_{IN} = 4.7 μF, C_{OUT} = 22 μF

图 6-182. IN Pin Quiescent Current vs V_{BIAS} for V_{OUT} = 0.5 V, V_{IN} = 0.7 V, CP Disabled, I_{OUT} = 5 A

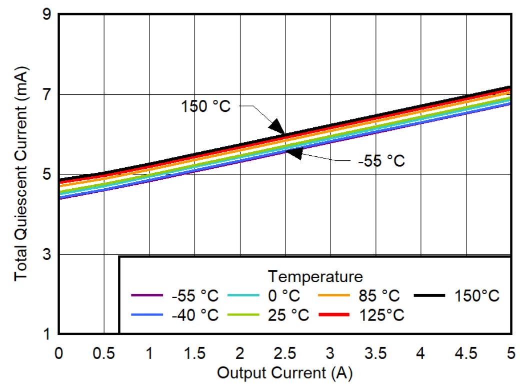
6.6 Typical Characteristics (continued)

V_{IN} = $V_{OUT(NOM)}$ + 0.4 V, V_{EN} = 1.8 V, V_{CP_EN} = 1.8 V, C_{IN} = 10 μF, $C_{NR/SS}$ = 4.7 μF, C_{OUT} = 22 μF, C_{BIAS} = 0 nF, SNS pin shorted to OUT pin, and PG pin pulled up to V_{IN} with 100 kΩ (unless otherwise noted); typical values are at T_J = 25°C



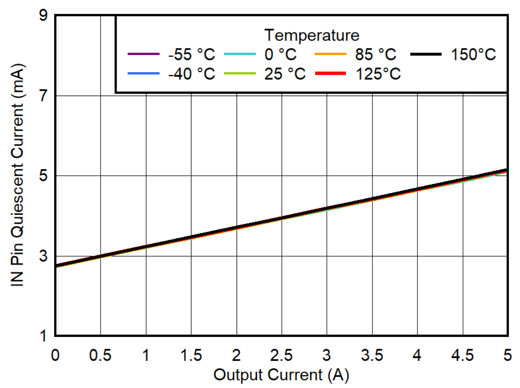
$C_{NR/SS}$ = C_{IN} = 4.7 μF, C_{OUT} = 22 μF

图 6-183. BIAS Pin Quiescent Current vs I_{OUT} for V_{OUT} = 0.5 V, V_{IN} = 0.7 V, V_{BIAS} = 3.7 V, CP Disabled



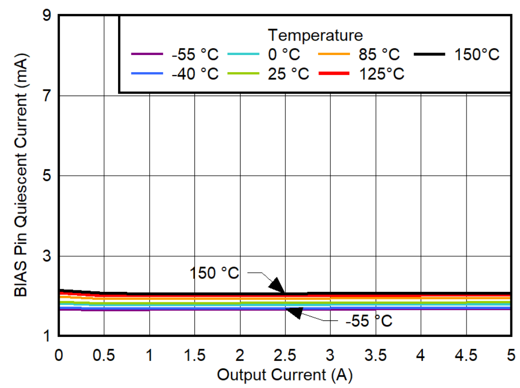
$C_{NR/SS}$ = C_{IN} = 4.7 μF, C_{OUT} = 22 μF

图 6-184. Total Quiescent Current vs I_{OUT} for V_{OUT} = 0.5 V, V_{IN} = 0.7 V, V_{BIAS} = 3.7 V, CP Disabled



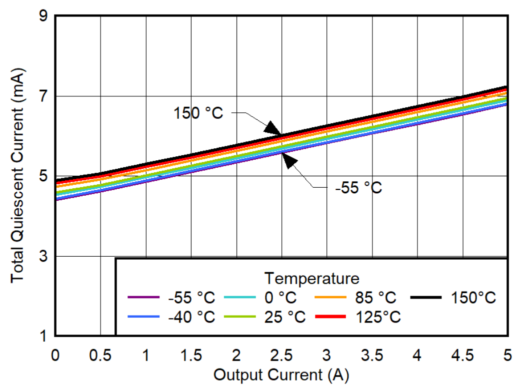
$C_{NR/SS}$ = C_{IN} = 4.7 μF, C_{OUT} = 22 μF

图 6-185. IN Pin Quiescent Current vs I_{OUT} for V_{OUT} = 0.5 V, V_{IN} = 0.7 V, V_{BIAS} = 3.7 V, CP Disabled



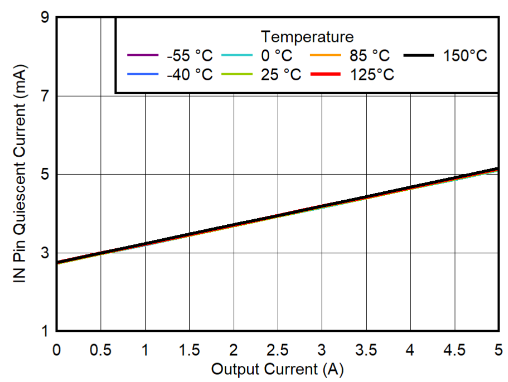
$C_{NR/SS}$ = C_{IN} = 4.7 μF, C_{OUT} = 22 μF

图 6-186. BIAS Pin Quiescent Current vs I_{OUT} for V_{OUT} = 0.5 V, V_{IN} = 0.7 V, V_{BIAS} = 11 V, CP Disabled



$C_{NR/SS}$ = C_{IN} = 4.7 μF, C_{OUT} = 22 μF

图 6-187. Total Quiescent Current vs I_{OUT} for V_{OUT} = 0.5 V, V_{IN} = 0.7 V, V_{BIAS} = 11 V, CP Disabled

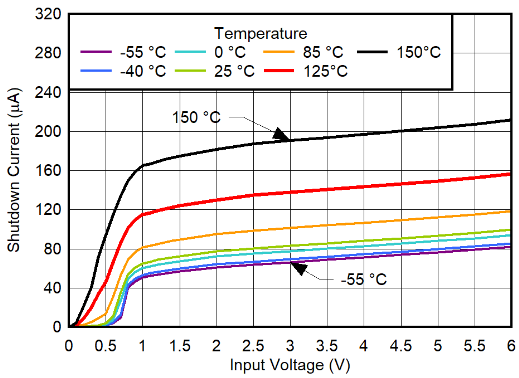


$C_{NR/SS}$ = C_{IN} = 4.7 μF, C_{OUT} = 22 μF

图 6-188. IN Pin Quiescent Current vs I_{OUT} for V_{OUT} = 0.5 V, V_{IN} = 0.7 V, V_{BIAS} = 11 V, CP Disabled

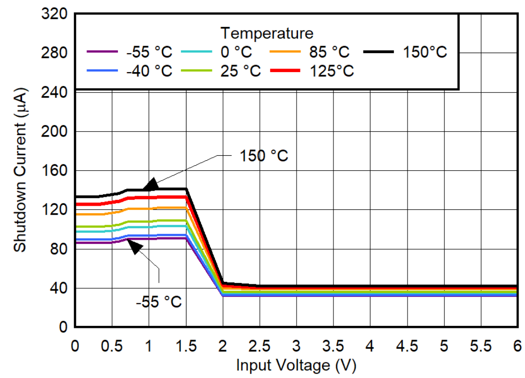
6.6 Typical Characteristics (continued)

V_{IN} = $V_{OUT(NOM)}$ + 0.4 V, V_{EN} = 1.8 V, V_{CP_EN} = 1.8 V, C_{IN} = 10 µF, $C_{NR/SS}$ = 4.7 µF, C_{OUT} = 22 µF, C_{BIAS} = 0 nF, SNS pin shorted to OUT pin, and PG pin pulled up to V_{IN} with 100 kΩ (unless otherwise noted); typical values are at T_J = 25°C



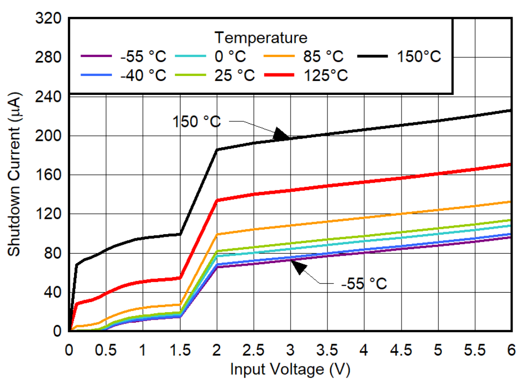
$C_{NR/SS}$ = C_{IN} = 4.7 µF, C_{OUT} = 22 µF, V_{CP_EN} = 1.8 V, V_{EN} = 0.4 V

图 6-189. Shutdown Current vs V_{IN} for V_{OUT} = 0.5 V, V_{BIAS} = 0 V, CP Enabled



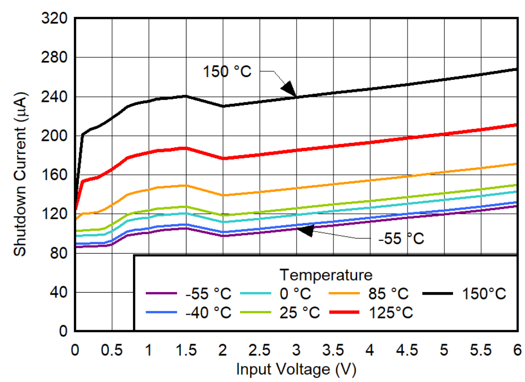
$C_{NR/SS}$ = C_{IN} = 4.7 µF, C_{OUT} = 22 µF, V_{CP_EN} = 0.4 V, V_{EN} = 0.4 V

图 6-190. BIAS Pin Shutdown Current vs V_{IN} for V_{OUT} = 0.5 V, V_{BIAS} = 11 V, CP Disabled



$C_{NR/SS}$ = C_{IN} = 4.7 µF, C_{OUT} = 22 µF, V_{CP_EN} = 0.4 V, V_{EN} = 0.4 V

图 6-191. IN Pin Shutdown Current vs V_{IN} for V_{OUT} = 0.5 V, V_{BIAS} = 11 V, CP Disabled

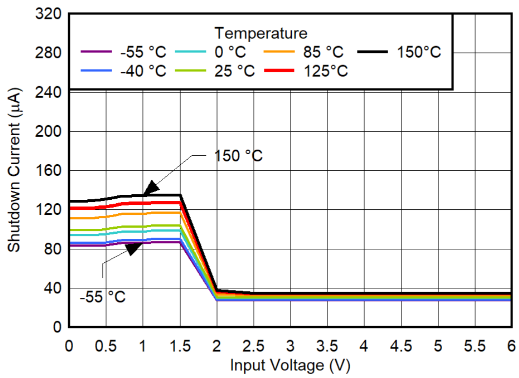


$C_{NR/SS}$ = C_{IN} = 4.7 µF, C_{OUT} = 22 µF, V_{CP_EN} = 0.4 V, V_{EN} = 0.4 V

图 6-192. Total Shutdown Current vs V_{IN} for V_{OUT} = 0.5 V, V_{BIAS} = 11 V, CP Disabled

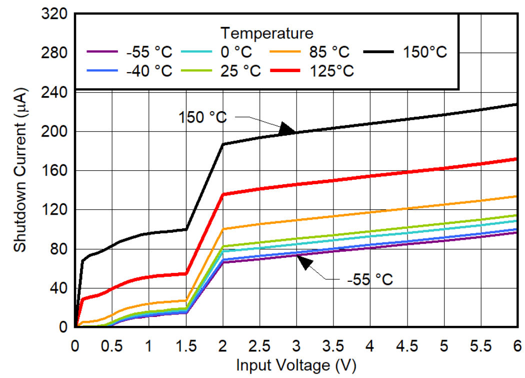
6.6 Typical Characteristics (continued)

V_{IN} = $V_{OUT(NOM)}$ + 0.4 V, V_{EN} = 1.8 V, V_{CP_EN} = 1.8 V, C_{IN} = 10 µF, $C_{NR/SS}$ = 4.7 µF, C_{OUT} = 22 µF, C_{BIAS} = 0 nF, SNS pin shorted to OUT pin, and PG pin pulled up to V_{IN} with 100 kΩ (unless otherwise noted); typical values are at T_J = 25°C



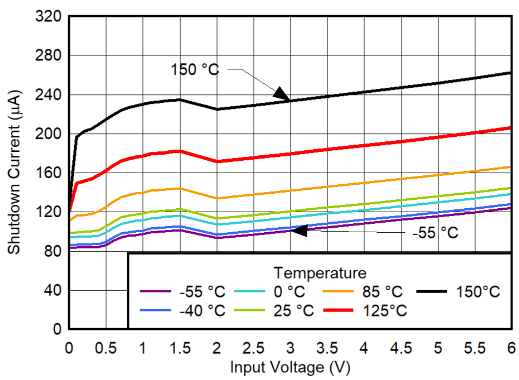
$C_{NR/SS}$ = C_{IN} = 4.7 µF, C_{OUT} = 22 µF, V_{CP_EN} = 1.8 V, V_{EN} = 0.4 V

图 6-193. BIAS Pin Shutdown Current vs V_{IN} for V_{OUT} = 0.5 V, V_{BIAS} = 3 V, CP Enabled



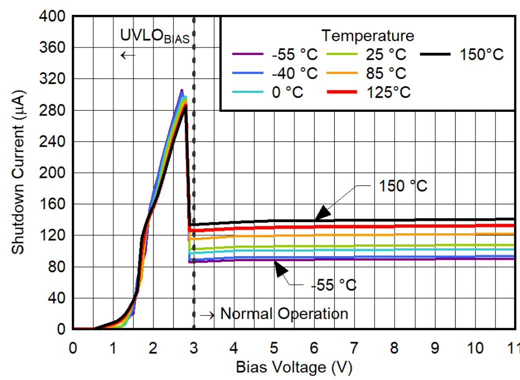
$C_{NR/SS}$ = C_{IN} = 4.7 µF, C_{OUT} = 22 µF, V_{CP_EN} = 1.8 V, V_{EN} = 0.4 V

图 6-194. IN Pin Shutdown Current vs V_{IN} for V_{OUT} = 0.5 V, V_{BIAS} = 3 V, CP Enabled



$C_{NR/SS}$ = C_{IN} = 4.7 µF, C_{OUT} = 22 µF, V_{CP_EN} = 1.8 V, V_{EN} = 0.4 V

图 6-195. Total Shutdown Current vs V_{IN} for V_{OUT} = 0.5 V, V_{BIAS} = 3 V, CP Enabled

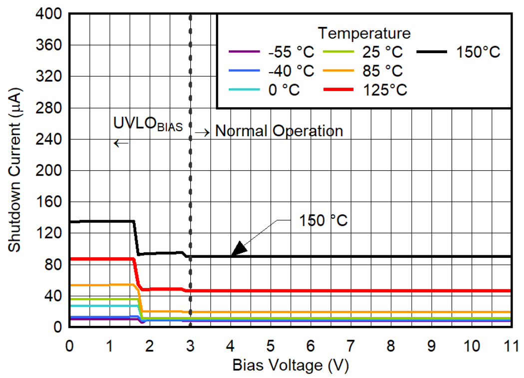


$C_{NR/SS}$ = C_{IN} = 4.7 µF, C_{OUT} = 22 µF, V_{CP_EN} = 1.8 V, V_{EN} = 0.4 V

图 6-196. BIAS Pin Shutdown Current vs V_{BIAS} for V_{IN} = 0.7 V, V_{OUT} = 0.5 V, CP Enabled

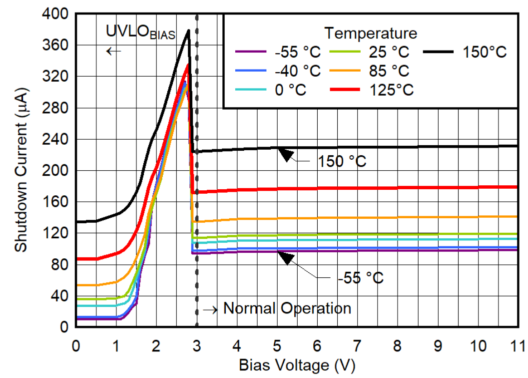
6.6 Typical Characteristics (continued)

V_{IN} = $V_{OUT(NOM)}$ + 0.4 V, V_{EN} = 1.8 V, V_{CP_EN} = 1.8 V, C_{IN} = 10 μF, $C_{NR/SS}$ = 4.7 μF, C_{OUT} = 22 μF, C_{BIAS} = 0 nF, SNS pin shorted to OUT pin, and PG pin pulled up to V_{IN} with 100 kΩ (unless otherwise noted); typical values are at T_J = 25°C



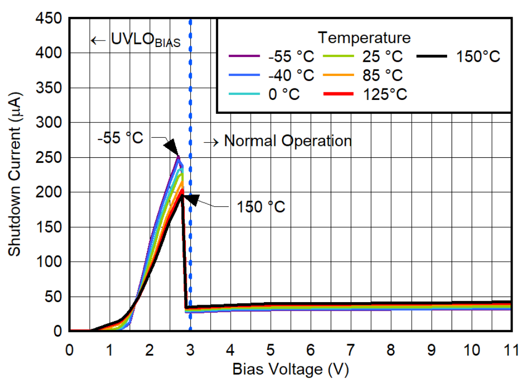
$C_{NR/SS}$ = C_{IN} = 4.7 μF, C_{OUT} = 22 μF, V_{CP_EN} = 1.8 V, V_{EN} = 0.4 V

图 6-197. IN Pin Shutdown Current vs V_{BIAS} for V_{IN} = 0.7 V, V_{OUT} = 0.5 V, CP Enabled



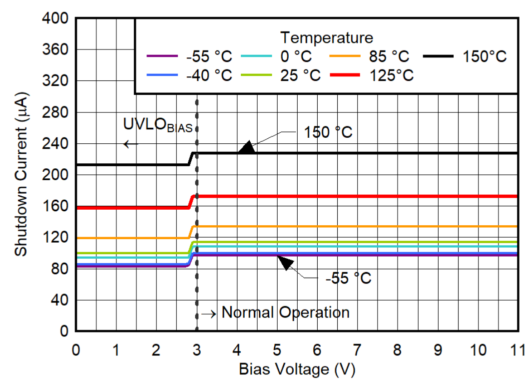
$C_{NR/SS}$ = C_{IN} = 4.7 μF, C_{OUT} = 22 μF, V_{CP_EN} = 1.8 V, V_{EN} = 0.4 V

图 6-198. Total Shutdown Current vs V_{BIAS} for V_{IN} = 0.7 V, V_{OUT} = 0.5 V, CP Enabled



$C_{NR/SS}$ = C_{IN} = 4.7 μF, C_{OUT} = 22 μF, V_{CP_EN} = 1.8 V, V_{EN} = 0.4 V

图 6-199. BIAS Pin Shutdown Current vs V_{BIAS} for V_{IN} = 6 V, $V_{OUT(nom)}$ = 0.5 V, CP Enabled

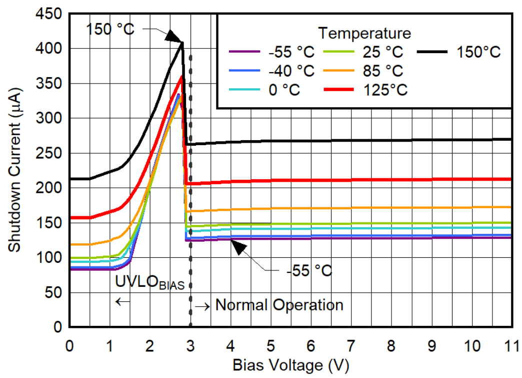


$C_{NR/SS}$ = C_{IN} = 4.7 μF, C_{OUT} = 22 μF, V_{CP_EN} = 1.8 V, V_{EN} = 0.4 V

图 6-200. IN Pin Shutdown Current vs V_{BIAS} for V_{IN} = 6 V, $V_{OUT(nom)}$ = 0.5 V, CP Enabled

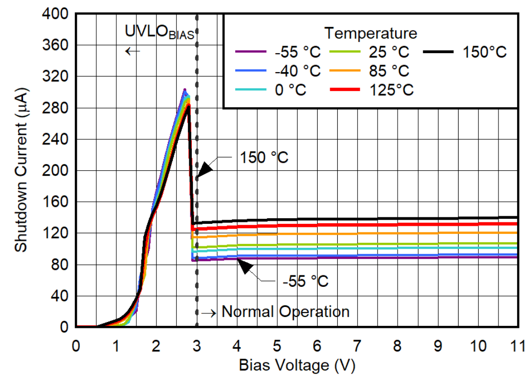
6.6 Typical Characteristics (continued)

V_{IN} = $V_{OUT(NOM)}$ + 0.4 V, V_{EN} = 1.8 V, V_{CP_EN} = 1.8 V, C_{IN} = 10 μF, $C_{NR/SS}$ = 4.7 μF, C_{OUT} = 22 μF, C_{BIAS} = 0 nF, SNS pin shorted to OUT pin, and PG pin pulled up to V_{IN} with 100 kΩ (unless otherwise noted); typical values are at T_J = 25°C



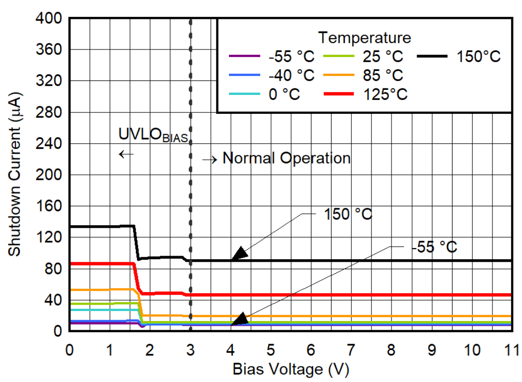
$C_{NR/SS}$ = C_{IN} = 4.7 μF, C_{OUT} = 22 μF, V_{CP_EN} = 1.8 V, V_{EN} = 0.4 V

图 6-201. Total Shutdown Current vs V_{BIAS} for V_{IN} = 6 V, $V_{OUT(nom)}$ = 0.5 V, CP Enabled



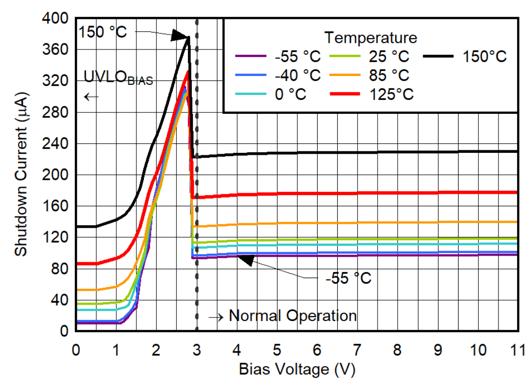
$C_{NR/SS}$ = C_{IN} = 4.7 μF, C_{OUT} = 22 μF, V_{CP_EN} = 0 V, V_{EN} = 0.4 V

图 6-202. BIAS Pin Shutdown Current vs V_{BIAS} for V_{IN} = 0.7 V, $V_{OUT(nom)}$ = 0.5 V, CP Disabled



$C_{NR/SS}$ = C_{IN} = 4.7 μF, C_{OUT} = 22 μF, V_{CP_EN} = 0 V, V_{EN} = 0.4 V

图 6-203. IN Pin Shutdown Current vs V_{BIAS} for V_{IN} = 0.7 V, $V_{OUT(nom)}$ = 0.5 V, CP Disabled

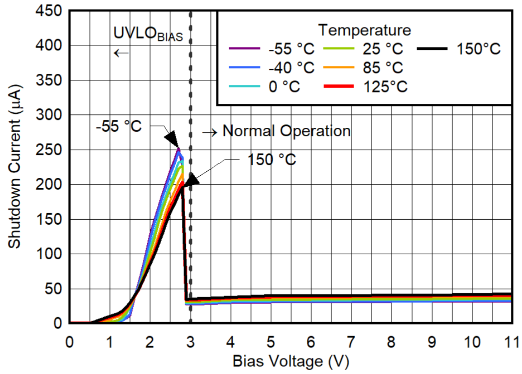


$C_{NR/SS}$ = C_{IN} = 4.7 μF, C_{OUT} = 22 μF, V_{CP_EN} = 0 V, V_{EN} = 0.4 V

图 6-204. Total Shutdown Current vs V_{BIAS} for V_{IN} = 0.7 V, $V_{OUT(nom)}$ = 0.5 V, CP Disabled

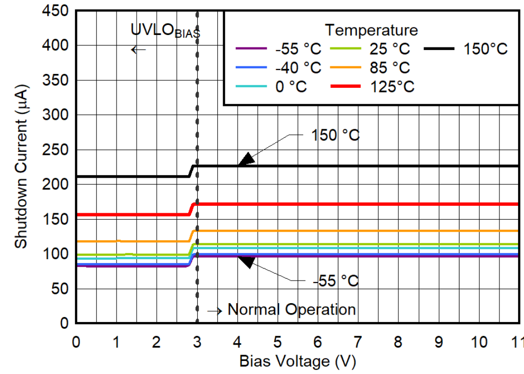
6.6 Typical Characteristics (continued)

$V_{IN} = V_{OUT(NOM)} + 0.4$ V, $V_{EN} = 1.8$ V, $V_{CP\_EN} = 1.8$ V, $C_{IN} = 10$ µF, $C_{NR/SS} = 4.7$ µF, $C_{OUT} = 22$ µF, $C_{BIAS} = 0$ nF, SNS pin shorted to OUT pin, and PG pin pulled up to V_{IN} with 100 kΩ (unless otherwise noted); typical values are at $T_J = 25°C$



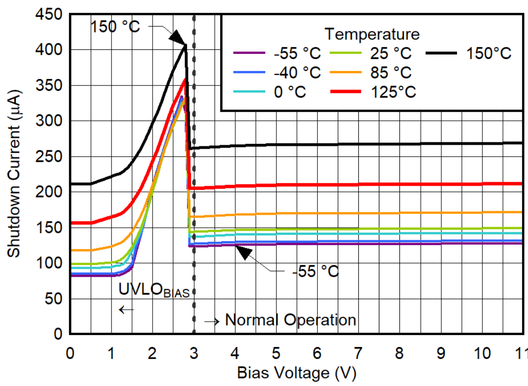
$C_{NR/SS} = C_{IN} = 4.7$ µF, $C_{OUT} = 22$ µF, $V_{CP\_EN} = 0$ V, $V_{EN} = 0.4$ V

图 6-205. BIAS Pin Shutdown Current vs V_{BIAS} for $V_{IN} = 6$ V, $V_{OUT(nom)} = 0.5$ V, CP Disabled



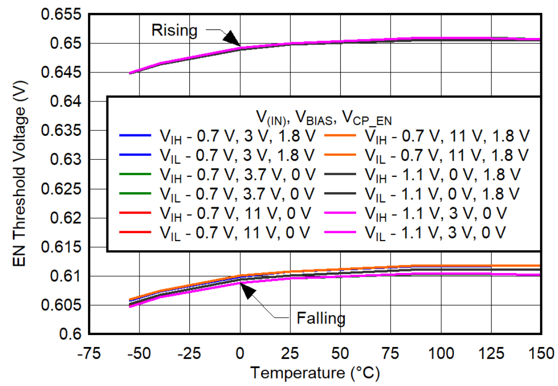
$C_{NR/SS} = C_{IN} = 4.7$ µF, $C_{OUT} = 22$ µF, $V_{CP\_EN} = 0$ V, $V_{EN} = 0.4$ V

图 6-206. IN Pin Shutdown Current vs V_{BIAS} for $V_{IN} = 6$ V, $V_{OUT(nom)} = 0.5$ V, CP Disabled



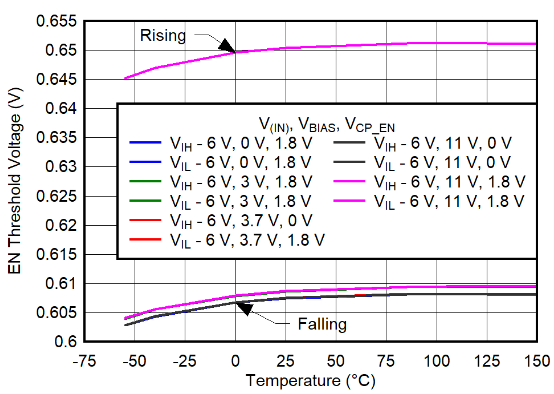
$C_{NR/SS} = C_{IN} = 4.7$ µF, $C_{OUT} = 22$ µF, $V_{CP\_EN} = 0$ V, $V_{EN} = 0.4$ V

图 6-207. Total Shutdown Current vs V_{BIAS} for $V_{IN} = 6$ V, $V_{OUT(nom)} = 0.5$ V, CP Disabled



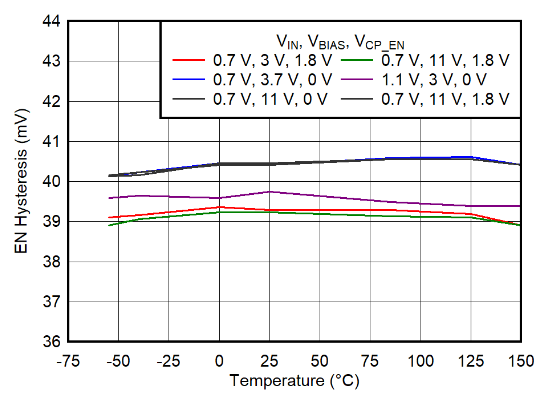
$C_{NR/SS} = C_{IN} = 4.7$ µF, $C_{OUT} = 22$ µF

图 6-208. EN Threshold Voltage vs Temperature for $V_{IN} = 0.7$ V and 1.1 V, $V_{OUT} = 0.5$ V



$C_{NR/SS} = C_{IN} = 4.7$ µF, $C_{OUT} = 22$ µF

图 6-209. EN Threshold Voltage vs Temperature for $V_{IN} = 6$ V, $V_{OUT} = 0.5$ V

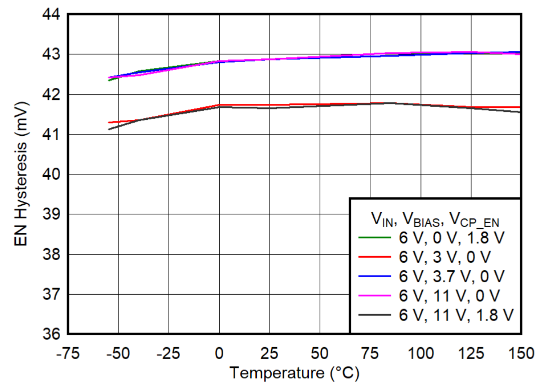


$C_{NR/SS} = C_{IN} = 4.7$ µF, $C_{OUT} = 22$ µF

图 6-210. EN Hysteresis vs Temperature for $V_{IN} = 0.7$ V and 1.1 V, $V_{OUT} = 0.5$ V

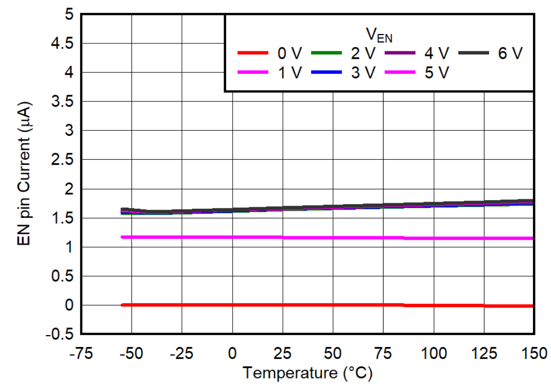
6.6 Typical Characteristics (continued)

$V_{IN} = V_{OUT(NOM)} + 0.4$ V, $V_{EN} = 1.8$ V, $V_{CP\_EN} = 1.8$ V, $C_{IN} = 10$ µF, $C_{NR/SS} = 4.7$ µF, $C_{OUT} = 22$ µF, $C_{BIAS} = 0$ nF, SNS pin shorted to OUT pin, and PG pin pulled up to V_{IN} with 100 kΩ (unless otherwise noted); typical values are at $T_J = 25$°C



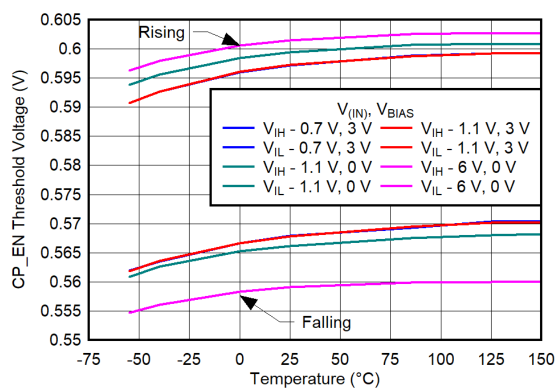
$C_{NR/SS} = C_{IN} = 4.7$ µF, $C_{OUT} = 22$ µF

图 6-211. EN Hysteresis vs Temperature for V_{IN} = 6 V, V_{OUT} = 0.5 V



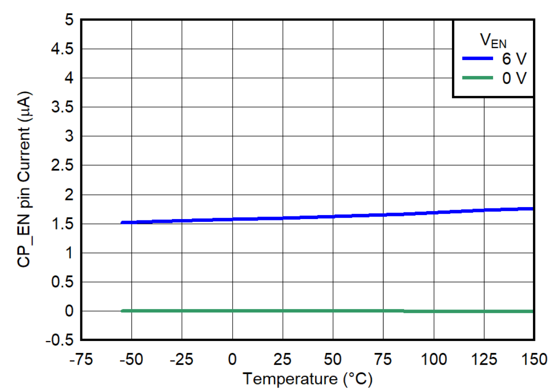
$C_{NR/SS} = C_{IN} = 4.7$ µF, $C_{OUT} = 22$ µF

图 6-212. EN Pin Current vs Temperature



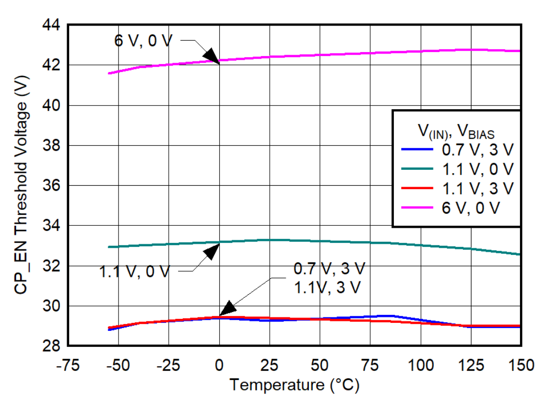
$C_{NR/SS} = C_{IN} = 4.7$ µF, $C_{OUT} = 22$ µF

图 6-213. CP_EN Threshold Voltage vs Temperature



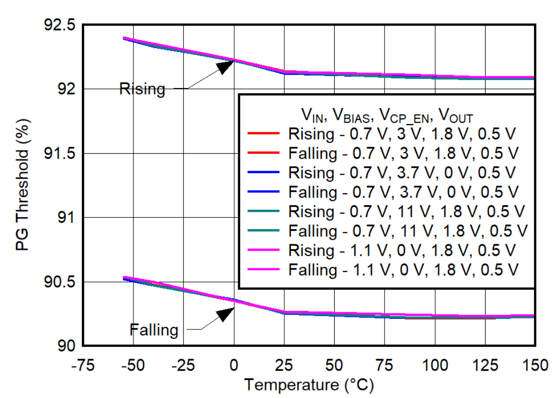
$C_{NR/SS} = C_{IN} = 4.7$ µF, $C_{OUT} = 22$ µF

图 6-214. CP_EN Pin Current vs Temperature



$C_{NR/SS} = C_{IN} = 4.7$ µF, $C_{OUT} = 22$ µF

图 6-215. CP_EN Hysteresis vs Temperature

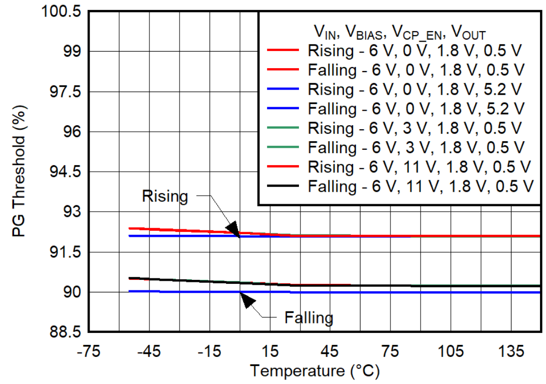


$C_{NR/SS} = C_{IN} = 4.7$ µF, $C_{OUT} = 22$ µF

图 6-216. PG Threshold Voltage vs Temperature for V_{IN} = 0.7 V and 1.1 V

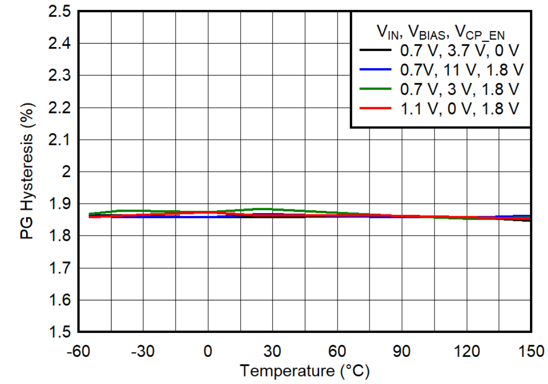
6.6 Typical Characteristics (continued)

$V_{IN} = V_{OUT(NOM)} + 0.4$ V, $V_{EN} = 1.8$ V, $V_{CP\_EN} = 1.8$ V, $C_{IN} = 10$ µF, $C_{NR/SS} = 4.7$ µF, $C_{OUT} = 22$ µF, $C_{BIAS} = 0$ nF, SNS pin shorted to OUT pin, and PG pin pulled up to V_{IN} with 100 kΩ (unless otherwise noted); typical values are at $T_J = 25°C$



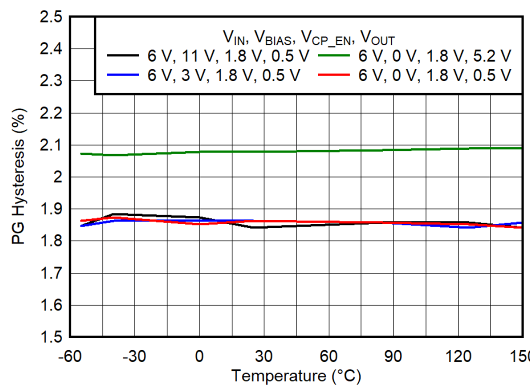
$C_{NR/SS} = C_{IN} = 4.7$ µF, $C_{OUT} = 22$ µF

图 6-217. PG Threshold Voltage vs Temperature for V_{IN} = 6 V



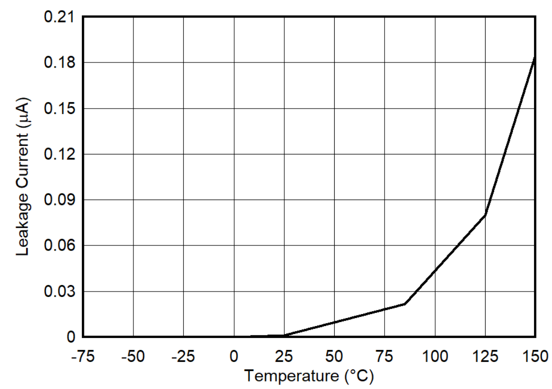
$C_{NR/SS} = C_{IN} = 4.7$ µF, $C_{OUT} = 22$ µF

图 6-218. PG Hysteresis vs Temperature for V_{IN} = 0.7 V and 1.1 V



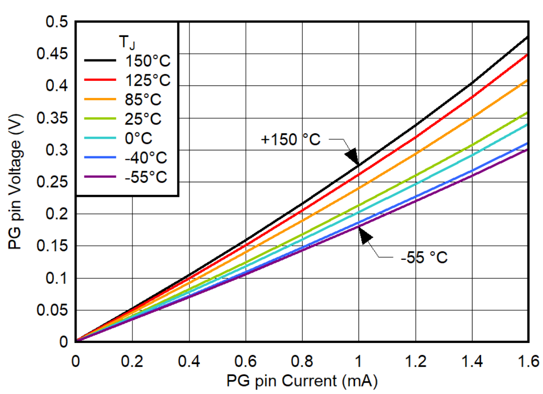
$C_{NR/SS} = C_{IN} = 4.7$ µF, $C_{OUT} = 22$ µF

图 6-219. PG Hysteresis vs Temperature for V_{IN} = 6 V



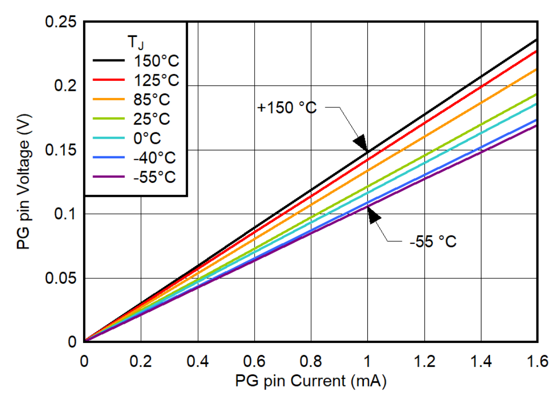
$C_{NR/SS} = C_{IN} = 4.7$ µF, $C_{OUT} = 22$ µF

图 6-220. PG Leakage Current vs Temperature



$C_{NR/SS} = C_{IN} = 4.7$ µF, $C_{OUT} = 22$ µF, $V_{BIAS} = 0$ V,
$V_{OUT} = 0.5$ V, $V_{CP\_EN} = 1.8$ V

图 6-221. PG Pin Low-Level Voltage vs PG Pin Current for V_{IN} = 1.1 V, No BIAS

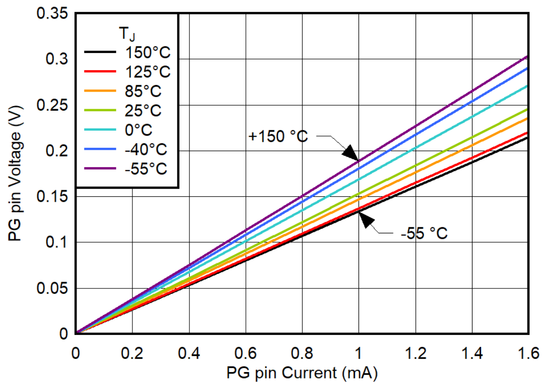


$C_{NR/SS} = C_{IN} = 4.7$ µF, $C_{OUT} = 22$ µF, $V_{BIAS} = 0$ V,
$V_{OUT} = 0.5$ V, $V_{CP\_EN} = 1.8$ V

**图 6-222. PG Pin Low-Level Voltage vs PG Pin Current for V_{IN} = 6 V,
No BIAS**

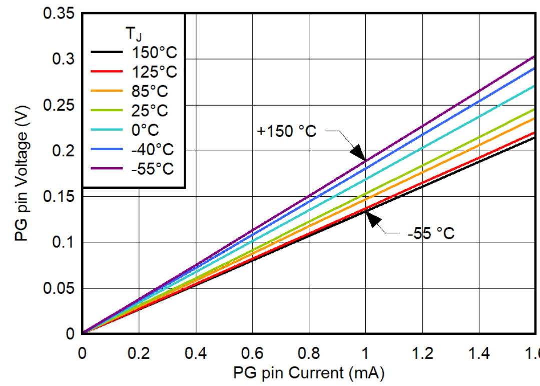
6.6 Typical Characteristics (continued)

V_{IN} = $V_{OUT(NOM)}$ + 0.4 V, V_{EN} = 1.8 V, V_{CP_EN} = 1.8 V, C_{IN} = 10 μF, $C_{NR/SS}$ = 4.7 μF, C_{OUT} = 22 μF, C_{BIAS} = 0 nF, SNS pin shorted to OUT pin, and PG pin pulled up to V_{IN} with 100 kΩ (unless otherwise noted); typical values are at T_J = 25°C



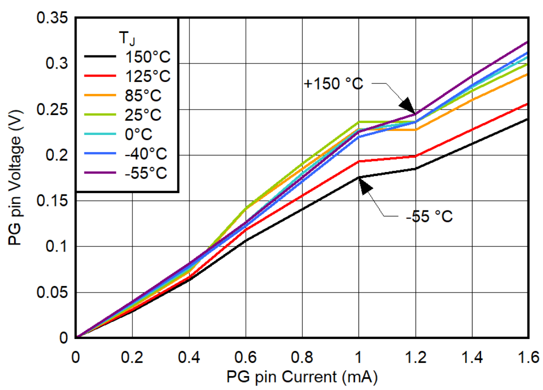
$C_{NR/SS}$ = C_{IN} = 4.7 μF, C_{OUT} = 22 μF, V_{OUT} = 0.5 V

图 6-223. PG Pin Low-Level Voltage vs PG Pin Current for V_{IN} = 0.7 V, V_{BIAS} = 3.7 V, V_{CP_EN} = 0 V



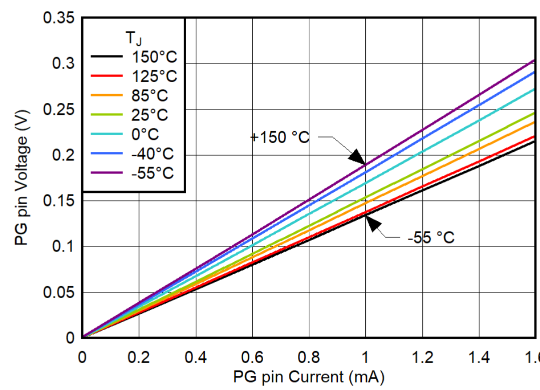
$C_{NR/SS}$ = C_{IN} = 4.7 μF, C_{OUT} = 22 μF, V_{OUT} = 0.5 V

图 6-224. PG Pin Low-Level Voltage vs PG Pin Current for V_{IN} = 0.7 V, V_{BIAS} = 11 V, V_{CP_EN} = 0 V



$C_{NR/SS}$ = C_{IN} = 4.7 μF, C_{OUT} = 22 μF, V_{OUT} = 0.5 V

图 6-225. PG Pin Low-Level Voltage vs PG Pin Current for V_{IN} = 0.7 V, V_{BIAS} = 3 V, V_{CP_EN} = 1.8 V



$C_{NR/SS}$ = C_{IN} = 4.7 μF, C_{OUT} = 22 μF, V_{OUT} = 0.5 V

图 6-226. PG Pin Low-Level Voltage vs PG Pin Current for V_{IN} = 0.7 V, V_{BIAS} = 11 V, V_{CP_EN} = 1.8 V

7 Detailed Description

7.1 Overview

The TPS7A57 is a low-noise (2.45 μV_{RMS} over 10-Hz to 100-kHz bandwidth), ultra-high PSRR (> 36 dB to 1 MHz), high-accuracy (1%), ultra-low-dropout (LDO) linear voltage regulator with an input range of 0.7 V to 6.0 V and an output voltage range from 0.5 V to 5.2 V. This device uses innovative circuitry to achieve wide bandwidth and high loop gain, resulting in ultra-high PSRR even with very low operational headroom [V_{OpHr} = (V_{IN} – V_{OUT})]. At a high level, the device has two main primary features (the current reference and the unity-gain LDO buffer) and a few secondary features (such as the adjustable soft-start inrush control, precision enable, charge pump enable, and PG pin).

The current reference is controlled by the REF pin. This pin sets the output voltage with a single resistor.

The NR/SS pin sets the start-up time, and filters the noise generated by the reference and external set resistor.

The unity-gain LDO buffer controls the output voltage. The low noise does not increase with output voltage and provides wideband PSRR. As such, the SNS pin is only used for remote sensing of the load.

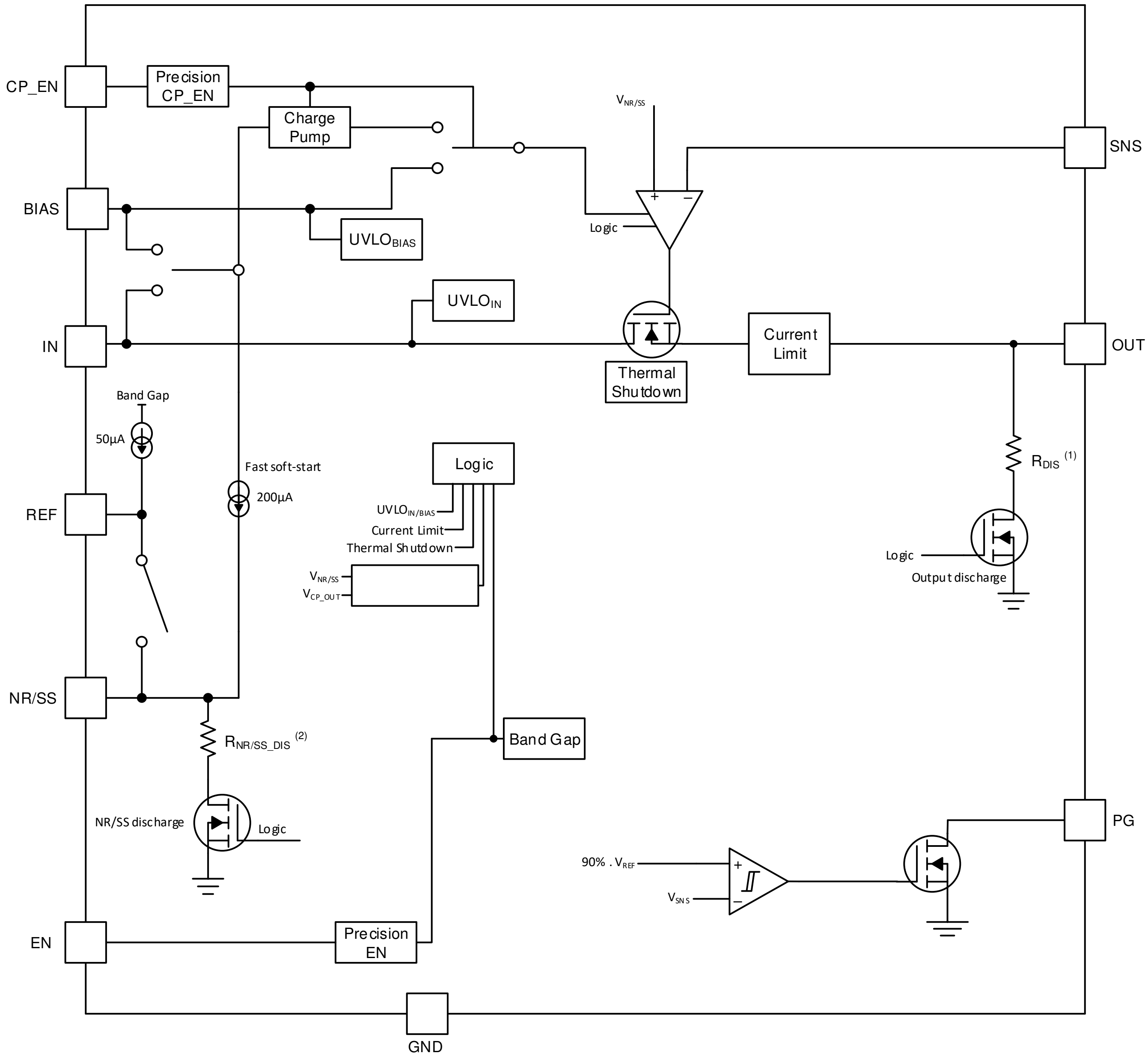
The low-noise current reference, 50 μA typical, is used in conjunction with an external resistor (R_{REF}) to set the output voltage. This process allows the output voltage range to be set from 0.5 V to 5.2 V. To achieve its low noise and allow for a soft-start inrush, an external capacitor, $C_{NR/SS}$ (typically 4.7 μF), is placed on the NR/SS pin. When start-up is completed and the switch between REF and NR/SS is closed, the $C_{NR/SS}$ capacitor is in parallel with the R_{REF} resistor attenuating the band-gap noise. The R_{REF} resistor sets the output voltage. This unity-gain LDO provides ultra-high PSRR over a wide frequency range without compromising load and line transients.

The EN pin sets the precision enable feature; a resistor divider on this pin selects the optimal input voltage at which the device starts. There are three independent undervoltage lockout (UVLO) voltages in this device: the internal fixed UVLO thresholds for the IN and BIAS rails, and the externally adjustable UVLO threshold using the EN pin.

The CP_EN pin enables or disables the internal charge pump. The TPS7A57 does not allow operation below 1.1 V without a BIAS rail. If the charge pump is disabled, a minimum operating headroom between OUT and BIAS is required.

This regulator offers current limit, thermal protection, is fully specified from –40°C to +125°C, and is offered in a 16-pin WQFN, 3-mm × 3-mm thermally efficient package.

7.2 Functional Block Diagram



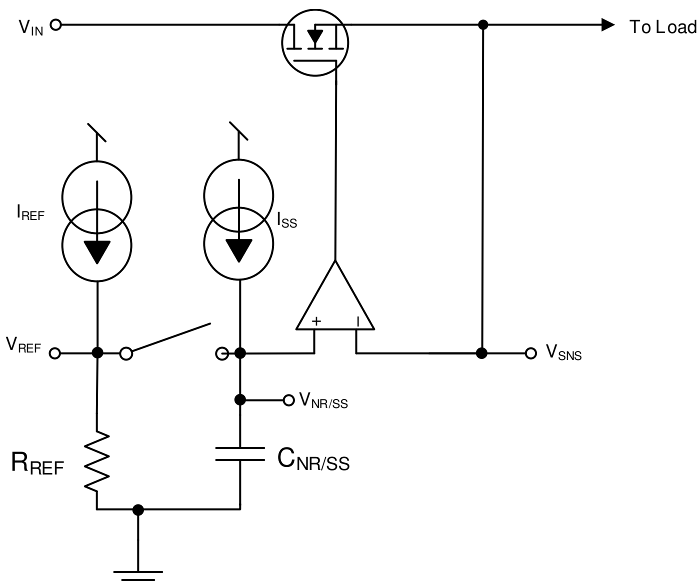
A. See the R_{DIS} (the output pin active discharge resistance) value in the *Electrical Characteristics* table.
B. See the R_{NR/SS_DIS} (the NR/SS pin active discharge resistance) value in the *Electrical Characteristics* table.

7.3 Feature Description

7.3.1 Output Voltage Setting and Regulation

The simplified regulation circuit is shown in 图 7-1, in which the input signal (V_{REF}) is generated by the internal current source (I_{REF}) and the external resistor (R_{REF}). The LDO output voltage is programmed by the V_{REF} voltage because the error amplifier is always operating in unity-gain configuration. The V_{REF} reference voltage is generated by an internal low-noise current source driving the R_{REF} resistor and is designed to have very low bandwidth at the input to the error amplifier through the use of a low-pass filter ($C_{NR/SS}$ || R_{REF}).

The unity-gain configuration is achieved by connecting SNS to OUT. Minimize trace inductance on the output and connect C_{OUT} as close to the output as possible.



$V_{OUT} = I_{REF} \times R_{REF}$.

图 7-1. Simplified Regulation Circuit

This unity-gain configuration, along with the highly accurate I_{REF} reference current, enables the device to achieve excellent output voltage accuracy. The low dropout voltage (V_{DO}) enables reduced thermal dissipation and achieves robust performance. This combination of features make this device an excellent voltage source for powering sensitive analog low-voltage (⩽ 5.5 V) devices.

7.3.2 Low-Noise, Ultra-High Power-Supply Rejection Ratio (PSRR)

The device architecture features a highly accurate, high-precision, low-noise current reference followed by a state-of-the-art, complementary metal oxide semiconductor (CMOS) error amplifier (6 nV/$\sqrt{Hz}$ at 10-kHz noise for V_{OUT} ⩾ 0.5 V). Unlike previous-generation LDOs, the unity-gain configuration of this device ensures low noise over the entire output voltage range. Additional noise reduction and higher output current can be achieved by placing multiple TPS7A57 LDOs in parallel, see the *Paralleling for Higher Output Current and Lower Noise* section.

7.3.3 Programmable Soft-Start (NR/SS Pin)

The device features a programmable, monotonic, current-controlled, soft-start circuit that uses the $C_{NR/SS}$ capacitor to minimize inrush current into the output capacitor and load during start-up. This circuitry can also reduce the start-up time for some applications that require the output voltage to reach at least 90% of its set value for fast system start up. See the *Soft-Start, Noise Reduction (NR/SS Pin), and Power-Good (PG Pin)* section for more details.

7.3.4 Precision Enable and UVLO

Depending on the circuit implementation, up to three independent undervoltage lockout (UVLO) voltage circuits can be active. An internally set UVLO on the input supply (IN pin) and the bias supply (BIAS pin) automatically disables the LDO when the input voltage reaches the minimum threshold. A precision EN function (EN pin) can also be used as a user-programmable UVLO.

1. The internal input supply voltage UVLO circuit prevents the regulator from turning on when the input voltage is not high enough, see the *Electrical Characteristics* table for more details.
2. The internal bias supply voltage UVLO circuit prevents the regulator from turning on when the bias voltage is not high enough, see the *Electrical Characteristics* table for more details.
3. The precision enable circuit allows a simple sequencing of multiple power supplies with a resistor divider from another supply. This enable circuit can be used to set an external UVLO voltage at which the device is enabled using a resistor divider on the EN pin; see the *Precision Enable (External UVLO)* section for more details.

7.3.5 Charge Pump Enable and BIAS Rail

This device allows the internal charge pump to be disabled for systems that cannot tolerate any switching noise.

When V_{IN} is less than 1.1 V, the BIAS rail is required because this rail sources the current needed by the internal circuitry. The charge pump can be either enabled or disabled. Consider adequate operating headroom requirements from OUT to BIAS if the charge pump is disabled. See the *Undervoltage Lockout (UVLO) Operation* section for more details.

When V_{IN} is greater than or equal to 1.1 V, the CP_EN pin connection determines how the internal circuitry is powered. If CP_EN is connected to GND (CP disabled), the internal circuitry is powered from the BIAS rail; see the *Undervoltage Lockout (UVLO) Operation* section for more details. If CP_EN is connected to the supply (CP enabled), any current required to power the internal circuitry comes from the IN pin. As such, the BIAS pin can be left open.

7.3.6 Power-Good Pin (PG Pin)

The PG pin is an output indicating if the LDO is ready to provide power. This pin is implemented using an open-drain architecture. During the start-up phase, the PG voltage threshold is set by the REF voltage when the fast soft-start is ongoing and is set by the NR/SS voltage when the fast soft-start is completed and the switch between REF and NR/SS is closed.

As shown in the *Functional Block Diagram*, the PG pin is implemented by comparing the SNS pin voltage to an internal reference voltage and, as such, is considered a voltage indicator reflecting the output voltage status.

For PG pin implementation, see the *Power-Good Functionality* section.

7.3.7 Active Discharge

To quickly discharge internal nodes, the device incorporates two internal pulldown metal-oxide semiconductor field effect transistors (MOSFETs). The first pulldown MOSFET connects a resistor (R_{DIS}) from OUT to ground when the device is disabled to actively discharge the output capacitor. The second pulldown MOSFET connects a resistor from NR/SS (R_{NR/SS_DIS}) to ground when the device is disabled and discharges the NR/SS capacitor. Both pulldown MOSFETs are activated by any of the following events:

- Driving the EN pin below the $V_{EN(LOW)}$ threshold
- The IN pin voltage falling below the undervoltage lockout $V_{UVLO(IN)}$ threshold
- The BIAS pin voltage falling below the undervoltage lockout $V_{UVLO(BIAS)}$ threshold

---

备注

A brownout event on BIAS during a low-input, low-output (LILO) operation (< 1.1 V_{IN}) can result in incomplete $C_{NR/SS}$ discharge. Consider the time constant on both the NR/SS and OUT pins for a proper system shutdown procedure.

7.3.8 Thermal Shutdown Protection (T_{SD})

A thermal shutdown protection circuit disables the LDO when the pass transistor junction temperature (T_J) rises to $T_{SD(shutdown)}$ (typical). Thermal shutdown hysteresis assures that the device resets (turns on) when the temperature falls to $T_{SD(shutdown)}$ (typical). The thermal time constant of the semiconductor die is fairly short, thus the device may cycle off and on when thermal shutdown is reached until power dissipation is reduced. Power dissipation during start up can be high from large V_{IN} – V_{OUT} voltage drops across the device or from high inrush currents charging large output capacitors. Under some conditions, the thermal shutdown protection disables the device before start up completes. For reliable operation, limit the junction temperature to the maximum listed in the *Electrical Characteristics* table. Operation above this maximum temperature causes the device to exceed its operational specifications. Although the internal protection circuitry of the device is designed to protect against thermal overload conditions, this circuitry is not intended to replace proper heat sinking. Continuously running the device into thermal shutdown or above the maximum recommended junction temperature reduces long-term reliability.

7.4 Device Functional Modes

7.4.1 Normal Operation

The device regulates to the nominal output voltage when the following conditions are met:

- The input voltage is greater than the nominal output voltage plus the dropout voltage ($V_{OUT(nom)}$ + V_{DO})
- The bias voltage is greater than the nominal output voltage plus the OUT-to-BIAS dropout voltage ($V_{OUT(nom)}$ + $V_{DO(BIAS)}$) if the charge pump is disabled or if the input voltage is less than 1.1 V
- The output current is less than the current limit ($I_{OUT} < I_{LIM}$)
- The device junction temperature is less than the thermal shutdown temperature ($T_J < T_{SD(shutdown)}$)
- The voltage on the EN pin has previously exceeded the $V_{IH(EN)}$ threshold voltage and has not yet decreased to less than the enable falling threshold

表 7-1 summarizes all valid modes of operation and shows what rail is sourcing the internal biasing current.

表 7-1. Valid Modes of Operation

V_{IN} RANGE	V_{OUT} RANGE	V_{BIAS} RANGE	CP MODE	RAIL SOURCING BIASING CURRENT
< 1.1 V	⩾ 0.5 V, ⩽ V_{IN} – V_{DO}	3 V to 11 V	On	BIAS
		Max (V_{OUT} + 2.1 V, 2.8 V) to 11 V	Off	BIAS
⩾ 1.1 V, < 2 V	⩾ 0.5 V, ⩽ V_{IN} – V_{DO}⩾ 0.5 V, ⩽ V_{IN} – V_{DO}	Not present	On	IN
		3 V to 11 V	On	BIAS
		Max (V_{OUT} + 2.1 V, 2.8 V) to 11 V	Off	BIAS
⩾ 2 V	⩾ 0.5 V, ⩽ V_{IN} – V_{DO}	Not required, does not source current even if present	On	IN
		Max (V_{OUT} + 2.1 V, 2.8 V) to 11 V	Off	BIAS

7.4.2 Dropout Operation

If the input voltage is lower than the nominal output voltage plus the specified dropout voltage, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode, the output voltage tracks the input voltage. In dropout operation, the transient performance is significantly degraded because the pass transistor is in the ohmic or triode region, and acts as a switch. Line or load transients in dropout can result in large output voltage deviations.

备注

Unlike traditional n-type field effect transistor (NMOS) LDOs with two supply rails, BIAS and IN, the TPS7A57 cannot enter an OUT-to-BIAS dropout mode. If the charge pump is disabled, a minimum UVLO (BIAS) voltage above the REF voltage must be maintained. If the charge pump is enabled, and if the IN voltage is less than 1.1 V, a voltage greater than or equal to the 3-V BIAS rail must be present. If the charge pump is enabled and the IN voltage is greater than or equal to 1.1 V, a BIAS rail is not required.

For additional information, see the *Undervoltage Lockout (UVLO) Operation* section.

7.4.3 Disabled

The output can be shutdown by forcing the voltage of the EN pin to less than the $V_{IH(EN)}$ threshold (see the *Electrical Characteristics* table). When disabled, the pass transistor is turned off, internal circuits are shutdown, and both the NR/SS pin and OUT pin voltages are actively discharged to ground by internal discharge circuits to ground when the IN pin voltage is higher than or equal to a diode-drop voltage.

7.4.4 Current-Limit Operation

If the output current is greater than or equal to the minimum current limit ($I_{LIM(Min)}$), then the device operates in current-limit mode. Current limit is a foldback implementation. For additional information, see the *Current Limit and Foldback Behavior* section.

8 Application and Implementation

备注

以下应用部分中的信息不属于 TI 器件规格的范围，TI 不担保其准确性和完整性。TI 的客 户应负责确定器件是否适用于其应用。客户应验证并测试其设计，以确保系统功能。

8.1 Application Information

Successfully implementing an LDO in an application depends on the application requirements. This section discusses key device features and how to best implement them to achieve a reliable design.

8.1.1 Precision Enable (External UVLO)

The precision enable circuit (EN pin) turns the device on and off. This circuit can be used to set an external undervoltage lockout (UVLO) voltage, as shown in 图 8-1, to turn on and off the device using a resistor divider between IN (or BIAS when the charge pump is disabled), EN, and GND.

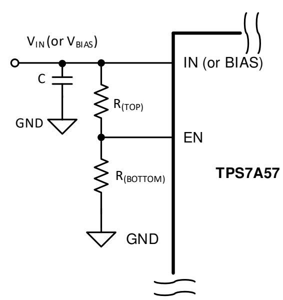


图 8-1. Precision EN Used as an External UVLO

This external UVLO solution is used to prevent the device from turning on when the input supply voltage is not high enough and can place the device in dropout operation. This solution also allows simple sequencing of multiple power supplies with a resistor divider from another supply. Another benefit from using a resistor divider to enable or disable the device is that the EN pin is never left floating because this pin does not have an internal pulldown resistor. However, a zener diode may be needed between the EN pin and ground to comply with the absolute maximum ratings on this pin.

Use 方程式 1 and 方程式 2 to determine the correct resistor values.

$$V_{ON} = V_{OFF} \times [(V_{IH(EN)} + V_{HYS(EN)}) / V_{EN}] \quad (1)$$

$$R_{(TOP)} = R_{(BOTTOM)} \times (V_{OFF} / V_{IH(EN)} - 1) \quad (2)$$

where:

- V_{OFF} is the input or bias voltage where the regulator turns off
- V_{ON} is the input or bias voltage where the regulator turns on

备注

For the EN pin input current, I_{EN}, effects are ignored.

8.1.2 Undervoltage Lockout (UVLO) Operation

表 8-1 lists the UVLO thresholds for different modes of operation.

表 8-1. Relative Threshold for Different Modes of Operation

UVLO THRESHOLD	NAME	CHARGE PUMP ON (With or Without a Bias Rail) UVLO LOGIC: (a, c) || b (Typ)	CHARGE PUMP OFF (With Bias Rail) (Typ)
$V_{UVLO(IN)}$ rising	a	0.67 V	0.67 V
	b	1.07 V	N/A
$V_{UVLO(BIAS)}$ rising	c	2.8 V	Max (V_{REF} + 2.1 V, 2.8 V)

8.1.2.1 IN Pin UVLO

The IN pin UVLO (UVLO(IN)) circuit makes sure that the device remains disabled before the input supply reaches the minimum operational voltage range, and that the device shuts down when the input supply falls too low.

The UVLO(IN) circuit has a minimum response time of several microseconds to fully assert. During this time, a downward line transient below approximately 0.67 V causes the input supply UVLO(IN) to assert for a short time. However, the UVLO(IN) circuit does not have enough stored energy to fully discharge the internal circuits inside of the device and may result in incomplete discharge of OUT and NR/SS capacitors.

备注

The effect of the downward line transient can trigger the overshoot prevention circuit and can be easily mitigated by using the solution proposed in the *Precision Enable (External UVLO)* section.

8.1.2.2 BIAS UVLO

The BIAS pin UVLO (UVLO(BIAS)) circuit makes sure that the device remains disabled before the input supply reaches the minimum operational voltage range, and that the device shuts down when the input supply falls too low.

The UVLO(BIAS) circuit has a minimum response time of several microseconds to fully assert. During this time, a downward line transient below approximately 2.8 V (with the charge pump enabled) or V_{REF} + 2.1 V (with the charge pump disabled) causes the input supply UVLO(BIAS) to assert for a short time. However, the UVLO(BIAS) circuit does not have enough stored energy to fully discharge the internal circuits inside of the device and may result in incomplete discharge of the OUT and NR/SS capacitors.

备注

The effect of the downward line transient can trigger the overshoot prevention circuit and can be easily mitigated by using the solution proposed in the *Precision Enable (External UVLO)* section.

8.1.2.3 Typical UVLO Operation

图 8-2 illustrates the UVLO (IN or BIAS) circuit response to various input voltage events. The diagram can be separated into the following regions:

- Region A: The device does not turn on until the input reaches the UVLO rising threshold.
- Region B: Normal operation with a regulated output.
- Region C: Brownout event above the UVLO falling threshold (UVLO rising threshold – UVLO hysteresis). The output may fall out of regulation but the device is still enabled.
- Region D: Normal operation with a regulated output.
- Region E: Brownout event below the UVLO falling threshold. The device is disabled in most cases and the output falls because of the load and active discharge circuit. The device is reenabled when the UVLO rising threshold is reached by the input voltage and a normal start up then follows.
- Region F: Normal operation followed by the input falling to the UVLO falling threshold.

- Region G: The device is disabled when the input voltage falls below the UVLO falling threshold to 0 V. The output falls because of the load and active discharge circuit.

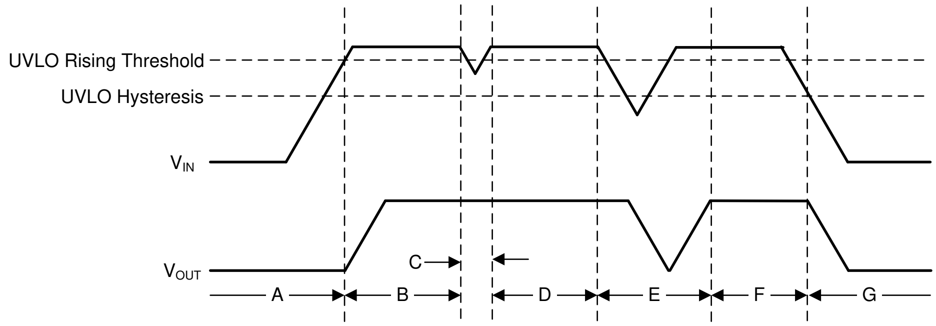


图 8-2. Typical UVLO Operation

8.1.2.4 UVLO(IN) and UVLO(BIAS) Interaction

When operating with IN between 1.07 V and 1.1 V with the internal charge pump on, a glitch can occur on the output during the shutdown power-supply sequence if the BIAS rail falls prior to the IN rail.

When the BIAS rail falls below the V_{UVLO_BIAS} threshold, the output is disabled. When the IN rail is above the minimum UVLO threshold to operate, the LDO restarts. 图 8-3 shows this behavior.

To prevent this behavior, ensure the proper turn-off power-supply sequence is followed, or select an operating mode (such as charge pump disabled).

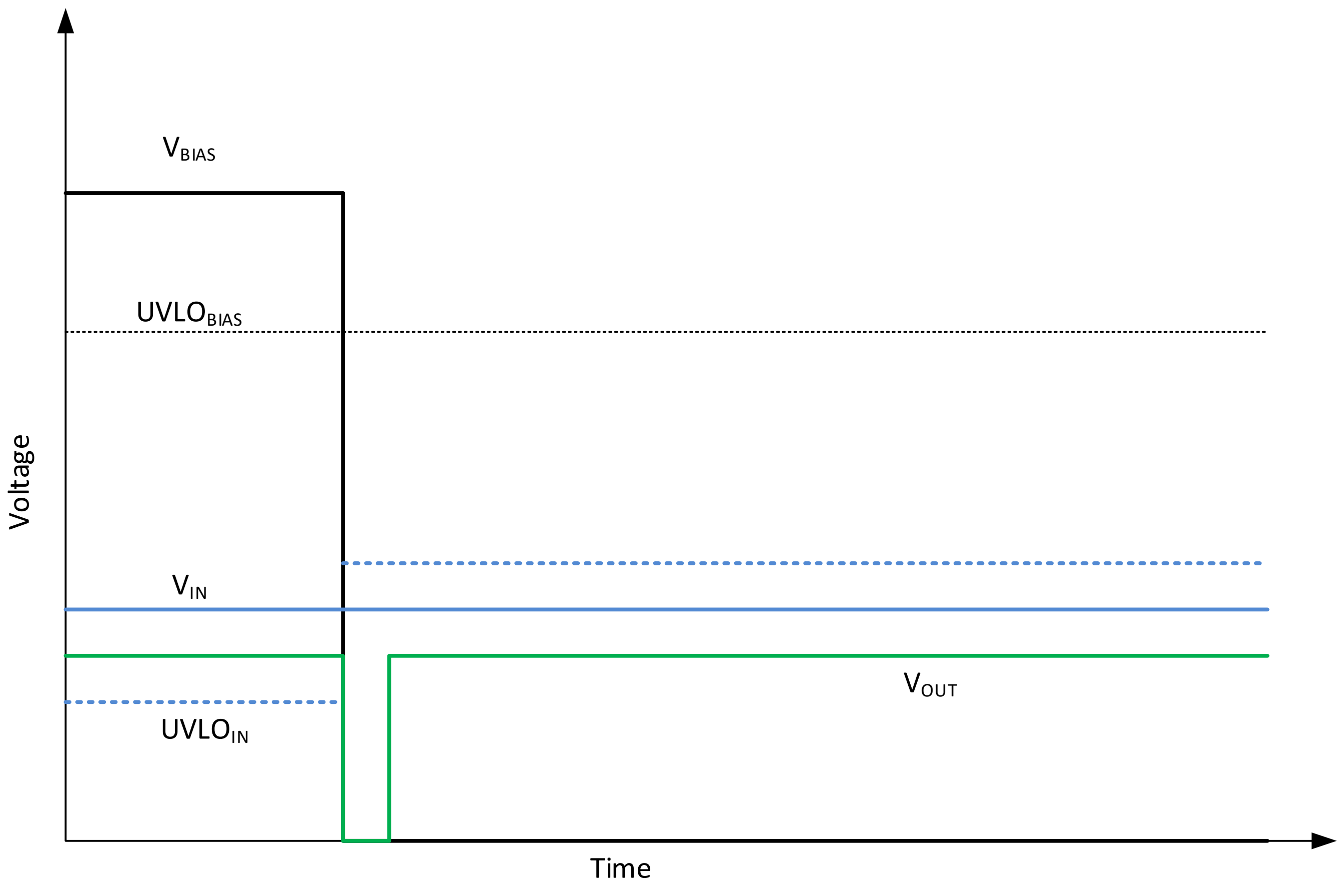


图 8-3. $UVLO_{IN}$ and $UVLO_{BIAS}$ Interaction

8.1.3 Dropout Voltage (V_{DO})

Generally speaking, the dropout voltage often refers to the minimum voltage difference between the input and output voltage ($V_{DO} = V_{IN} - V_{OUT}$) that is required for regulation. When V_{IN} drops to or below the set V_{DO} for the given load current, the device functions as a resistive switch and does not regulate output voltage. When the device is operating in dropout, the output voltage tracks the input voltage and the dropout voltage (V_{DO}) is proportional to the output current because the device is operating as a resistive switch. Operating the device at or near dropout significantly degrades the device transient performance and PSRR. Maintaining sufficient V_{OpHr} significantly improves the device transient performance and PSRR.

备注

If the minimum BIAS rail is set 3.2 V above the REF pin voltage with the internal charge pump disabled, the pass transistor cannot be in BIAS-to-OUT dropout, thus leaving only the IN-to-OUT dropout conditions to be considered. For other operating conditions, see the *Undervoltage Lockout (UVLO) Operation* section.

8.1.4 Input and Output Capacitor Requirements (C_{IN} and C_{OUT})

The TPS7A57 is designed and characterized for operation with ceramic capacitors of 22 µF or greater (15 µF or greater of capacitance) at the output and 10 µF or greater (5 µF or greater of capacitance) at the input. Use at least a 10-µF capacitor at the input to minimize input impedance. Place the input and output capacitors as near as practical to the respective input and output pins in order to minimize trace parasitics. If the trace inductance from the input supply to the TPS7A57 is high, a fast current transient can cause V_{IN} to ring above the absolute maximum voltage rating and damage the device. This situation can be mitigated by adding additional input capacitors to dampen the ringing, thereby keeping any voltage spike below the device absolute maximum ratings.

备注

Because of its wide bandwidth, the LDO error amplifier may react faster than the output capacitor. In such a case, the load behavior appears directly on the LDO supply, potentially dragging the supply down. To avoid such behaviors, minimize both ESR and ESL present on the output; see the *Recommended Operating Conditions* table.

8.1.5 Recommended Capacitor Types

The device is designed to be stable using low equivalent series resistance (ESR) and low equivalent series inductance (ESL) ceramic capacitors at the input, output, and noise-reduction pin. Multilayer ceramic capacitors have become the industry standard for these types of applications and are recommended, but must be used with good judgment. Ceramic capacitors that employ X7R-, X5R-, and COG-rated dielectric materials provide relatively good capacitive stability across temperature. The use of Y5V-rated capacitors is discouraged because of large variations in capacitance.

Regardless of the ceramic capacitor type selected, ceramic capacitance varies with operating voltage and temperature. Make sure to derate ceramic capacitors by at least 50%. The input and output capacitors recommended herein account for a capacitance derating of approximately 50%, but at high V_{IN} and V_{OUT} conditions (V_{IN} = 5.5 V to V_{OUT} = 5.0 V) and temperature extremes, the derating can be greater than 50%, and must be taken into consideration.

The device requires input, output, and noise-reduction capacitors for proper operation of the LDO. Use the nominal or larger than nominal input and output capacitors as specified in the *Recommended Operating Conditions* table. Place input and output capacitors as close as possible to the corresponding pin and make the capacitor GND connections are as close as possible to the device GND pin to shorten transient currents on the return path. Using a larger input capacitor or a bank of capacitors with various values is always good design practice to counteract input trace inductance, improve transient response, and reduce input ripple and noise. Similarly, multiple capacitors on the output reduce charge pump ripple and optimize PSRR; see the *Optimizing Noise and PSRR* section.

Use the nominal noise-reduction $C_{NR/SS}$ capacitor because using a larger C_{NRSS} capacitor can lengthen the start-up time as mentioned previously.

8.1.6 Soft-Start, Noise Reduction (NR/SS Pin), and Power-Good (PG Pin)

The NR/SS pin has the dual function of controlling the soft-start time and reducing the noise generated by the internal band-gap reference and the external resistor R_{REF}. The NR/SS capacitor ($C_{NR/SS}$) reduces the output noise to very low levels and sets the output ramp rate to limit inrush current.

The device features a programmable, monotonic, voltage-controlled, soft-start circuit that is set to work with an external capacitor ($C_{NR/SS}$). In addition to the soft-start feature, the $C_{NR/SS}$ capacitor also lowers the output voltage noise of the LDO. The soft-start feature can be used to eliminate power-up initialization problems. The controlled output voltage ramp also reduces peak inrush current during start up, minimizing start-up transients to the input power bus.

To achieve a monotonic start up, the device output voltage tracks the $V_{NR/SS}$ reference voltage until this reference reaches its set value (the set output voltage). The $V_{NR/SS}$ reference voltage is set by the R_{REF} resistor and, during start up, the device uses a fast charging current (I_{FAST_SS}), as shown in 图 8-4, to charge the $C_{NR/SS}$ capacitor.

备注
Any leakage on the NR/SS and REF pins directly impacts the accuracy of the reference voltage.

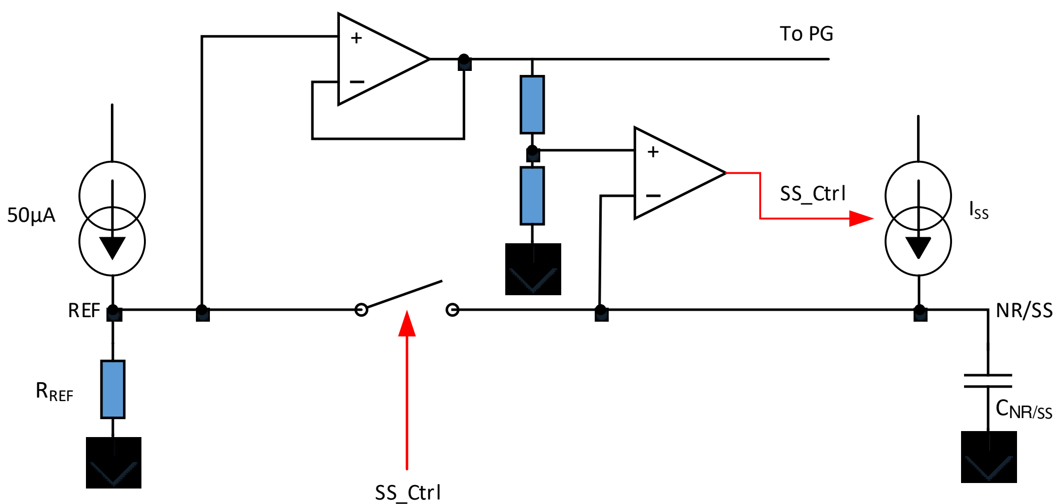


图 8-4. Simplified Soft-Start Circuit

The 200-µA (typical) $I_{NR/SS}$ current quickly charges $C_{NR/SS}$ until its voltage reaches approximately 97% of the set output voltage, then the I_{SS} current turns off, the switch between REF and NR/SS closes, and only the I_{REF} current continues to charge $C_{NR/SS}$ to its set output voltage level.

备注
The discharge pulldown resistor on NR/SS (see the *Functional Block Diagram*) is engaged when any of the GND referenced UVLOs have been tripped, or when any faults occur (overtemp, PORs, IREF bad, or OTP error) and the NRSS pin is above 50 mV.

The soft-start ramp time depends on the fast start-up ($I_{NR/SS}$) charging current, the reference current (I_{REF}), $C_{NR/SS}$ capacitor value, and the targeted output voltage ($V_{OUT(target)}$). *方程式 3* calculates the soft-start ramp time.

$$\text{Soft-start time } (t_{SS}) = (V_{OUT(target)} \times C_{NR/SS}) / (I_{SS}) \quad (3)$$

The I_{SS} current is provided in the *Typical Characteristics* section and has a value of 200 µA (typical). The I_{REF} current has a value of 50 µA (typical). The remaining 3% of the start-up time is determined by the R_{REF} × $C_{NR/SS}$ time constant. 图 8-5 shows the PG threshold at start up.

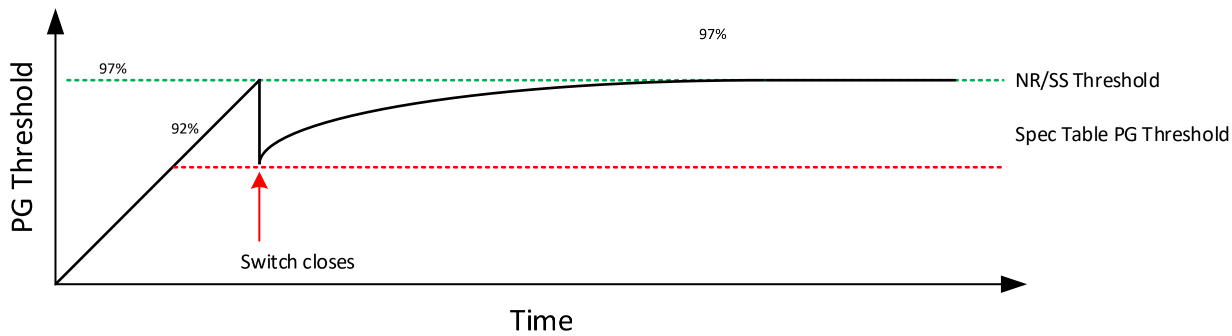


图 8-5. PG Threshold During Start-Up

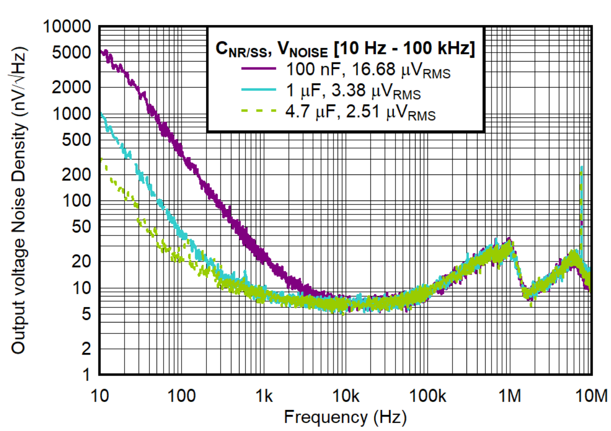
The output voltage noise can be lowered significantly by increasing the $C_{NR/SS}$ capacitor. The $C_{NR/SS}$ capacitor and R_{REF} resistor form a low-pass filter (LPF) that filters out noise from the V_{REF} voltage reference, thereby reducing the device noise floor. The LPF is a single-pole filter and 方程式 4 calculates the LPF cutoff frequency. Increasing the $C_{NR/SS}$ capacitor can significantly lower output voltage noise, however, doing so lengthens start-up time. For low-noise applications, use a 4.7-µF $C_{NR/SS}$ for optimal noise and start-up time trade off.

$$\text{Cutoff Frequency } (f_{cutoff}) = 1 / (2 \times \pi \times R_{REF} \times C_{NR/SS}) \quad (4)$$

备注

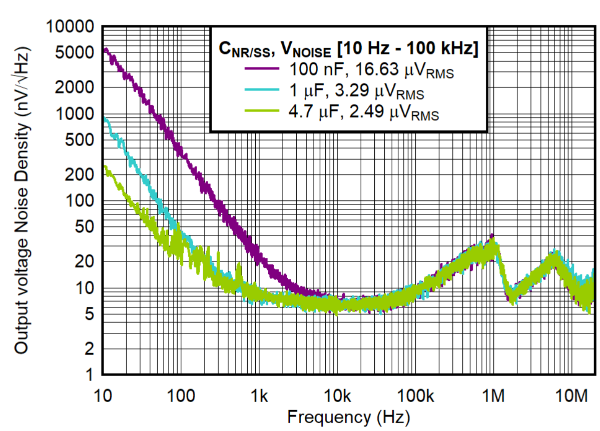
Current limit can be entered during start up with a small $C_{NR/SS}$ and large C_{OUT} because V_{OUT} no longer tracks the soft-start ramp.

图 8-6 and 图 8-7 show the impact of the $C_{NR/SS}$ capacitor on the LDO output voltage noise.



C_{IN} = 4.7 µF, C_{OUT} = 22 µF, V_{CP_EN} = V_{IN}, V_{IN} = 5.3 V, V_{OUT} = 5 V, I_{OUT} = 5 A

图 8-6. Output Voltage Noise Density vs $C_{NR/SS}$ With Charge Pump Enabled



C_{IN} = 4.7 µF, C_{OUT} = 22 µF, V_{IN} = 5.3 V, V_{OUT} = 5 V, V_{BIAS} = 11 V

图 8-7. Output Voltage Noise Density vs $C_{NR/SS}$ With Charge Pump Disabled

8.1.7 Optimizing Noise and PSRR

Noise can be generally defined as any unwanted signal combining with the desired signal (such as the regulated LDO output) that results in degraded power-supply source quality. Noise can be easily noticed in audio as a hissing or popping sound. Extrinsic and intrinsic are the two basic groups that noise can be categorized into. Noise produced from an external circuit or natural phenomena such as 50 to 60 hertz power-line noise (spikes), along with its harmonics, is an excellent representative of extrinsic noise. Intrinsic noise is produced by components within the device circuitry such as resistors and transistors. For this device, the two dominating sources of intrinsic noise are the error amplifier and the internal reference voltage (V_{REF}). Another term that sometimes combines with extrinsic noise is PSRR, which refers to the ability of the circuit or device to reject or filter out input supply noise and is expressed as a ratio of output voltage noise ripple to input voltage noise ripple.

Optimize the device intrinsic noise and PSRR by carefully selecting:

- $C_{NR/SS}$ for the low-frequency range up to the device bandwidth
- C_{OUT} for the high-frequency range close to and higher than the device bandwidth
- Operating headroom, V_{IN} – V_{OUT} (V_{OpHr}), mainly for the low-frequency range up to the device bandwidth, but also for higher frequencies to a less effect

The device noise performance can be significantly improved by using a larger $C_{NR/SS}$ capacitor to filter out noise coupling from the input into the device V_{REF} reference. This coupling is especially apparent from low frequencies up to the device bandwidth. The low-pass filter formed by $C_{NR/SS}$ and R_{REF} can be designed to target low-frequency noise originating in the input supply. One downside of a larger $C_{NR/SS}$ capacitor is a longer start-up time. The device unity-gain configuration eliminates the noise performance degradation that other LDOs suffer from because of their feedback network. Furthermore, increasing the device load current has little to no effect on the device noise performance.

Further improvement to the device noise at a higher frequency range than the device bandwidth can be achieved by using a larger C_{OUT} capacitor. However, a larger C_{OUT} increases inrush current and slows down the device transient response.

These behaviors are described in the *Typical Characteristics* section. 图 6-17 and 图 6-19 list the measured 10-Hz to 100-kHz RMS noise for a 5-V device and a 0.5-V output voltage with a 300-mV headroom for different $C_{NR/SS}$ and C_{OUT} conditions with a 5-A load current. 表 8-2 and 表 8-3 list the typical output noise for these capacitors.

Increasing the operational headroom between V_{IN} and V_{OUT} has little to no effect on improving noise performance. However, this increase does improve PSRR significantly for frequency ranges up to the device bandwidth. Higher headroom can also improve transient performance of the device as well. Although C_{OUT} has little to no affect on improving PSRR at low frequency, C_{OUT} can improve PSRR for higher frequencies beyond the device bandwidth. A larger C_{OUT} can also lengthen start-up time and increase start-up inrush current. A combination of capacitors, such as 470 μF || 22 μF is more effective because a combination provides lower ESR and ESL. This behavior is illustrated in 图 6-12.

表 8-2. Output Noise for 0.5-V_{OUT} vs C_{OUT}, and Typical Start-Up Time

V_n (μV_{RMS}), 10-Hz to 100-kHz BW	$C_{NR/SS}$ (µF)	C_{OUT} (µF)	START-UP TIME (ms)
2.4	4.7	22	11.75
2.48	4.7	470	11.75

表 8-3. Output Noise for 5-V_{OUT} vs $C_{NR/SS}$, C_{OUT}, and Typical Start-Up Time for V_{CP_EN} = 5.3 V

V_n (μV_{RMS}), 10-Hz to 100-kHz BW	$C_{NR/SS}$ (µF)	C_{OUT} (µF)	START-UP TIME (ms)
16.68	0.1	22	2.5
3.38	1	22	25
2.51	4.7	22	117.5

8.1.8 Adjustable Operation

As shown in 图 8-8, the output voltage of the device can be set using a single external resistor (R_{REF}).

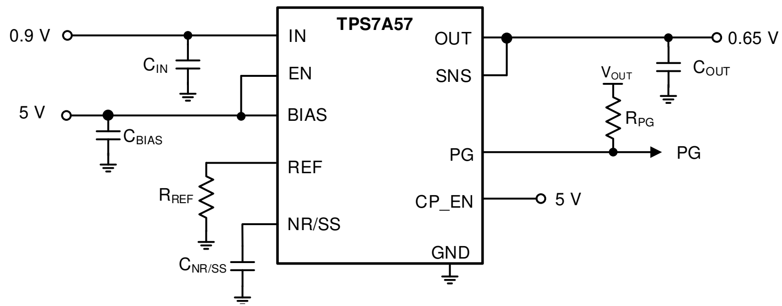


图 8-8. Typical Circuit

Use 方程式 5 to calculate the R_{REF} value needed for the desirable output voltage.

$$V_{OUT} = I_{REF(NOM)} \times R_{REF} \quad (5)$$

表 8-4 shows the recommended R_{REF} resistor values to achieve several common rails using a standard 1%-tolerance resistor.

表 8-4. Recommended R_{REF} Values

TARGETED OUTPUT VOLTAGE (V)	R_{REF} (kΩ)[1]	CALCULATED OUTPUT VOLTAGE (V)
0.5	10.0	0.500
0.6	12.1	0.605
0.7	14.0	0.700
0.8	16.2	0.810
0.9	18.2	0.910
1.0	20.0	1.000
1.2	24.3	1.215
1.5	30.1	1.505
2.5	49.9	2.495
3.0	60.4	3.020
3.3	66.5	3.325
3.6	71.5	3.575
4.7	95.3	4.765
5.0	100.0	5.000

(1) 1% resistors.

8.1.9 Load Transient Response

The load-step transient response is the LDO output voltage response to load current, whereby output voltage regulation is maintained. There are two key transitions during a load transient response: the transition from a light to a heavy load, and the transition from a heavy to a light load. The regions shown in 图 8-9 are broken down in this section. Regions A, E, and H are where the output voltage is in steady-state regulation.

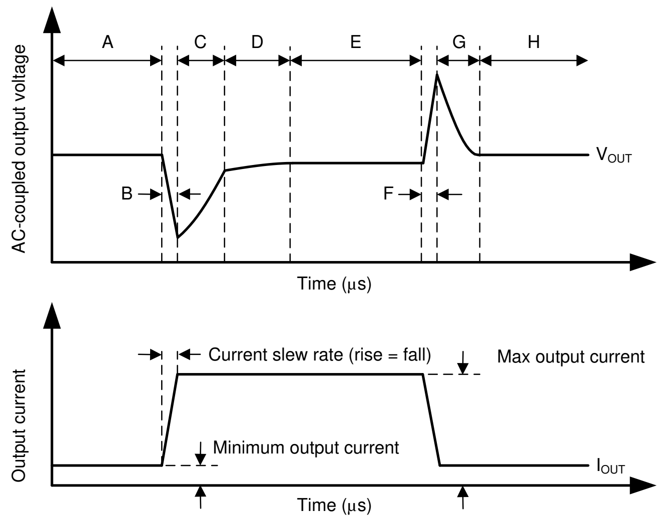


图 8-9. Load Transient Waveform

During transitions from a light load to a heavy load:

- The initial voltage dip is a result of the depletion of the output capacitor charge and parasitic impedance to the output capacitor (region B)
- Recovery from the dip results from the LDO increasing its sourcing current, and leads to output voltage regulation (region C)

During transitions from a heavy load to a light load:

- The initial voltage rise results from the LDO sourcing a large current, and leads to the output capacitor charge to increase (region F)
- Recovery from the rise results from the LDO decreasing its sourcing current in combination with the load discharging the output capacitor (region G)

Transitions between current levels changes the internal power dissipation because the device is a high-current device (region D). The change in power dissipation changes the die temperature during these transitions, and leads to a slightly different voltage level. This temperature-dependent output voltage level shows up in the various load transient responses.

A larger output capacitance reduces the peaks during a load transient but slows down the response time of the device. A larger dc load also reduces the peaks because the amplitude of the transition is lowered and a higher current discharge path is provided for the output capacitor.

备注

The TPS7A57, with its high bandwidth, may react faster than the output capacitors. Make sure that there is sufficient capacitance at the input of the LDO.

8.1.10 Current Limit and Foldback Behavior

图 8-10 shows the foldback current limit behavior for output voltages ranging from 0.5 V to 5 V.

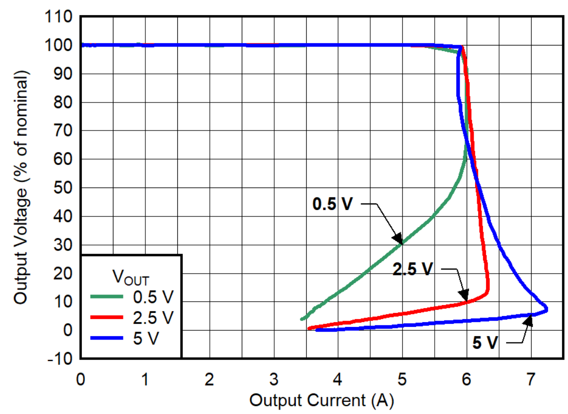


图 8-10. Current Limit Foldback Behavior

8.1.11 Charge Pump Operation

As discussed in the *Charge Pump Enable and BIAS Rail* section, the internal charge pump can be enabled or disabled using the CP_EN pin, allowing operation as low as 1.1 V without a BIAS rail.

The CP_EN pin voltage threshold and hysteresis are defined in the *Electrical Characteristics* table.

Depending on the circuit implementation, the internal charge pump is powered from either the IN or the BIAS rails. This pin is not designed to be digitally controlled with a digital I/O pin, but is instead intended to be tied on the printed circuit board (PCB) to an analog rail.

Although not intended to be controlled dynamically, the CP_EN pin can be controlled by using a low impedance source and ensuring adequate sequencing between EN and CP_EN because the CP_EN pin is latched when the EN pin is turned on and only an EN reset or a power cycle clears and resets the CP_EN latch.

图 8-11 shows the switching frequency of the charge pump at no-load and full load.

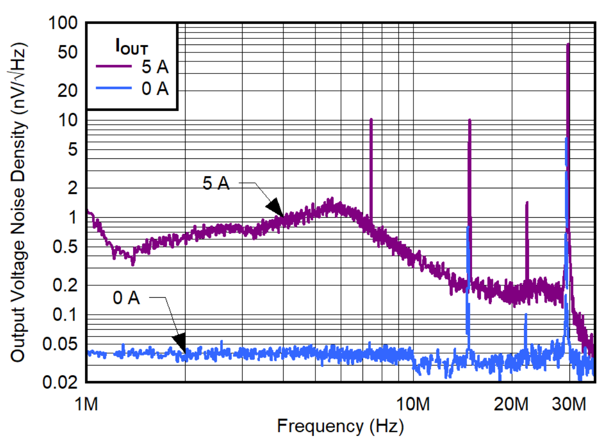


图 8-11. Charge Pump Noise

8.1.12 Sequencing

There is no sequencing requirement between IN, BIAS, and EN. CP_EN is an analog signal and must be connected to either IN, BIAS, or GND.

As with devices having an internal MUX and charge pump, a false PG can be triggered during shutdown if the BIAS rail is faster than the IN rail to discharge.

As shown in 图 8-12, when the bias rail decreases below $V_{UVLO(BIAS)}$, the internal MUX between IN and BIAS switches over and the LDO is fully powered from the IN rail.

When the BIAS rail goes below UVLO(BIAS) with the IN rail greater than 1.1 V with the charge pump enabled, the LDO may restart because IN is still a valid condition for operations.

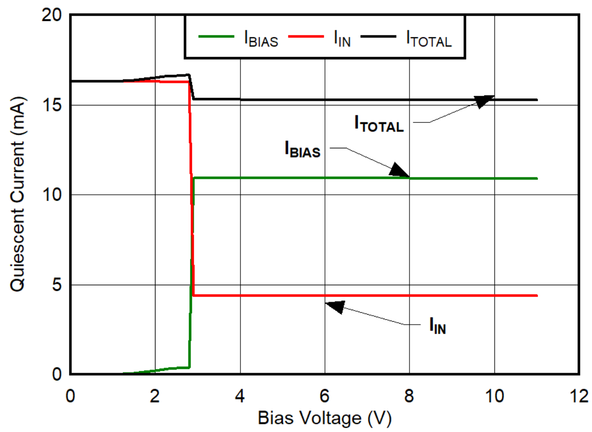


图 8-12. Total Quiescent Current vs BIAS

8.1.13 Power-Good Functionality

As described in the *Functional Block Diagram*, the PG pin is a open-drain MOSFET driven by a Schmitt trigger. The Schmitt trigger compares the SNS pin voltage to a preselected voltage equal to 90% that of the reference voltage.

As mentioned in the *Recommended Operating Conditions* table, the pullup resistance must be between 10 kΩ and 100 kΩ for optimal performance. If the PG functionality is not desired, the PG pin can either be left floating or connected to GND.

There are two UVLO circuits present on the BIAS rail, one referenced to GND ($V_{UVLO(BIAS)}$) and one referenced to V_{REF} ($V_{UVLO(BIAS)}$ – V_{REF}). A false PG event can occur as a result of logic priorities when the charge pump is disabled.

To eliminate any false PG events, consider setting V_{BIAS} 3.2 V above V_{OUT}.

表 8-5 describes the various UVLO behaviors.

表 8-5. UVLO Triggered PG Events

V_{IN}	$V_{UVLO(BIAS)}$ RISING	$V_{UVLO(BIAS)}$ FALLING	$V_{UVLO(BIAS)}$ – V_{REF} RISING	$V_{UVLO(BIAS)}$ – V_{REF} FALLING
0.5 V	2.8 V	2.685 V	2.1 + 0.5 = 2.6 V	1.86 + 0.5 = 2.36 V
0.7 V	2.8 V	2.685 V	2.1 + 0.7 = 2.8 V	1.86 + 0.7 = 2.56 V
1.4 V	2.8 V	2.685 V	2.1 + 1.4 = 3.5 V	1.86 + 1.4 = 3.26 V
5.2 V	2.8 V	2.685 V	2.1 + 5.2 = 7.3 V	1.86 + 5.2 = 7.06 V

8.1.14 Output Impedance

Output impedance can be modeled, as shown in 图 8-13, as an ideal voltage source followed by a series R (R_{OUT}) and series L (L_{OUT}) output.

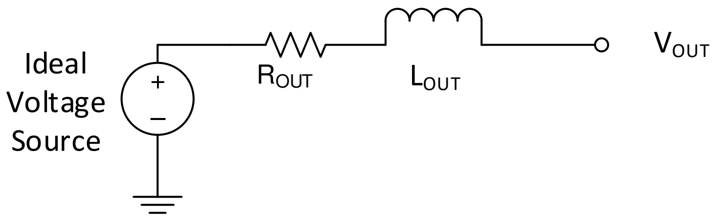


图 8-13. Output Impedance Model

Output impedance curves were measured using the EVM and are provided for the following conditions:

1. 图 8-14, 图 8-15, and 图 8-16 are provided for the 5.5-V_{IN}, 5-V_{OUT}, and I_{OUT} = 200-mA, 500-mA, and 5-A conditions
2. 图 8-17 is provided for the 0.9-V_{IN}, 0.5-V_{OUT}, and I_{OUT} = 4.6-A conditions
3. 图 8-18 to 图 8-21 are provided for the 0.75 -V_{IN}, 0.5-V_{OUT}, 3-V_{BIAS}, and I_{OUT} = 20-mA, 200-mA, 500-mA, and 1-A conditions.

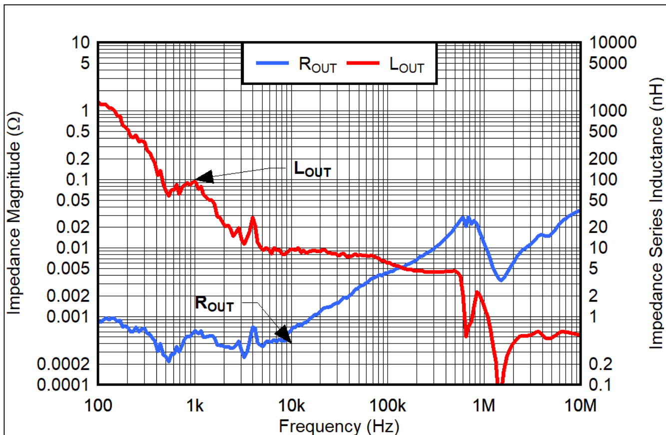


图 8-14. V_{IN} = 5.5 V, V_{OUT} = 5 V, V_{BIAS} = 8 V, CP_EN = 0, I_{OUT} = 200 mA

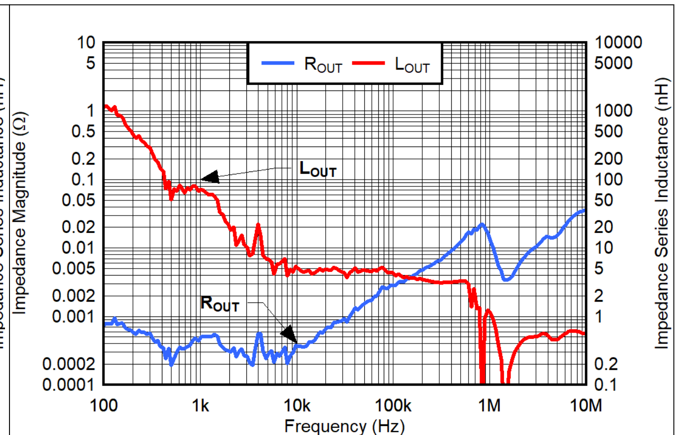


图 8-15. V_{IN} = 5.5 V, V_{OUT} = 5 V, V_{BIAS} = 8 V, CP_EN = 0, I_{OUT} = 500 mA

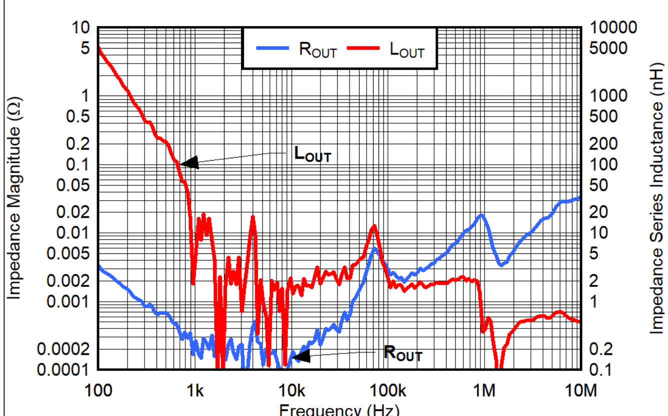


图 8-16. V_{IN} = 5.5 V, V_{OUT} = 5 V, V_{BIAS} = 8 V, CP_EN = 0, I_{OUT} = 5 A

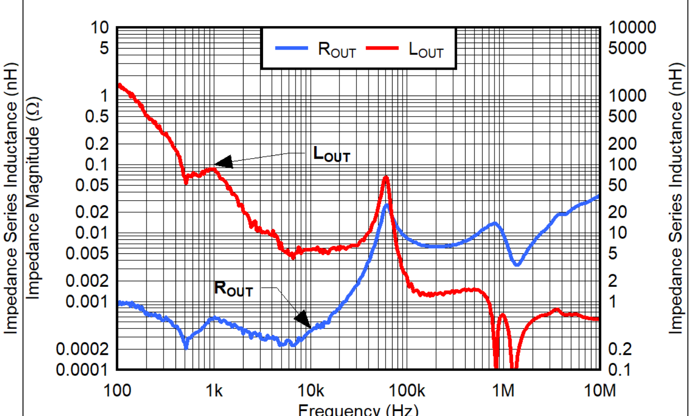


图 8-17. V_{IN} = 0.9 V, V_{BIAS} = 3 V, V_{OUT} = 0.5 V , CP_EN = 0, I_{OUT} = 4.6 A

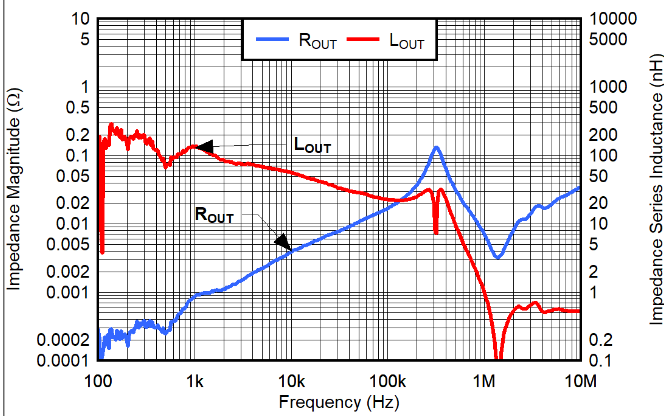


图 8-18. V_{IN} = 0.75 V, V_{BIAS} = 3 V, V_{OUT} = 0.5 V , CP_EN = 0, I_{OUT} = 20 mA

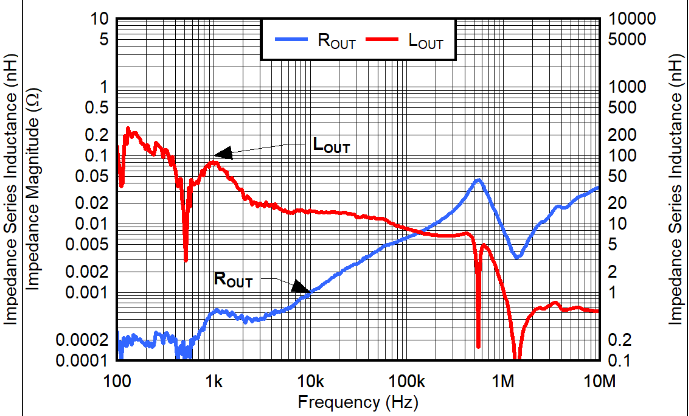


图 8-19. V_{IN} = 0.75 V, V_{BIAS} = 3 V, V_{OUT} = 0.5 V, CP_EN = 0, I_{OUT} = 100 mA

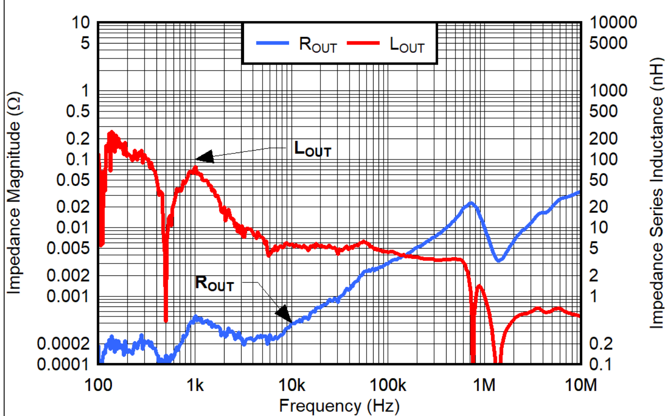


图 8-20. V_{IN} = 0.75 V, V_{BIAS} = 3 V, V_{OUT} = 0.5 V, CP_EN = 0, I_{OUT} = 500 mA

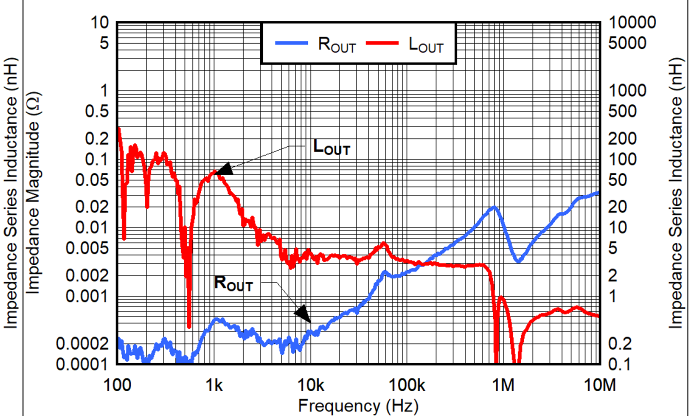


图 8-21. V_{IN} = 0.75 V, V_{BIAS} = 3 V, V_{OUT} = 0.5 V, CP_EN = 0, I_{OUT} = 1 A

表 8-6 provides a summary of the tested conditions described in this section.

表 8-6. Model for Tested Conditions Summary

V_{IN}	V_{OUT}	V_{BIAS}	I_{OUT}	CP_EN	R_{OUT}	L_{OUT}
0.75 V	0.5 V	3 V	20 mA	Off	200 μΩ	0.5 nH
0.75 V	0.5 V	3 V	200 mA	Off	200 μΩ	0.5 nH
0.75 V	0.5 V	3 V	500 mA	Off	200 μΩ	0.5 nH
0.75 V	0.5 V	3 V	1 A	Off	200 μΩ	0.5 nH
0.9 V	0.5 V	3 V	4.6 A	Off	200 μΩ	0.5 nH
5.5 V	5 V	8 V	200 mA	Off	400 μΩ	0.5 nH
5.5 V	5 V	8 V	500 mA	Off	300 μΩ	0.5 nH
5.5 V	5 V	8 V	5 A	Off	200 μΩ	0.5 nH

8.1.15 Paralleling for Higher Output Current and Lower Noise

Achieving higher output current and lower noise is achievable by paralleling two or more LDOs. Implementation must be carefully planned out to optimize performance and minimize output current imbalance.

Because the TPS7A57 output voltage is set by a resistor driven by a current source, the REF resistor and capacitor must be adjusted as per the following:

$$R_{REF} = V_{OUT\_TARGET} / (n \times I_{REF}) \quad (6)$$

$$C_{NR/SS\_parallel} = n \times C_{NR/SS\_single} \quad (7)$$

where:

- n is the number of LDOs in parallel
- I_{REF} is the REF current as provided in the *Electrical Characteristics* table
- $C_{NR/SS}$_single is the NR/SS capacitor for a single LDO. Note that each LDO must have its own $C_{NR/SS}$ capacitor.

When connecting the IN pins together, and with the LDO being a buffer, the current imbalance is only affected by the error offset voltage of the error amplifier. As such, the current imbalance can be expressed as:

$$\varepsilon_I = V_{OS} \times 2 \times R_{BALLAST} / (R_{BALLAST}^2 - \Delta R_{BALLAST}^2) \quad (8)$$

where:

- ε_I is the current imbalance
- V_{OS} is the LDO error offset voltage
- $R_{BALLAST}$ is the ballast resistor
- $\Delta R_{BALLAST}$ is the deviation of the ballast resistor value from the nominal value

With the typical offset voltage of 200 μV, the ballast resistor must be 2 mΩ or greater (as shown in 图 8-22), considering no error from the design of the PCB ballast resistor ($\Delta R_{BALLAST}$ = 0 Ω) and a 100-mA maximum current imbalance.

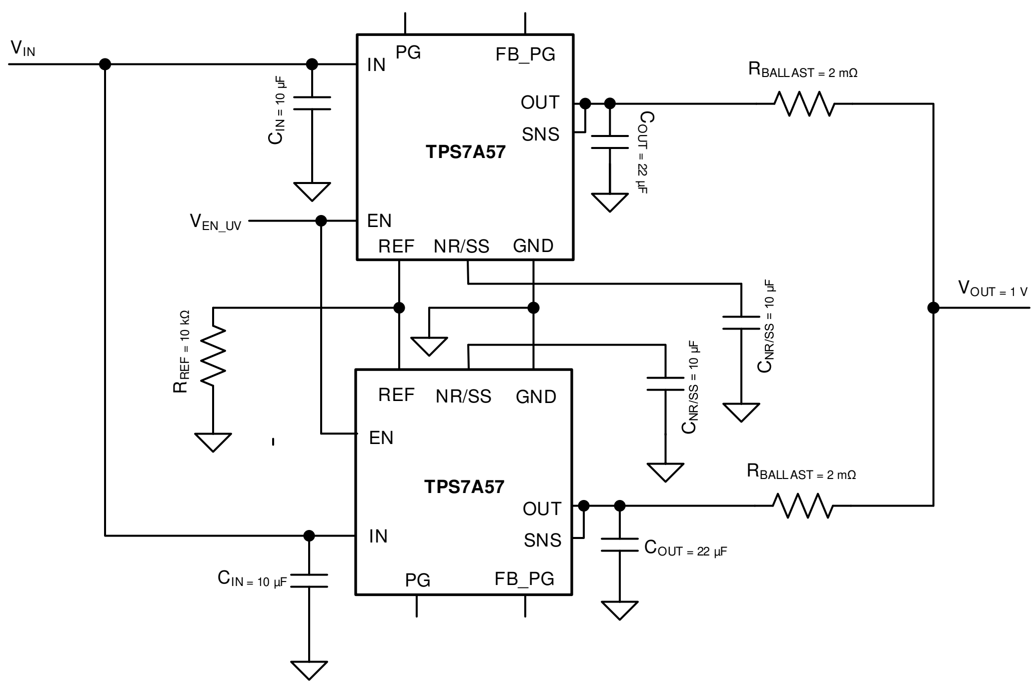


图 8-22. Paralleling Multiple TPS7A57 Devices

Using the configuration described, the LDO output noise is reduced by:

$$e_{O\_parallel} = (1 / \sqrt{n}) \times e_{O\_single} \quad (9)$$

where:

- n is the numbers of LDOs in parallel
- e_{O_single} is the output noise density from a single LDO

- $e_{O\_parallel}$ is the output noise density for the resulting parallel LDO

In 图 8-22, the noise is reduced by $1/\sqrt{2}$.

8.1.16 Current Mode Margining

Output voltage margining is a technique that allows a circuit to be evaluated for how well changes are tolerated in the power supply. This test is typically performed by adjusting the supply voltage to a fixed percentage above and below its nominal output voltage.

This section discusses the implementation of a voltage margining application using the TPS7A57. A margining target of ±2.5% is used to demonstrate the chosen implementation.

图 8-23 shows a simplified visualization of the TPS7A57 REF pin with a current DAC.

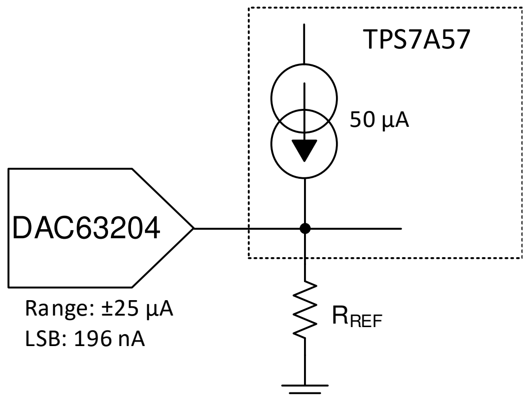


图 8-23. Simplified Margining Schematic

表 8-7 summarizes the design requirements.

表 8-7. Design Requirement

PARAMETER	Design Values
V_{IN}	2.5 V
V_{OUT}	1.8 V nominal with ±2.5% margining
$C_{NR/SS}$	4.7 µF
R_{REF}	36 kΩ
DAC I_{OUT} range	±25 µA

In this example, the output voltage is set to a nominal 1.8 V using 36 kΩ at the REF pin to GND. 方程式 10 calculates the R_{REF} resistor value.

$$R_{REF} = V_{OUT} / I_{REF} \tag{10}$$

The DAC63204, a 4-channel, 12-bit voltage and current output DAC with I^2C, was selected and programmed into the current-output mode with an output range set to ±25 µA. In conjunction with the 8-bit current DAC resolution, this output range allows a minimum step size (or LSB) of approximately 196 nA. Into the 36-kΩ resistor, the LSB translates into a 7-mV voltage resolution or 0.38% of the nominal 1.8-V targeted voltage. To achieve the full ±2.5% swing around the nominal voltage, the DAC63204 must source or sink ±1.25 µA.

The current flowing through R_{REF} changes to 51.25 µA and 48.75 µA and adjusts the output voltage to 1.845 V and 1.75 V, respectively.

图 8-24 and 图 8-25 show the current margining results.

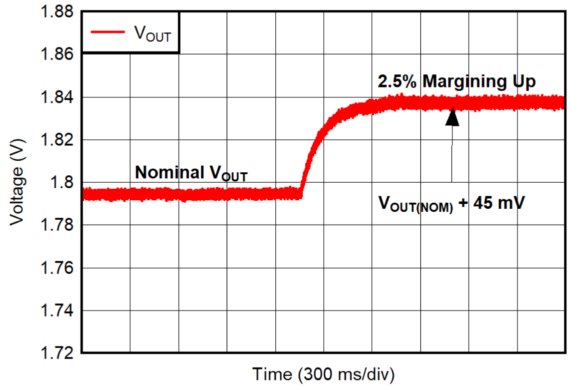


图 8-24. Margining Up

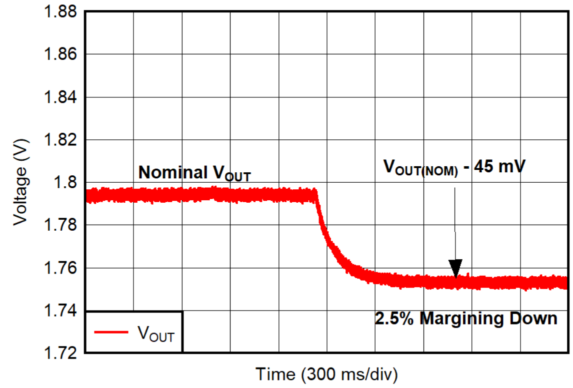


图 8-25. Margining Down

When implementing voltage margining with this LDO, a time constant is associated with its response. This RC time constant is a result of the parallel combination of R_{REF} and $C_{NR/SS}$, see 图 8-23. This RC effect is illustrated in 图 8-24 and 图 8-25.

方程式 11 calculates the time constant for this implementation:

$$\tau = R_{REF} \times C_{NR/SS} \tag{11}$$

where:

- R_{REF} is 36 kΩ
- $C_{NR/SS}$ is 4.7 µF
- τ = 169 ms

8.1.17 Voltage Mode Margining

Output voltage margining is a technique that allows a circuit to be evaluated for how well changes are tolerated in the power supply. This test is typically performed by adjusting the supply voltage to a fixed percentage above and below its nominal output voltage.

This section discusses the implementation of a voltage mode margining application using the TPS7A57. A margining target of ±5% is used to demonstrate the chosen implementation.

图 8-26 shows a simplified visualization of the TPS7A57 REF pin with a voltage DAC.

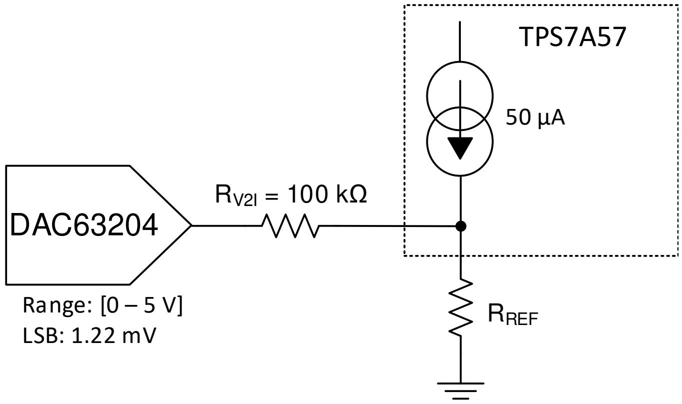


图 8-26. Simplified Voltage Mode Margining Schematic

表 8-7 summarizes the design requirements.

表 8-8. Design Requirement

PARAMETER	DESIGN VALUES
V_{IN}	2.5 V
V_{OUT}	1.8 V nominal with ±5% margining
$C_{NR/SS}$	4.7 µF
R_{REF}	36 kΩ
DAC V_{OUT} range	1.432 V to 2.108 V

In this example, the output voltage is set to a nominal 1.8-V using a 36-kΩ resistor at the REF pin to GND. 方程式 12 calculates the value for the R_{REF} resistor.

$$R_{REF} = V_{OUT} / I_{REF} \quad (12)$$

The DAC63204, a 4-channel, 12-bit voltage and current output DAC with I²C, was selected and programmed into the voltage-output mode with an output range set between 1.432 V and 2.108 V. In conjunction with the 12-bit voltage DAC resolution, this output range allows a minimum step size (or LSB) of approximately 1.22 mV or 122 µA when the voltage-to-input (V2I) conversion or R_{V2I} (100 kΩ) is taken into consideration. Into the 36-kΩ resistor, this LSB translates into a 0.44-mV voltage resolution or approximately 0.025% of the nominal 1.8-V targeted voltage. To achieve the full ±5% swing around the nominal voltage, the DAC63204 must source 3.1 µA or sink 3.7 µA.

The current flowing through R_{REF} changes to 53.1 µA and 46.3 µA, thus adjusting the output voltage to 1.88 V and 1.7 V respectively.

节 8.1.17 and 图 8-28 show the voltage margining results.

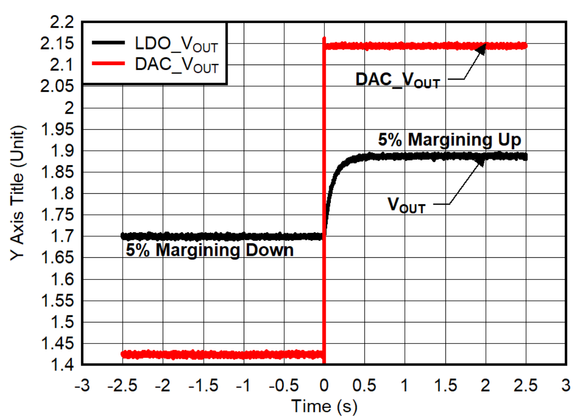


图 8-27. Margining From –5% to +5%

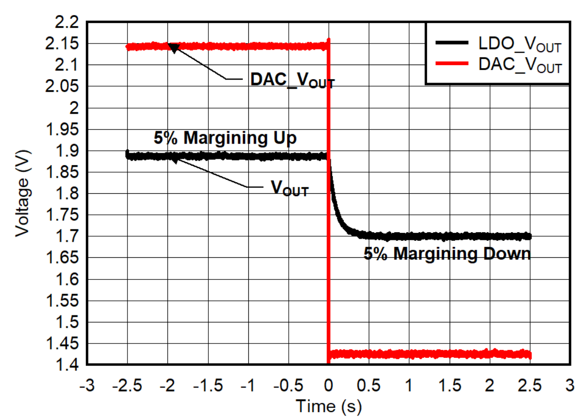


图 8-28. Margining from +5% to –5%

When implementing voltage margining with this LDO, there is a time constant associated with its response. This RC time constant originates from the parallel combination of R_{REF} and $C_{NR/SS}$. 节 8.1.17 and 图 8-28 show this RC effect.

方程式 13 calculates the time constant for this implementation:

$$\tau = R_{REF} \times C_{NR/SS} \quad (13)$$

where:

- R_{REF} is 36 kΩ
- $C_{NR/SS}$ is 4.7 µF
- τ = 169 ms

8.1.18 Power Dissipation (P_D)

Circuit reliability demands that proper consideration be given to device power dissipation, location of the circuit on the printed circuit board (PCB), and correct sizing of the thermal plane. The PCB area around the regulator must be as free as possible of other heat-generating devices that cause added thermal stresses.

As a first-order approximation, power dissipation in the regulator depends on the input-to-output voltage difference and load conditions. 方程式 14 calculates P_D:

$$P_D = (V_{OUT} - V_{IN}) \times I_{OUT} \tag{14}$$

备注

Power dissipation can be minimized, and thus greater efficiency achieved, by proper selection of the system voltage rails. Proper selection allows the minimum input-to-output voltage differential to be obtained. The low dropout of the device allows for maximum efficiency across a wide range of output voltages.

The primary heat conduction path for the package is through the thermal pad to the PCB. Solder the thermal pad to a copper pad area under the device. This pad area contains an array of plated vias that conduct heat to any inner plane areas or to a bottom-side copper plane.

The power dissipation through the device determines the junction temperature (T_J) for the device. Power dissipation and junction temperature are most often related by the junction-to-ambient thermal resistance ($R_{\theta JA}$) of the combined PCB and device package and the temperature of the ambient air (T_A), according to 方程式 15. The equation is rearranged for output current in 方程式 16.

$$T_J = T_A = (R_{\theta JA} \times P_D) \tag{15}$$

$$I_{OUT} = (T_J - T_A) / [R_{\theta JA} \times (V_{IN} - V_{OUT})] \tag{16}$$

Unfortunately, this thermal resistance ($R_{\theta JA}$) is highly dependent on the heat-spreading capability built into the particular PCB design, and therefore varies according to the total copper area, copper weight, and location of the planes. The $R_{\theta JA}$ recorded in the *Thermal Information* table is determined by the JEDEC standard, PCB, and copper-spreading area, and is only used as a relative measure of package thermal performance. For a well-designed thermal layout, $R_{\theta JA}$ is actually the sum of the RTE package junction-to-case (bottom) thermal resistance ($R_{\theta JCbot}$) plus the thermal resistance contribution by the PCB copper.

8.1.19 Estimating Junction Temperature

The JEDEC standard now recommends the use of psi (Ψ) thermal metrics to estimate the junction temperatures of the LDO when in-circuit on a typical PCB board application. These metrics are not strictly speaking thermal resistances, but rather offer practical and relative means of estimating junction temperatures. These psi metrics are determined to be significantly independent of the copper-spreading area. The key thermal metrics (Ψ_{JT} and Ψ_{JB}) are used in accordance with 方程式 17 and are given in the *Electrical Characteristics* table.

$$\Psi_{JT}: T_J = T_T + \Psi_{JT} \times P_D$$
$$\Psi_{JB}: T_J = T_B + \Psi_{JB} \times P_D \tag{17}$$

where:

- P_D is the power dissipated as explained in 方程式 14
- T_T is the temperature at the center-top of the device package
- T_B is the PCB surface temperature measured 1 mm from the device package and centered on the package edge

8.1.20 TPS7A57EVM-081 Thermal Analysis

The TPS7A57EVM-081 was used to develop the TPS7A5701RTE thermal model. The RTE package is a 3-mm × 3-mm, 16-pin WQFN with 25-µm plating on each via. The EVM is a 3.5-inch × 3.5-inch (89 mm × 89 mm) PCB comprised of six layers. 表 8-9 lists the layer stackup for the EVM. 图 8-29 to 图 8-36 illustrate the various layer details for the EVM.

表 8-9. TPS7A57EVM-081 PCB Stackup

LAYER	NAME	MATERIAL	THICKNESS (mil)
1	Top overlay	—	—
2	Top solder	Solder resist	0.4
3	Top layer	Copper	2.756
4	Dielectric 1	FR-4 high Tg	9
5	Mid layer 1	Copper	2.756
6	Dielectric 2	FR-4 high Tg	9
7	Mid layer 2	Copper	2.756
8	Dielectric 3	FR-4 high Tg	9
9	Mid layer 3	Copper	2.756
10	Dielectric 4	FR-4 high Tg	9
11	Mid Layer 4	Copper	2.756
12	Dielectric 5	FR-4 high Tg	9
13	Bottom layer	Copper	2.756
14	Bottom solder	Solder resist	0.4

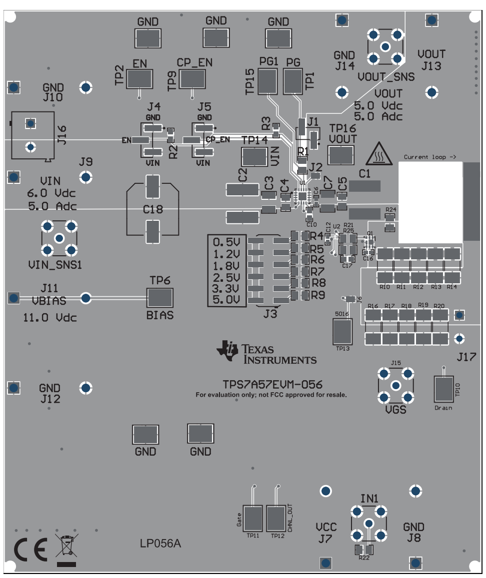


图 8-29. Top Assembly Layer and Silkscreen

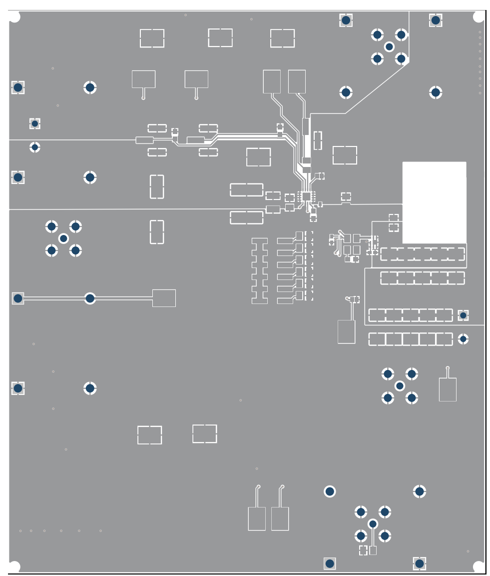


图 8-30. Top Layer Routing

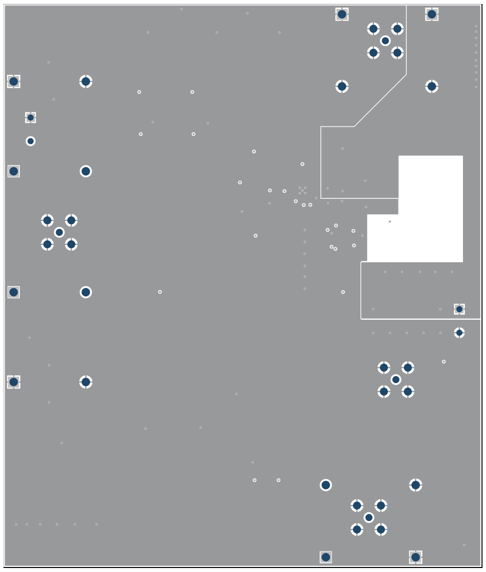


图 8-31. Layer 2 Routing

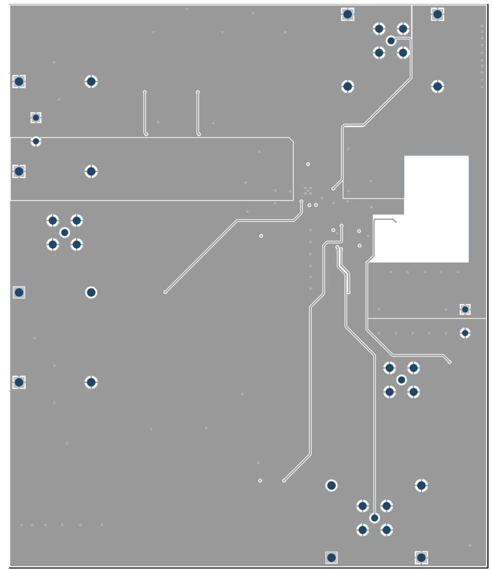


图 8-32. Layer 3 Routing

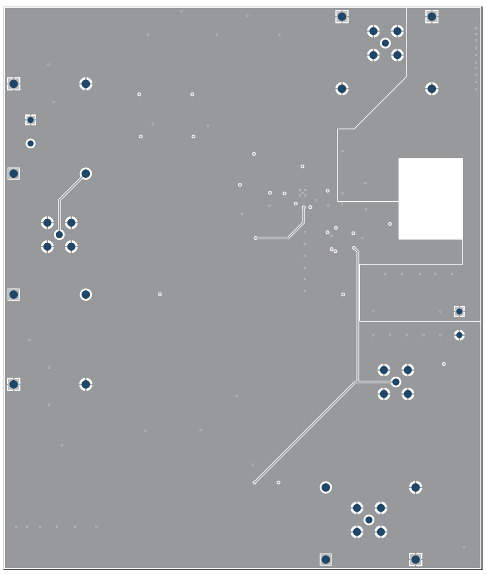


图 8-33. Layer 4 Routing

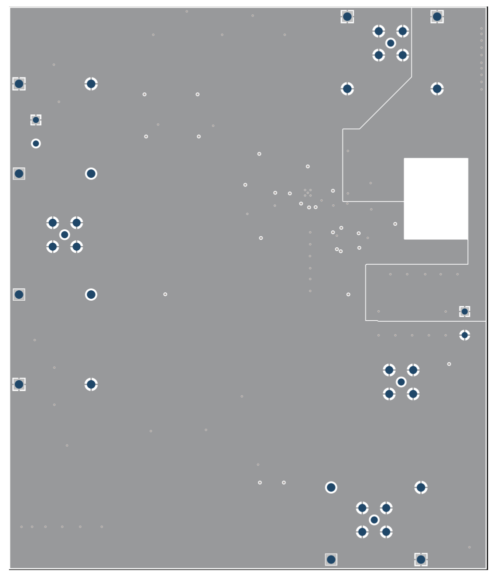


图 8-34. Layer 5 Routing

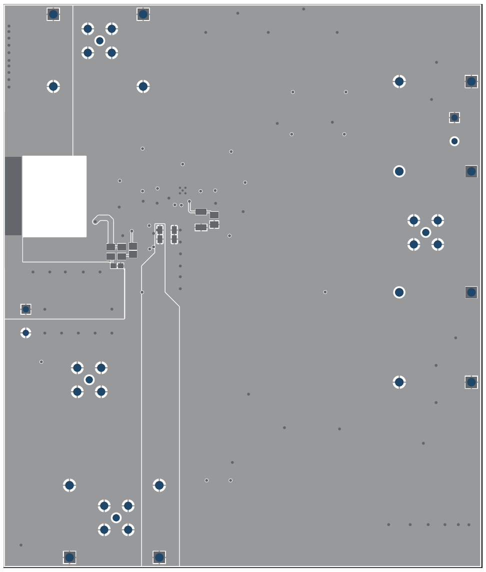


图 8-35. Bottom Layer Routing

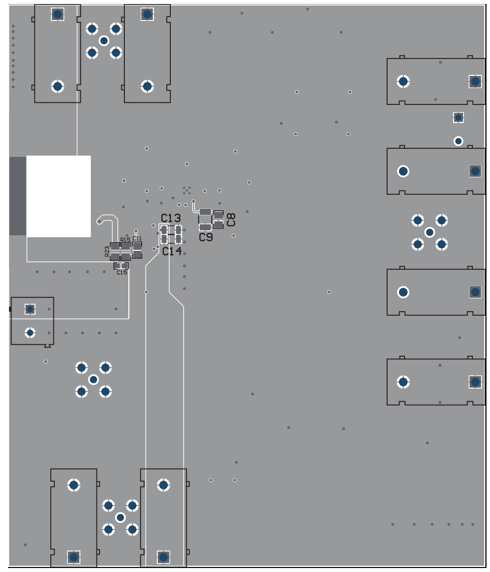


图 8-36. Bottom Assembly Layer and Silkscreen

表 8-10 shows thermal simulation data for the TPS7A57EVM-056. 图 8-37 and 图 8-38 show the thermal gradient on the PCB and device that results when a 1-W power dissipation is used through the pass transistor with a 25°C ambient temperature.

表 8-10. TPS7A57EVM-081 Thermal Simulation Data

DUT	$R_{\theta JA}$(° C/W)	Ψ_{JB}(° C/W)	Ψ_{JT}(°C/W)
TPS7A57EVM-056	21.9	11.9	0.4

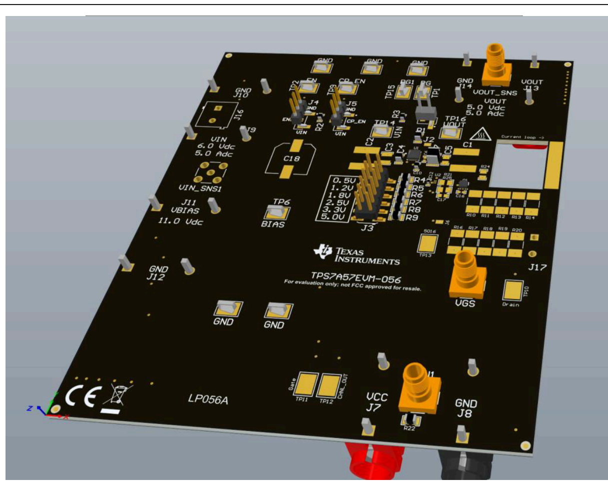


图 8-37. TPS7A57EVM-081 3D View

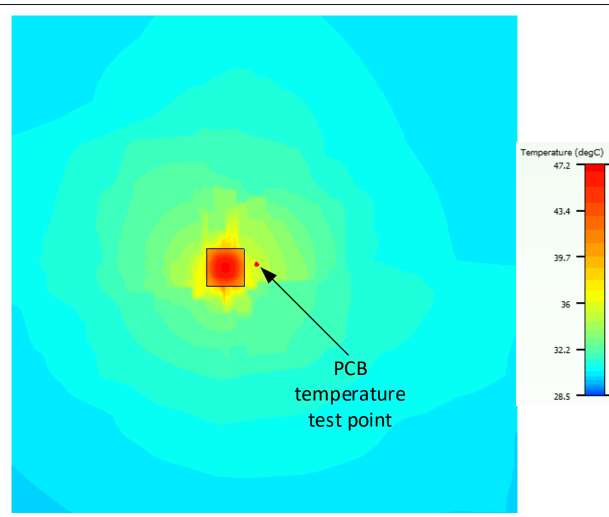


图 8-38. TPS7A57EVM-081 PCB Thermal Gradient

8.2 Typical Application

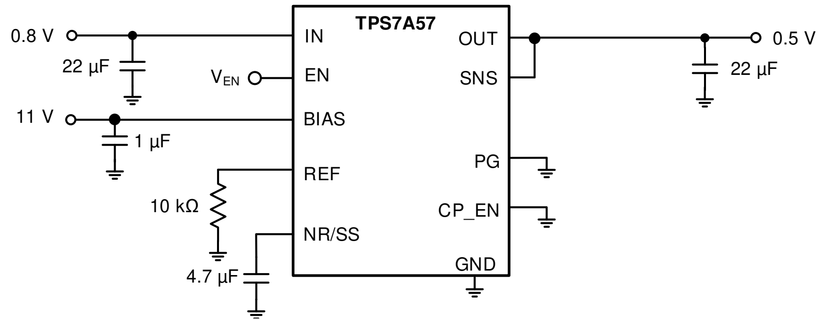


图 8-39. Typical Application Schematic

8.2.1 Design Requirements

表 8-11 lists the required application parameters for this design example.

表 8-11. Design Parameters

PARAMETER	DESIGN REQUIREMENT
Input voltage	0.8 V, ±3%, provided by the dc/dc converter switching at 1 MHz
Bias voltage	11 V
Output voltage	0.5 V, 1%
Charge pump	Disabled
Output current	4.2 A (maximum), 3.5 A (minimum)
Noise	Less than 5 µV_{RMS}
PSRR at 10 kHz	80 dB at max load current
PSRR at 1 MHz	> 35 dB at max load current
Maximum load transient	±5 mV, 100 mA to 3.5 A
Start-up environment	Start-up time < 15 ms

8.2.2 Detailed Design Procedure

In this design example, the device is powered by a dc/dc convertor switching at 1 MHz. The load requires a 0.5-V clean rail with less than 5 µV_{RMS}. The typical 22-µF input and output capacitors and 4.7-µF NR/SS capacitors are used to achieve a good balance between fast start-up time and excellent noise, and PSRR performance and load transient.

The output voltage is set using a 10-kΩ, thin-film resistor value calculated as described in the *Output Voltage Setting and Regulation* section. The PG pin is not used and is thus connected to ground to help with thermals. The enable voltage is provided by a external I/O. 图 8-41 illustrates that the device meets all design noise requirements. 图 8-40 depicts adequate PSRR performance.

As illustrated in 图 8-42, the load transient is adequate to the power-supply requirement.

图 8-39 depicts the implementation of these components.

8.2.3 Application Curves

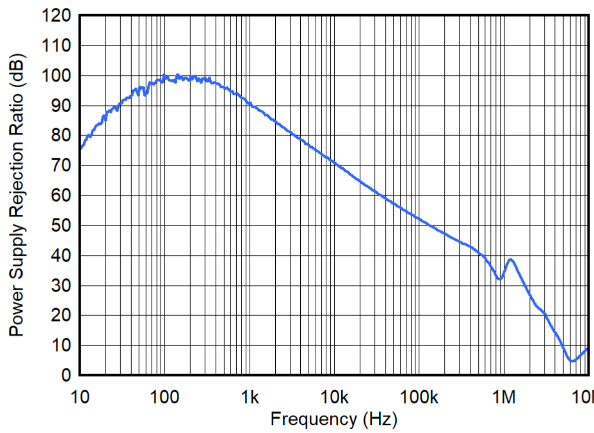


图 8-40. PSRR vs Frequency

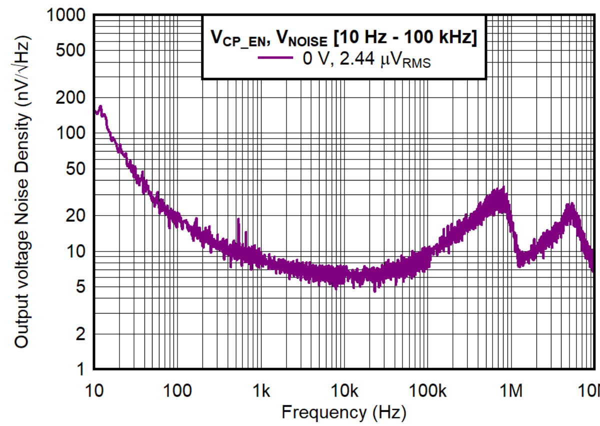


图 8-41. Noise vs Frequency

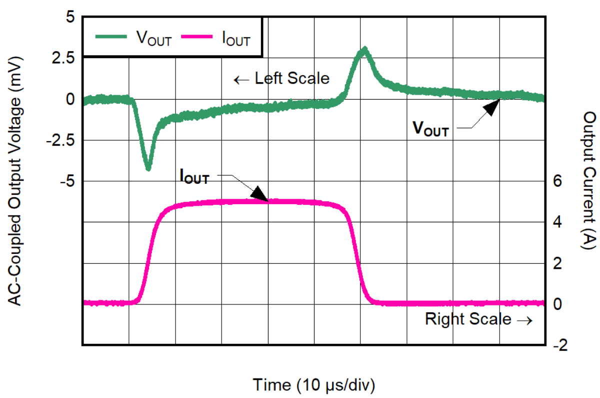


图 8-42. Load Transient

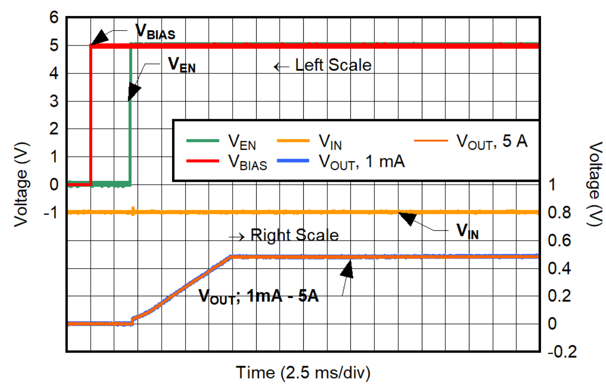


图 8-43. Start-Up Rail Sequence

8.3 Power Supply Recommendations

The device is designed to operate from an input voltage supply ranging from 0.7 V to 6.0 V and a BIAS rail up to 11 V. Ensure that the input voltage range provides adequate operational headroom for the device to have a regulated output. This input supply must be well regulated and low impedance. If the input supply is noisy, use additional input capacitors with low ESR and increase the operating headroom to achieve the desired output noise, PSRR, and load transient performance.

There is no sequencing requirement between IN, BIAS, and EN. CP_EN is an analog signal and must be connected to either IN, BIAS, or GND.

8.4 Layout

8.4.1 Layout Guidelines

For best overall performance, place all circuit components on the same side of the circuit board and as near as practical to the respective LDO pin connections. Place ground return connections to the input and output capacitor, and to the LDO ground pin as close to each other as possible, connected by a wide, component-side, copper surface. To avoid negative system performance, do not use vias and long traces to the input and output capacitors. The grounding and layout scheme illustrated in 图 8-44 minimizes inductive parasitics, and thereby reduces load-current transients, minimizes noise, and increases circuit stability.

Because of its wide bandwidth and high output current capability, inductance present on the output negatively impacts load transient response. For best performance, minimize trace inductance between the output and load.

A low ESL capacitor combined with low trace inductance limits the total inductance present on the output and optimizes the high-frequency PSRR.

To improve performance, use a ground reference plane, either embedded in the PCB itself or placed on the bottom side of the PCB opposite the components. This reference plane serves to assure accuracy of the output voltage, shield noise, and behaves similar to a thermal plane to spread (or sink) heat from the LDO device when connected to the thermal pad. In most applications, this ground plane is necessary to meet thermal requirements.

8.4.2 Layout Example

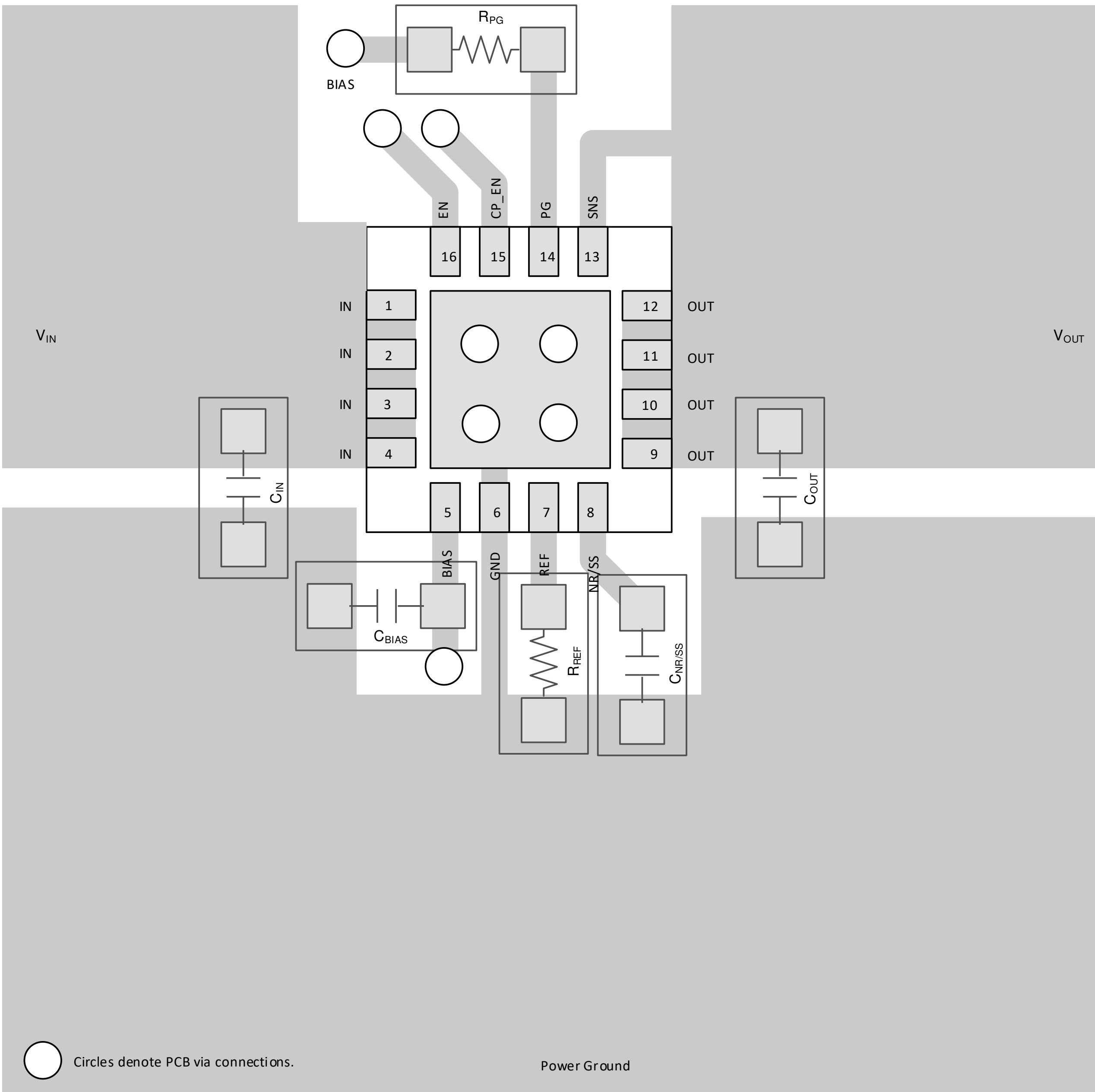


图 8-44. Recommended Layout

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *TPS7A57EVM-056 Evaluation Module* user guide
- Texas Instruments, *High-Current, Low-Noise Parallel LDO Reference Design* design guide

9.2 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*订阅更新* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.3 支持资源

TI E2E™ 支持论坛是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

9.4 商标

TI E2E™ is a trademark of Texas Instruments.
所有商标均为其各自所有者的财产。

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

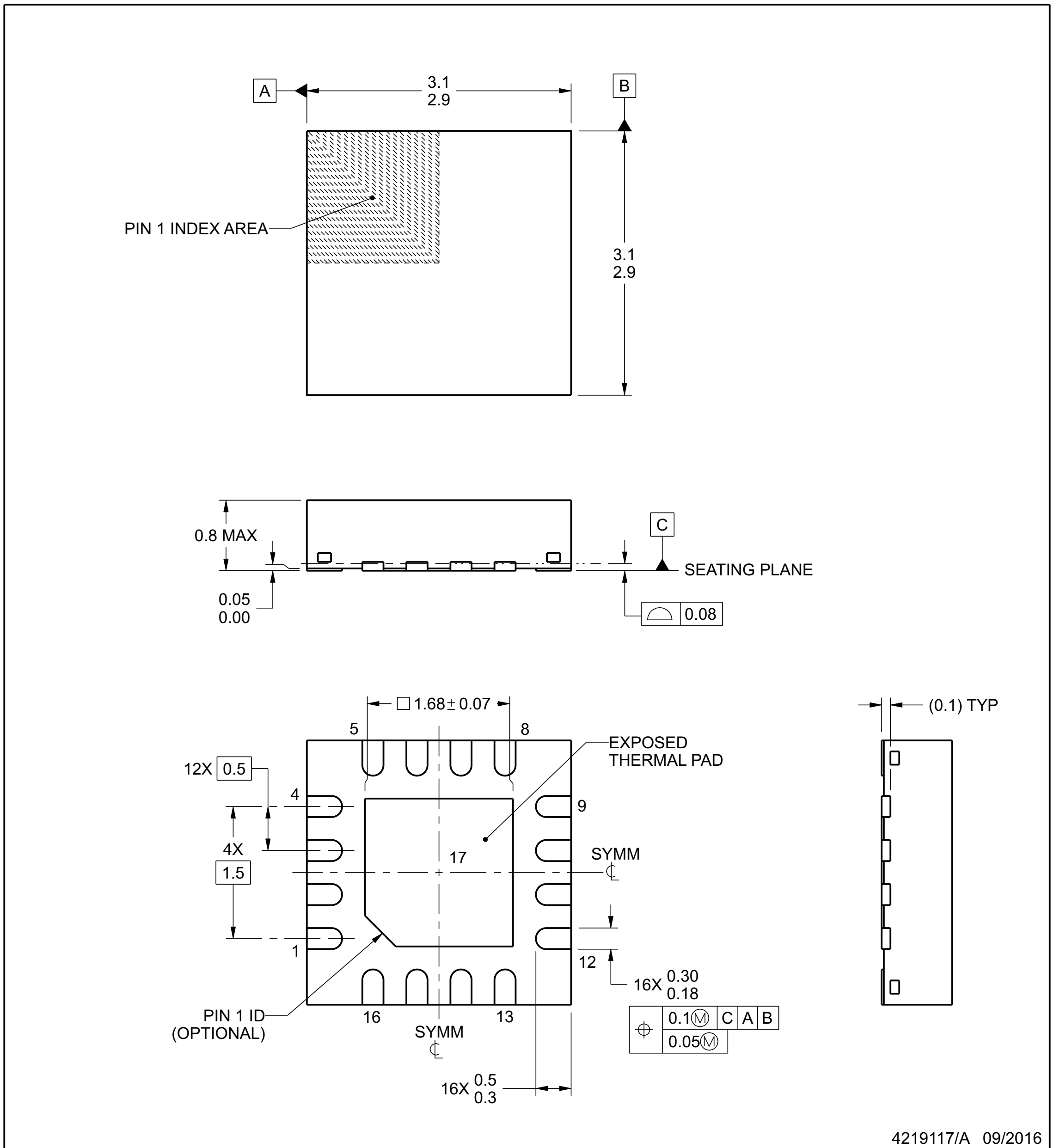
10.1 Mechanical Data

PACKAGE OUTLINE

RTE0016C

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

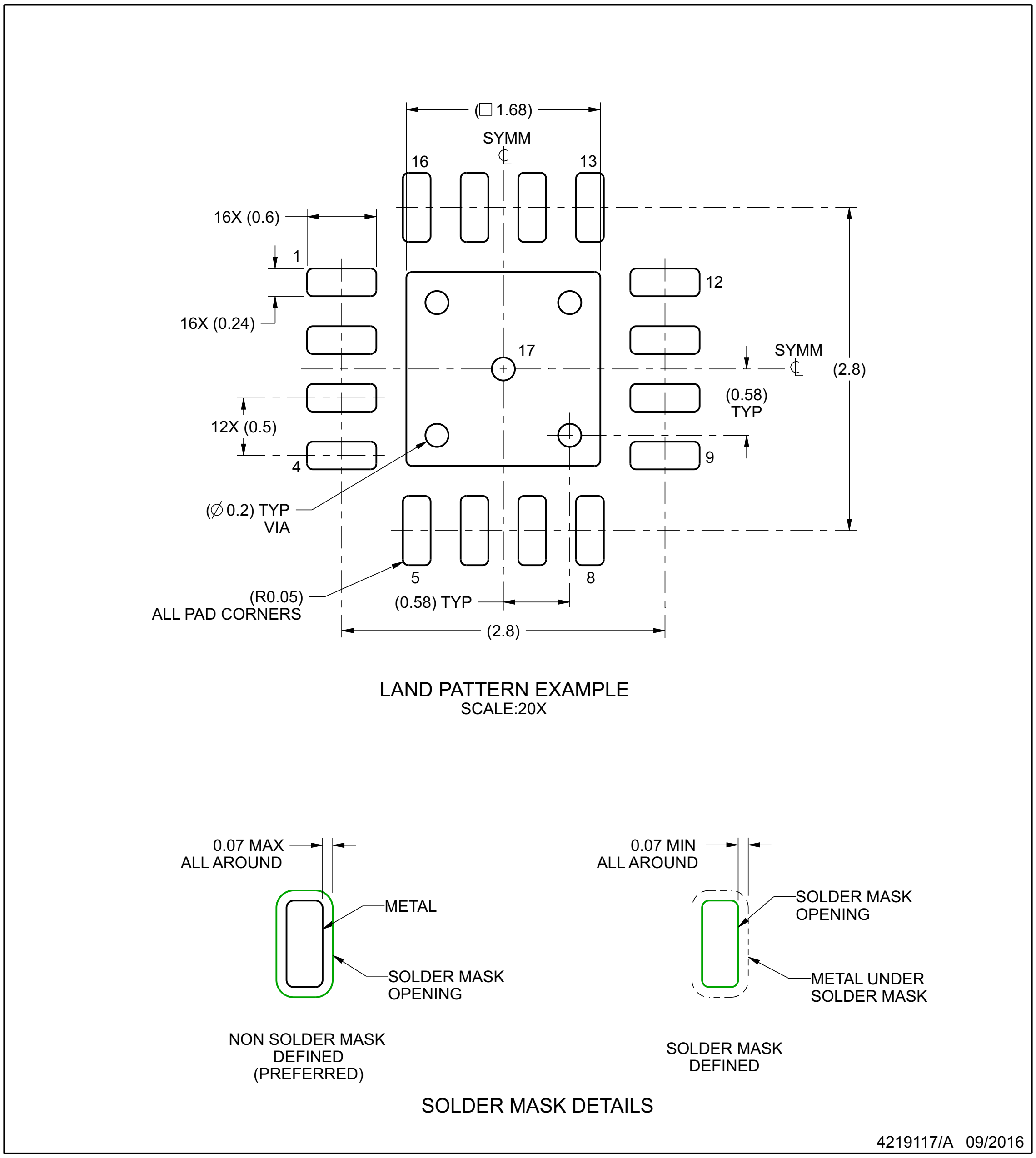
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

RTE0016C

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

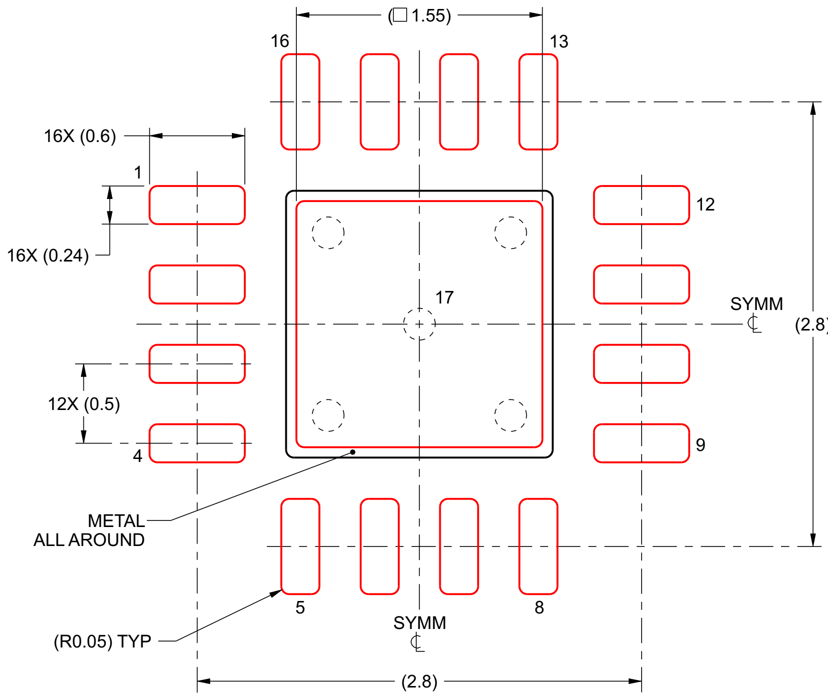
www.ti.com

EXAMPLE STENCIL DESIGN

RTE0016C

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4219117/A 09/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS7A5701RTER	ACTIVE	WQFN	RTE	16	5000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	7A5701	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

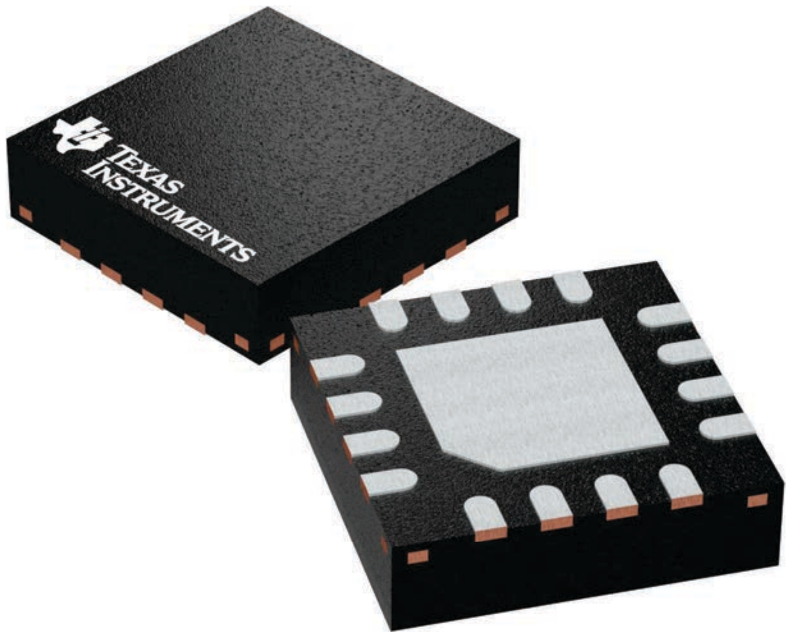
RTE 16

WQFN - 0.8 mm max height

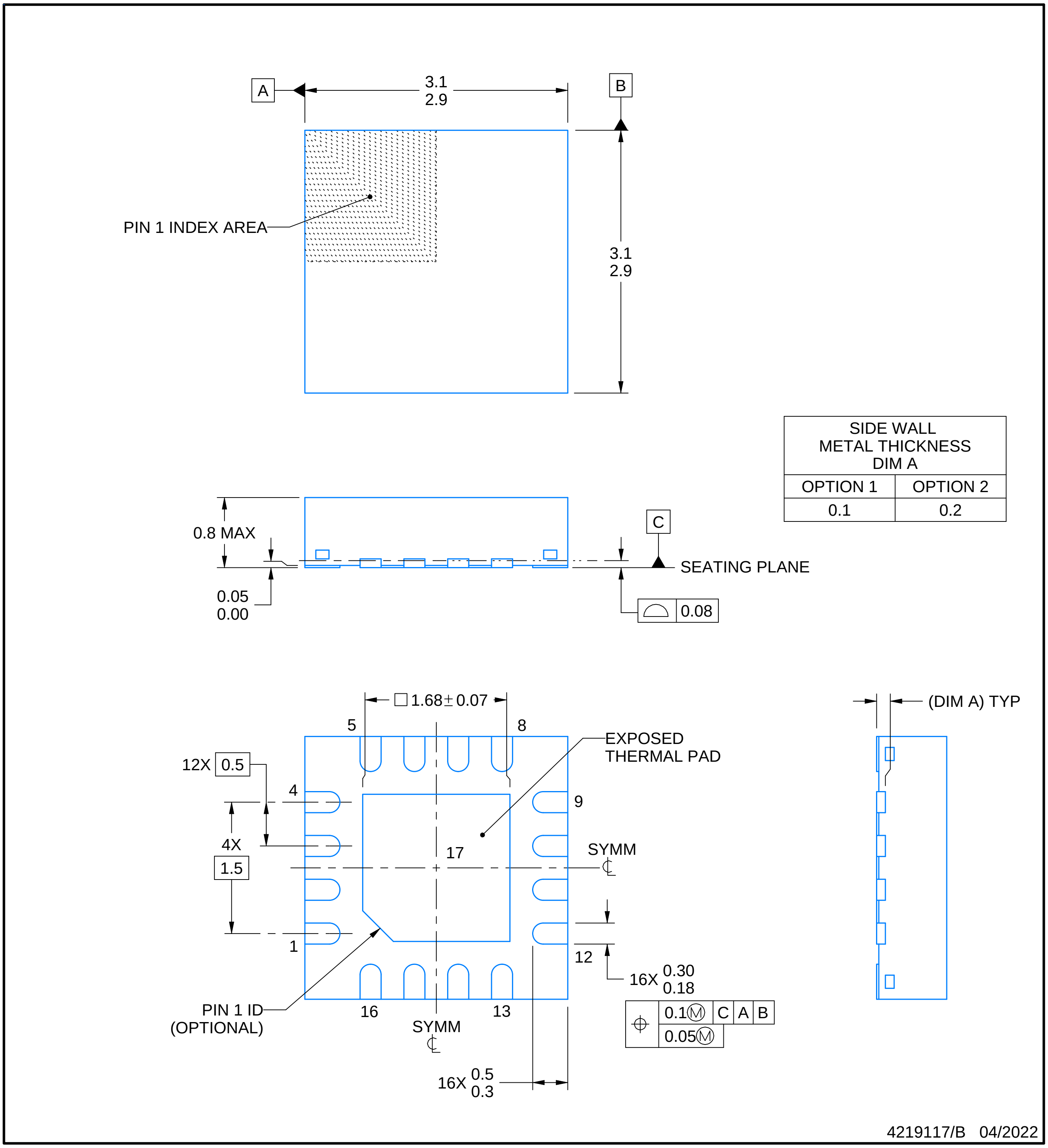
3 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



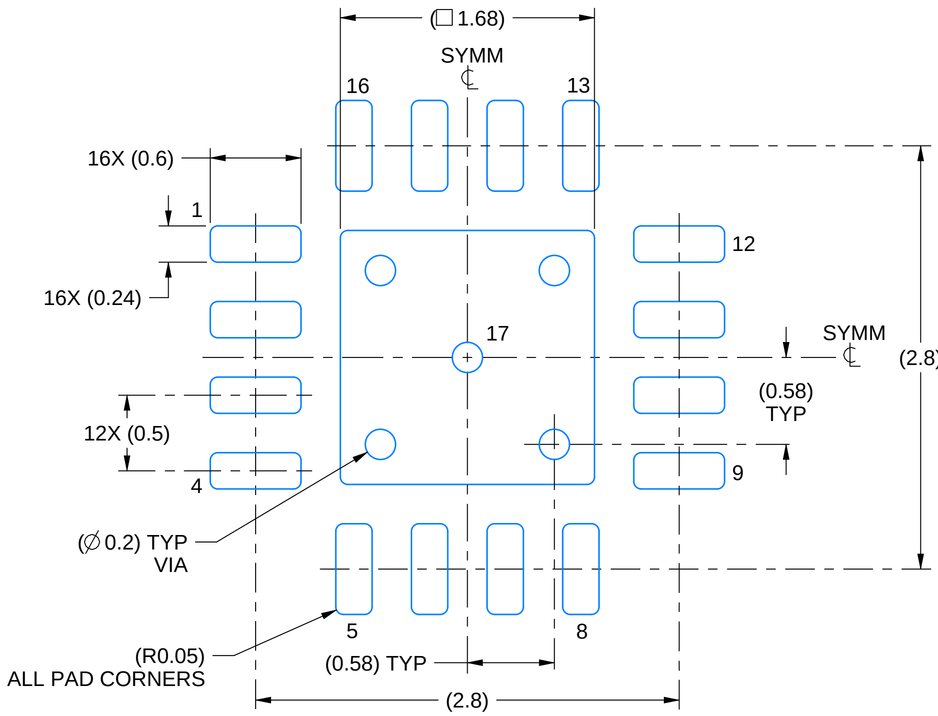
4225944/A



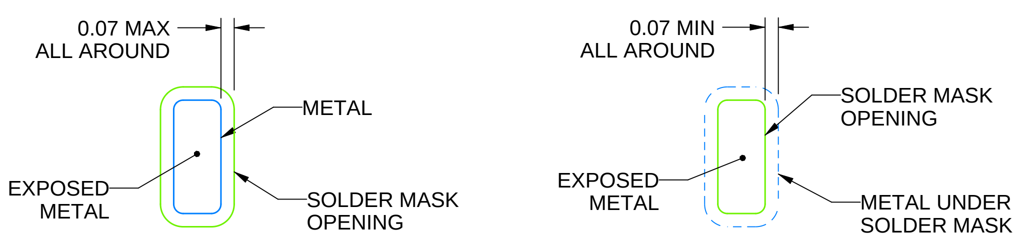
SIDE WALL METAL THICKNESS DIM A	
OPTION 1	OPTION 2
0.1	0.2

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



NON SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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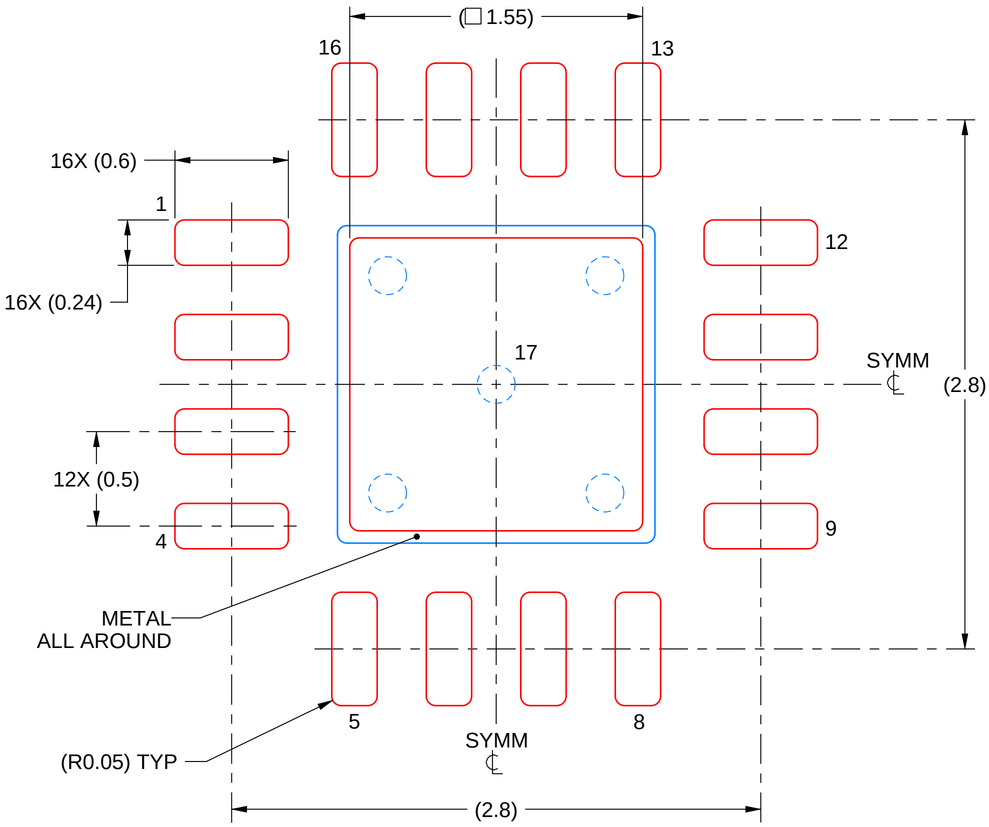
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要声明和免责声明

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265