具有电平转换器的 1.8V/3V 智能身份模块 (SIM) 卡电源

查询样品: TXS4555

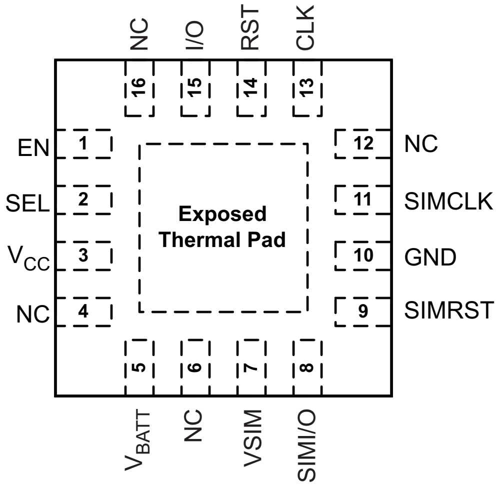
特性

- 电平转换器
  - 1.65V 至 3.3V 的 V_{CC}范围
  - 2.3 至 5.5V 的 V_{BATT}范围
- 低压降 (LDO) 稳压器
  - 带有使能的 50mA LDO 稳压器
  - 1.8V 至 2.95V 可选输出电压
  - 2.3V 至 5.5V 输入电压范围
  - 极低压降：电流为 50mA 时为 100mV（最大值）
- 为 SIM 卡信号整合了关断特性，符合 ISO-7816-3 标准
- 静电放电 (ESD) 保护性能超过 JESD 22 规范要求
  - 2000V 人体模型 (A114-A)
  - 500V 充电器件模型 (C101)
  - 针对 SIM 引脚的 8kV
- 封装
  - 16 引脚四方扁平无引线封装 (QFN) (3mm x 3mm)
  - 12 引脚四方扁平无引线封装 (QFN) (2mm x 1.7mm)

说明

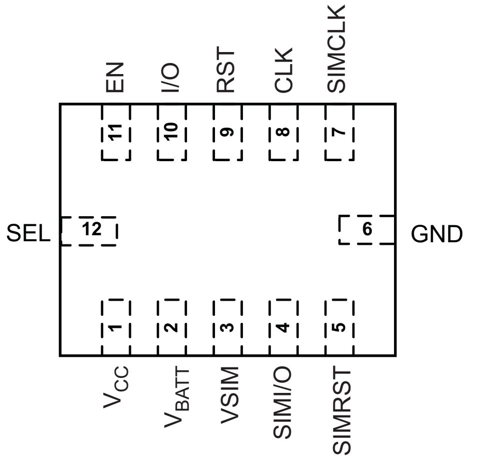
TXS4555 是一款完整的智能身份模块 (SIM) 卡解决方案，可用来将无线基带处理器与 SIM 卡对接，从而可为移动手持终端应用存储 I/O 数据。 该器件不但符合 ISO/IEC 智能卡接口要求，而且还支持 GSM 与 3G 移动标准。 它包含能够支持 B 类 (2.95V) 与 C 类 (1.8V) 接口的高速电平转换器，一个低压降 (LDO) 稳压器，此稳压器具有可在 2.95V B 类与 1.8V C 类接口之间选择的输出电压。

RGT Package
(Top View)



请注意：裸露的中心散热焊盘必须连接至接地。

RUT Package
(Top View)



该器件具有两组电源电压引脚。 VCC 支持 1.65V 至 3.3V 的整个电压范围，而 V_{BATT}则支持 2.3 至 5.5V 间的电压。VPWR 可设置为 1.8V 或 2.95V，并由内部 LDO 供电。 集成型 LDO 可接受高达 5.5V 的输入电压，并可在 50mA 电流下向 B 端电路系统及外部 SIM 卡输出 1.8V 或 2.95V 的电压。 TXS4555 可帮助系统设计人员轻松将低电压微处理器连接至工作电压为 1.8V 或 2.95V 的 SIM 卡。

此外，TXS4555 还根据针对 SIM 卡的 ISO 7816-3 技术规范为 SIM 卡引脚整合了关断定序功能。 SIM 卡信号的适当关断可在电话意外关机时保护数据免受损坏。 该器件不但可为 SIM 引脚提供 8kV HBM 保护，而且还可为所有其它引脚提供标准 2kV HBM 保护。

English Data Sheet: SBOS550

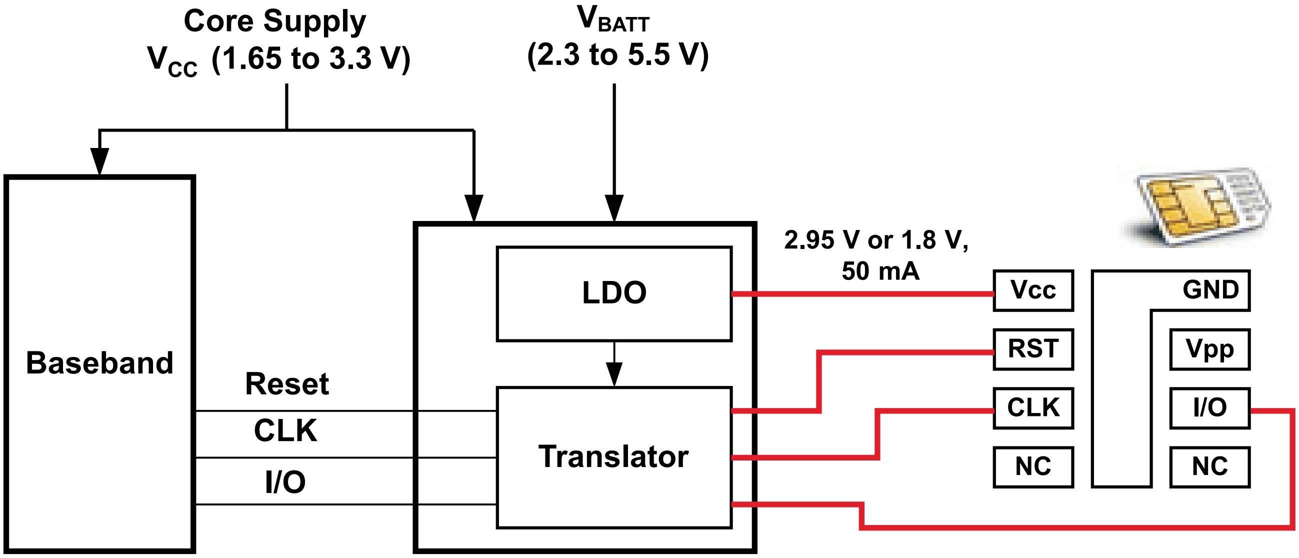


Figure 1. Interfacing with SIM Card

PIN FUNCTIONS

PIN NAME	PIN NO.		TYPE[1]	DESCRIPTION
	RGT	RUT		
EN	1	11	I	Enable/disable control input. Pull EN low to place all outputs in Hi-Z state and to disable the LDO. Referenced to VCC.
SEL	2	12	I	Pin to program VSIM value (Low = 1.8V, High = 2.95V)
Vcc	3	1	P	Power supply voltage which powers all A-port I/Os and control inputs
VBATT	5	2	P	Battery power supply
VSIM	7	3	O	SIM card Power-Supply pin (1.8V or 2.95V)
SIM_I/O	8	4	I/O	Bidirectional SIM I/O pin which connected to I/O pin of the SIM card connector
SIM_RST	9	5	O	SIM Reset pin which connects to RESET pin of the SIM card connector
GND	10	6	G	Ground
SIM_CLK	11	7	O	Clock signal pin which connects to CLK pin of the SIM card connector
CLK	13	8	I	Clock signal pin connected from baseband processor
RST	14	9	I	SIM Reset pin connected from baseband processor
I/O	15	10	I/O	Bidirectional SIM I/O pin which connected from baseband processor
NC	4, 6, 12, 16	–	NC	No Connects

(1) G = Ground, I = Input, O = Output, P = Power

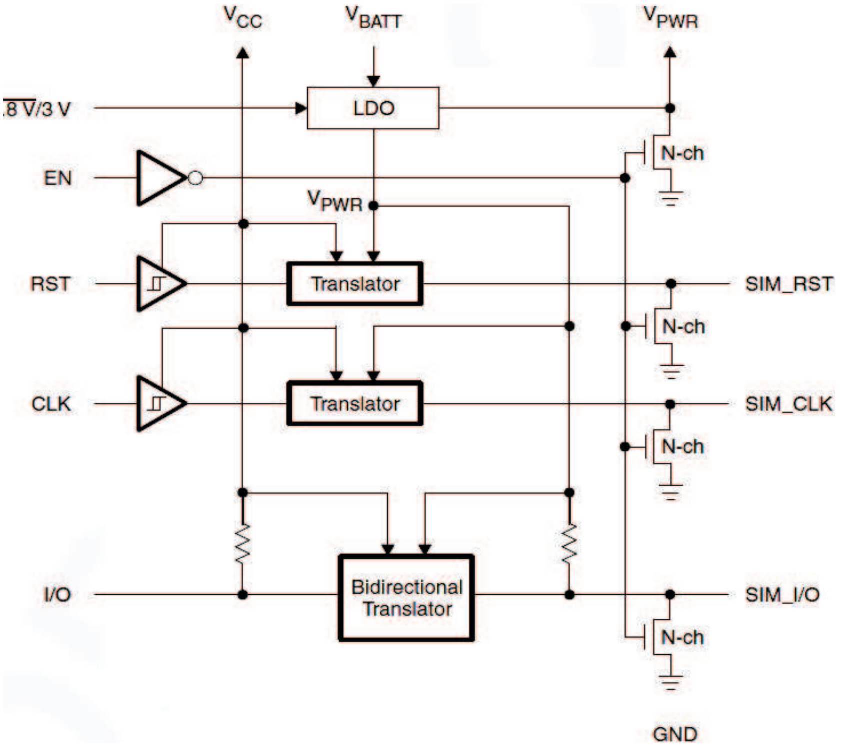


Figure 2. Block Diagram

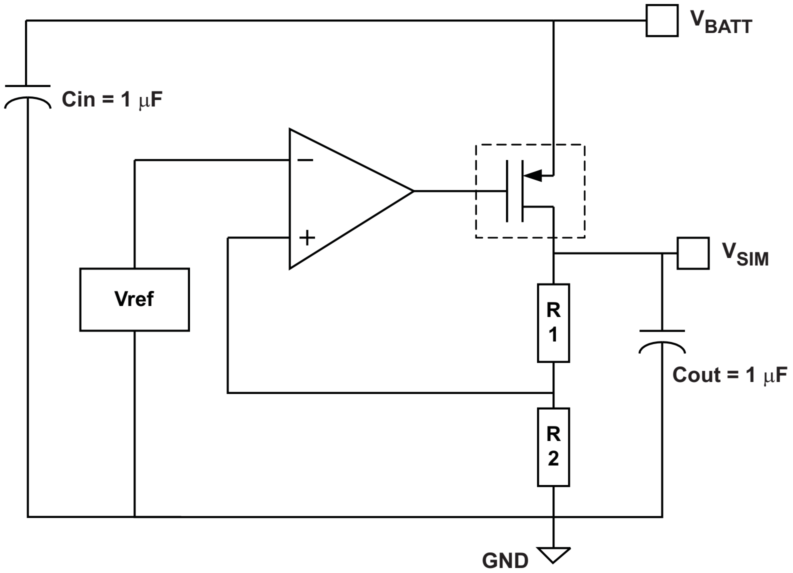


Figure 3. Block Diagram of the LDO

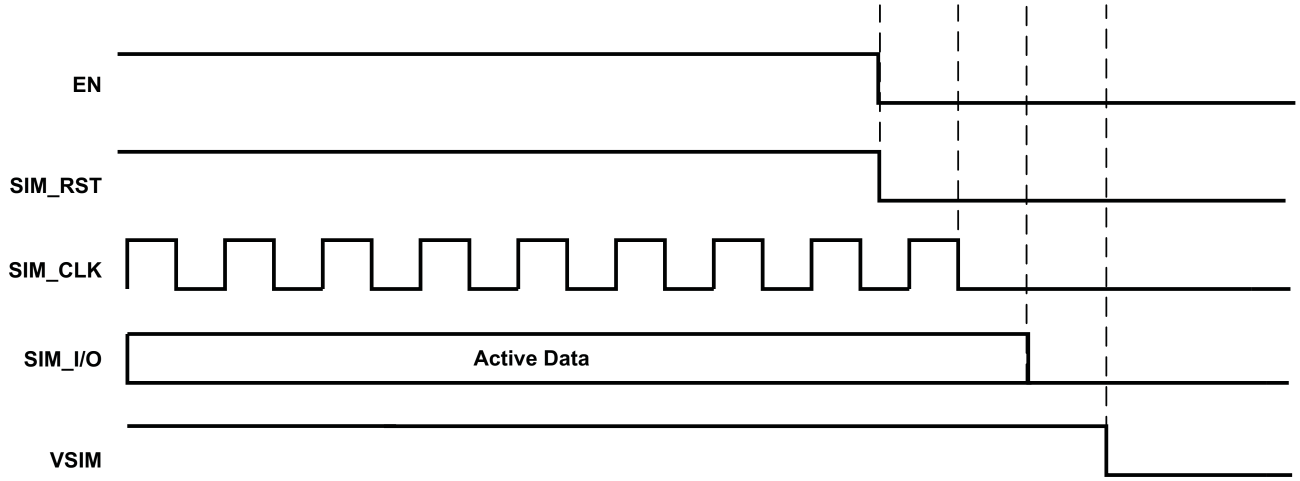


Figure 4. Shutdown Sequence for SIM_RST, SIM_CLK, SIM_IO and VSIM

The shutdown sequence for the SIM signals is based on the ISO 7816-3 specification. The shutdown sequence of these signals helps to properly disable these channels and not have any corruption of data accidently. Also, this is also helpful when the SIM card is present in a hot swap slot and when pulling out the SIM card, the orderly shutdown of these signals help avoid any improper write/corruption of data.

When EN is taken low, the shutdown sequence happens by powering of the SIM_RST channel. Once that is achieved, SIM_CLK, SIM_I/O and VSIM are powered sequentially one by one. There is an internal 2K pull-down value on the SIM pins and helps to pull these channels low. The shutdown time sequence is in the order of a few microseconds. It is important that EN is taken low before VBAT and VCC supplies go low so that the shutdown sequence can be initiated properly.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			VALUE		UNIT
			MIN	MAX	
LEVEL TRANSLATOR					
V_{CC}	Supply voltage range		–0.3	4.0	V
V_I	Input voltage range	V_{CC}-port	–0.5	4.6	V
		SIM-port	–0.5	4.6	
		Control inputs	–0.5	4.6	
V_O	Voltage range applied to any output in the high-impedance or power-off state	V_{CC} -port	–0.5	4.6	V
		VSIM-port	–0.5	4.6	
		Control inputs	–0.5	4.6	
V_O	Voltage range applied to any output in the high or low state	V_{CC}-port	–0.5	4.6	V
		SIM-port	–0.5	4.6	
		Control inputs	–0.5	4.6	
I_{IK}	Input clamp current	$V_I < 0$		–50	mA
I_{OK}	Output clamp current	$V_O < 0$		–50	mA
I_O	Continuous output current			±50	mA
	Continuous current through VCCA or GND			±100	mA
T_{stg}	Storage temperature range		–65	150	°C
LDO					
VBAT	Input voltage range		–0.3	6	V
V_{OUT}	Output voltage range		–0.3	6	V
	Peak output current		TBD		mA
	Continuous total power dissipation			TBD	
T_J	Junction temperature range		–55	150	°C
T_{stg}	Storage temperature range		–55	150	°C
	ESD rating (host side)	Human-Body Model (HBM)		2	kV
		Charged-Device Model (CDM)		500	V
	ESD rating (SIM side)	Human-Body Model (HBM)		8	kV

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

THERMAL INFORMATION

	THERMAL METRIC(1)	TXS4555		UNITS
		RGT	RUT	
		16 PINS	12 PINS	
$θ_{JA}$	Junction-to-ambient thermal resistance	47	87.2	°C/W
$θ_{JB}$	Junction-to-board thermal resistance	25.12	N/A	
$ψ_{JT}$	Junction-to-top characterization parameter	1.3	1.7	
$θ_{JCbot}$	Junction-to-case (bottom) thermal resistance	3.6	n/A	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS(1)

				MIN	MAX	UNIT
LEVEL TRANSLATOR						
V_{CC}	Supply voltage			1.65	3.3	V
V_{IH}	High-level input voltage	VCC - port	EN, SEL, RST, CLK, I/O	$V_{CC} \times 0.7$	V_{CC}	V
		SIM - port	SIM_I/O	$V_{sim} \times 0.7$	V_{sim}	
V_{IL}	Low-level input voltage	VCC - port	EN, SEL, RST, CLK, I/O	0	$V_{CC} \times 0.3$	V
		SIM - port	SIM_I/O	0	$V_{sim} \times 0.3$	
Δt/Δv	Input transition rise or fall rate				5	ns/V
T_A	Operating free-air temperature			–40	85	°C

(1) All unused data inputs of the device must be held at V_{CCI} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

ELECTRICAL CHARACTERISTICS – LEVEL TRANSLATOR

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	VSIM	MIN	TYP(1)	MAX	UNIT
V_{OH}	SIM_RST	$I_{OH} = –1mA$	1.65 V to 3.3 V	1.8 V / 2.95 V (2)	$V_{SIM} \times 0.8$			V
	SIM_CLK	$I_{OH} = –1mA$			$V_{SIM} \times 0.8$			
	SIM_I/O	$I_{OH} = –20\ \mu A$			$V_{SIM} \times 0.8$			
	I/O	$I_{OH} = –20\ \mu A$			$V_{CC} \times 0.8$			
V_{OL}	SIM_RST	$I_{OL} = 1$ mA	1.65 V to 3.3 V	1.8 V / 2.95 V (2)			$V_{SIM} \times 0.2$	V
	SIM_CLK	$I_{OL} = 1mA$					$V_{SIM} \times 0.2$	
	SIM_I/O	$I_{OL} = 1$ mA					0.3	
	I/O	$I_{OL} = 1$ mA					0.3	
I_I	Control inputs	V_I = EN, 1.8V/3V	1.65 V to 3.3 V	1.8 V / 2.95 V (2)			±1	µA
I_{CC}	I/O	$V_I = V_{CCI}$, $I_O = 0$	1.65 V to 3.3 V	1.8 V / 2.95 V(2)			±5	µA
C_{io}	I/O port					8		pF
	SIM ports					4		
C_i	Control inputs	$V_I = V_{CC}$ or GND				4		pF

(1) All typical values are at T_A = 25°C.
(2) (Supplied by LDO)

LDO ELECTRICAL CHARACTERISTICS

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{BAT}	Input voltage			2.3		5.5	V
V_{SIM}	Output voltage	Class-B Mode (SEL = V_{CC})		2.85	2.95	3.05	V
		Class-C Mode (SEL = 0)		1.7	1.8	1.9	
V_{DO}	Dropout voltage	I_{OUT} = 50 mA				100	mV
I_{GND}	Ground-pin current	I_{OUT} = 0 mA				35	µA
I_{SHDN}	Shutdown current (IGND)	$V_{ENx} \leq 0.4$ V, (VSIM + V_{DO}) ≤ VBAT ≤ 5.5 V, T_J = 85°C				3.5	µA
$I_{OUT(SC)}$	Short-circuit current	$R_L = 0\ \Omega$			145		mA
C_{OUT}	Output Capacitor				1		µF
PSRR	Power-supply rejection ratio	VBAT = 3.25 V, VSIM = 1.8 V or 2.95 V, C_{OUT} = 1 µF, I_{OUT} = 50 mA	f = 1 kHz	50			dB
			f = 10 kHz	40			
T_{STR}	Start-up time	VSIM = 1.8 V or 2.95 V, I_{OUT} = 50 mA, C_{OUT} = 1 µF				400	µS
T_J	Operating junction temperature			–40		125	°C

(1) All typical values are at T_A = 25°C.

GENERAL ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{I/OPU}$	I/O pull-up		16	20	24	kΩ
R_{SIMPU}	SIM_I/O pull-up		10	14	18	kΩ
R_{SIMPD}	SIM_I/O pull-down	Active pull-downs are connected to the VSIM regulator output to the SIM_CLK, SIM_RST, SIM_I/O when EN = 0			3	kΩ

SWITCHING CHARACTERISTICS

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC} = 1.8 V ± 0.15 V		UNIT
			MIN	MAX	
VSIM = 1.8 V or 2.95 V SUPPLIED BY INTERNAL LDO					
t_{rA}	SIM_I/O	$_{CL}$ = 50 pF		1	µs
t_{rB}	SIM_RST			1	µs
	SIM_CLK			18	ns
	SIM_I/O			1	us
f_{max}	SIM_CLK			25	MHz
Duty Cycle	SIM_CLK		40%	60%	

OPERATING CHARACTERISTICS

T_A = 25°C, V_{SIM} = 1.8 V

PARAMETER		TEST CONDITIONS	Vcc TYP	UNIT
			1.8 V	
C_{pdA} (1)	Class B	C_L = 0, f = 5 MHz, t_r = t_f = 1 ns	13	pF
	Class C		11	

(1) Power dissipation capacitance per transceiver.

TYPICAL CHARACTERISTICS

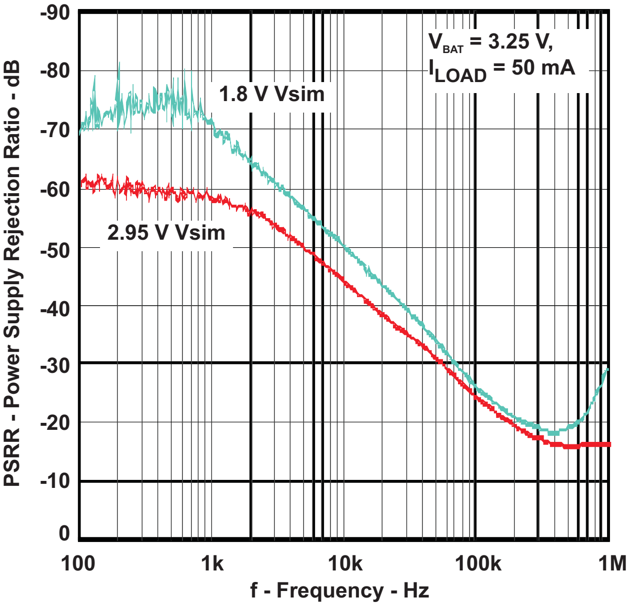


Figure 5. PSRR

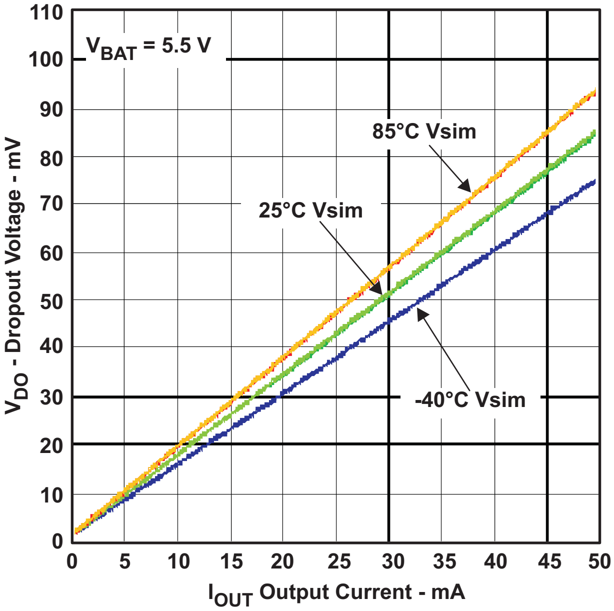


Figure 6. Dropout Voltage vs Output Current

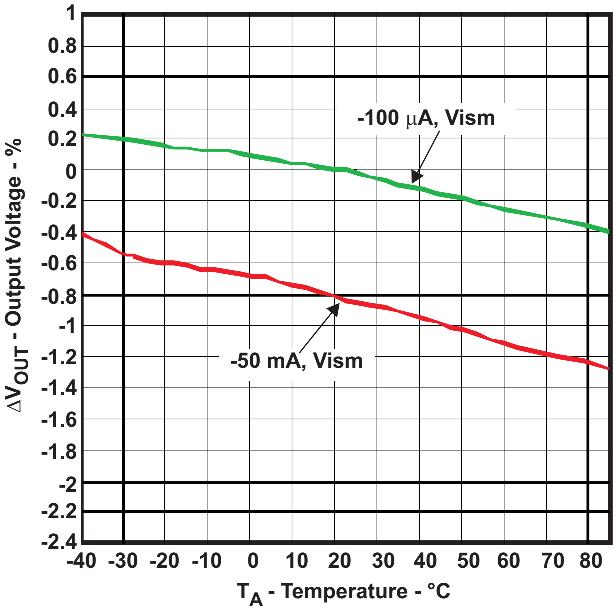


Figure 7. Output Voltage vs Temperature, Class-B/C

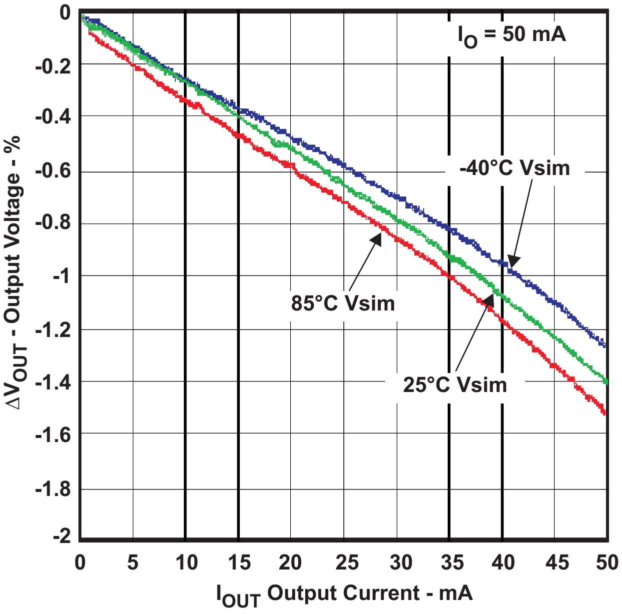


Figure 8. Load Regulation, Iout = 50 mA, Class-C

APPLICATION INFORMATION

The LDO's included on the TXS4555 achieve ultra-wide bandwidth and high loop gain, resulting in extremely high PSRR at very low headroom (V_{BAT} – V_{SIM}). The TXS4555 provides fixed regulation at 1.8V or 2.95V. Low noise, enable, low ground pin current make it ideal for portable applications. The device offers sub-bandgap output voltages, current limit and thermal protection, and is fully specified from –40°C to 125°C.

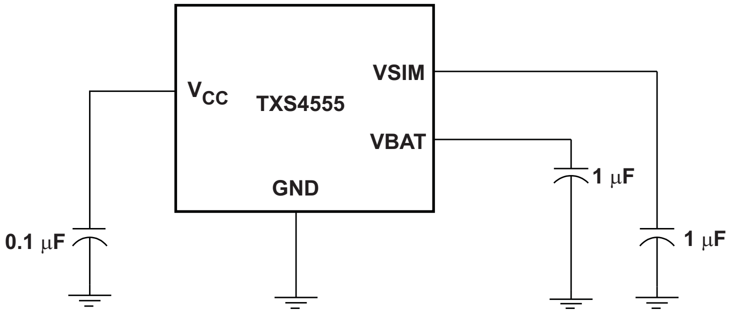


Figure 9. Typical Application Circuit for TXS4555

INPUT AND OUTPUT CAPACITOR REQUIREMENTS

It is good analog design practice to connect a 1.0 µF low equivalent series resistance (ESR) capacitor across the input supply (VBAT) near the regulator. Also, a 0.1µF is required for the logic core supply (VDDIO).

This capacitor will counteract reactive input sources and improve transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated or if the device is located several inches from the power source. The LDO's are designed to be stable with standard ceramic capacitors of values 1.0 µF or larger. X5R- and X7R-type capacitors are best because they have minimal variation in value and ESR over temperature. Maximum ESR should be < 1.0 Ω.

OUTPUT NOISE

In most LDO's, the bandgap is the dominant noise source. To improve ac performance such as PSRR, output noise, and transient response, it is recommended that the board be designed with separate ground planes for V_{IN} and V_{OUT}, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the bypass capacitor should connect directly to the GND pin of the device.

INTERNAL CURRENT LIMIT

The TXS4555 internal current limit helps protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of output voltage. For reliable operation, the device should not be operated in a current limit state for extended periods of time.

The PMOS pass element in the TXS4555 has a built-in body diode that conducts current when the voltage at VSIM exceeds the voltage at VBAT. This current is not limited, so if extended reverse voltage operation is anticipated, external limiting may be appropriate.

DROPOUT VOLTAGE

The TXS4555 uses a PMOS pass transistor to achieve low dropout. When (V_{BAT} – V_{SIM}) is less than the dropout voltage (V_{DO}), the PMOS pass device is in its linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass element. V_{DO} will approximately scale with output current because the PMOS device behaves like a resistor in dropout.

STARTUP

The TXS4555 uses a quick-start circuit which allows the combination of very low output noise and fast start-up times.

TRANSIENT RESPONSE

As with any regulator, increasing the size of the output capacitor reduces over/undershoot magnitude but increases duration of the transient response.

MINIMUM LOAD

The TXS4555 is stable and well-behaved with no output load. Traditional PMOS LDO regulators suffer from lower loop gain at very light output loads. The TXS4555 employs an innovative low-current mode circuit to increase loop gain under very light or no-load conditions, resulting in improved output voltage regulation performance down to zero output current.

THERMAL INFORMATION

Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately +160°C, allowing the device to cool. When the junction temperature cools to approximately +140°C the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage because of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heat sink. For reliable operation, junction temperature should be limited to +125°C maximum. To estimate the margin of safety in a complete design (including heat sink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least +35°C above the maximum expected ambient condition of your particular application. This configuration produces a worst-case junction temperature of +125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TXS4555 has been designed to protect against overload conditions. It was not intended to replace proper heat sinking. Continuously running the TXS4555 into thermal shutdown will degrade device reliability.

REVISION HISTORY

Changes from Revision A (March 2011) to Revision B	Page
• Removed Ordering Information table.	2
• Updated V_{IH} and V_{IL} to specify additional information.	6

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TXS4555RGTR	ACTIVE	VQFN	RGT	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ZUT	Samples
TXS4555RUTR	ACTIVE	UQFN	RUT	12	3000	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 85	69R	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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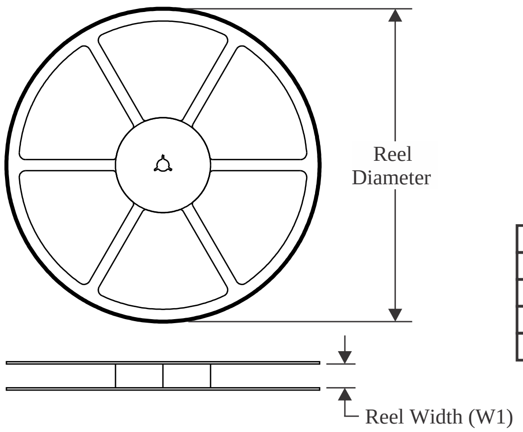
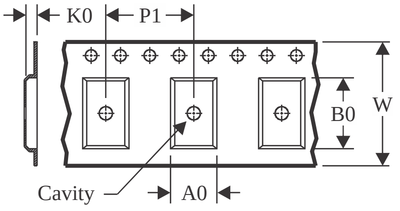
TAPE AND REEL INFORMATION

REEL DIMENSIONS

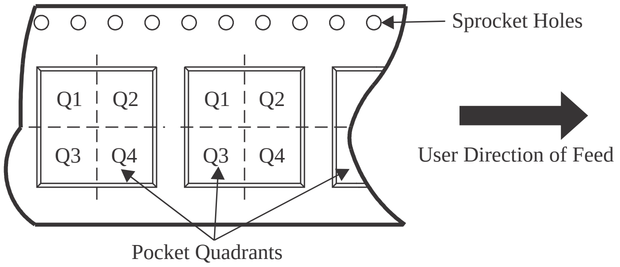


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

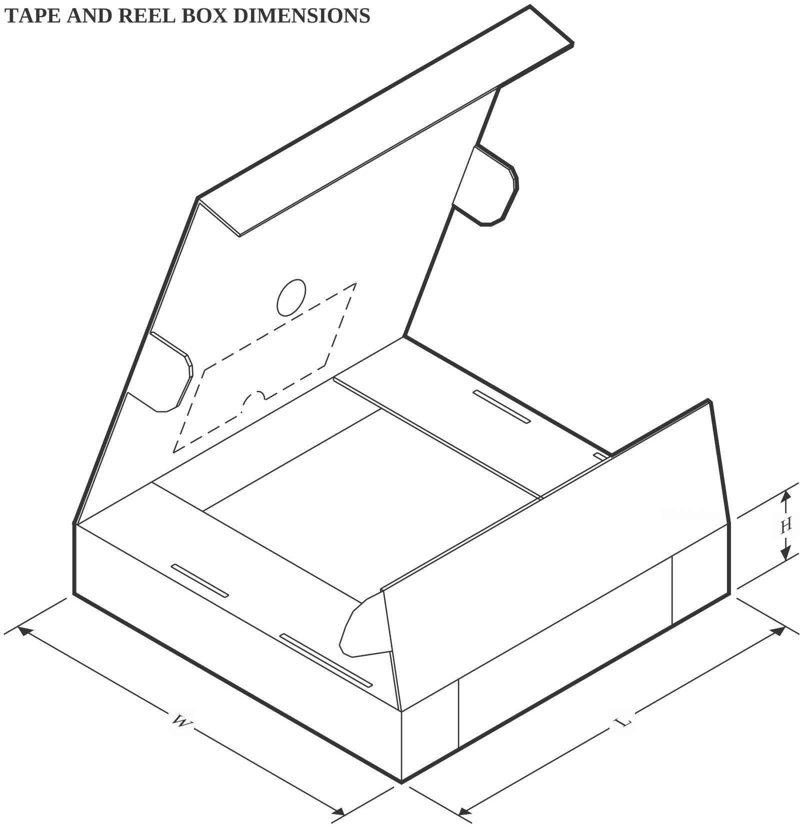
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TXS4555RGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TXS4555RUTR	UQFN	RUT	12	3000	180.0	8.4	1.95	2.3	0.75	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



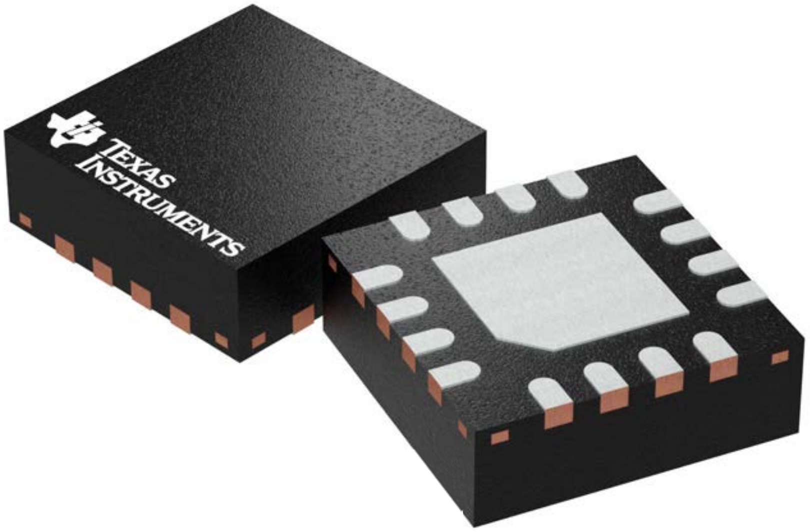
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TXS4555RGTR	VQFN	RGT	16	3000	356.0	356.0	35.0
TXS4555RUTR	UQFN	RUT	12	3000	202.0	201.0	28.0

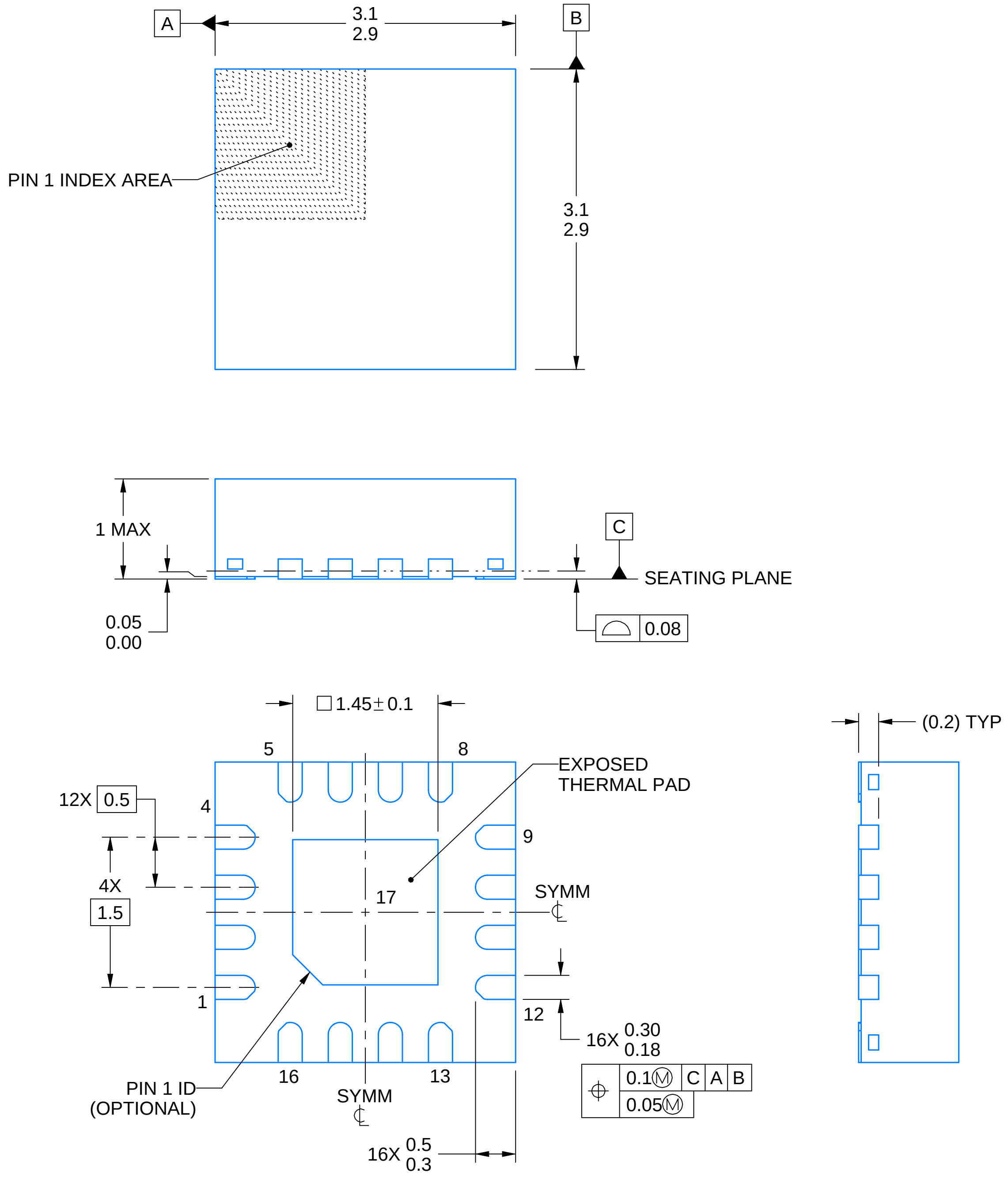
RGT 16

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



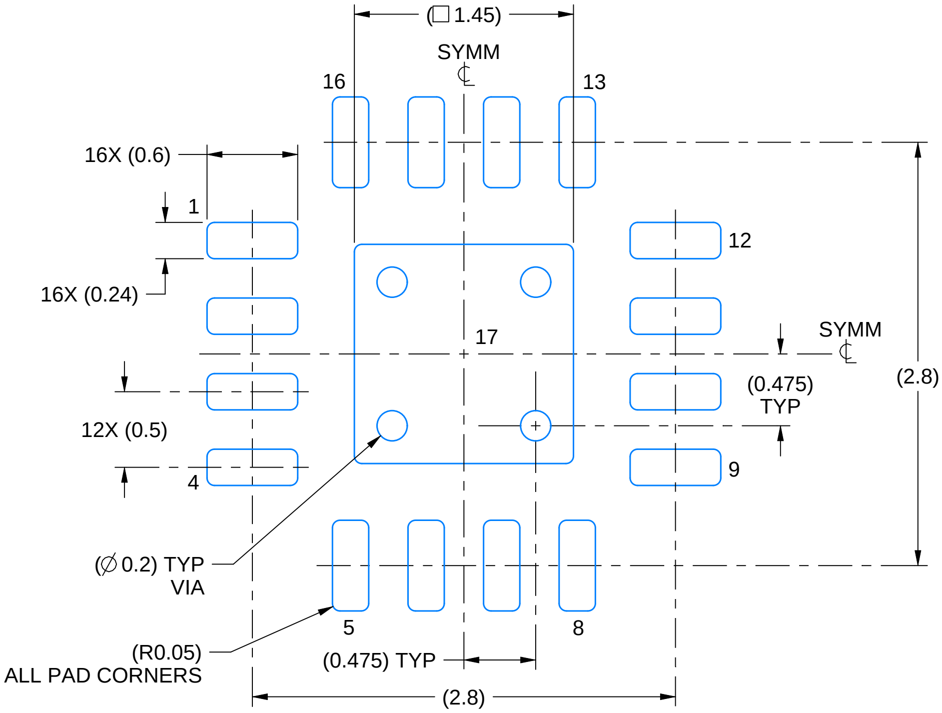
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



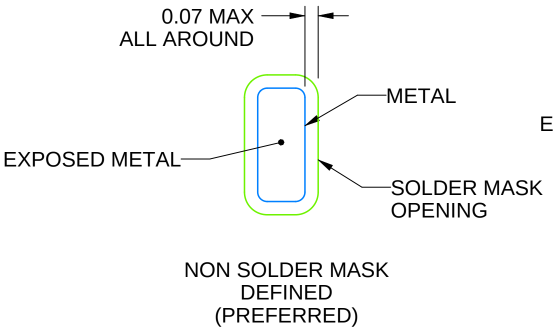
4219032/A 02/2017

NOTES:

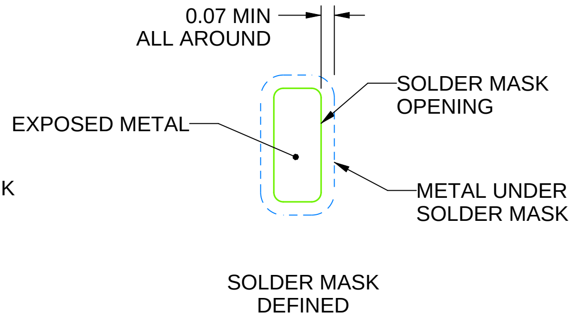
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Reference JEDEC registration MO-220



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



NON SOLDER MASK
DEFINED
(PREFERRED)



SOLDER MASK
DEFINED

SOLDER MASK DETAILS

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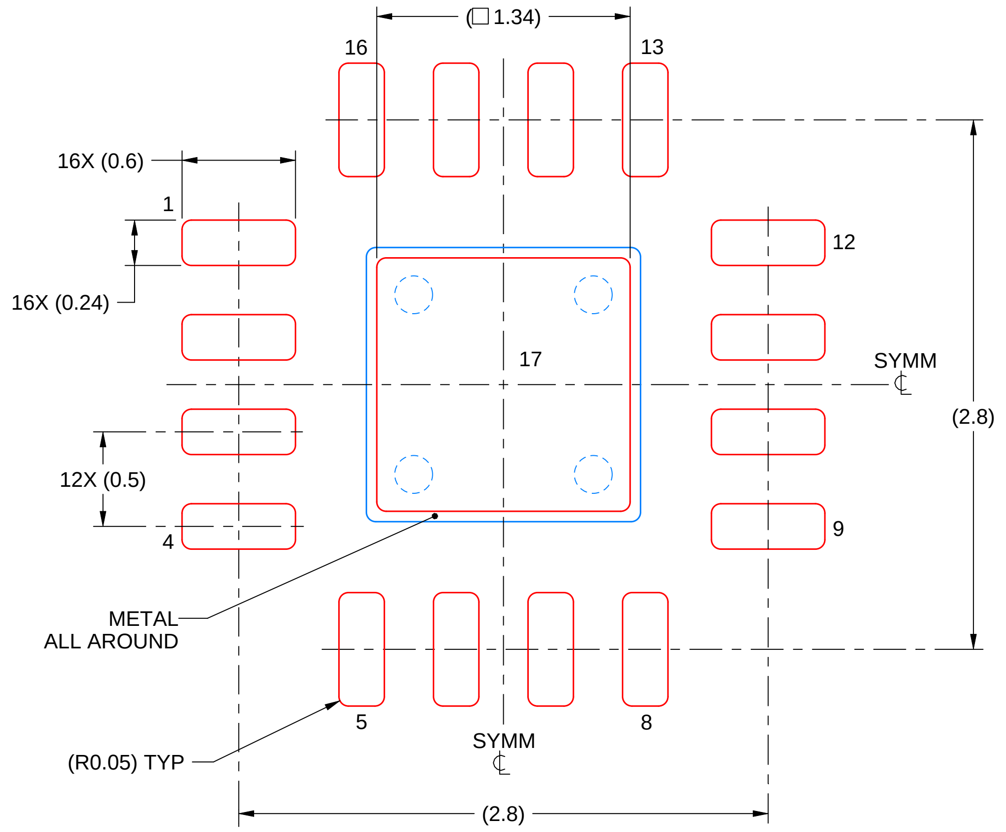
NOTES: (continued)

5. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



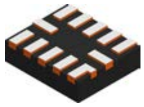
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

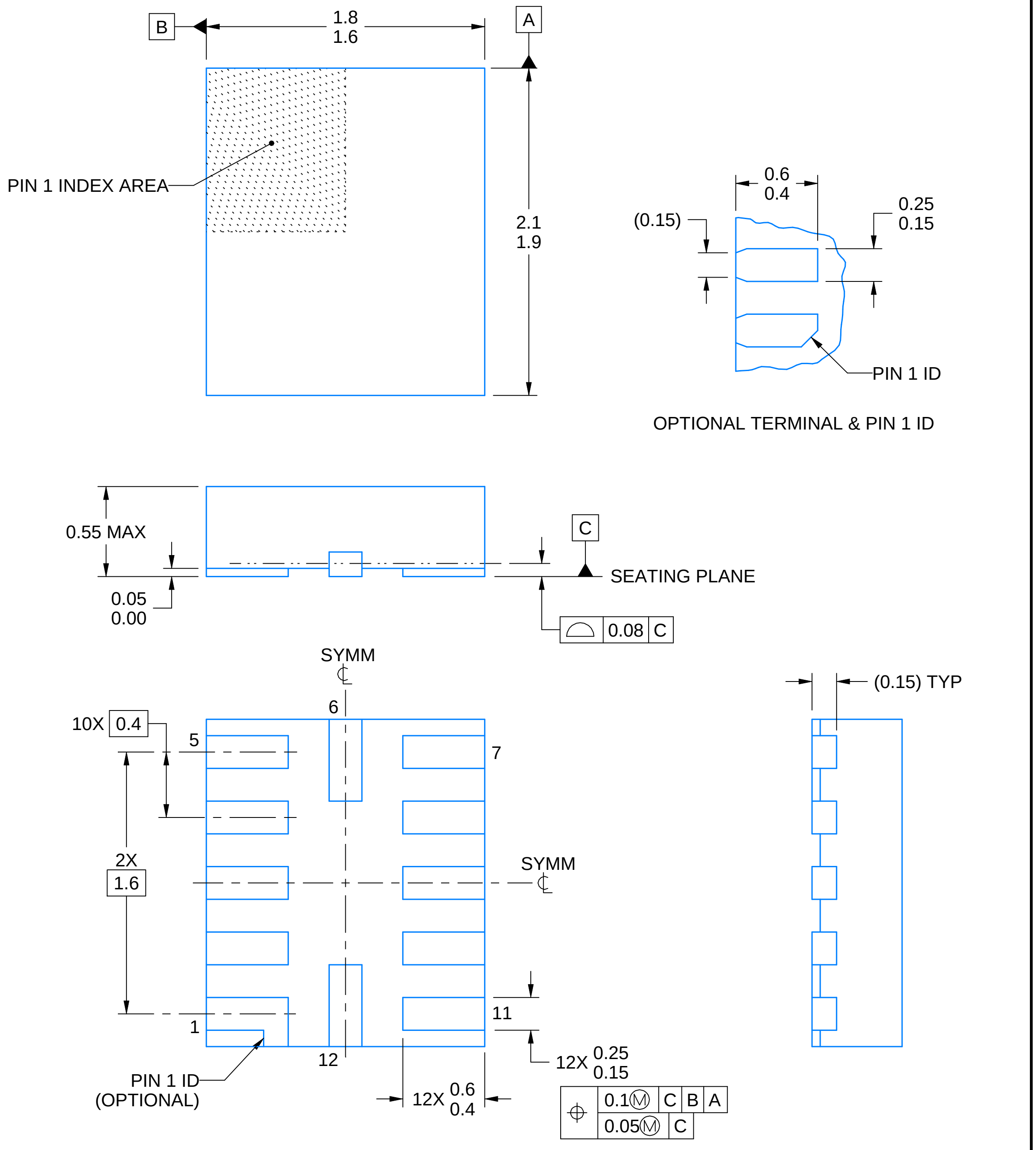
EXPOSED PAD 17:
86% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4219032/A 02/2017

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

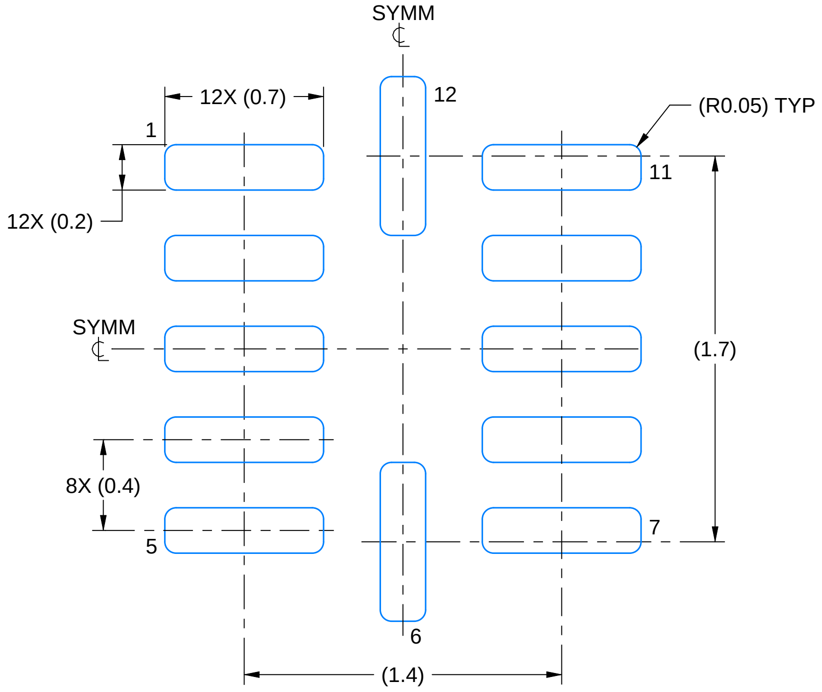




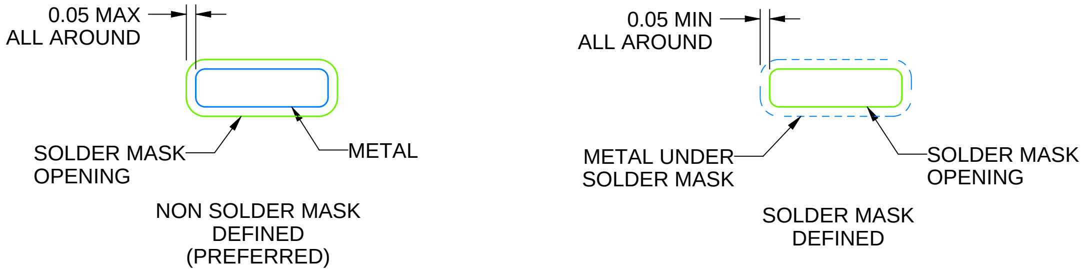
4220310/A 11/2016

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SCALE:30X

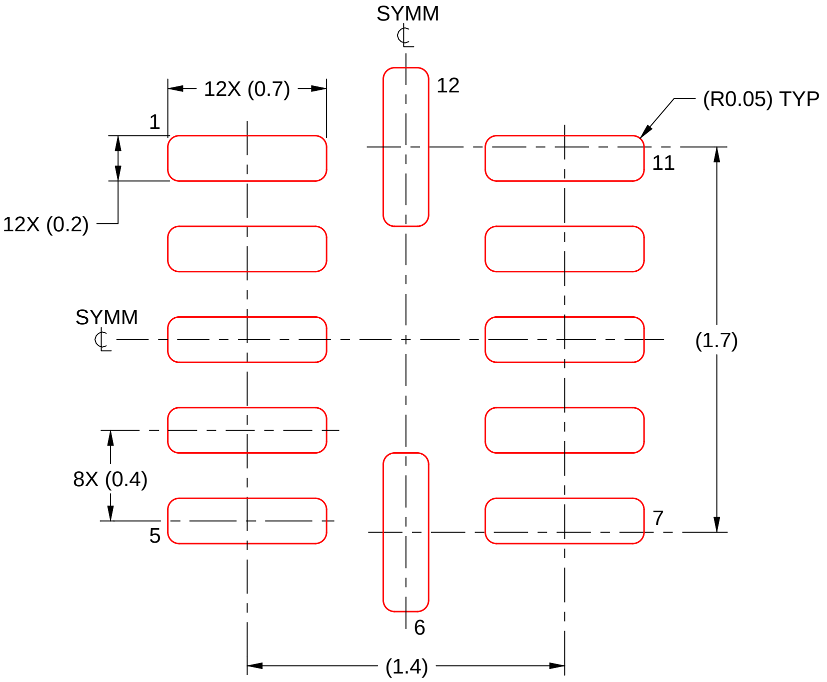


SOLDER MASK DETAILS

4220310/A 11/2016

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 30X

4220310/A 11/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要声明和免责声明

邮寄地址：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265