uA9638C 双路高速差分线路驱动器

1 特性

- 符合或超出 ANSI 标准 EIA/TIA-422-B
- 由单个 5V 电源供电
- 驱动低至 50Ω 负载，高达 15Mbps
- TTL 和 CMOS 输入兼容性
- 输出短路保护
- 可与 DS9638 互换

2 应用

- 工厂自动化
- ATM 和点钞机
- 智能电网
- 交流和伺服 电机驱动器

3 说明

uA9638 是一款双路高速差分线路驱动器，可满足 ANSI 标准 EIA/TIA-422-B 的要求。输入是 TTL 和 CMOS 兼容型输入，并且具有输入钳位二极管。肖特基(Schottky)钳位二极管晶体管用于大大减少传播延迟时间。该器件由单个 5V 电源供电并采用 8 引脚封装。

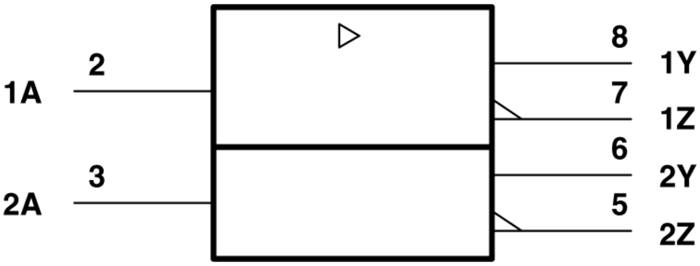
uA9638 提供高速驱动低阻抗负载所需的电流。在设计正确的系统中，通常搭配使用双绞线电缆和差分接收器，基带数据速率传输可高达甚至超过 15Mbps。uA9637A 双路线路接收器通常用作接收器。要在同样的引脚配置下获得更快的开关速度，请参阅 SN75ALS191。

uA9638 的工作温度范围是 0°C 至 70°C。

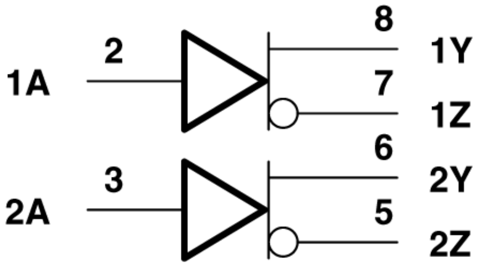
封装信息

器件型号	封装[1]	封装尺寸[2]
uA9638	SOIC（D，8）	4.9mm × 6mm
	PDIP（P，8）	9.81mm × 9.43mm

[1] 有关更多信息，请参阅节 10。
[2] 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。



逻辑符号†



逻辑图

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† 此符号符合 ANSI/IEEE 标准 91-1984 和 IEC 出版物 617-12。

Table of Contents

4 Pin Configuration and Functions

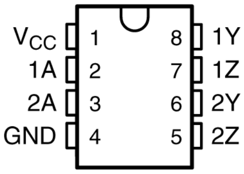


图 4-1. D (SOIC) or P (PDIP) Package (Top View)

表 4-1. Pin Functions

PIN		TYPE[(1)]	DESCRIPTION
NAME	NO.		
V_{CC}	1	P	5V Supply Positive Terminal Connection
1A	2	I	Single Ended Data Input for Channel 1
2A	3	I	Single Ended Data Input for Channel 2
GND	4	GND	Device Ground
2Z	5	O	Inverting Output of Differential Driver for Channel 2
2Y	6	O	Non-Inverting Output of Differential Driver for Channel 2
1Z	7	O	Inverting Output of Differential Driver for Channel 1
1Y	8	O	Non-Inverting Output of Differential Driver for Channel 1

(1) Signal Types: I = Input, O = Output, I/O = Input or Output, P = Power, GND = GND.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	−0.5	7	V
V_I	Input voltage range	−0.5	7	V
	Continuous total power dissipation	See Dissipation Rating Table		
T_A	Operating free-air temperature range	0	70	°C
T_{stg}	Storage temperature range	−65	150	°C
	Lead temperature 1,6 mm (1/16 inch) from 10 seconds		260	°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. NOTE 1: Voltage values except differential output voltages are with respect to network GND.

5.2 Dissipation Rating Table

PACKAGE	T_A = 25 °C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70 °C POWER RATING
D	725 mW	5.8 mW/°C	464 mW
P	1000 mW	8.0 mW/°C	640 mW

5.3 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.75	5	5.25	V
High-level input voltage, V_{IH}	2			V
Low-level input voltage, V_{IL}			0.8	V
High-level output current, I_{OH}			−50	mA
Low-level output current, I_{OL}			50	mA
Operating free-air temperature, T_A	0		70	°C

5.4 Thermal Information

THERMAL METRIC(1)		D (SOIC)	P (PDIP)	UNIT
		8-Pins		
$R_{\theta JA}$	Junction-to-ambient thermal resistance	116.7	84.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56.3	65.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	63.4	62.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	8.8	31.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	62.6	60.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN TYP(1)	MAX	UNIT
V_{IK}	Input clamp voltage	V_{CC} = 4.75V,	I_I = -18mA		-1	-1.2	V
V_{OH}	High-level output voltage	V_{CC} = 4.75V,	V_{IH} = 2V,	I_{OH} = -10mA	2.5 3.5		V
		V_{IL} = 0.8V		I_{OH} = -40mA	2		
V_{OL}	Low-level output voltage	V_{CC} = 4.75V, I_{OL} = 40mA	V_{IH} = 2V,	V_{IL} = 0.8V,		0.5	V
$\|V_{OD1}\|$	Magnitude of differential output voltage	V_{CC} = 5.25V,	I_O = 0			$2V_{OD2}$	V
$\|V_{OD2}\|$	Magnitude of differential output voltage	V_{CC} = 4.75V to 5.25V, See 图 6-1		R_L = 100 Ω	2		V
$\Delta \|V_{OD}\|$	Change in magnitude of differential output voltage(2)					±0.4	V
V_{OC}	Common-mode output voltage(3)					3	V
$\Delta \|V_{OC}\|$	Change in magnitude of common-mode output voltage(2)					±0.4	V
I_O	Output current with power off	V_{CC} = 0	V_O = 6V		0.1	100	μA
			V_O = - 0.25V		-0.1	-100	
			V_O = - 0.25V to 6V			± 100	
I_I	Input current	V_{CC} = 5.25V,	V_I = 5.5V			50	μA
I_{IH}	High-level input current	V_{CC} = 5.25V,	V_I = 2.7V			25	μA
I_{IL}	Low-level input current	V_{CC} = 5.25V,	V_I = 0.5V			-200	μA
I_{OS}	Short-circuit output current(4)	V_{CC} = 5.25V,	V_O = 0		-50	-150	mA
I_{CC}	Supply current (both drivers)	V_{CC} = 5.25V,	No load,	All inputs at 0V	45	65	mA

(1) All typical values are at V_{CC} = 5 V and T_A = 25°C.
(2) $\Delta |V_{OD}|$ and $\Delta |V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level or vice versa.
(3) In Standard EIA-422-A, V_{OC}, which is the average of the two output voltages with respect to ground, is called output offset voltage, V_{OS}.
(4) Only one output at a time should be shorted, and duration of the short circuit should not exceed one second.

5.6 Switching Characteristics

V_{CC} = 5V, T_A = 25°C

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
$t_{d(OD)}$	Differential output delay time	C_L = 15pF,	R_L = 100	See 图 6-2		10	20	ns
$t_{t(OD)}$	Differential output transition time					10	20	ns
$t_{sk(o)}$	Output skew	See 图 6-2						1

6 Parameter Measurement Information

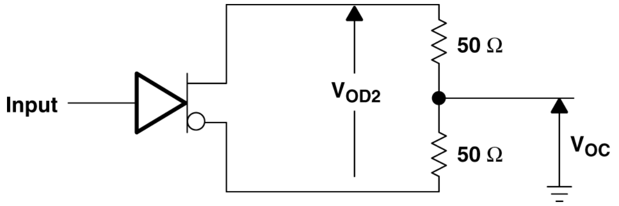
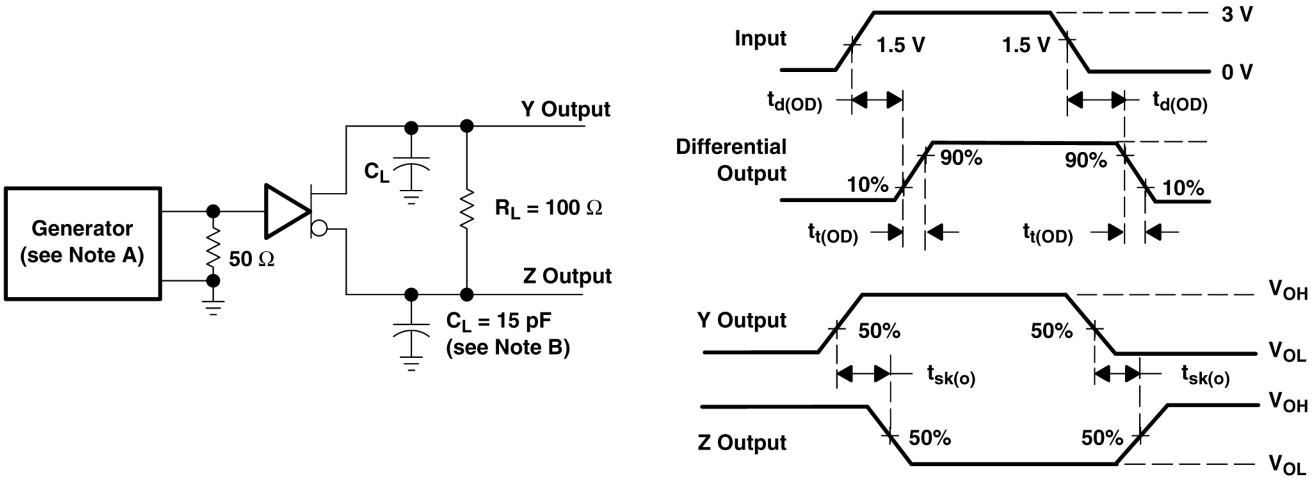


图 6-1. Differential and Common-Mode Output Voltages



TEST CIRCUIT VOLTAGE WAVEFORMS

A. The input pulse generator has the following characteristics: Z_O = 50 Ω, PRR ⩽ 500kHz, t_w = 100ns, t_r = ⩽ 5ns.

B. C_L includes probe and jig capacitance.

图 6-2. Test Circuit and Voltage Waveforms

7 Device Functional Modes

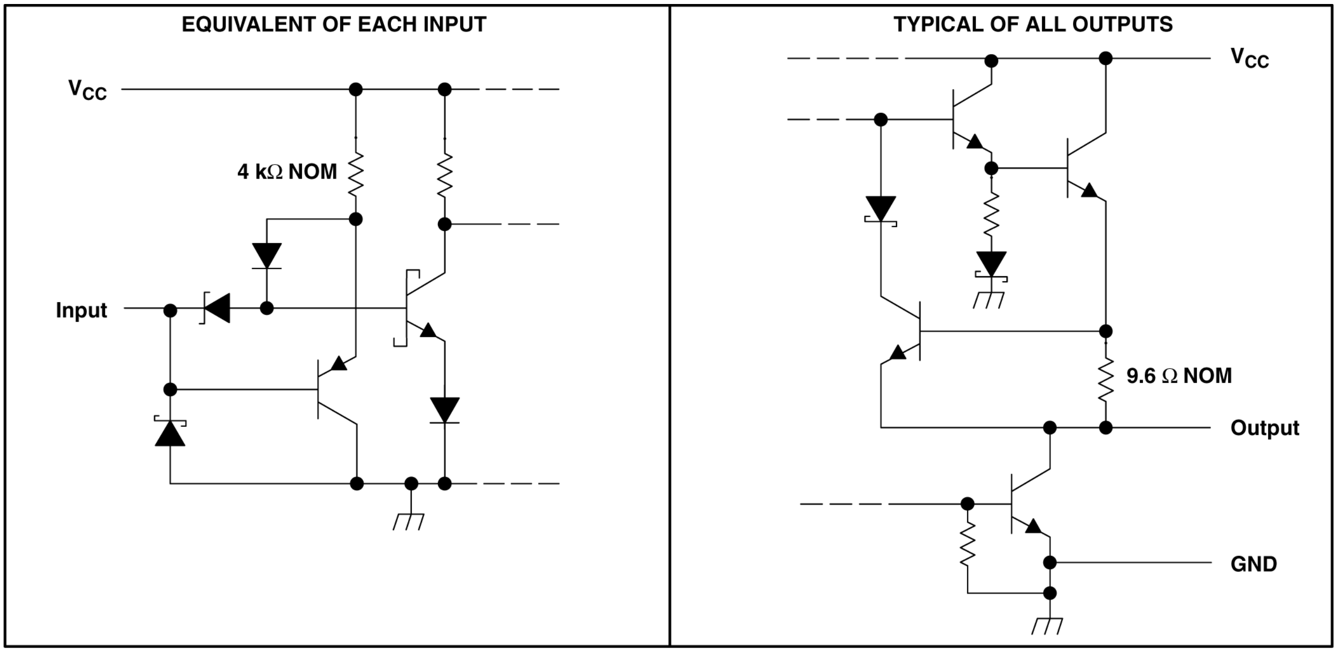


图 7-1. Schematics of Inputs and Outputs

8 Device and Documentation Support

8.1 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

8.2 商标

TI E2E™ is a trademark of Texas Instruments.
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8.3 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

8.4 术语表

TI 术语表	本术语表列出并解释了术语、首字母缩略词和定义。

9 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision C (April 1994) to Revision D (March 2024)	Page
• 更改了整个文档中的表格、图和交叉参考的编号格式	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OPTION ADDENDUM

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UA9638CD	OBSOLETE	SOIC	D	8		TBD	Call TI	Call TI	0 to 70	9638C	
UA9638CDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	9638C	Samples
UA9638CDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	0 to 70	9638C	Samples
UA9638CP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	UA9638CP	Samples
UA9638CPE4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	UA9638CP	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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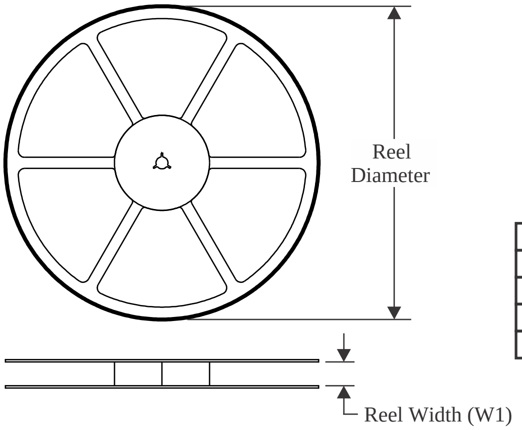
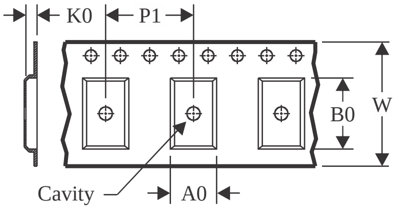
TAPE AND REEL INFORMATION

REEL DIMENSIONS

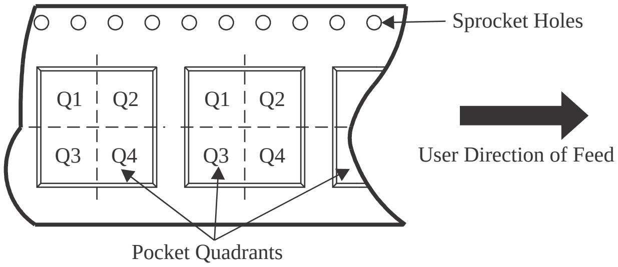


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

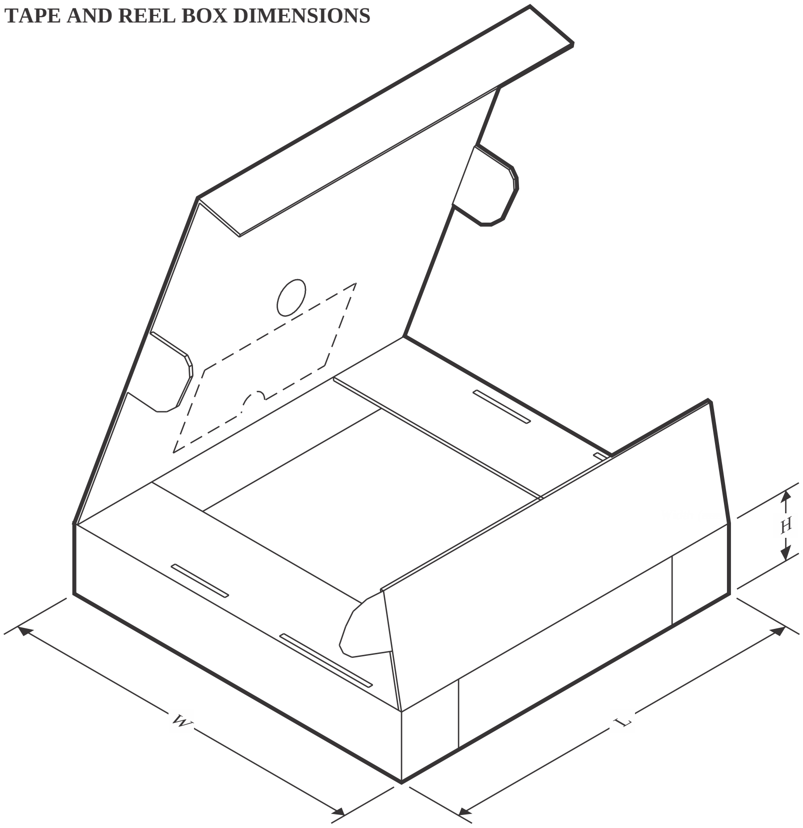
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UA9638CDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

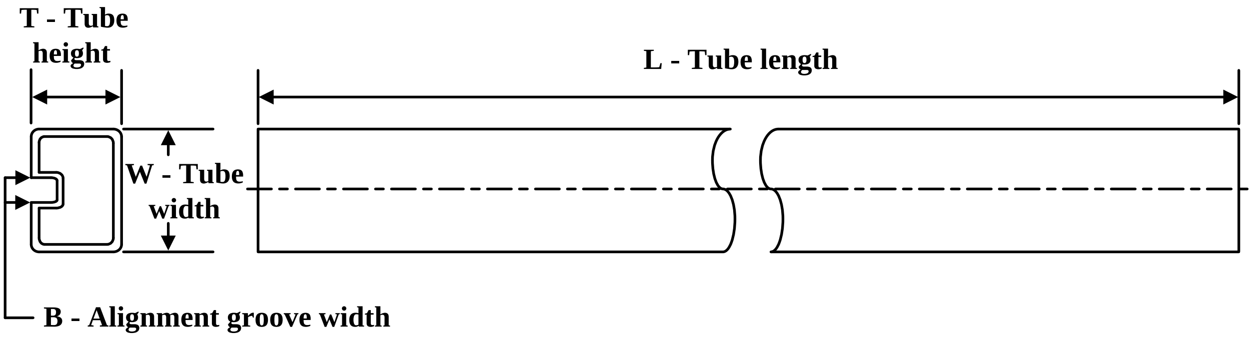
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

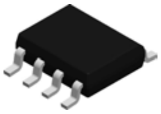
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UA9638CDR	SOIC	D	8	2500	340.5	338.1	20.6

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
UA9638CD	D	SOIC	8	75	507	8	3940	4.32
UA9638CDE4	D	SOIC	8	75	507	8	3940	4.32
UA9638CP	P	PDIP	8	50	506	13.97	11230	4.32
UA9638CPE4	P	PDIP	8	50	506	13.97	11230	4.32

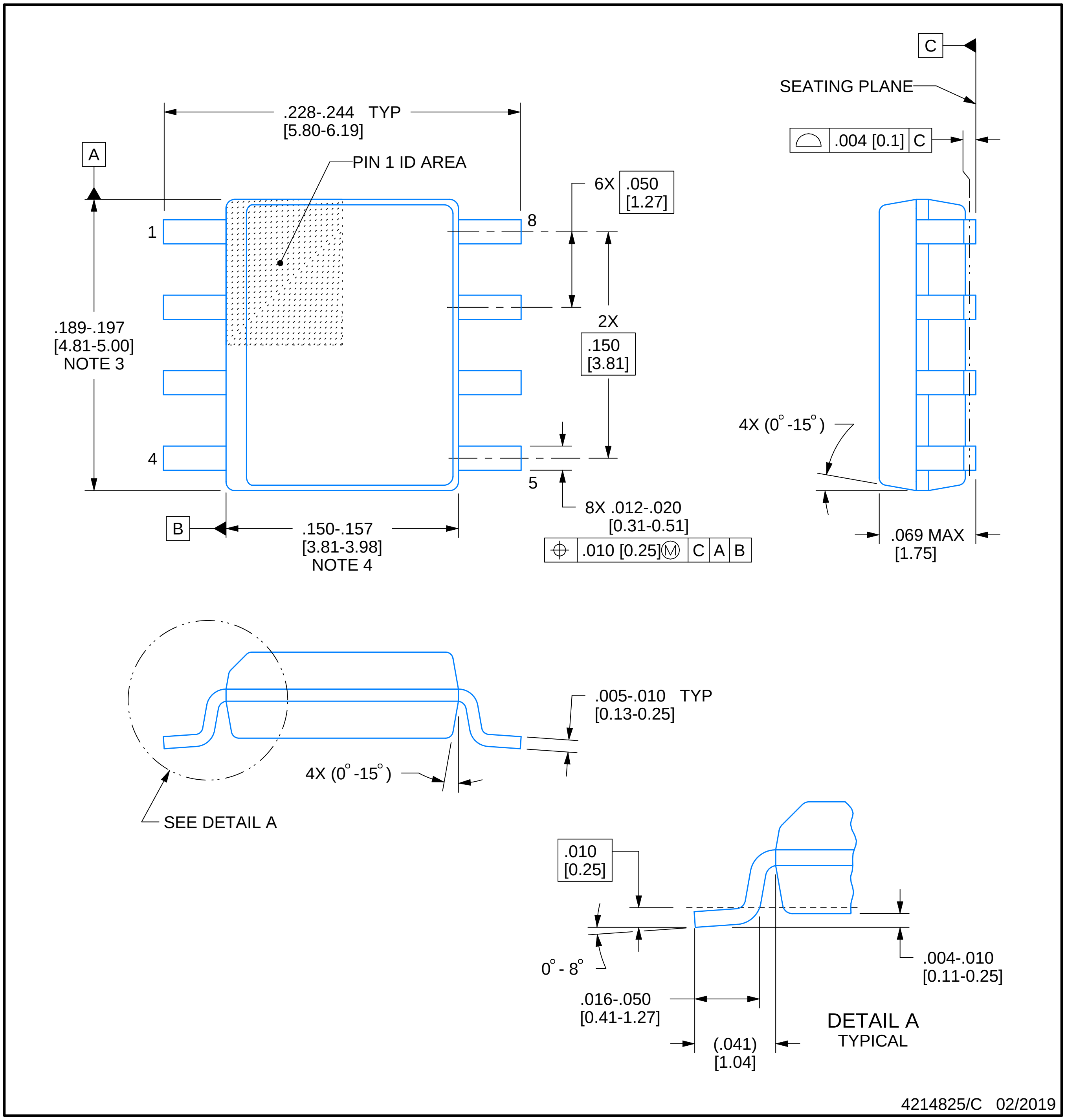


PACKAGE OUTLINE

D0008A

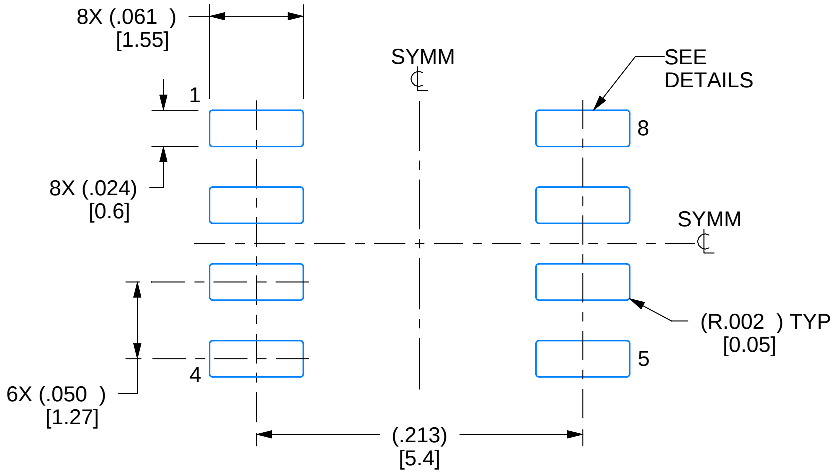
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

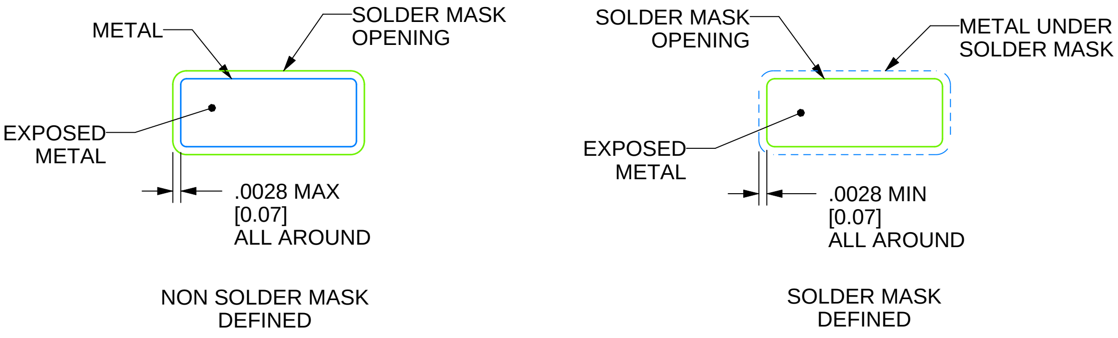


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

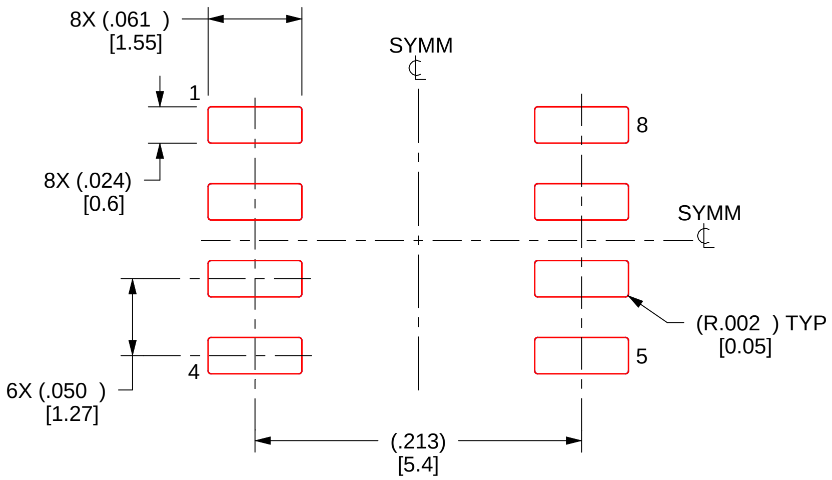


SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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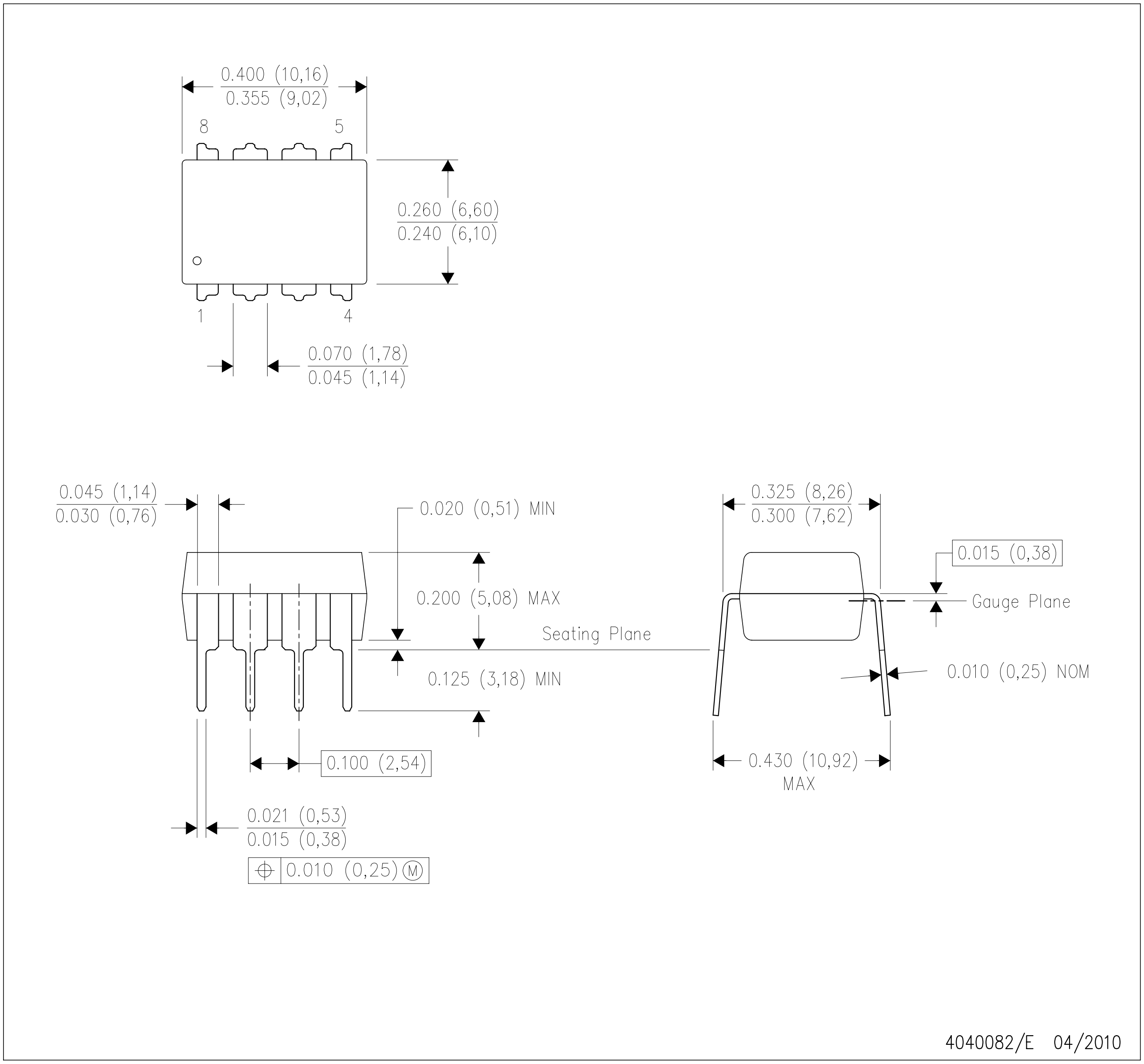
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

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