UC2843A-Q1 电流模式 PWM 控制器

1 特性

- 符合汽车应用要求
- 工作温度范围为 –40°C 至 125°C
- 针对离线和 DC-DC 转换器进行了优化
- 低启动电流 (<0.5mA)
- 经修整的振荡器放电电流
- 自动前馈补偿
- 逐脉冲电流限制
- 增强型负载响应特性
- 带有迟滞功能的欠压锁定
- 双脉冲抑制
- 高电流图腾柱输出
- 内部调整的带隙参考
- 500kHz 工作频率
- 低 R_O 误差放大器
- 使用 UC2843A-Q1 并借助 WEBENCH® Power Designer 创建定制设计方案

2 应用

- 开关模式电源 (SMPS)
- 直流/直流转换器
- 电源模块
- 工业 PSU
- 电池供电型 PSU

3 说明

UC2843A-Q1 控制器件是 UC2843 的引脚对引脚兼容改进版本。该器件提供了控制开关模式电源电流模式所必需的功能，并且具备下述改进的特性。规定的启动电流不到 0.5mA。振荡器放电电流调整为 8.3mA。欠压锁定期间，输出级可在 V_{CC} 高于 5V 时，以低于 1.2V 的电压灌入至少 10mA 的电流。

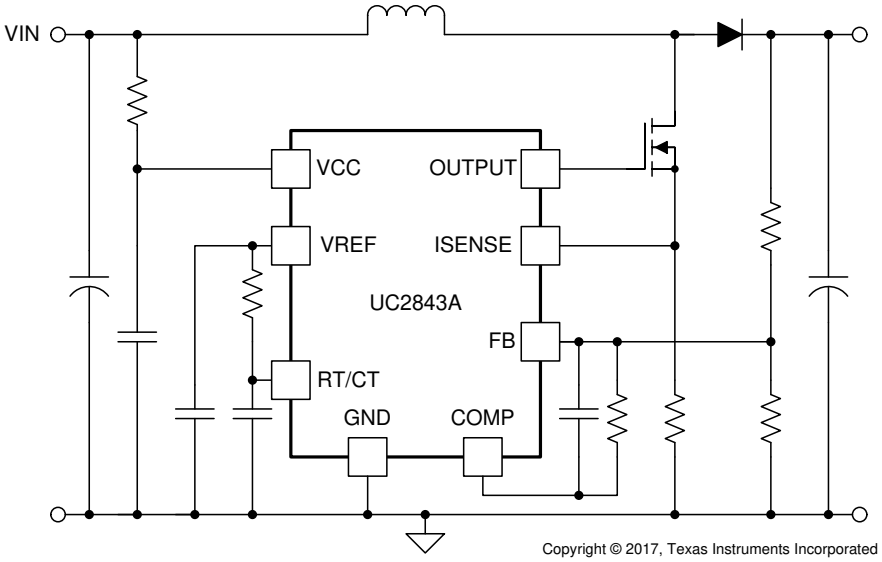
封装信息

器件型号	封装(1)	封装尺寸(2)
UC2843A-Q1	D（SOIC，8）	4.90mm x 6.00mm

(1) 如需了解所有可用封装，请参阅数据表末尾的可订购产品附录。
(2) 封装尺寸（长 × 宽）为标称值，并包括引脚（如适用）。

器件比较表

器件	UVLO ON	UVLO OFF	最大占空比
UC2843A-Q1	8.5V	7.9V	<100%



简化版应用示意图

Table of Contents

4 Pin Configuration and Functions

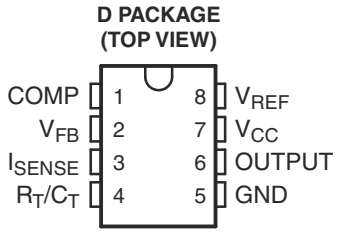


图 4-1. SOIC Package 8-Pin D Top View

Pin Functions

表 4-1. Pin Functions

SOIC (8)		Type[1]	DESCRIPTION
NAME	NO.		
COMP	1	O	Outputs the low impedance 1-MHz internal error amplifier that is also the input to the peak current limit or PWM comparator, with an open-loop gain (AVOL) of 90 dB. This pin is capable of sinking a maximum of 6 mA and is not internally current limited.
FB	2	I	Input to the error amplifier that can be used to control the power converter voltage-feedback loop for stability.
ISENSE	3	I	Input to the peak current limit, PWM comparator of the UCx84xA controllers. When used in conjunction with a current sense resistor, the error amplifier output voltage controls the power systems cycle-by-cycle peak current limit. The maximum peak current sense signal is internally clamped to 1 V. See Functional Block Diagram
RT/CT	4	I	Input to the internal ocsillator that is programmed with an external timing resistor (RT) and timing capacitor (CT). See Oscillator for information on properly selecting these timing components. TI recommends using capacitance values from 470 pF to 4.7 nF. TI also recommends that the timing resistor values chosen be from 5 kΩ to 100 kΩ.
GND	5	-	This is the controller signal ground.
OUTPUT	6	O	Output of 1-A totem pole gate driver. This pin can sink and source up to 1 A of gate driver current. A gate driver resistor must be used to limit the gate driver current.
VCC	7	I	Bias input to the gate driver. This pin must have a biasing capacitor that is at least 10 times greater than the gate capacitance of the main switching FET used in the design.
VREF	8	O	Reference voltage output of the PWM controller. This pin must supply no more than 10 mA under normal operation. This output is short-circuit protected at roughly 100 mA. This reference is also used for internal comparators and needs a high frequency bypass capacitor of 1 µF. The VCC capacitor also must be at least 10 times greater than the capacitor on the VREF pin.

(1) I = Input; O = Output

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

PARAMETER		MIN	MAX	UNIT
V_{CC} voltage (low impedance source)	VCC pin		30	V
V_{CC} voltage (I_{CC} mA)			Self limiting	
Output current, I_{OUT}			±1	A
Output energy (capacitive load)			5	μJ
Analog inputs (pins 2, 3, and 4)		–0.3	6.3	V
Maximum negative voltage	All pins	–0.3		V
Error amplifier output sink current, I_{COMP}			10	mA
Power dissipation at $T_A \leq 25°C$			1	W
Lead temperature (soldering, 10 s)			300	°C
Junction temperature, T_J		–55	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Bias supply voltage	VCC pin		11		V
V_{FB}, V_{RC}, V_{VFB}	Voltage on analog pins	FB, ISENSE, and RT/CT pins	–0.1		5	V
V_{OUT}	Gate driver output voltage		–0.1		V_{CC}	V
I_{VCC}	Supply bias current				25	mA
I_{VREF}	Output current	VREF pin			10	mA
f_{OSC}	Oscillator frequency				500	kHz
T_A	Operating free-air temperature		–40		125	°C

5.4 Thermal Information

THERMAL METRIC			UNIT
θ_{JA}	Package Thermal impedance	117.4	°C/W

5.5 Electrical Characteristics

Unless otherwise stated, these specifications apply for T_A = –40°C to 125°C (UC2843A-Q1); $T_A = T_J$; V_{CC} = 15 V[1]; R_T = 10 kΩ; C_T = 3.3 nF.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
REFERENCE					
Output voltage	T_J = 25°C, I_O = 1 mA	4.95	5	5.05	V
Line regulation	12 ≤ V_{IN} ≤ 25 V		6	20	mV
Load regulation	1 ≤ I_O ≤ 20 mA		6	25	mV
Temperature stability[2]			0.2	0.4	mV/°C
Total output variation	Line, Load, Temperature	4.9		5.1	V
Output noise voltage[7]	10 Hz ≤ f ≤ 10 kHz; T_J = 25°C		50		μV
Long-term stability[7]	T_A = 125°C, 1000 hrs		5	25	mV
Output short circuit		–30	–100	–180	mA
OSCILLATOR					
Initial accuracy	T_J = 25°C	47	52	57	kHz
Voltage stability	12 ≤ V_{CC} ≤ 25 V		0.2	1	%
Temperature stability[7]	T_{MIN} ≤ T_A ≤ T_{MAX}		5		%
Amplitude[7]	$V_{RT/CT}$ (pin 4) peak to peak		1.7		V
Discharge current[4]	T_J = 25°C, $V_{RT/CT}$ = 2 V	7.8	8.3	8.8	mA
	$V_{RT/CT}$ = 2 V	7.5		8.8	

Unless otherwise stated, these specifications apply for T_A = –40°C to 125°C (UC2843A-Q1); $T_A = T_J$; V_{CC} = 15 V[1]; R_T = 10 kΩ; C_T = 3.3 nF.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ERROR AMPLIFIER						
	Input voltage	V_{COMP} = 2.5 V	2.45	2.5	2.55	V
	Input bias current			–0.3	–1	µA
A_{VOL}	Open-loop gain	2 ≤ V_O ≤ 4 V	65	90		dB
	Unity gain bandwidth[7]	T_J = 25°C	0.7	1		MHz
CMRR	Common mode rejection ratio	12 ≤ V_{CC} ≤ 25 V	60	70		dB
	Output sink current	V_{FB} = 2.7 V, V_{COMP} = 1.1 V	2	6		mA
	Output source current	V_{FB} = 2.3 V, V_{COMP} = 5 V	–0.5	–0.8		mA
	V_{OUT} high	V_{FB} = 2.3 V, R_L = 15 kΩ to ground	5	6		V
	V_{OUT} low	V_{FB} = 2.7 V, R_L = 15 kΩ to VREF		0.7	1.1	V
CURRENT SENSE						
	Gain[5] [6]		2.85	3	3.15	V/V
	Maximum input signal[5]	V_{COMP} = 5 V	0.9	1	1.1	V
PSRR	Power supply rejection ratio[5]	12 ≤ V_{CC} ≤ 25 V		70		dB
	Input bias current			–2	–10	µA
	Delay to output[7]	V_{ISENSE} = 0 to 2 V		150	300	ns
OUTPUT						
	Output low level	I_{SINK} = 20 mA		0.1	0.4	V
		I_{SINK} = 200 mA		1.5	2.2	
	Output high level	I_{SOURCE} = 20 mA	13	13.5		V
		I_{SOURCE} = 200 mA	12	13.5		
	Rise time[7]	T_J = 25°C, C_L = 1 nF		25	150	ns
	Fall time[7]	T_J = 25°C, C_L = 1 nF		25	150	ns
	UVLO saturation	V_{CC} = 5 V, I_{SINK} = 10 mA		0.7	1.2	V
UNDERVOLTAGE LOCKOUT						
	Start threshold		7.8	8.4	9	V
	Minimum operation voltage after turnon		7	7.6	8.2	V
PWM						
	Maximum duty cycle		92	96	100	%
	Minimum duty cycle				0	%
TOTAL STANDBY CURRENT						
	Start-up current			0.3	0.5	mA
	Operating supply current	V_{FB} = V_{ISENSE} = 0 V		11	17	mA
	V_{CC} Zener voltage	I_{CC} = 25 mA	30	39		V

5.6 Typical Characteristics

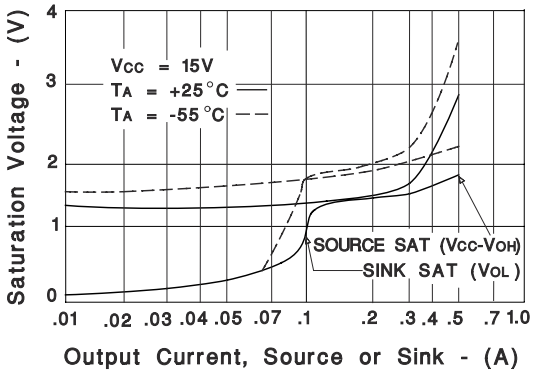


图 5-1. Output Saturation Characteristics

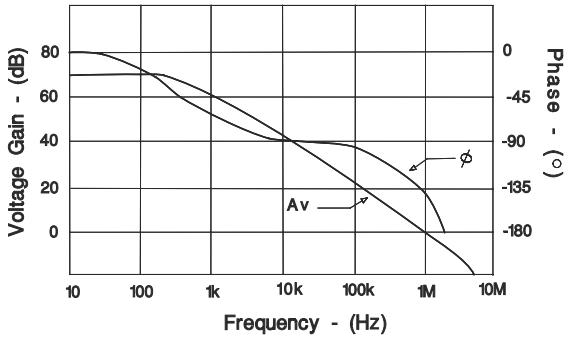


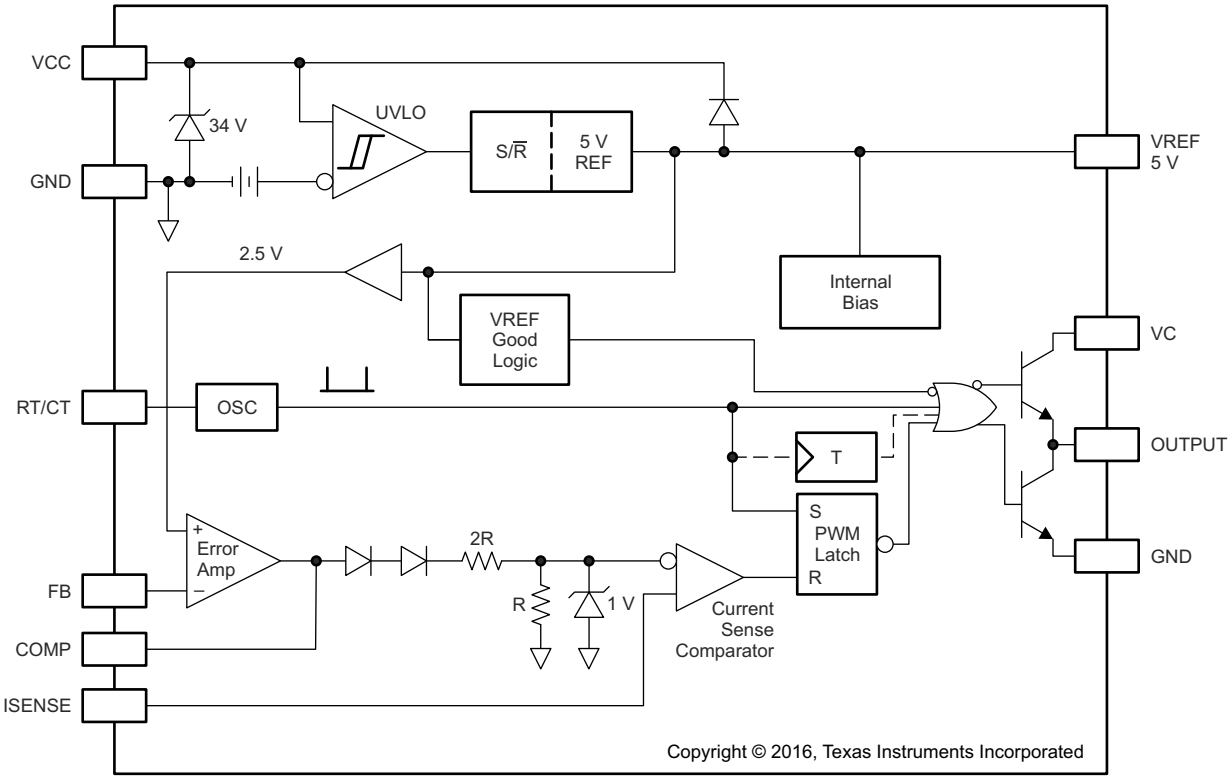
图 5-2. Error Amplifier Open-Loop Frequency Response

6 Detailed Description

6.1 Overview

The UC2843A-Q1 fixed-frequency pulse-width-modulator (PWM) controllers are designed to operate at switching frequencies up to 500 kHz. This controller is designed for peak current mode (PCM) and can be used in isolated and non-isolated power supply designs. These controllers can drive FETs directly from the output, which is capable of sourcing and sinking up to 1 A of gate driver current. These devices also have a built-in low-impedance amplifier that can be used in non-isolated designs to control the power supply output voltage and feedback loop.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Pulse-by-Pulse Current Limiting

Pulse-by-pulse limiting is inherent in the current mode control scheme. An upper limit on the peak current can be established by simply clamping the error voltage. Accurate current limiting allows optimization of magnetic and power semiconductor elements while ensuring reliable supply operation.

6.3.2 Current Sense Circuit

Peak current (I_S) is determined by 方程式 1:

$$I_{S(max)} \times \frac{1\,V}{R_S} \tag{1}$$

A small RC filter may be required to suppress switch transients.

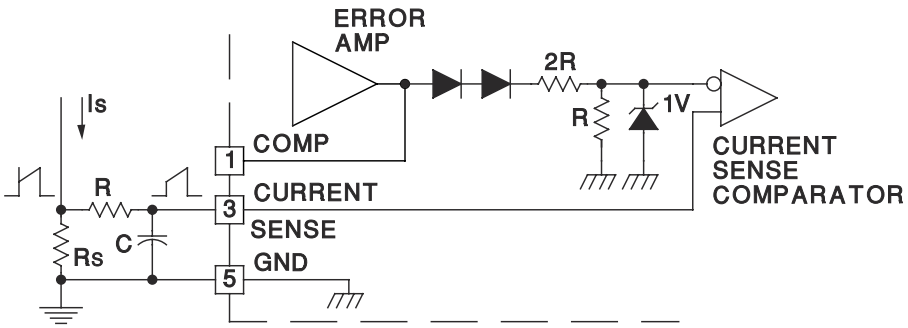


图 6-1. Current Sense Circuit Diagram

6.3.3 Error Amplifier Configuration

The error amplifier can source up to 0.8 mA, and sink up to 6 mA.

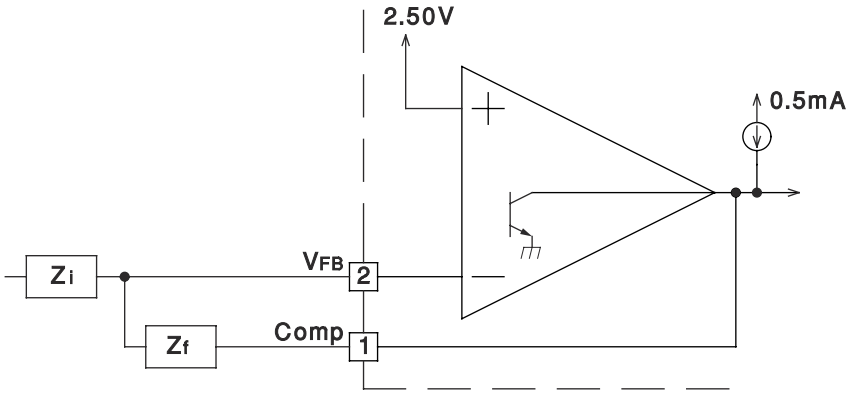


图 6-2. Error Amplifier Configuration Diagram

6.3.4 Undervoltage Lockout

The UC2843A-Q1 device features undervoltage lockout protection circuits for controlled operation during power-up and power-down sequences. Undervoltage lockout thresholds for the UC2843A-Q1 device is optimized for two groups of applications: off-line power supplies and DC-DC converters. The UC2843A-Q1 controller has a much narrower VCC_{ON} to VCC_{OFF} hysteresis and may be used in DC to DC applications where the input is considered regulated.

During UVLO the device draws typically 0.3 mA of supply current. The low VCC current of the UC2843A-Q1 results in lower power drawn from the line. The reduced start-up current is of particular concern in off-line supplies where the devive is *powered-up* from the high-voltage DC rail, then bootstrapped to an auxiliary winding on the main transformer. Power is then dissipated in the start-up resistor which is sized by the devive’s start-up current. Lowering this by 50% in the UC2843A-Q1 reduces the resistors power loss by the same percentage. Once crossing the turnon threshold the device supply current increases typically to about 11 mA, During undervoltage lockout, the UC2843A-Q1 device prevent the power MOSFET from parasitically turning on due to the *Miller* effect at power-up. This improved design to the lower totem-pole transistor’s operation during undervoltage lockout allows the devives to sink higher currents, up to 10 mA, at saturation voltages as low as 0.7 V, compared to the UCx84x devices which would only sink up to 0.2 mA under the same conditions.

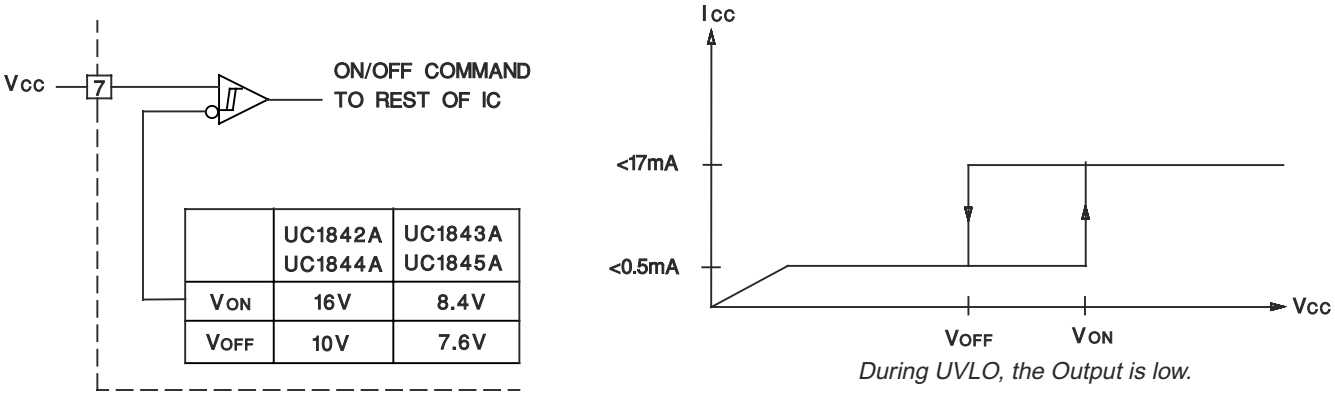


图 6-3. Undervoltage Lockout

6.3.5 Oscillator

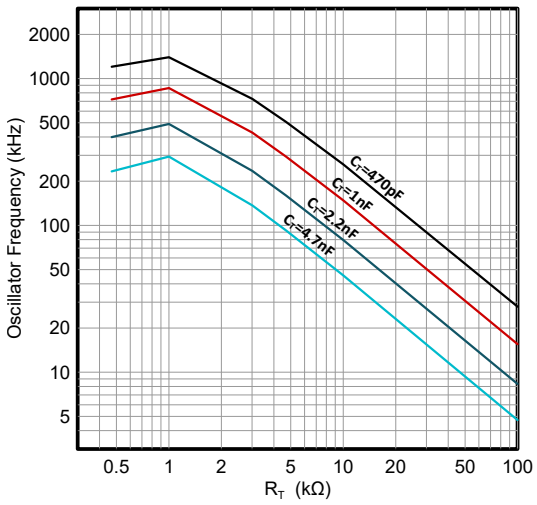


图 6-4. Oscillator Frequency vs Timing Resistance

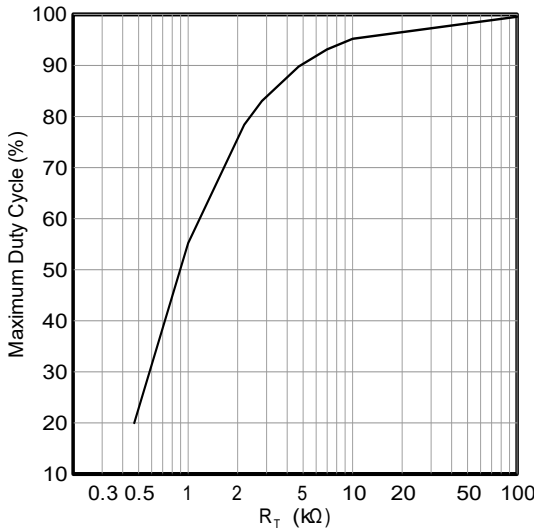
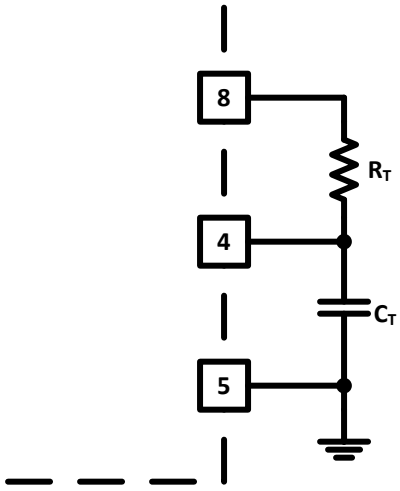


图 6-5. Maximum Duty Cycle vs Timing Resistance



$$\text{For } R_T > 5\text{ k} \quad f \approx \frac{1.72}{R_T \times C_T}$$

图 6-6. Oscillator Section

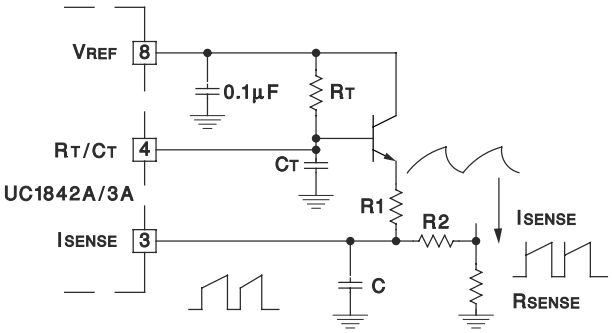


图 6-7. Slope Compensation

Precision operation at high frequencies with an accurate maximum duty cycle, see 图 6-5, can now be obtained with the UC2843A-Q1 device due to its trimmed oscillator discharge current. This nullifies the effects of production variations in the initial discharge current or dead time.

A fraction of the oscillator ramp can be resistively summed with the current sense signal, to provide slope compensation for converters requiring duty cycles over 50%. Capacitor C forms a filter with R2 to suppress the leading-edge switch spikes.

6.4 Device Functional Modes

6.4.1 Normal Operation

The device can be used in peak current mode (PCM) control or voltage mode (VM) control. When the converter is operating in PCM, the voltage amplifier output will regulate the converter's peak current and duty cycle. When the device is used in VM control, the voltage amplifier output will regulate the power converter's duty cycle. The regulation of the system's peak current and duty cycle can be achieved with the use of the integrated error amplifier and external feedback circuitry.

6.4.2 Undervoltage Lockout (UVLO) Start-Up

During system start-up, VCC voltage starts to rise from 0. Before the VCC voltage reaches its corresponding start threshold, the device is operating in UVLO mode. After the UVLO turn start-up threshold is met the device will become active and the reference will come up to 5 V.

6.4.3 UVLO Turnoff Mode

If the bias voltage to VCC drops below the UVLO minimum operating voltage, PWM switching stops and the reference will become inactive, returning to 0 V. The device can be restarted by applying a voltage greater than the UVLO start threshold to the VCC pin.

7 Application and Implementation

备注

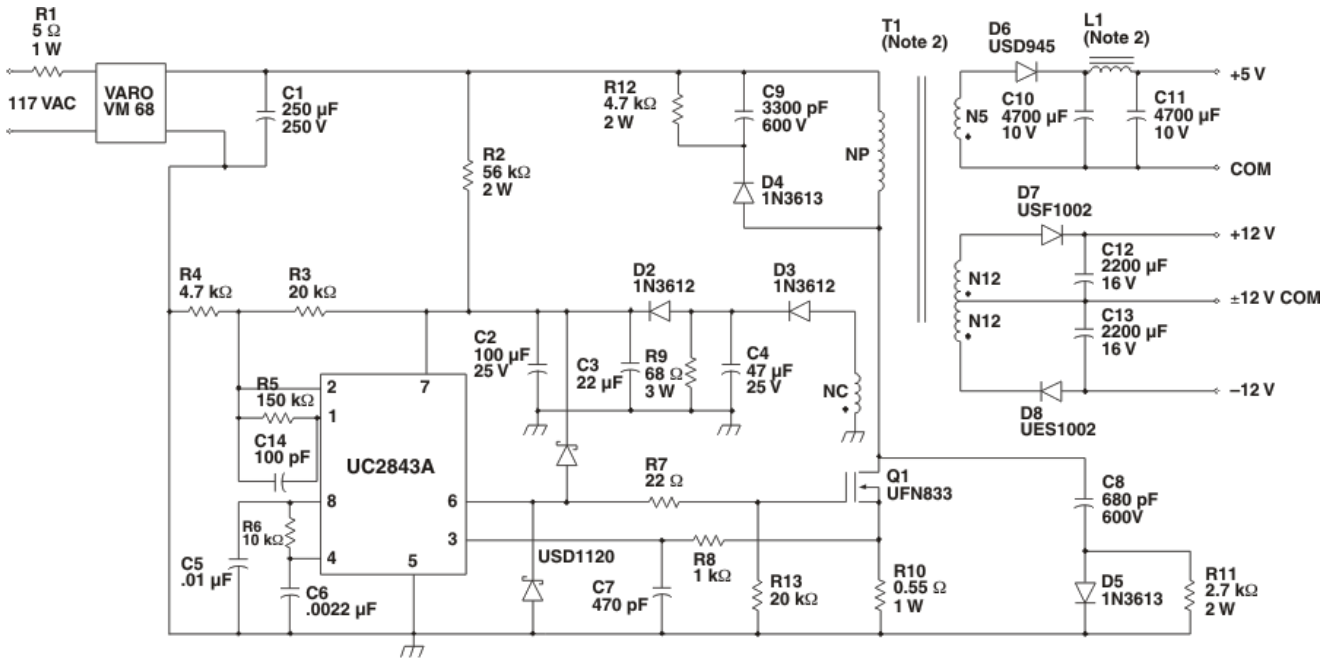
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

The UC2843A-Q1 controller ia a peak-current mode pulse-width modulators. The controller has an onboard amplifier and can be used in isolated or nonisolated power supply designs. There is an onboard totem-pole gate driver capable of delivering 1 A of peak current. This is a high-speed PWM capable of operating at switching frequencies up to 500 kHz.

7.2 Typical Application

A typical application for the UC2843A-Q1 in an off-line flyback converter is shown in 图 7-1. The UC2843A uses an inner current control loop that contains a small current sense resistor which senses the primary inductor current ramp. This current sense resistor transforms the inductor current waveform to a voltage signal that is input directly into the primary side PWM comparator. This inner loop determines the response to input voltage changes. An outer voltage control loop involves comparing a portion of the output voltage to a reference voltage at the input of an error amplifier. When used in an off-line isolated application, the voltage feedback of the isolated output is accomplished using a secondary-side error amplifier and adjustable voltage reference, such as the TL431. The error signal crosses the primary to secondary isolation boundary using an opto-isolator whose collector is connected to the VREF pin and the emitter is connected to FB. The outer voltage control loop determines the response to load changes.



Power Supply Specifications

1. Input Voltage 95 VAC to 130 VAC (50 Hz/60 Hz)
2. Line Isolation 3750 V
3. Switching Frequency 40 kHz
4. Efficiency, Full Load 70%
5. Output Voltage:
   A. 5 V ±5%; 1-A to 4-A Load
   B. 12 V ±3%; 0.1-A to 0.3-A Load; Ripple voltage: 100 mV P-P Max
   C. –12 V ±3%; 0.1-A to 0.3-A Load; Ripple voltage: 100 mV P-P Max

图 7-1. Typical Flyback Application Circuit

8 Power Supply Recommendations

TI recommends using the UCx84xA in isolated or non-isolated peak current mode control power supplies. The device can be used in buck, boost, flyback, and forwarded converter-based power supply topologies.

9 Layout

9.1 Layout Guidelines

- Star grounding techniques must be used.
- Current loops must be kept as short and narrow as possible.
- The IC ground and power ground must meet at the return for the input bulk capacitor. Ensure that high frequency and high current from the power stage does not go through the signal ground paths.
- A high-frequency bypass capacitor (C_3) must be placed across VCC and GND pins as close as possible to the pins.
- Resistor R_8 and capacitor C_7 form a low-pass filter for the current sense signal. C_7 must be as close to CS and GND pins as possible.
- Capacitor C_5 must be as close to VREF and GND pins as possible.

10 Device and Documentation Support

10.1 Device Support

10.1.1 Development Support

- TI Engineer-to-Engineer Support Forum, https://e2e.ti.com/

10.1.1.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the UCx84xA device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

10.1.2 Device Nomenclature

C_{IN}	Input bulk capacitance
C_{OUT}	Output capacitance
D	Duty cycle
ESR	Equivalent series resistance
$G_{BC}(f)$	An estimate of the transfer function from the output of the opto-isolator to the PWM control voltage.
G_O	The DC gain of the control to output transfer function.
$G_{OPTO}(f)$	The approximate transfer function across the opto-isolator in the design.
I_{LPM}	Transformer primary average current
I_{LpPK}	Peak transformer primary current
L_{PM}	Transformer primary magnetizing inductance
L_{SM}	Transformer secondary magnetizing inductance
N_{PS}	Primary to secondary transformer turns ratio
N_{AS}	Auxiliary to secondary transformer turns ratio
$T_V(f)$	is the feedback control loop transfer function.
$V_{INripple}$	Input ripple voltage

10.2 Documentation Support

10.2.1 Related Documentation

For related documentation see the following:

Design Review: 150 Watt Current-Mode Flyback (SLUP078)

10.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 10-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
UC1842A	Click here	Click here	Click here	Click here	Click here
UC1843A	Click here	Click here	Click here	Click here	Click here
UC1844A	Click here	Click here	Click here	Click here	Click here
UC1845A	Click here	Click here	Click here	Click here	Click here
UC2842A	Click here	Click here	Click here	Click here	Click here
UC2843A	Click here	Click here	Click here	Click here	Click here
UC2844A	Click here	Click here	Click here	Click here	Click here
UC2845A	Click here	Click here	Click here	Click here	Click here
UC3842A	Click here	Click here	Click here	Click here	Click here
UC3843A	Click here	Click here	Click here	Click here	Click here
UC3844A	Click here	Click here	Click here	Click here	Click here
UC3845A	Click here	Click here	Click here	Click here	Click here

10.4 接收文档更新通知

要接收文档更新通知，请导航至 ti.com 上的器件产品文件夹。点击*通知* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

10.5 支持资源

TI E2E™ 中文支持论坛是工程师的重要参考资料，可直接从专家处获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题，获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的使用条款。

10.6 Trademarks

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10.7 静电放电警告

静电放电 (ESD) 会损坏这个集成电路。德州仪器 (TI) 建议通过适当的预防措施处理所有集成电路。如果不遵守正确的处理和安装程序，可能会损坏集成电路。

ESD 的损坏小至导致微小的性能降级，大至整个器件故障。精密的集成电路可能更容易受到损坏，这是因为非常细微的参数更改都可能会导致器件与其发布的规格不相符。

10.8 术语表

TI 术语表　　本术语表列出并解释了术语、首字母缩略词和定义。

11 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision A (July 2022) to Revision B (October 2024)	Page
• 更新了整个文档中的表格、图和交叉参考的编号格式	1
• Changed in Absolute Maximum Ratings, Lead Temperature (soldering, 10s) from 260°C to 300°C	4
• Changed Thermal Information, Package Thermal Impedance from 97°C/W to 117.4°C/W	4
• Added missing "≤" in Electrical Characteristics table, CURRENT SENSE: PSRR, test conditions	5

- Changed in Electrical Characteristics table, OUTPUT SECTION: Rise and fall time, typical value from 50ns to 25ns.....5
- Changed in Electrical Characteristics table, PWM SECTION: maximum duty cycle, minimum value from 94% to 92%.....5
- Changed Electrical Characteristics table, TOTAL STANDBY CURRENT, Vcc Zener voltage, typical value from 34V to 39V.....5
- Updated Typical Characteristics Frequency vs Rt and Maximum Duty Cycle vs Rt graphs.....7

Changes from Revision * (May 2008) to Revision A (July 2022) **Page**

- Updated analog input pins 3 and 5 to 2, 3, and 4.....4
- Added Junction Temperature, T_J to the Absolute Maximum Ratings table.....4
- Added Recommended Operating Conditions.....4
- Changed Low-level Output Voltage from 15 V to 1.5 V.....5

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UC2843AQD8RQ1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(2843AQ, UC2843AQ)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF UC2843A-Q1 :

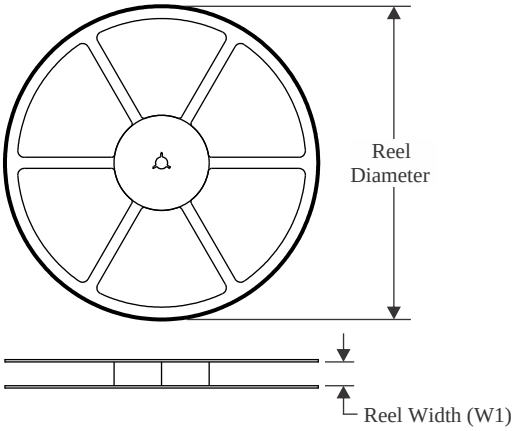
- Catalog : UC2843A

NOTE: Qualified Version Definitions:

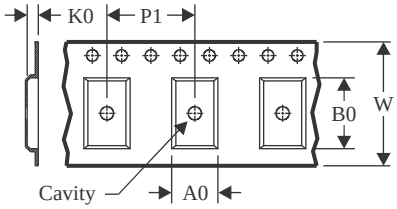
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

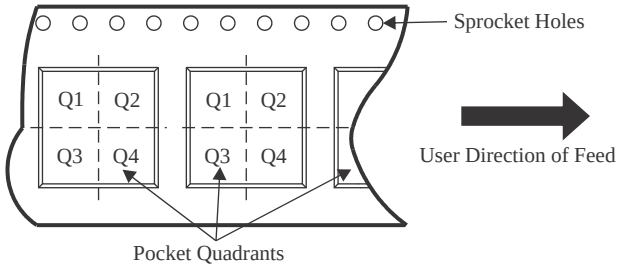


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

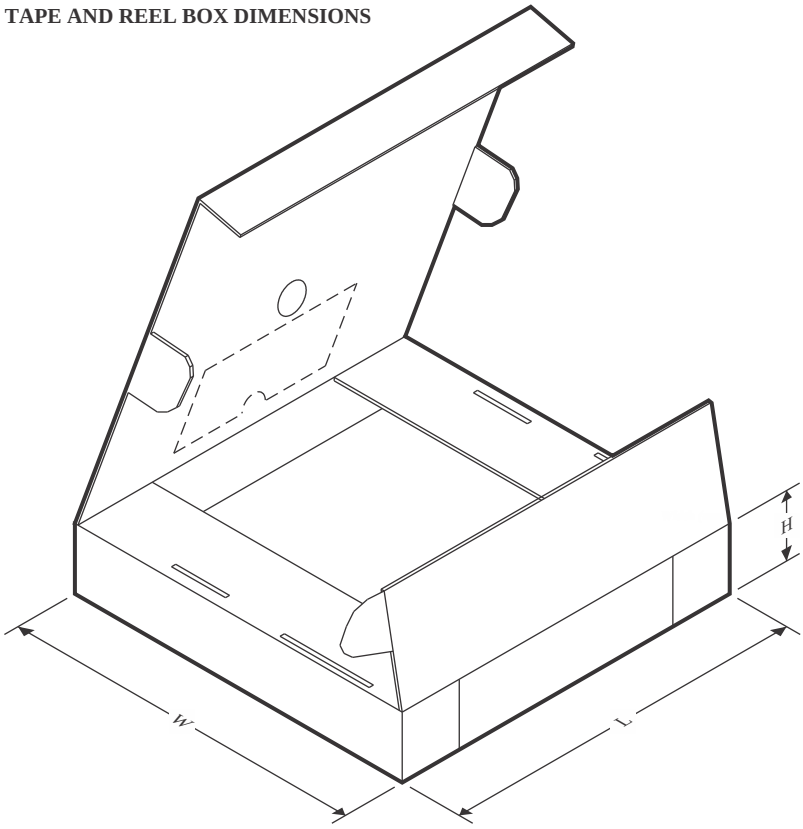
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

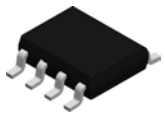
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UC2843AQD8RQ1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UC2843AQD8RQ1	SOIC	D	8	2500	356.0	356.0	35.0

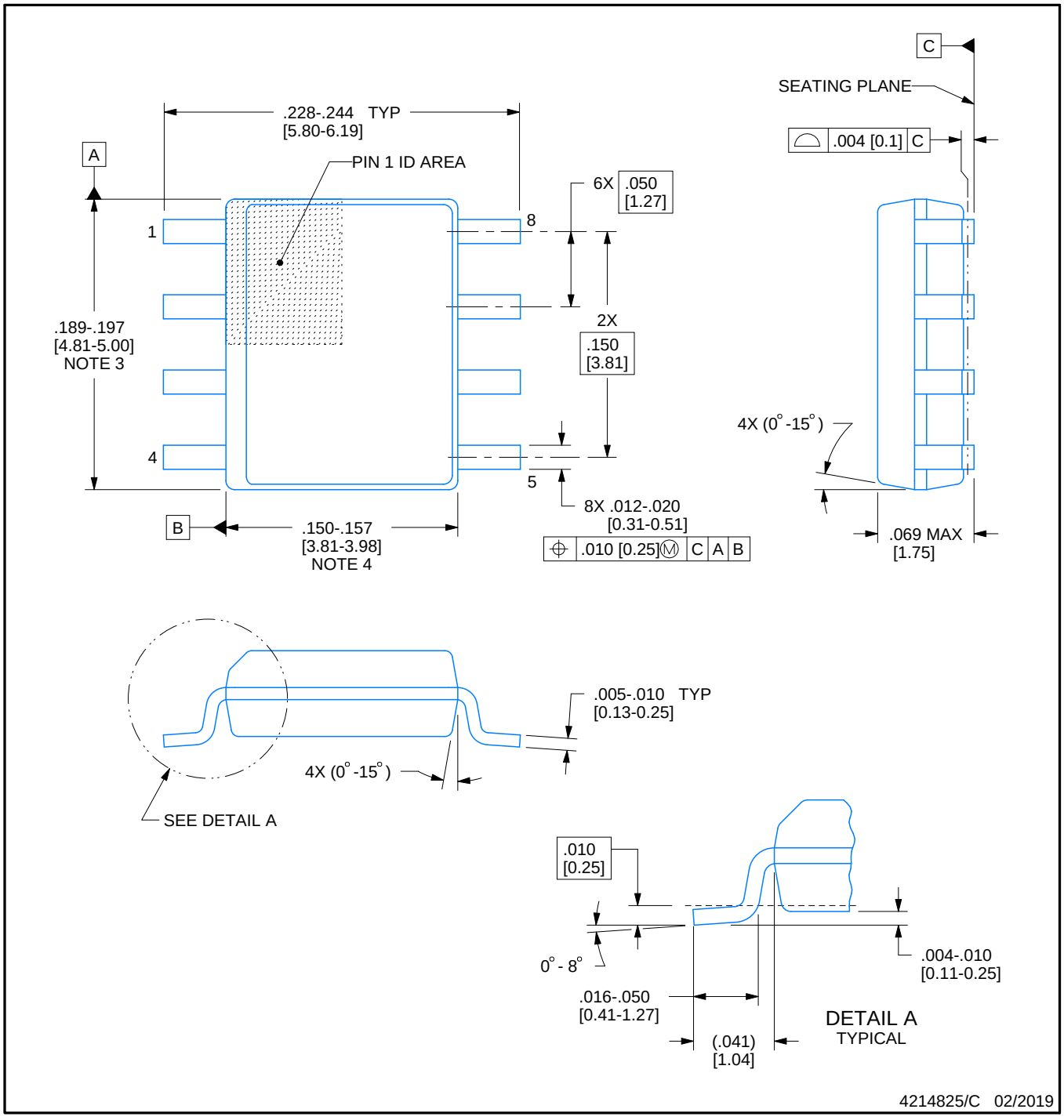


PACKAGE OUTLINE

D0008A

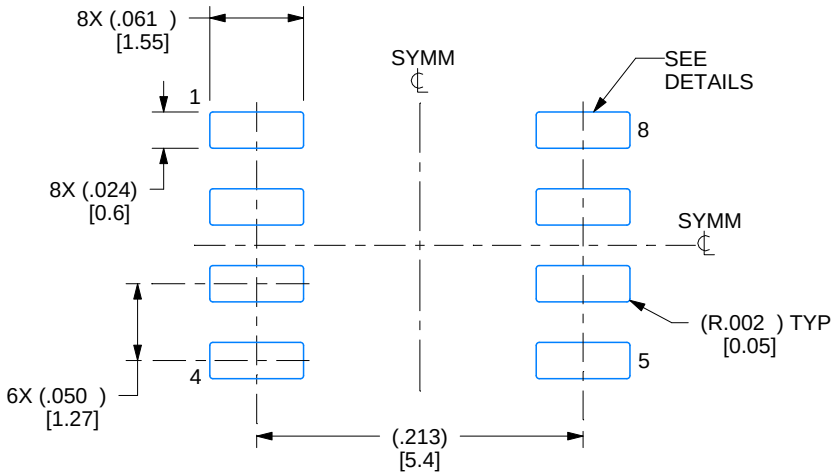
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

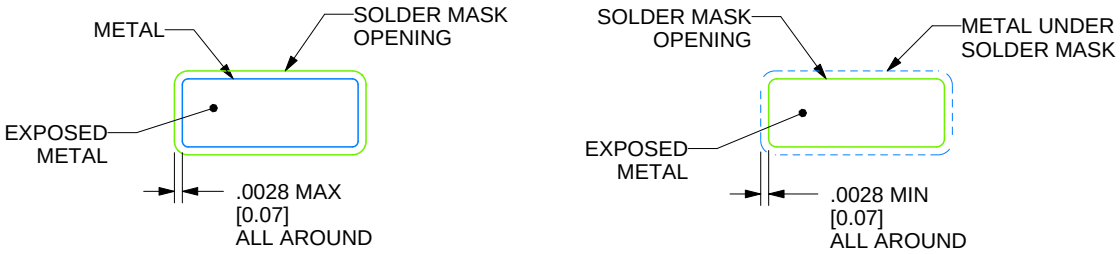


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

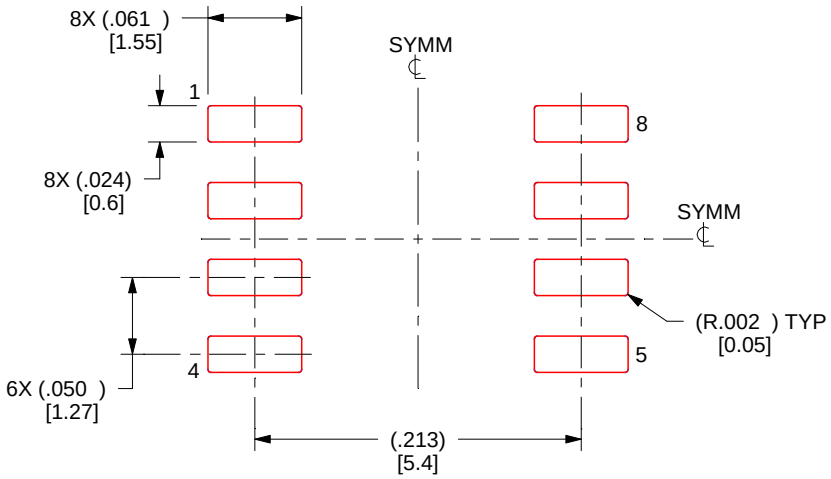
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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