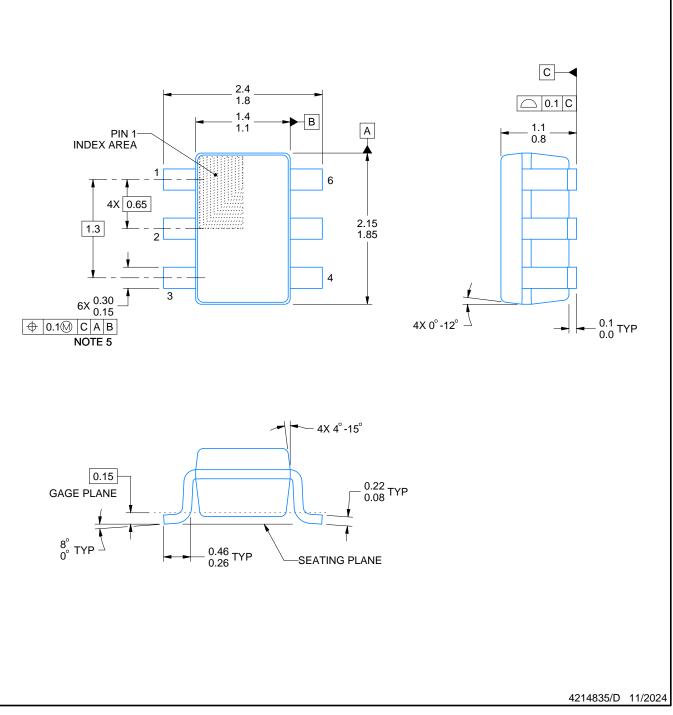
DCK0006A



PACKAGE OUTLINE

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing an integration of a constraint of the minimeters. Any dimensions in parentnesis are for reference only. Dimensioning and to per ASME Y14.5M.
 This drawing is subject to change without notice.
 Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 Falls within JEDEC MO-203 variation AB.



DCK0006A

EXAMPLE BOARD LAYOUT

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

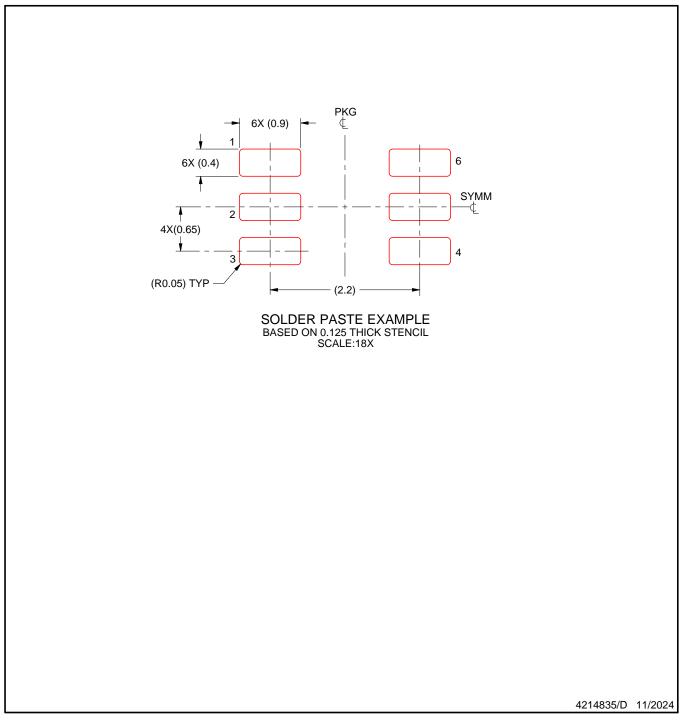


DCK0006A

EXAMPLE STENCIL DESIGN

SOT - 1.1 max height

SMALL OUTLINE TRANSISTOR



NOTES: (continued)

8. Board assembly site may have different recommendations for stencil design.



^{7.} Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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