Radiation Evaluation of Ferroelectric Random Access Memory Embedded in 180nm CMOS Technology

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***Abstract*—Radiation and Temperature Characterization results of a 2T-2C ferroelectric random access memory (FRAM) are presented. This includes Total Ionizing Dose (TID), Single Event Effects (SEE) and Temperature evaluation at 215 ^{o}C.**

I. Introduction

Ferroelectric Random Access Memory (FRAM) is a technology that combines the best of Flash and SRAM. It provides non-volatile storage like Flash, but offers faster writes, high read-write cycle endurance (>10^{15} cycles), and very low power consumption [1]. The FRAM in this paper was fabricated with the Texas Instruments (TI) 180nm CMOS process [2]. Two additional masks are utilized for the Ferroelectric Capacitor (FeCap) and the via interconnect layer [2,3]. As compared with TI's 130nm FRAM, the new 180nm process has a thicker ferroelectric layer to boost signal margin – the target application for this new FRAM is high reliability embedded non-volatile memory (NVM).

Three different FRAMs were used for this study (see Table I). The first device, CITO, was a proof-of-concept test chip designed for commercial use, optimized for low power – it was used for the thermal bake retention capability studies. The second device, FEDC, was designed for industrial applications and utilizes the 2T-2C structure for improved voltage margin. Organized as a 64-bit wide, 16k-word 1Mbit FRAM, it also has single-error correction double-error detection (SECDED) error correction circuit (ECC). The FEDC underwent thermal, TID, and SEE testing. The FEHT was based on the FEDC but was radiation hardened by design and had additional modifications for high temperature operation. This macro was tested most recently for SEE performance. A diagram of the 2T-2C configuration is shown in fig. 1. Note that while this configuration effectively halves the memory density as compared with 1T-1C configurations, the 2T-2C design provides double the sensing margin enabling significantly higher reliability margin.[1]

Table I. Three FRAM macros used in this study.

Macro Name	Tech (nm)	Array Arch.	Density (Mbit)	Notes
CITO	180	1T-1C, 2T-2C	0.5	Low power/slow
FEDC	180	2T-2C	1.0	Enhanced industrial
FEHT	**180**	**2T-2C**	**1.0**	**High temp., RHBD**

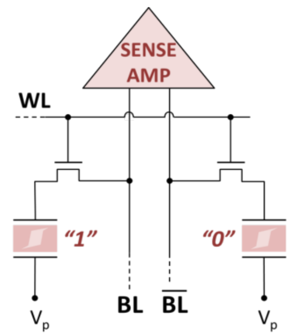

Fig. 1. Block level representation of the 2T-2C FRAM. This configuration doubles the margin of typical 1T-1C designs since the data and its complement are compared during read operations.

II. Total Ionizing Dose Results

TI tested the 180nm FRAM FEDC macro up to 300krad(Si) utilizing the Gammacell 220 Excel (GC-220E) Co-60 gamma ray source at TI's Santa Clara facility according to MIL-STD-883J, Test Method 1019.9 Condition A. Since the exposure facility did not have automated test equipment (ATE) devices were pre-screened and shipped to the exposure facility. The ATE pre-screen program tested data retention, functionality, margin voltages in both 1T-1C and 2T-2C modes, IDDQ values and I/O leakage currents. The material also went through normal production flows such as wafer probe to screen outliers, and package mold/cure steps. Since the circuit exclusively uses MOSFETs the total dose study was done under the high dose rate conditions of 87 Rad (Si)/s. A step-stress test method was used to characterize the TID hardness level. That is, after a predetermined TID level was reached, an electrical test was performed on a given sample of parts to verify that the units pass predefined electrical specification limits. Exposure levels are given in table II and control units were used as well.

During irradiation, the devices were biased with the supply voltage at nominal conditions (1.8V), circuit ground tied to ground (0V), and all other pins left floating. The supply current was monitored during exposure to log any changes that occurred. There was only a slight increase in device supply current (~ 10nA worst-case) during the TID exposure. Devices

Table II. TID exposure levels, # of units, and result.

Dose (kRad[Si])	75	100	150	200	250	300
# Units	3	3	3	3	3	3
Result	**Pass**	**Pass**	**Pass**	**Pass**	**Pass**	**Pass**

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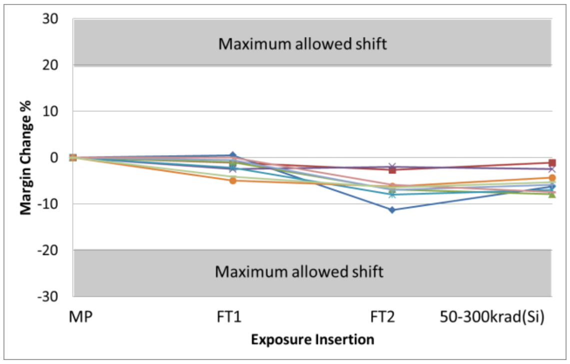

Fig. 2. 1T-1C Margin change pecent over different test insertions and TID exposures. Each line is an individual device at all steps through the screening process. It should be noted that the maximum allowed shift is not a functional failure. There is still much more margin in the design.

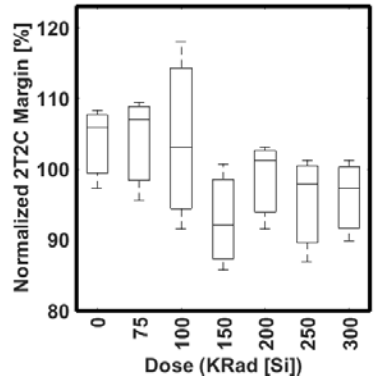

Fig. 3. 2T-2C Normalized margin change over different test insertions and TID exposures. The average normalized margin varies less than 10% over all TID exposure levels with worst-case observed margin of ~ 85%. The FRAM can read data down to a normalized margin of ~ 20%.

were then placed on dry ice according to MIL-STD-883J, Test Method 1019 Section 3.10 and shipped back to the ATE testing facility. Devices were brought up to room temperature and tested using the same pre-exposure test program. Tests included bit cell margin tests, leakage current tests, supply current tests and functional data retention and active write/read tests. The 2T-2C bit cell margin measurement provides the 'goodness' of the bit cell in its ability to store the value and return the value when read. The bit state for each bit cell is always a result of the difference between the non-commutative difference between TRUE and COMPLEMENT. The sense amp inside the cell will compare the contents of the two FeCaps storing the data value and its compliment respectively. The greater the charge difference between the two data states, the more margin the device has and the more robust it is. The margin test individually tests each FeCap in the 2T-2C mode. The 1T-1C mode can also be tested by looking at the voltage at the sense amplifier generated by only one of the FeCaps. An external voltage reference is applied to either side of the 2T-pair to determine the value stored on each FeCap [4]. V_{REF} is swept until a minimum voltage needed to correctly write and read a known pattern for the entire array is found. In this way the exact margin voltage needed at the sense amplifier is measured directly for every FRAM bit.

The voltage margin was tested for both the 2T-2C and 1T-1C modes. This test was performed at both maximum and minimum input supply voltages. The margin voltage was tested pre-irradiation and post-irradiation to determine the maximum shift seen. The worst case margin shift in the 2T-2C mode was found to be 14% at the 100k Rad(Si) read point. The average shift for all devices over all exposure levels was found to be less than 7%. The worst case shift seen in the 1T-1C configuration was found to be less than 10% at 50kRad(Si) The overall average shift was found to be just less than 10%. This value is only a small percentage of the overall margin that is designed into the FRAM architecture demonstrating the robustness of the FRAM over TID testing. The change in margin voltages over the TID exposure levels were plotted in fig. 2 for 1T-1C mode which is the worst-case since the 2T-2C have much more margin than what is considered the maximum allowed shift in fig. 2. Even if a device exhibited a shift of greater than the allowed 20% shift, it would still function properly, given the large signal margin inherent in the design.

The change in percent margin is plotted to show the difference at each exposure level. The 2T-2C normalized margin data is shown in fig. 3 demonstrating that the margin voltage in 2T-2C mode changes less than 10% over the total dose range of 0 – 300 krad(Si). This plot is zoomed-in to show the change in percent. The overall drift is only a small fraction of the overall margin and is not a functional failure. A shmoo test was also performed to determine the margin of the entire bit distribution. A result for a single device exposed to 100kRad (Si) is shown in fig. 4 for 1T-1C. The shift in margin, from multi-probe all the way through pre-irradiation and post irradiation is less than 10% All the margin readings were well outside the limit that Texas Instruments has determined to be a failing margin. This again shows that the FRAM voltage margin is much greater than any shift seen during radiation exposure. This value is plotted in the graphs.

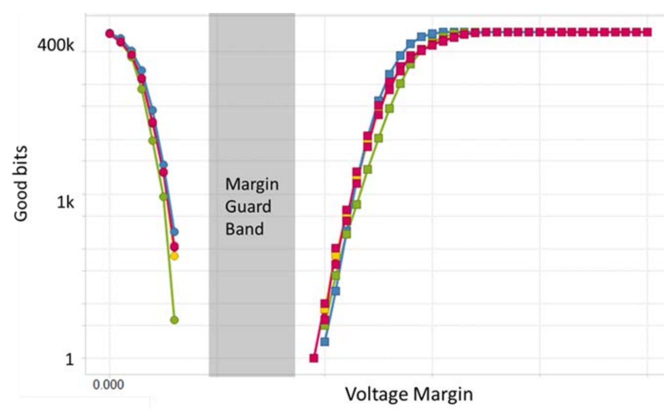

Fig. 4. 1T-1C bit distributions of voltage margin across entire FRAM array for Pre- and Post- TID exposure for all devices exposed from 75krad(Si) to 300krad(Si). The "1"s distribution is on the right and the "0"s is on the left. Reliability mechanisms tend to reduce "1"s margin (shifting the right-hand curve to lower margins)

During the pre-irradiation characterization, a checker board pattern was written into the array to test for FRAM data retention during the TID exposure. None of the devices exposed to any radiation level showed any retention failures. A second set of pattern writes and reads were executed in order to determine the overall functionality of the devices. All data patterns tested (checkerboard, inverse checkerboard, all

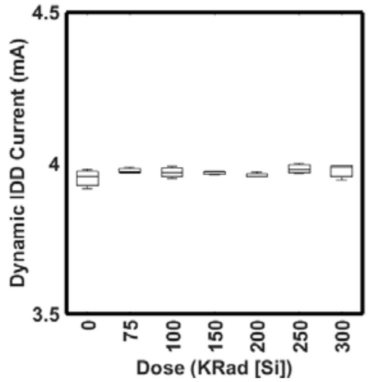

Fig. 5. Dynamic Write/Read current vs. dose. The dynamic W/R current was essentially independent of the TID exposure levels in this FRAM.

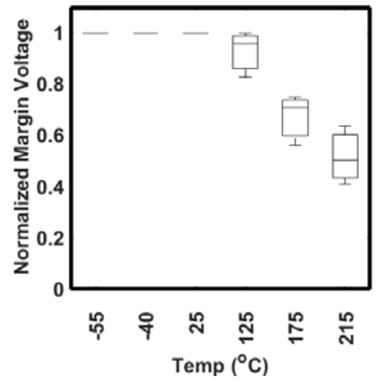

Fig. 6. Normalized Margin % Change vs. Temperature. Decrease in the spontaneous polarization is expected as temperature is increased in ferroelectric materials due to the thermal depolarization effect [2].

zeroes, all ones) were shown to be fully functional post irradiation over all levels of TID. Finally, the overall supply current was measured pre-irradiation, during exposure and post irradiation to determine the shift seen due to irradiation.

The pre-exposure dynamic ICC (current consumed during an active write/read cycle, as well as the total current from all CMOS circuitry) was measured to be ~3.95mA on average across all devices. Post-irradiation currents under the same conditions were measured to be ~4.05mA for the 300kRad(Si) devices as shown in fig. 5. It is not too surprising that this current is within nominal operating parameters even after full TID exposure since it is dominated by current generated by the FeCap switching, which should be independent of TID.

Static ICC current was also monitored during exposure. The average value seen just prior to exposure was ~20nA per device. The ending ICC average value was just over 30nA per device showing a worst-case 50% increase from 0 to 300krad(Si). The increase in current, both active and static, did not affect functionality of the device or data retention. The FEDC FRAM functionality as well as data retention was shown to be unaffected by TID exposure. No failures were seen at any read point throughout the process.

III. High Temp. Function and Reliability Results

FEDC FRAM functionality testing was performed at -55, -40, 25, 125, 175 and 215°C. Three main tests were performed on the FEDC including margin testing, supply current consumption and functional write and read operations. All tests were performed as described in the previous section of this paper. Since FeCap signal margin is dependent on the spontaneous polarization of the ferroelectric layer, which decreases with increasing temperature (due to thermal depolarization), as expected the signal margin test showed margin degradation with increasing temperature. The margin decreased to ~50% of the starting value at 25°C. However, the margin voltage seen at 215°C is still far above the minimum acceptable margin required for reliable read-write operation of the FEDC FRAM. The plot of the margin voltage behavior as a function of temperature is shown in fig. 6 (the values were normalized with respect to the 25^{o}C readings). The functionality of the FEDC FRAM was demonstrated using several different data patterns including, zeroes, ones, checkerboard and inverse checkerboard. The dynamic supply current during write and read operations was also tested across temperature and showed a very similar trend to the TID results. The initial current at lower temperatures started about 2.2mA. As the temperature increased, the current trended higher as expected and peaked just below 3mA at 215°C. The small temperature dependence of the read-write current was expected since the magnitude of the current is largely defined by the magnitude of ferroelectric switching current which does not have a strong temperature dependence (the switching current is a function of the number of ferroelectric domains that are switched and the magnitude of their spontaneous polarization). The device was fully functional at 215°C with no write or read failures. The graph of supply current over temperature can be seen in fig. 7 (the plot is normalized with respect to the 25°C). The static or standby current, of the device was also characterized as a function of temperature and is plotted in fig. 8. Static current is dominated by junction leakage which increases exponentially with temperature, thus static current increase is much more pronounced.

In addition to functionality over temperature extremes and stability against depolarization, FRAM must also be tested for “imprinting”, a reliability concern where a first data pattern, commonly referred to as the “Same-State (SS)” pattern stored, stabilizes during retention for a long period of time (the effect gets worse at higher temperatures). The SS pattern can become “imprinted”, becoming the preferred polarization state

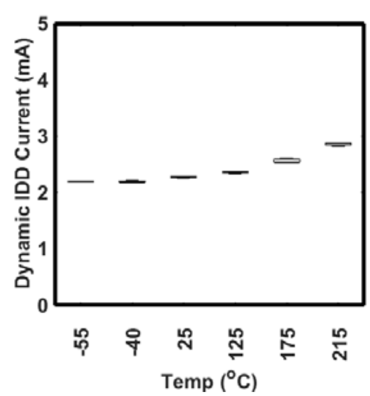

Fig. 7. Normalized dynamic supply current during active write/read vs. temperature. This is expected since dynamic current is dominated by the FeCap switching current which is not a strong function of temperature.

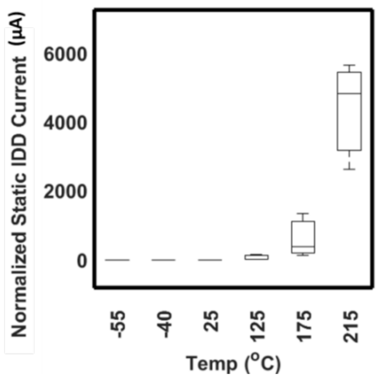

Fig. 8. Normalized static supply current vs. temperature. Dominated by junction leakage, the current rises exponentially with increasing temperature.

of the FeCap. This preference for SS orientation degrades the signal margin for the complement or "Opposite-State (OS)" pattern. To accelerate the imprinting mechanism, the SS data pattern must first be baked at a high temperature for a cumulative period of time equivalent to that expected at the use condition. The FRAM retention test consists of two bake insertions. In the first insertion, the SS pattern is baked at a high temperature to accelerate imprint. The bake is interrupted periodically to monitor the retention results. At each read point, the SS pattern is read, the OS is written and the second short depolarization bake is performed. The OS pattern is read, and other tests may be performed such as a margin test, before the SS pattern is written back to continue the imprint bake.

Several hundred CITO FRAM units were used for these look-ahead retention tests. All retention testing was done with ECC-off to maximize sensitivity. Two accelerated retention bake temperatures were used for this test, 175 and 200°C. As listed in table III, the FRAM passed all retention tests demonstrating that imprinting is not a major reliability limiter for this NVM. In space applications, these results imply that data retention is stable and reliable for > 10 years @ 125°C. Indeed, even for one of the main high temperature applications requirements specifying 175°C for > 1000hrs, the CITO FRAM study confirmed that this technology has margin to spare in that it can operate as a fully functional NVM at 200°C for more than 1000 hours!

Table III. Summary of FRAM data retention testing

# of units	Retention temp. (°C)	Test Type	Retention time (hrs.)	Result
450	175	SS	10,000	No fails
450	175	OS	10,000	No fails
272	200	SS	5,300	No fails
272	200	OS	5,300	No fails

IV. Single Event Latch-up (SEL) Results

The FEDC and FEHT FRAMs were tested for SEL sensitivity using several different ions and angles. These are listed in table IV. The FRAMs were biased to 2V (10% over max recommended) and heated to 125°C to maximize their sensitivity to SEL. Some SEL tests were performed with a rotation angle of 90 degrees to insure that there was no angle dependence in the SEL response [8]. The power supply current was monitored during the exposure. For all different ion species, a flux of 10^5 ions/cm^2/sec was used to a fluence of 10^7 ions/cm^2. Fig. 9 shows a typical power supply current response curve during exposure. This is the typical average current measured over time. No SEL was observed during any of the runs, but a slight increase in current was observed during the ion beam exposure due to the generation of excess carriers.

Table IV. Ions, angles, LETs and SEL Results.

Ion	Angle Degrees	LET$_{eff}$ (MeV·cm^2/mg)	SEL Result
Pr	0 / 45	64 / 90	SEL-Free
Ho	35	91	SEL-Free
Au	0	86	SEL-Free
Kr	0	30	SEL-Free

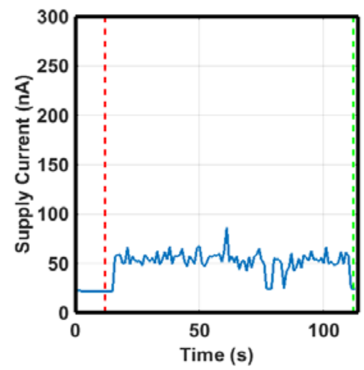

Fig. 9. Typical power supply curve seen during SEL testing. The red/green dotted lines represent where the beam was turned on/off respectively. Supply current increases during irradiation because of ion generated charge. If SEL occurs, a large jump in current is expected as the parasitic SCR is established. No SEL events were observed in any of the FEDC or FEHT FRAM tests.

V. Single Event Upset (SEU) And Single Event Functional Interrupt (SEFI) Results

The FEDC and FEHT FRAMs were tested for Single Event Effects (SEE) under multiple heavy ion conditions from 30 – 87 MeV·cm^2/mg. (details are included in table IV). Active write/read dynamic tests were performed as well as data retention in powered and powered-down configurations. No single bit failures were observed on FEDC or FEHT FRAM during any of the heavy ion tests. This was proven from active write and read operations as well as powered and un-powered retention tests. The active write and read tests consisted of checkerboard, inverse checkerboard, all ones and all zeros patterns. The dynamic tests were performed using write and immediate read tests as well as full array write and then full array read tests. The retention tests involved writing the full array with a known pattern (checkerboard) and then powering down and exposing the device. After the beam was shut down, the memory was read and the data compared to pre-exposure patterns. A summary of the SEU results obtained from the FEDC and FEHT FRAM devices is shown in table V. The only caveat is that in the FEHT FRAM tests, the latency in the hardware was such that dynamic tests had such a low duty cycle to be very nearly retention tests (long periods

Table V. LET = 87 MeV-cm^2/mg SEU results for FEDC and FEHT FRAM.

Unit	FRAM type	ECC	Mode	Fluence (ions/cm^2)	SEU	σ (cm^2)
1	FEDC	On	Dyn.	1.33 x 10^6	0	< 7.5 x 10^{-7}
1	FEDC	Off	Dyn.	1.85 x 10^6	0	< 7.5 x 10^{-7}
1	FEDC	On	Ret.	1.37 x 10^6	0	< 7.5 x 10^{-7}
2	FEDC	On	Dyn.	1.34 x 10^6	0	< 7.5 x 10^{-7}
2	FEDC	Off	Dyn.	1.28 x 10^6	0	< 7.5 x 10^{-7}
2	FEDC	On	Ret.	1.74 x 10^6	0	< 7.5 x 10^{-7}
3	FEHT	On	Dyn.	2.87 x 10^6	0	< 3.5 x 10^{-7}
4	FEHT	On	Dyn.	2.81 x 10^6	0	< 3.6 x 10^{-7}
5	FEHT	On	Dyn.	2.14 x 10^6	0	< 4.7 x 10^{-7}
3	FEHT	On	Ret.	1.00 x 10^6	0	< 1.0 x 10^{-6}
5	FEHT	On	Ret.	1.00 x 10^6	0	< 1.0 x 10^{-6}
3	FEHT	On	Ret.	1.00 x 10^6	0	< 1.0 x 10^{-6}
4	FEHT	On	Dyn.	1.00 x 10^6	0	< 1.0 x 10^{-6}
3	FEHT	On	Dyn.	1.12 x 10^6	0	< 8.9 x 10^{-7}
4	FEHT	On	Dyn.	2.93 x 10^6	0	< 3.4 x 10^{-7}
5	FEHT	Off	Dyn.	1.17 x 10^6	0	< 8.6 x 10^{-7}
5	FEHT	Off	Dyn.	1.09 x 10^6	0	< 9.2 x 10^{-7}
5	FEHT	Off	Dyn.	1.21 x 10^6	0	< 8.3 x 10^{-7}

of time between successive reads and writes). The data acquisition software is being updated to eliminate the test latency and we will repeat dynamic SEU testing of the FEHT FRAM at minimum cycle time at a later date.

Several problems were identified during initial SEE testing of the FEDC FRAM. The FEDC FRAM had a known weakness in its redundancy-SRAM or RSRAM. The RSRAM contains memory mapping information which reroutes incoming addresses to repaired sections of memory (if a repair is needed). A single-bit SEU corruption in the RSRAM will lead to block failures since the incoming addresses are rerouted to an erroneous block. In SEE tests of the FEDC FRAM, SEU in the RSRAM caused a large number of SEFIs. The failures that were observed were not single-bit failures, but large block failures of multiples of 128 addresses. The RSRAM addressing scheme works on 128 address sections. It was observed that these failures would occur on 128 address boundaries and would clear on the final boundary of these

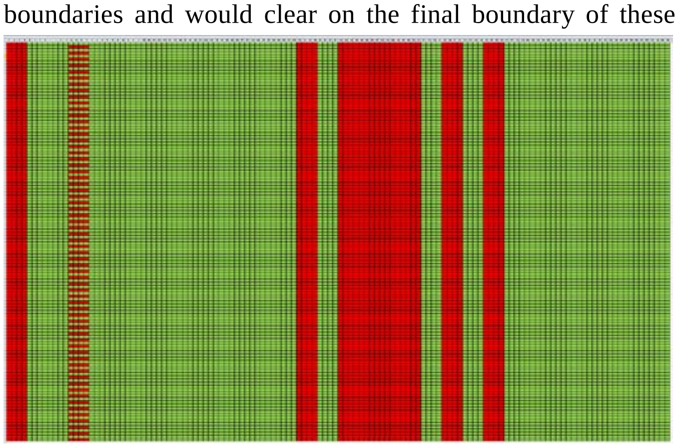

Fig. 10 Bit map showing block level failures seen due to redundant SRAM upsets during SEU testing of the FEDC FRAM. The bitmap shows the boundary fails (red stripes) on 128 bit intervals - implying that SEU in the RSRAM are the root cause. No SEFIs were observed in the FEHT FRAM.

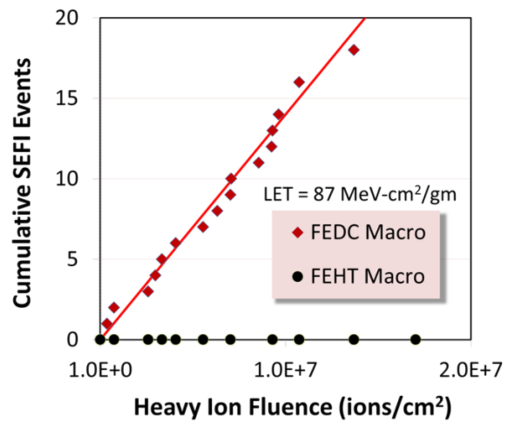

Fig. 11. Plot of observed RSRAM-induced SEFI events (block failures) as a function of heavy ion fluence (LET=87 MeV-cm^2/mg). Note that while FEDC FRAM exhibited many SEFI events, NO SEFI events were observed in the FEHT FRAM with hardened RSRAM block.

Table VI. Summary of SEFI events in FEDC and FEHT FRAM.

Unit	FRAM type	ECC	Mod	Fluence (ions/cm^2)	SEFI	σ (cm^2)
1,2	FEDC	On/Off	Dyn.	1.33 x 10^6	44	5.8 x 10^{-6}
3,4,5	FEHT	On/Off	Dyn.	1.85 x 10^6	0	< 5.2 x 10^{-8}

sections or run for several more sections until another boundary was reached. An example of a bit map obtained in testing is shown in fig. 10 clearly showing the failing blocks on consistent RSRAM boundaries. It should be noted that 44 SEFI block failures were observed in the FEDC FRAM but it is likely that the actual SEFI rate may have been double this since the checkerboard pattern used would show no error depending on the physical bitmap and the indexing error caused by the failing RSRAM (in other words, if the checkerboard pattern was overwritten "in phase" with the existing pattern, no error would have occurred with respect to the original pattern – this pattern aliasing would not occur in an actual use case where the pattern would be random and hence every SEFI would cause some bits to be erroneous within a block). In addition, the SEFIs caused failures in 128 x N addresses (where N was often greater than 1) with each address having 64-bits. Therefore the actual bit-error rate from the observed SEFIs in the FEDC FRAM would likely be unacceptable for many space applications. In sharp contrast, the FEHT FRAM used a more robust SRAM cell with ECC and thus was expected to be robust against the RSRAM SEFI mechanism. Indeed, during SEE testing of the FEHT FRAM, no SEFIs of any kind were observed. The results from FEDC and FEHT SEFI studies are plotted in fig. 11 and tabulated in table VI.

Power ramp rates were also identified as a potential issue for data retention. If there were any fast fluctuations in the power supply voltage, failures would occur in active write and read scenarios as well as data retention. By limiting the slew rates of the power supplies, stable results were obtained with two different pieces of equipment, the National Instruments PXI and the ATE used. This sensitivity demonstrates that stable power regulation is needed to enable reliable operation of the FRAM. Finally, the FEDC FRAM device had several test modes that were designed for debug and testability. These tests modes were entered by writing values to test mode register bits. If any of these registers were flipped during testing, the test mode could be triggered anomalously, causing the data that was being written or read to change. The device would enter an invalid state and cause false fails. In the FEHT FRAM design the test mode is pin protected so test register hits will not cause the FRAM to enter a test mode state.

V. Summary

The high temperature and radiation performance of the 180nm FEHT FRAM device is very impressive. The FEHT is based on a commercially designed core (the FEDC FRAM) that was not intended for high radiation environments, but modified so that it would function in extreme environments. The original failure signature for the test mode issue has already been solved and unlike the FEDC FRAM whose SEE was dominated by a large number of SEFIs in the redundancy SRAM, no SEFIs were observed in the FEHT FRAM when exposed to heavy ions. In addition to reliability characteristics reported elsewhere [2], this FRAM technology provides virtually unlimited R/W cycle endurance ($>10^{15}$), robust retention (175°C > 1000hrs.) and, specifically the FEHT FRAM, optimized for harsh environments has been confirmed to provide unparalleled NVM performance for high temperature and space environments:

- Full R/W functionality confirmed at 215°C
- Full R/W functionality to at least 300 krad(Si)
- Reliable data retention for > 10 years @ 125°C
- SEU-free operation in retention @ LET =87
- and SEL-free and SEFI-Free @ LET = 87

More characterization work on the FEHT FRAM is planned to get better dynamic test data (no SEU were observed in any of the dynamic tests but these were not executed at the highest duty cycle). FEDC SEU was tested dynamically near its maximum frequency and no SEU were observed, so we expect the FEHT FRAM to be better (since it was designed with hardened control logic) and to fully characterize the limits of the FRAMs high temperature performance and reliability.

VI. Acknowledgment

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