TI Designs

EMI-Compliant Industrial Ethernet PHY Brick

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Design Resources

TIDA-00190	Tool Folder Containing Design Files
EK-TM4C1294XL	MCU LaunchPad
TLK105L	Product Folder
TPD4E1U06	Product Folder
TPS75433	Product Folder

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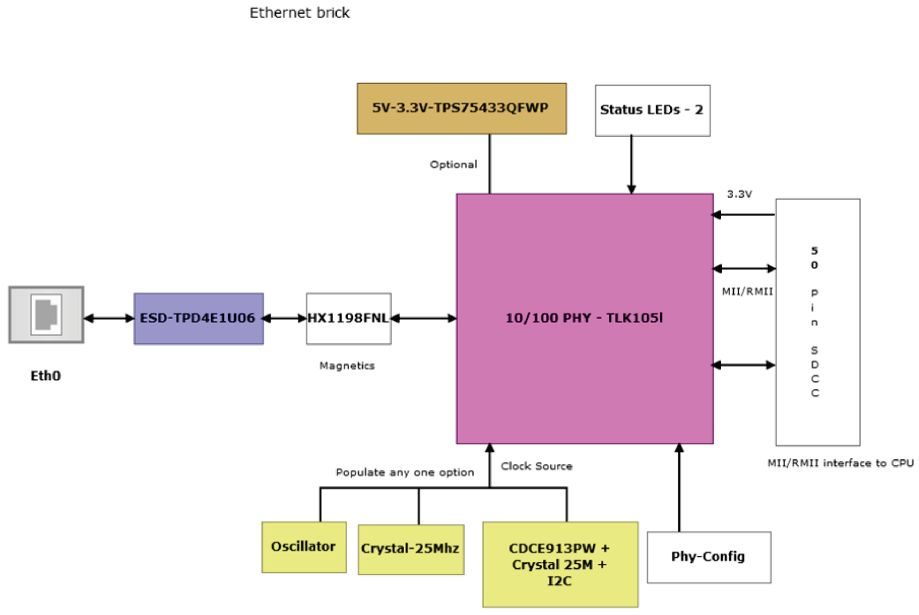
Design Features

- Low Power Consumption < 275 mW
- Meets EN55011 Class A Radiated Emission Requirements
- TLK105L Ethernet PHY Configured for MII Interface
- Programmable LED Support Link, Activity
- External Isolation Transformer with Common Mode Choke on PHY Side for Improved EMI and EMC Performance
- HBM ESD Protection on RD± and TD± of 16 kV

Featured Applications

- Industrial Applications – Circuit Breakers, Protection Relays, Smart Meters (AMI), Panel Mount Multi-Function Power and Energy Meters
- Substation Automation Products like RTU, Protection Relay, IEDs, Gateways, and Serial Converters
- Drives and Motion Control
- IndustriaL Remote Monitoring – Remote I/O and Data Loggers



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1 System Description

A simple and effective design makes Ethernet the most popular networking solution at the physical and data link levels of the Open Systems Interconnection (OSI) model. With high speed options and a variety of media types to choose from, Ethernet is efficient and flexible. In addition, the low cost of Ethernet hardware makes Ethernet an attractive option for industrial networking applications. The opportunity to use open protocols such as TCP/IP over Ethernet networks offers a high level of standardization and interoperability. The result has been an ongoing shift to the use of Ethernet for industrial control and automation applications. Ethernet is increasingly replacing proprietary communications.

This Ethernet PHY Brick reference design enables TI customers to quickly design and release to market systems using TI industrial Ethernet PHY transceiver devices compliant with EN55011 Class A EMI requirements. The design provides a 50-terminal interface to a 32-Bit Cortex M4 processor-based controller board. The board design is a small (2 inches x 3 inches) form factor, which makes it easy to fit into a variety of products.

The reference design platform demonstrates the advanced performance of TLK10xL Ethernet PHY transceiver devices. The design supports 10/100 Base-T and is compliant with the IEEE 802.3 standard. The reference design uses a single power supply (5 V with onboard regulator or 3.3 V). All other voltages required for the Ethernet PHY transceiver are internally generated within the device.

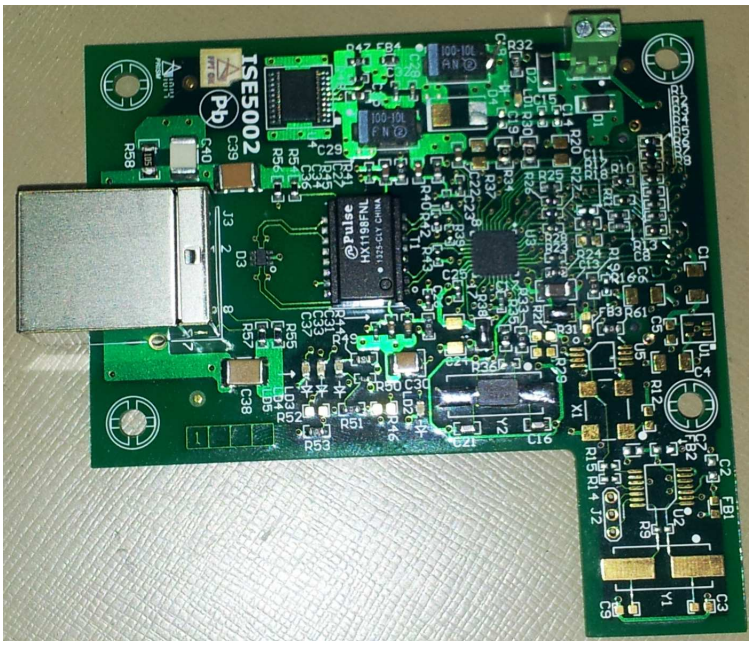

Figure 1. EMI-Compliant Industrial Ethernet PHY Brick

2 Design Features

Ethernet PHY	TLK105L Ethernet PHY features:
	• Industrial temperature rating: –40°C to 85°C
	• Configurable PHY Addresses – resistor strapping options
	• MII or RMII – resistor strapping options
Power Consumption	Single Supply: < 275 mW
Power supply	The device is designed for power-supply flexibility and can operate with a single 3.3-V power supply
	Possible power input options:
	• 5 V from external 2 terminal connector
	• 5-V DC input from MII interface connector and onboard regulator to generate 3.3 V
	• 3.3-V DC input from MII interface with no onboard regulator
MAC - Controller Interface	50-terminal MII interface connector
Clock	25-MHz crystal with internal oscillator
Status LEDs	Two LEDs (link and activity with option to configure as PU or PD) (for further information, see Section 3.1.3, Table 1, and Section 3.8 LED Interface in the TLK105 Data Sheet SLLSEB8B).
ESD	IEC61000-4-2 – Level 3 , Criterion B
Radiated Emission	EN55011 , Class A

3 Block Diagram

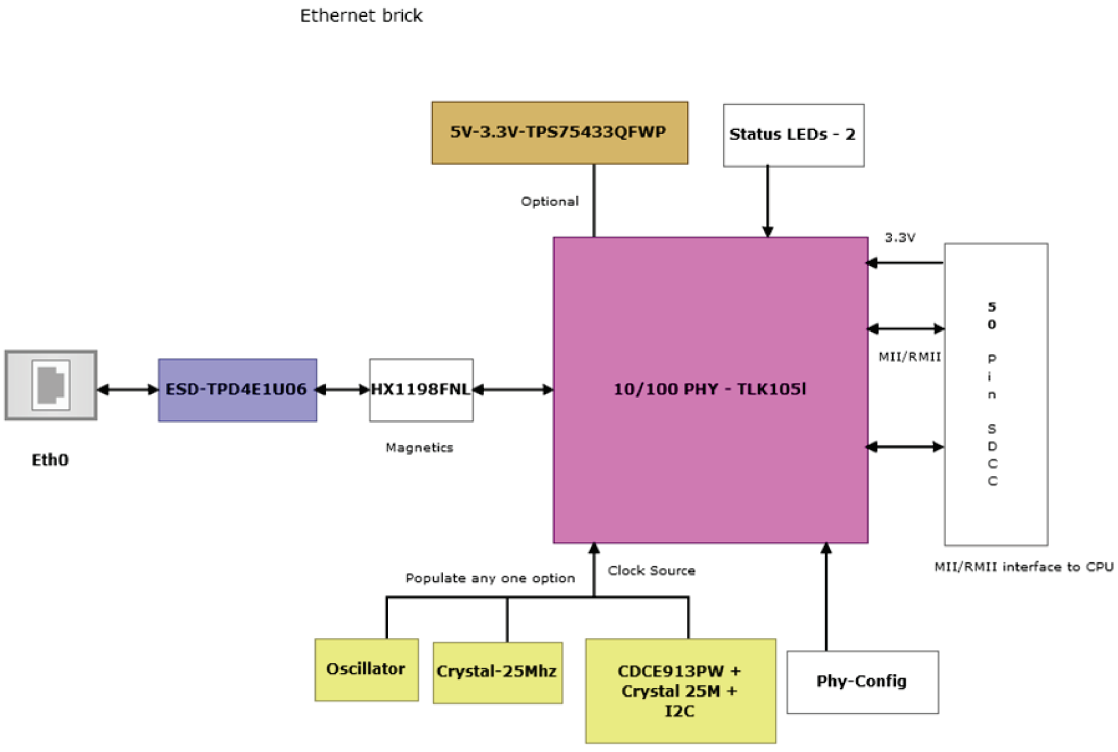

Figure 2. TIDA-00190 Block Diagram

3.1 Single Port 10/100 Mb Ethernet Physical Layer Transceiver

The Ethernet PHY used in the reference design is TLK105L. The major features of the Ethernet PHY are described below.

3.1.1 MAC Data Interface (MII)

TLK105L is a Single Port 10/100 Mb ethernet physical layer transceiver. In this reference design, the Ethernet PHY brick is interfaced to the MAC through an MII interface.

3.1.2 Bootstrap Configuration

The design configures PHY through resistors. The details are provided in Section 4.

3.1.3 LED

The design provides an option for two LEDs:

1. LINK_LED – terminal 17
2. Multi-configurable LED (MLED) by register access

Please refer to Table 1 and Section 3.8 LED Interface in the TLK105 Data Sheet SLLSEB8B for more details.

Table 1. LED Mode Select

MODE	LED_CFG[0] L(BIT 5) OR (PIN 27)	LED_LINK
1	1	ON for Good Link OFF for No Link
2	0	ON for Good Link BLINK for Activity

The LEDs can be configured as active pull-up or active pull-down.

3.1.4 Clock Circuit

For the MII interface, the clock source is 25-MHz crystal with an internal oscillator.

3.1.5 RJ-45 and Isolation Transformer

The design uses magnetics with a choke on the side of the PHY.

3.2 MAC – Controller Interface

The interface to the controller is through a 50-terminal high-speed connector. The male connector is mounted on the controller board and the female connector is mounted on the Ethernet PHY brick board. The high-speed connector has the MII interface signals and the power input (5-V or 3.3-V DC).

3.3 Power Supply

The Ethernet PHY operates on a single power supply. The Ethernet PHY brick board can be powered:

1. By external 5 V
2. 5 V from the Controller board
3. 3.3 V from the controller board

Filtering

The design provides the required filter capacitors.

3.4 ESD Protection

The network or Medium Dependent Interface (MDI) connection via transmit (TD+ and TD–) and receive (RD+ and RD–) is ESD protected.

4 Circuit Design and Component Selection

4.1 MAC Data Interface (MII)

TLK105L is a Single Port 10/100 mb Ethernet Physical Layer Transceiver. TLK105L has the signals in Figure 3 for the MII interface:

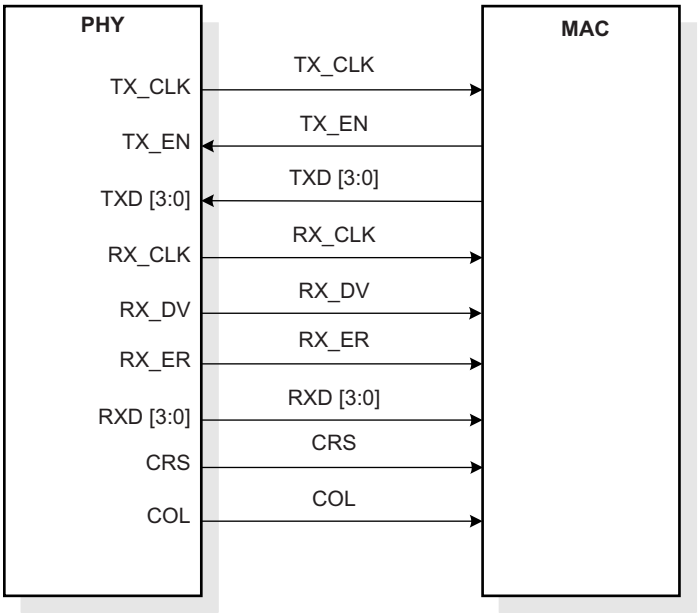

Figure 3. MII Signaling

The Media Independent Interface (MII) is a synchronous four-bit wide nibble-data interface that connects the PHY to the CPU MAC in 100B-TX and 10B-T modes. The MII is fully compliant with IEEE802.3-2002 clause 22. The MII signals are summarized below:

- Data signals TXD [3:0], RXD [3:0]
- Transmit and receive-valid signals TX_EN, RX_DV
- Line-status signals Carrier Sense Signal (CRS)
- COL (LED_LINK)

Additionally, the MII interface includes the CRS, as well as a collision detect signal COL. The CRS signal asserts to indicate the reception of data from the network or as a function of transmit data in half-duplex mode. The COL signal asserts as an indication of a collision which can occur during half-duplex operation, when both transmit and receive operations occur simultaneously.

4.1.1 Bootstrap Configuration

Bootstrap configuration is a convenient way to configure the TLK10xL device into specific modes of operation. Some of the functional terminals are used as configuration inputs. The logic states of these terminals are sampled during reset and are used to configure the TLK10xL device into specific modes of operation. Table 2 describes bootstrap configuration. A 2.2-kΩ resistor is used for pull-down or pull-up to change the default configuration. If the default option is desired, there is no need for external pull-up or pull-down resistors. Because these terminals may have alternate functions after reset is de-asserted, these terminals must not be connected directly to VCC or GND.

Table 2. Bootstrap Configuration

<table>
<tr><th>TERMINAL</th><th>COMPONENTS OF THE BOARD</th><th>DESCRIPTION</th></tr>
<tr><td>PHYAD0 (COL)
PHYAD1 (RXD_0)
PHYAD2 (RXD_1)
PHYAD3 (RXD_2)
PHYAD4 (RXD_3)</td><td>R52,R53
R64,
R65,
R66,
R67</td><td>PHY Address [4:0]: The TLK10xL provides five PHY address terminals, the states of which are latched into an internal register at system hardware reset. The TLK10xL supports PHY Address values 0 (<00000>) through 31 (<11111>). PHYAD [4:1] terminals have weak internal pull-down resistors, and PHYAD [0] has a weak internal pull-up resistor, setting the default PHYAD if no external resistors are connected.</td></tr>
<tr><td>AN_0 (LED_LINK)</td><td>R46,R51</td><td>AN_0: FD-HD config. FD = pull-up.
The default wake-up is auto negotiation enable 100BT.
<table>
<tr><th>AN_0</th><th>Forced Mode</th></tr>
<tr><td>0</td><td>10Base-T, Half-Duplex
100Base-TX, Half-Duplex</td></tr>
<tr><td>1</td><td>10Base-T, Half- or Full-Duplex
100Base-TX, Half- or Full-Duplex</td></tr>
</table></td></tr>
<tr><td>LED_CFG (CRS)</td><td>R69</td><td>LED Configuration: This option selects the operation mode of the LED_LINK terminal (the default mode is Mode 1). All modes are also configurable via register access. See PHY Control Register (PHYCR), Address 0x0019.</td></tr>
<tr><td>AMDIX_EN (RX_ER)</td><td>R70</td><td>Auto-MDIX Enable: This option sets the Auto-MDIX mode. By default, it enables Auto-MDIX. An external pull-down resistor disables Auto-MDIX mode.</td></tr>
<tr><td>MII_MODE (RX_DV</td><td>R63</td><td>MII Mode Select: This option selects the operating mode of the MAC data interface. This terminal has a weak internal pull-down, and it defaults to normal MII operation mode. An external pull-up causes the device to operate in RMII mode.</td></tr>
</table>

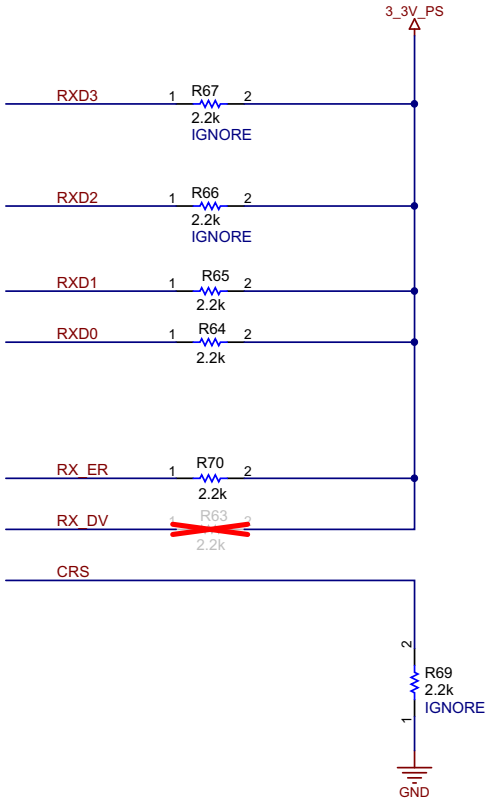

Figure 4. Configuration Terminals

4.1.2 LED

The TLK10xL device supports the use of 2 LEDs. The LEDs can be configured for pull-up or pull-down using the resistors as shown in Figure 5.

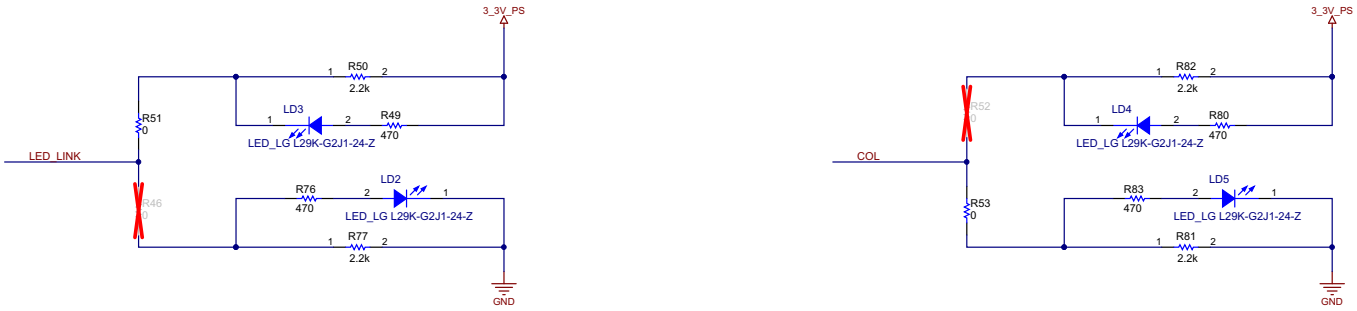

Figure 5. LED Configuration

4.1.3 Clock Circuit (Clock In (XI) Requirements)

The TLK10xL devices support an external CMOS-level oscillator source or an internal oscillator with an external crystal. The use of a 25-MHz, parallel, 20-pF load crystal is recommended if a crystal source is desired. Figure 6 shows a typical connection for a crystal resonator circuit. The load capacitor values will vary with the crystal vendors; check with the vendor for the recommended capacitor loads.

The design uses the oscillator circuit to drive a parallel-resonance AT-cut crystal with a minimum drive level of 100 µW and a maximum level of 500 µW. If a crystal is specified for a lower drive level, a current-limiting resistor must be placed in series between XO and the crystal. As a starting point for evaluating an oscillator circuit, if the requirements for the crystal are not known, set the values for C_{L1} and C_{L2} at 33 pF. Set R_1 at 0 Ω. Specifications for a 25-MHz crystal are listed in Figure 6 and Table 3.

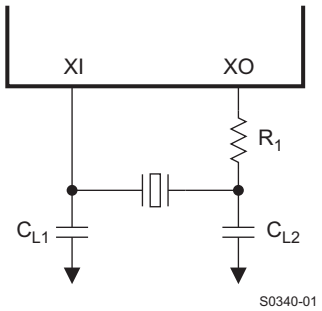

Figure 6. Crystal Oscillator Circuit

Table 3. 25-MHz Oscillator Specification

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Frequency			25		MHz
Frequency Tolerance	Operational Temperature			±50	ppm
Frequency Stability	1 year aging			±50	ppm
Rise / Fall Time	10%–90%			8	nsec
Jitter (Short term)	Cycle-to-cycle		50		psec
Jitter (Long Term)	Accumulative over 10 ms			1	nsec
Symmetry	Duty Cycle	40%		60%	
Load capacitance		15		30	pF

4.1.4 RJ-45 and Isolation Transformer

The reference design uses a shielded RJ-45 connector without internal isolation transformer. An external isolation transformer is interfaced. The details of the RJ-45 connector and the isolation transformer have been provided in Figure 7.

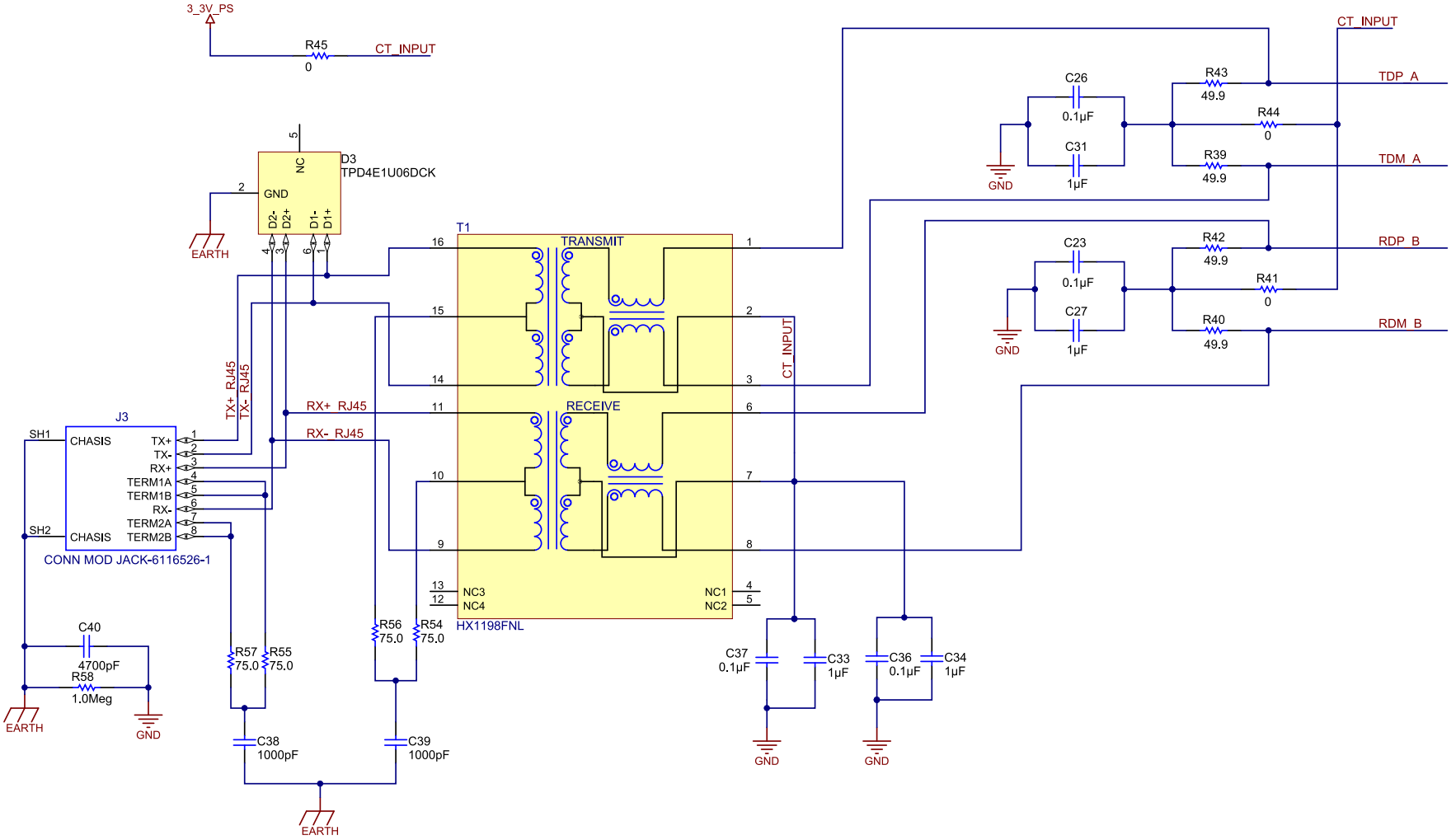

Figure 7. RJ-45 and Isolation Transformer

4.2 Controller Interface

The Ethernet PHY has been interfaced and tested with a *TM4C129XNCZAD 32-bit ARM® Cortex™-M4F MCU Controller Board*, EK-TM4C1294XI. The drivers required to interface the TLK105Ldevice to the MCU are available.

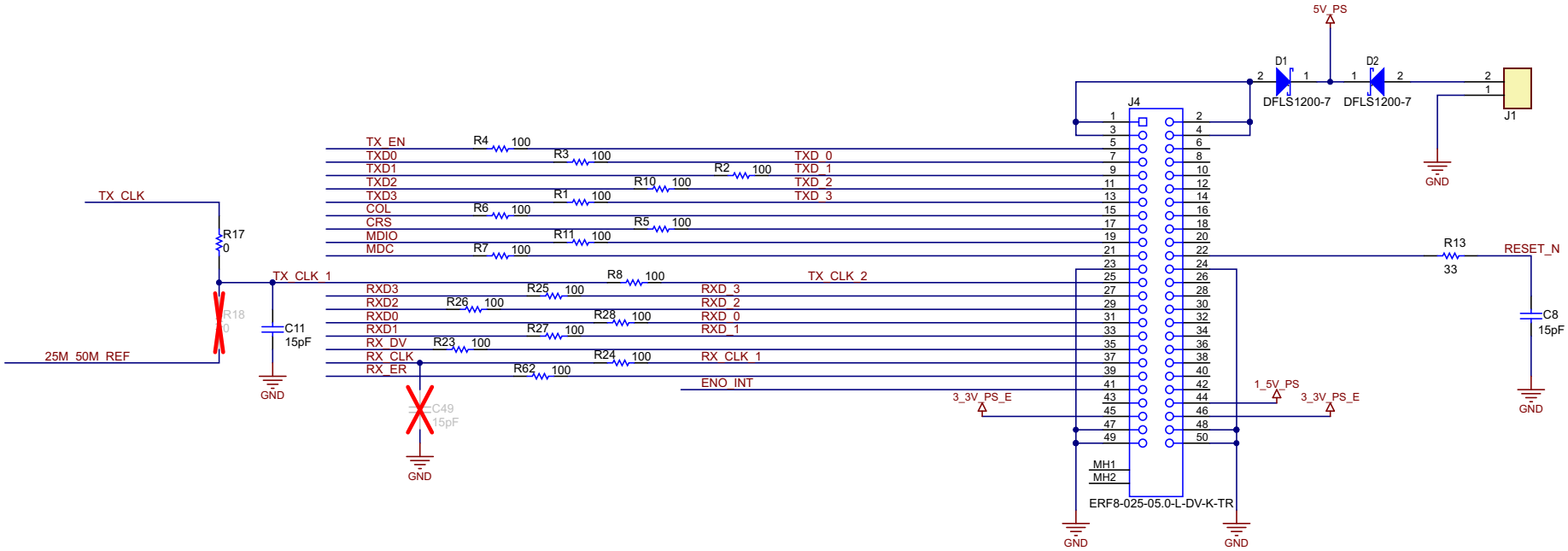

Figure 8. Controller Interface

Figure 9 shows how the Ethernet Brick will mount on the Tiva board.

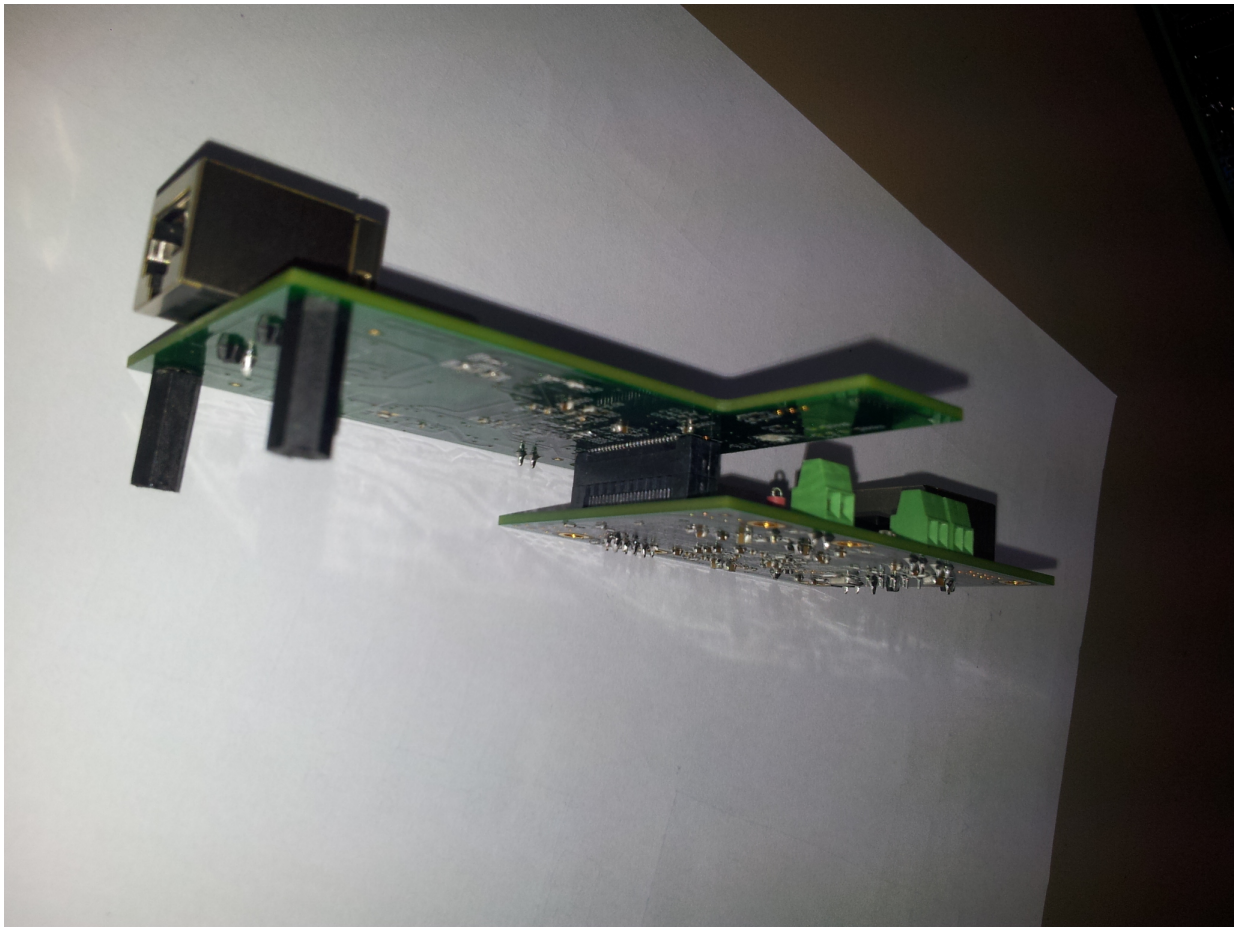

Figure 9. Ethernet Brick Mounted on the Tiva Board

4.3 Power Supply

The Ethernet PHY can be powered by a single 3.3 V as shown in Figure 10.

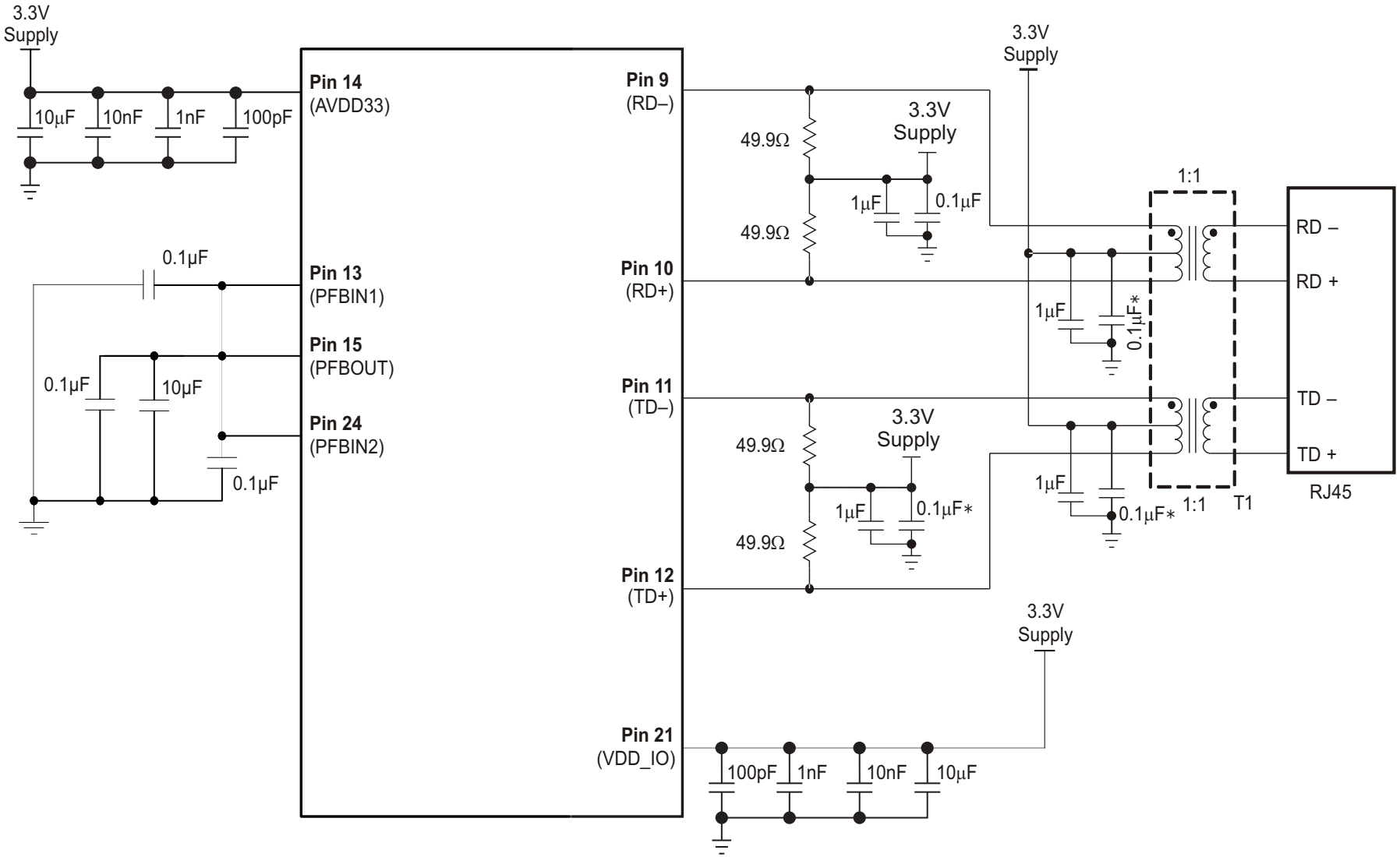

Figure 10. Power Connections for Single Supply Operation

The Ethernet PHY Brick board can be powered by either of the following two methods:

1. By external 5 V or 5 V from the controller board as shown in Figure 11.

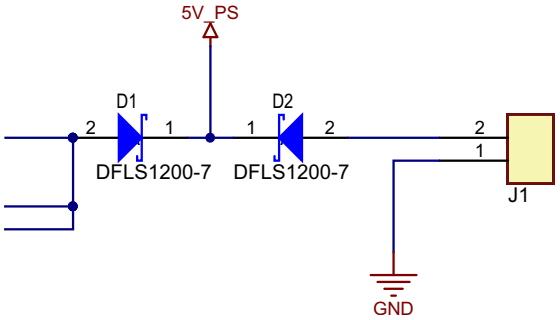

Figure 11. 5-V Power

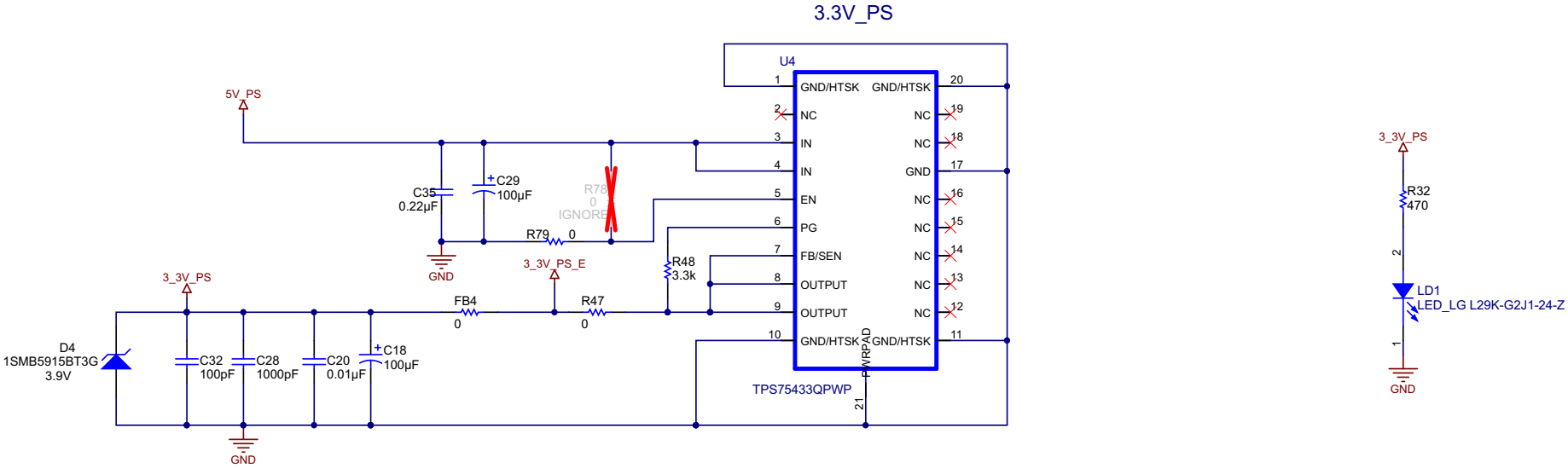

Figure 12. 3.3-V Power

2. By 3.3 V from the controller board as shown in Figure 12.
   Remove R47 when 3.3-V power supply is supplied from a controller 50-terminal interface.

4.3.1 Filtering

Bypass the power rails with the following low-impedance surface mount capacitors: 10 µF, 10 nF, 1 nF, and 100 pF. To reduce EMI, place the capacitors as close as possible to the component's V_{DD} supply terminals, preferably between the supply terminals and the vias connecting to the power plane.

NOTE: TI does not recommend using Ferrite-Beads on TLK supplies.

It is recommended that PCB have at least one solid ground plane and one solid V_{DD} plane to provide a low impedance power source to the component. The planes also provide a low impedance return path for non-differential digital MII and clock signals. Place a 10-µF capacitor near the PHY component for local bulk bypassing between the V_{DD} and the ground planes. The rise time of the V_{DD} should be typically 500 µs.

4.4 ESD Protection

The network or Medium Dependent Interface (MDI) connection is via the transmit (TD+ and TD–) and receive (RD+ and RD–) differential pair terminals. The transmit and receive terminals connect to a termination network, then to 1:1 magnetics (transformer), then to ESD protection diodes and an RJ-45 connector.

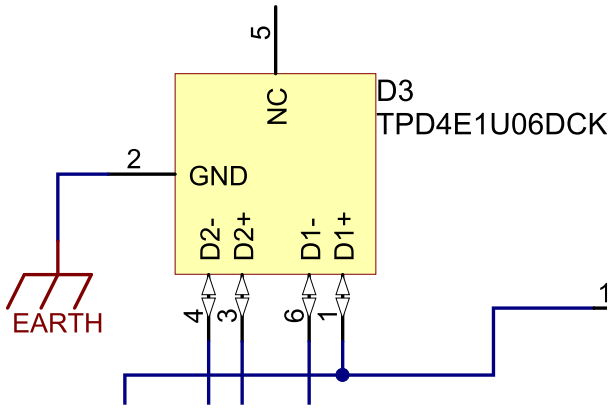

Figure 13. MDI Connection

4.5 PCB Dimensions and PCB Physical Layout

The design provides a small form factor, four-layer PCB with a dedicated ground and power plane.

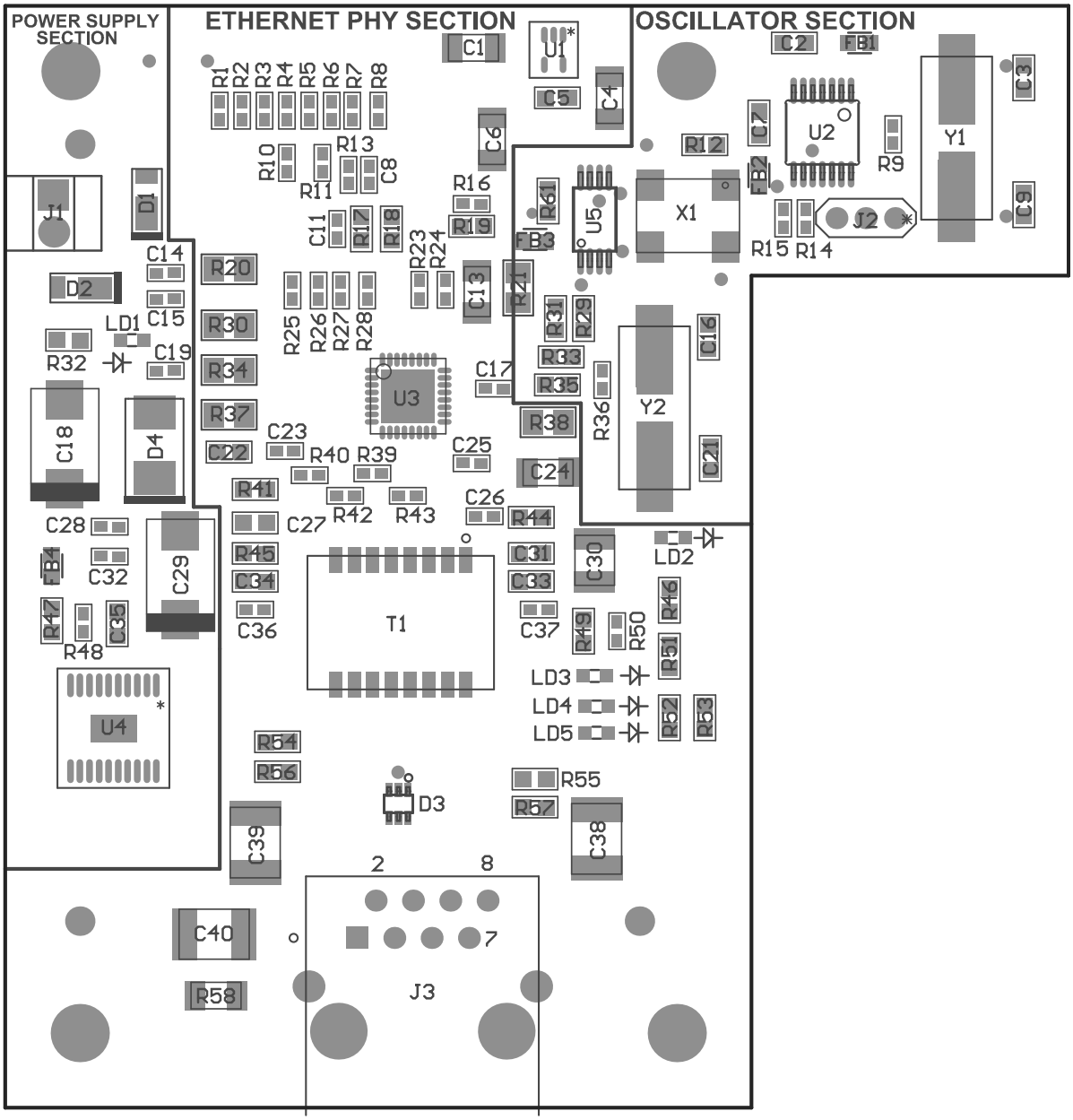

Figure 14. PCB Dimensions and PCB Physical Layout

Total dimensions:

The current board is 3 inches × 2 inches.

The board has a provision for these components:

1. Power supply
2. Ethernet PHY and associated components
3. 50 Mhz oscillator or programmable clock option for RMII interface (for potential future use - not implemented at this time)

The dimension of different blocks is indicated in Figure 14 and the size can be reduced based on the application.

5 Software Description

Table 4. Software Configuration Description

FUNCTIONALITY	CONFIGURATION DESCRIPTION
Hardware Reset	A hardware reset is accomplished by applying a low pulse (TTL level), with a duration of at least 1 µs, to /RESET. This pulse resets the device such that all registers are reinitialized to default values, and the hardware configuration values are re-latched into the device (similar to the power-up/reset operation). The time from the point when the reset terminal is de-asserted to the point when the reset has concluded internally is approximately 200 µs.
External MII PHY Initialization	Set the external PHY address (as per the boot strap configuration).
	All the read and write requests to the PHY, shall use the configured external PHY address. Reset the PHY. 1. MII reset - Set the BMCR (0x00) register bit 15 to one. 2. Software/ Digital reset – Set PHYRCR (0x1F) data register bit 15 and bit14 to one. Issue a delay of 500 microseconds. Set the BMCR (0x00) register to auto negotiation enable and auto negotiation restart by setting bit 12 and bit 8 to one. Poll the BMSR (0x01) register bit 5 to check if auto negotiation is complete.
MII_MODE	The MII_MODE is selected by the pin26 (RX_DV). This terminal has internal weak pull down defaults to MII mode. (External pull-up makes the PHY to operate in RMII mode).
PHY ID	The PHY ID is decided by the pull-up resistors (see Section 3.1 Bootstrap Configuration in SLLSEB8B). Care has to be taken that appropriate PHY ID is used for appropriate hardware bootstrap configuration (as per pull-up registers). The values of terminals 29, 30, 31, 32, 1 (PHYAD0/COL, PHYAD1/ RXD0, PHYAD2/ RXD1, PHYAD3/ RXD2, PHYAD4/ RXD3) are latched into an internal register at hardware reset.
LED configuration	Terminal 17 and terminal 29 can be used for LED configuration either as pull-up or pull-down. Terminal 17 indicates link status (fully lit) by default and activity is indicated by blinking the same LED. If there is a need to use terminal 29 for indicating LED status, MLEDCR must be configured. MLEDCR configuration provides an option to route the activity signal to terminal 29 instead of 17. To route the activity signal to terminal 29 instead of 17, the COL signal must be disabled (see Section 3.8 LED Interface in SLLSEB8B).
Testing TLK105L	Assuming the hardware is connected to Ethernet cable and the other end of Ethernet cable is connected to the PC, the TX clock and RX clock can be probed and measured (after PHY is powered up and not in reset state). Initiate a ping request with an IP address that is within the PC's subnet. Example: 192.16.0.100 is PC IP address, 255.255.255.0 is the subnet mask, initiate a ping command. Example: ***ping 192.16.0.1 –t*** TX[0:3] and RX[0:3] will show some data patterns. Ping will create traffic at every plug in of Ethernet cable. After sometime, when the destination host unreachable message is seen, there may not be a further Ethernet message on the wire.

6 Test Results

6.1 Functional Testing

Table 5. Functional Testing

FUNCTION	RESULTS
Clock	25 MHz
VCC (3 – 3.6V)	3.31 V-DC
Internal 1.55V	1.55 DC
MII interface	OK
Link and Activity LED	OK

6.2 Communication Interface Testing (Computer to Device)

6.2.1 Ping Test

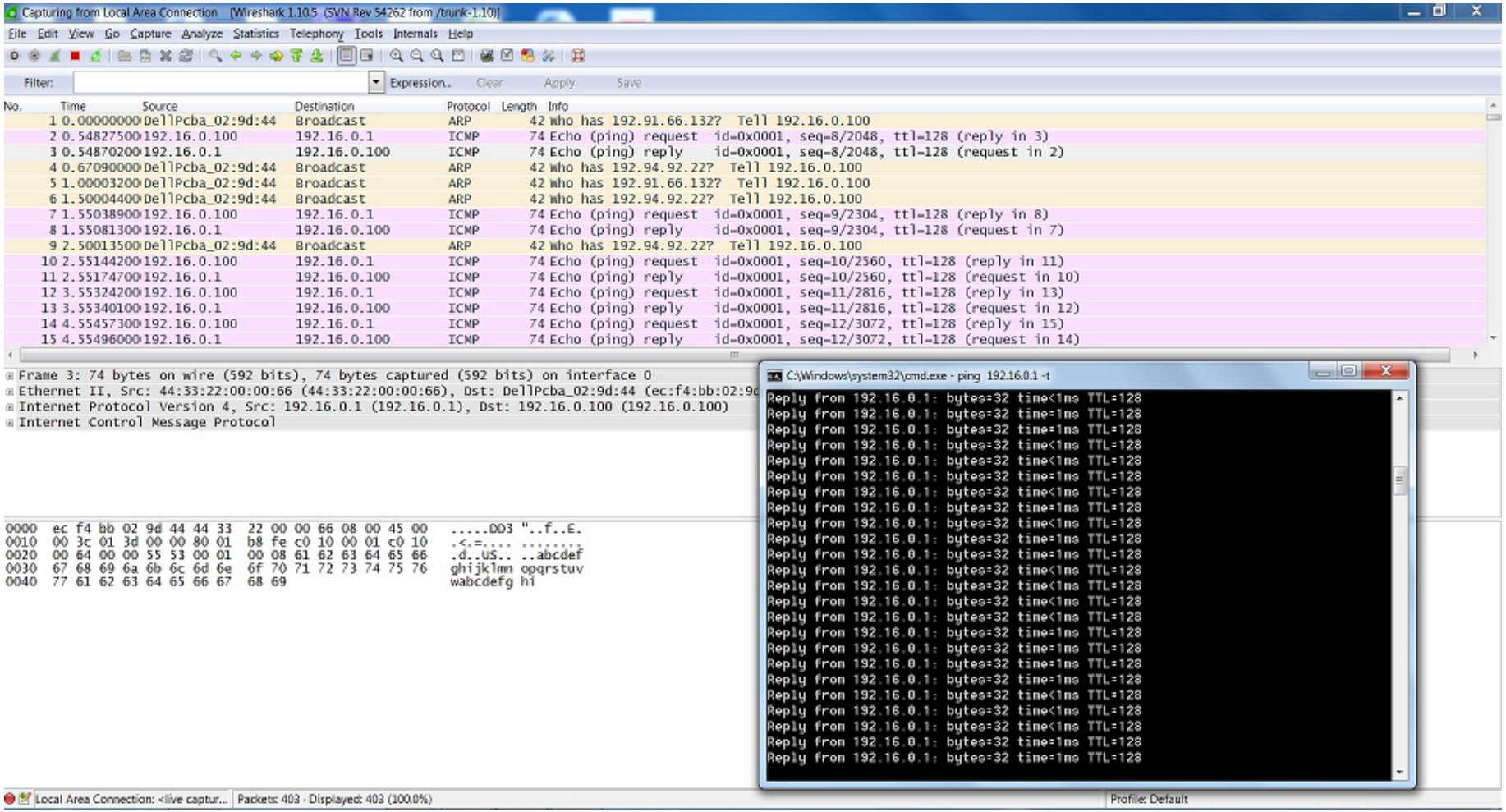

Figure 15. Ping Test

6.2.2 Webserver Interface

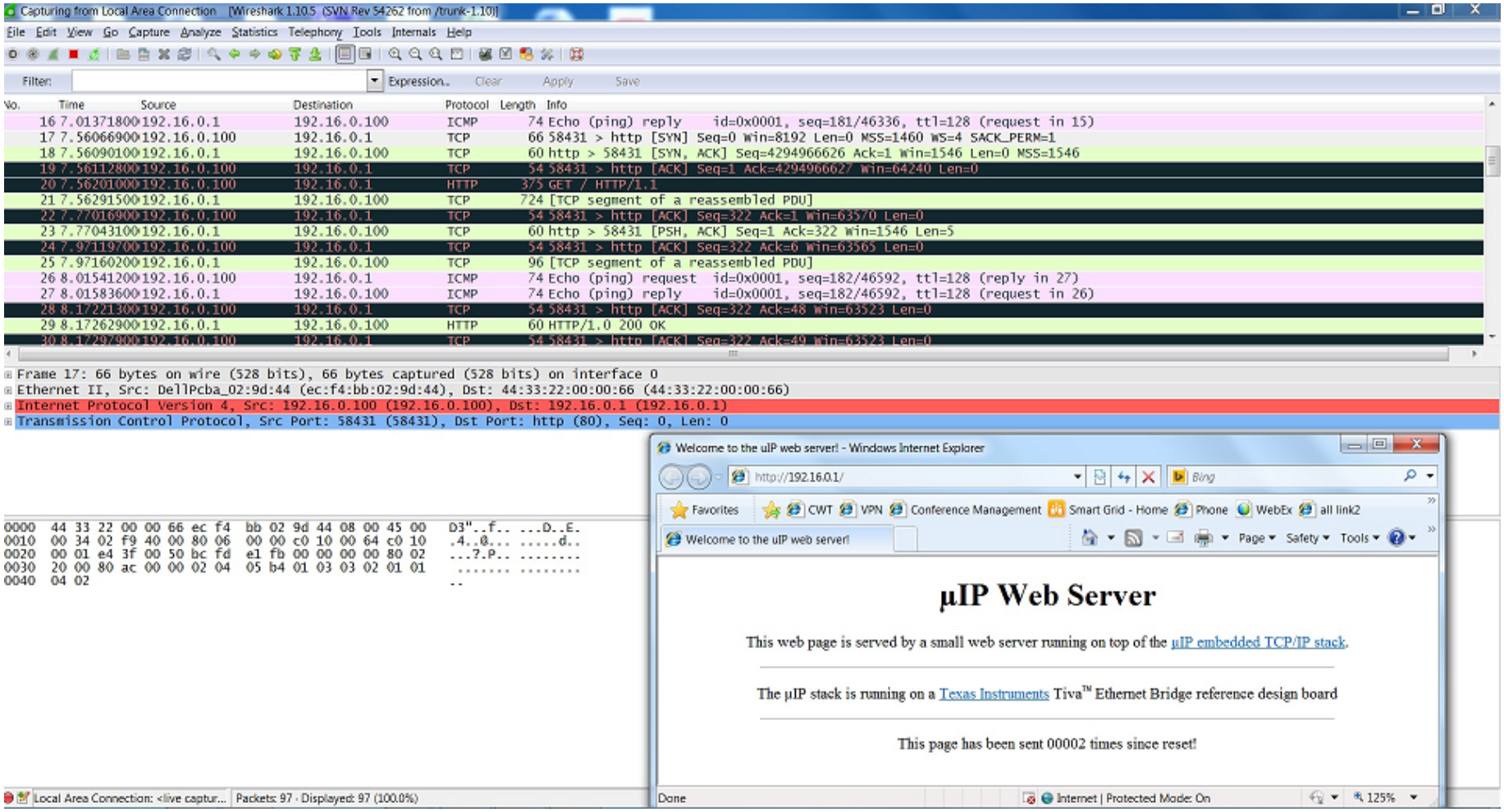

Figure 16. Webserver Interface

6.3 EMI-Radiated Emission

The test distance for radiated emission from EUT to Antenna is 10 M. The test was performed in a semi-aneochic chamber, which conforms to the Volumetric Normalized Site Attenuation (VNSA) for ten-meter measurements.

Table 6. Specifications for Radiated Emissions

FREQUENCY RANGE	CLASS A LIMITS QUASI-PEAK	CLASS B LIMITS QUASI-PEAK
30 MHz to 230 MHz and 230 MHz to 1 GHz	40 and 47 dB µV/m	30 and 37 dB µV/m

Table 7. Observation for Radiated Emissions

REQUIREMENTS	FREQUENCY	RESULT
EN 55011:2009+A1:2010, Class “A”	30 MHz to 1 GHz	PASS

6.4 Test Result Graphs

NOTE:

1. Measurements are made in Peak Detection Mode for all the scans shown in Figure 17 through Figure 20.
2. Limits line drawn for all the scans shown in Figure 17 through Figure 20 are per Class B emission limits.

Test 1: The Ethernet PHY has been interfaced and tested with TM4C129XNCZAD 32-bit ARM® Cortex™-M4F MCU.

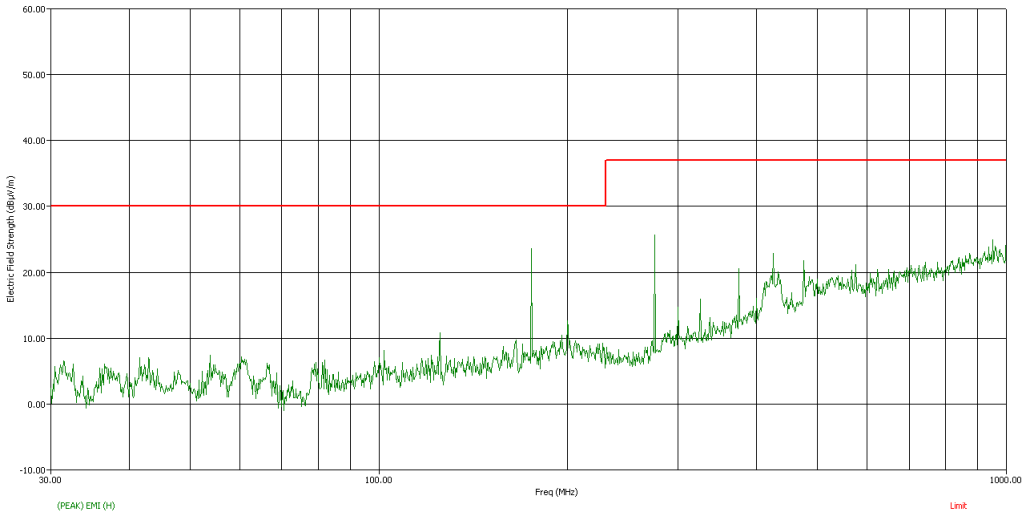

Figure 17. Test 1 Horizontal Polarization

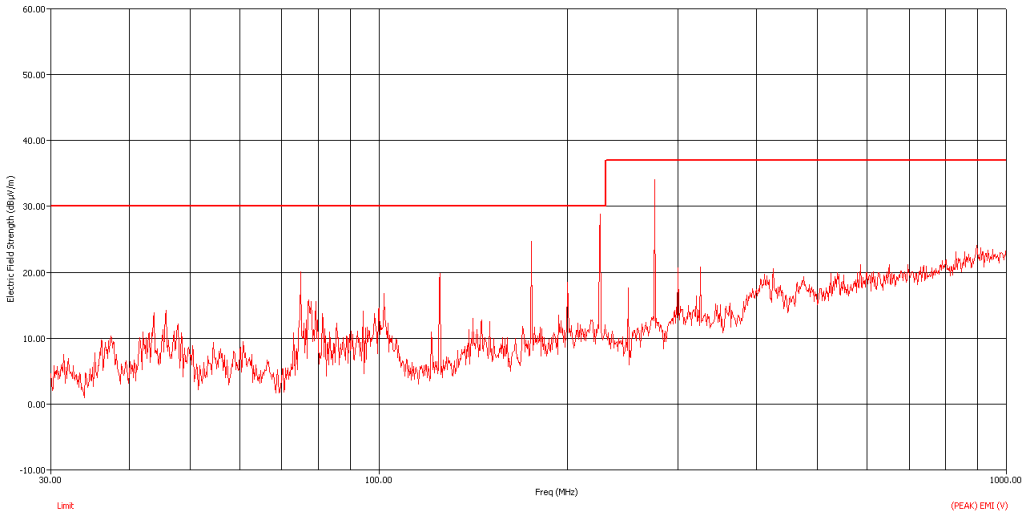

Figure 18. Test 1 Vertical Polarization

Test 2: Tested with Ethernet PHY (with no MCU connected).

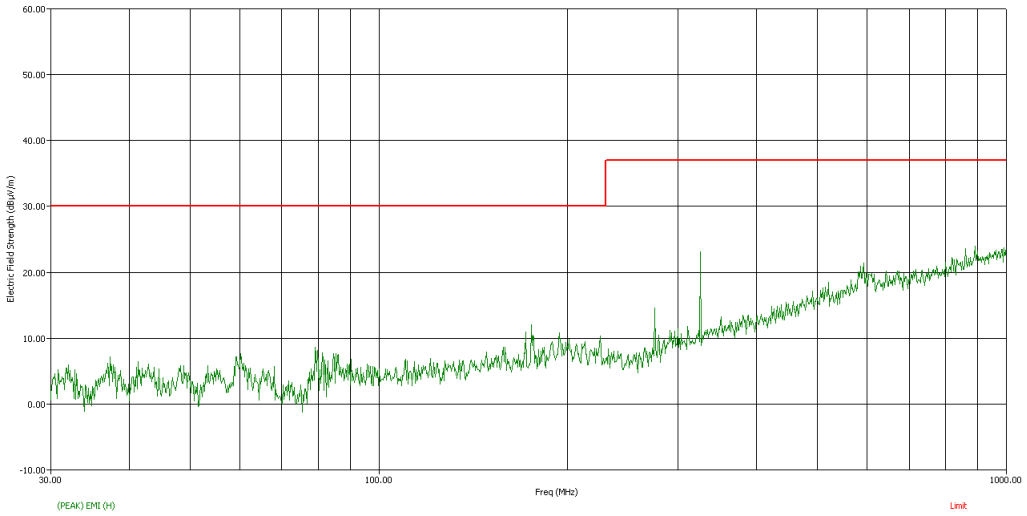

Figure 19. Test 2 Horizontal Polarization

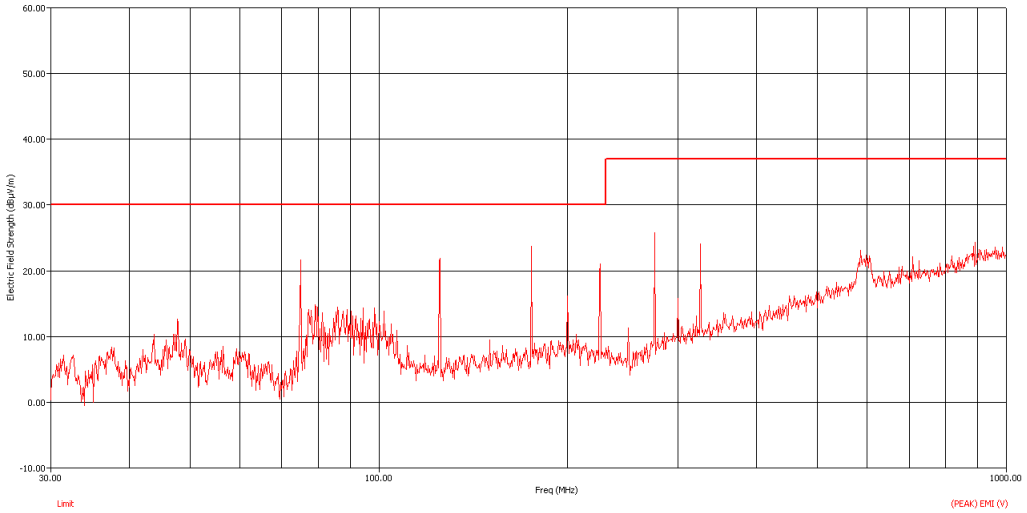

Figure 20. Test 2 Vertical Polarization

6.5 ESD

Table 8. ESD Test Results

DISCHARGE TYPE	LEVELS	CRITERIA	RESULTS
Contact	7 KV	Criteria B	Pass
Air discharge	10 KV	Criteria B	Pass

6.6 ESD, EMI, EMC Recommendations and Design Guidelines

The following recommendations are provided to improve EMI performance:

1. Series resistors on all MII signals.
2. Guard ring for crystal.
3. Use a metal shielded RJ-45 connector, and connect the shield to the chassis ground.
4. Use magnetics with integrated common-mode choking devices with the choke on the side of the PHY (for example, PULSE HX1198FNL).
5. Do not overlap the circuit and chassis ground planes (keep the circuit and chassis ground planes isolated). Connect chassis ground and system ground together using one 4700-pF NPO 2000-V 10% across the void between the ground planes on the 1, 2 pair side of the RJ-45.

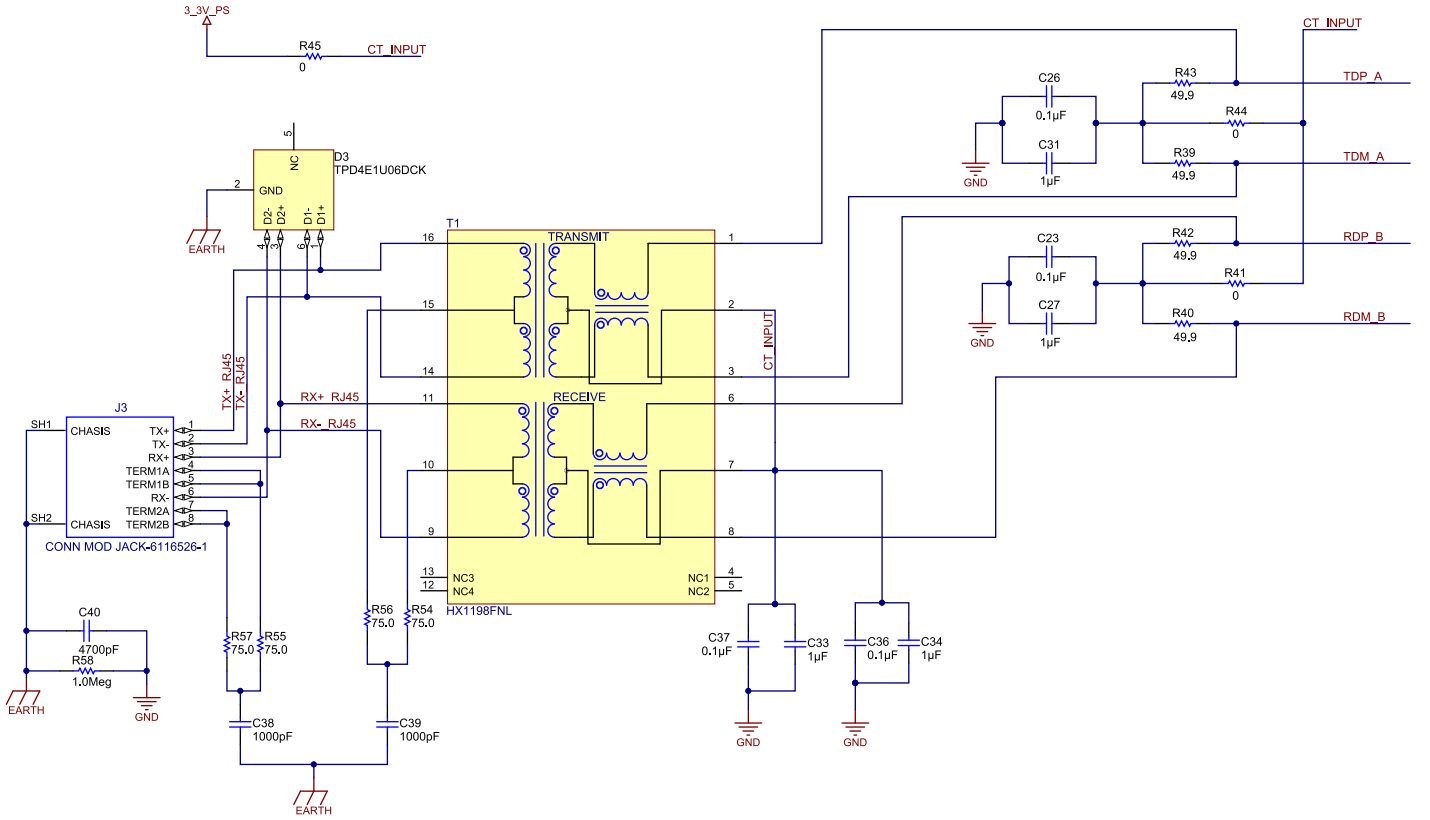

Figure 21. ESD, EMI, EMC Recommendations and Design Guidelines

7 Design Files

7.1 Schematics

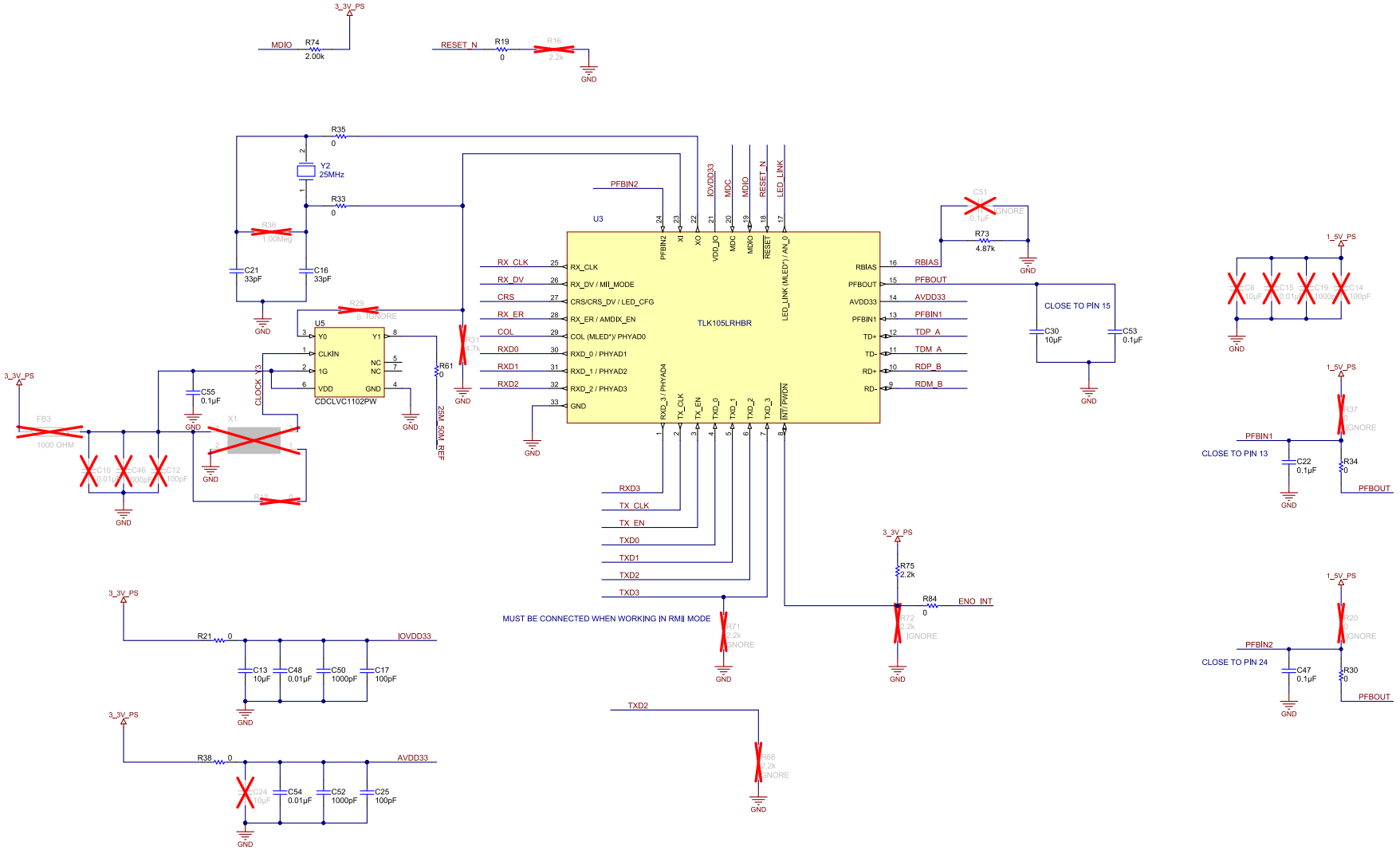

Figure 22. Schematics Page 3

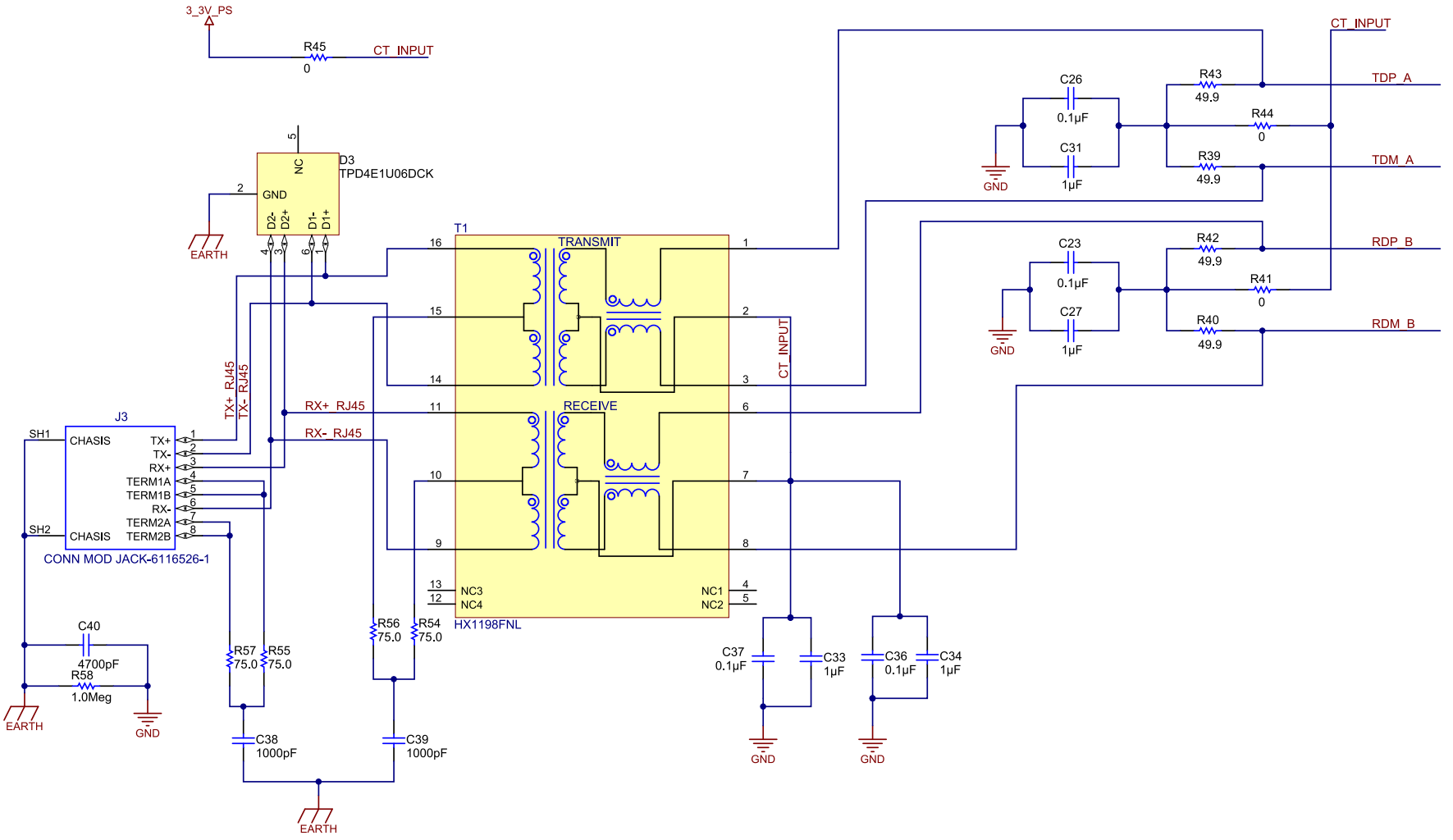

Figure 23. Schematics Page 5

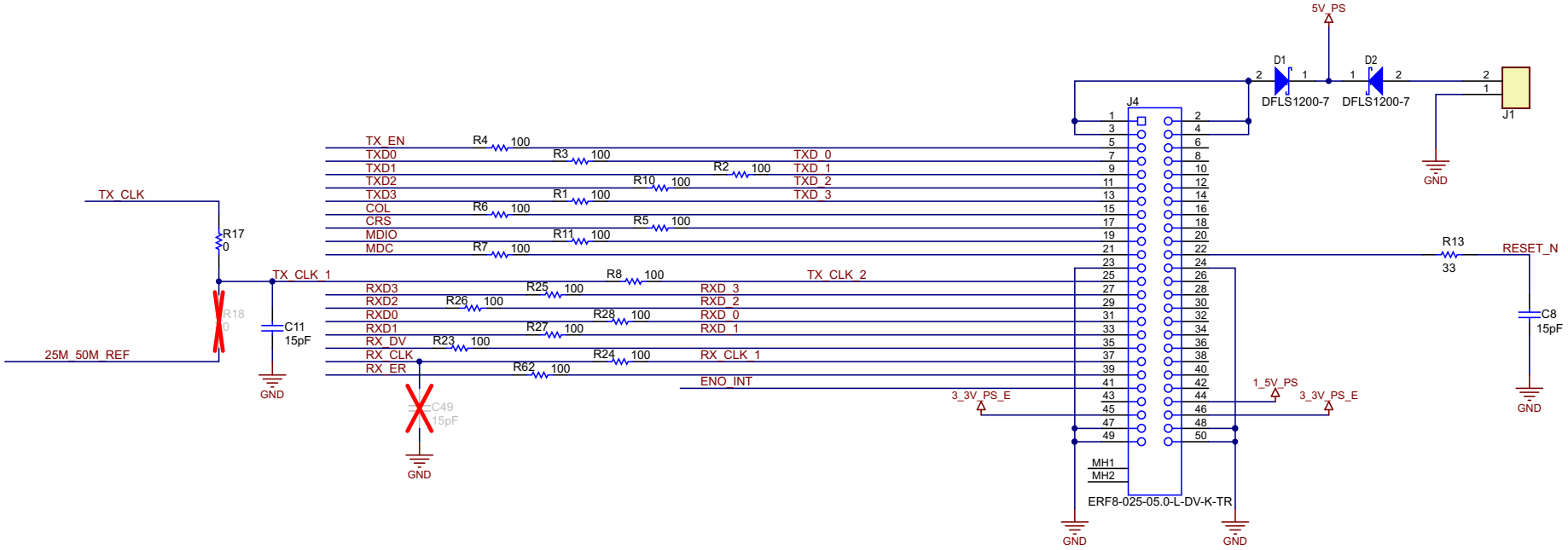

Figure 24. Schematics Page 6

Figure 25. Schematics Page 7, Part A

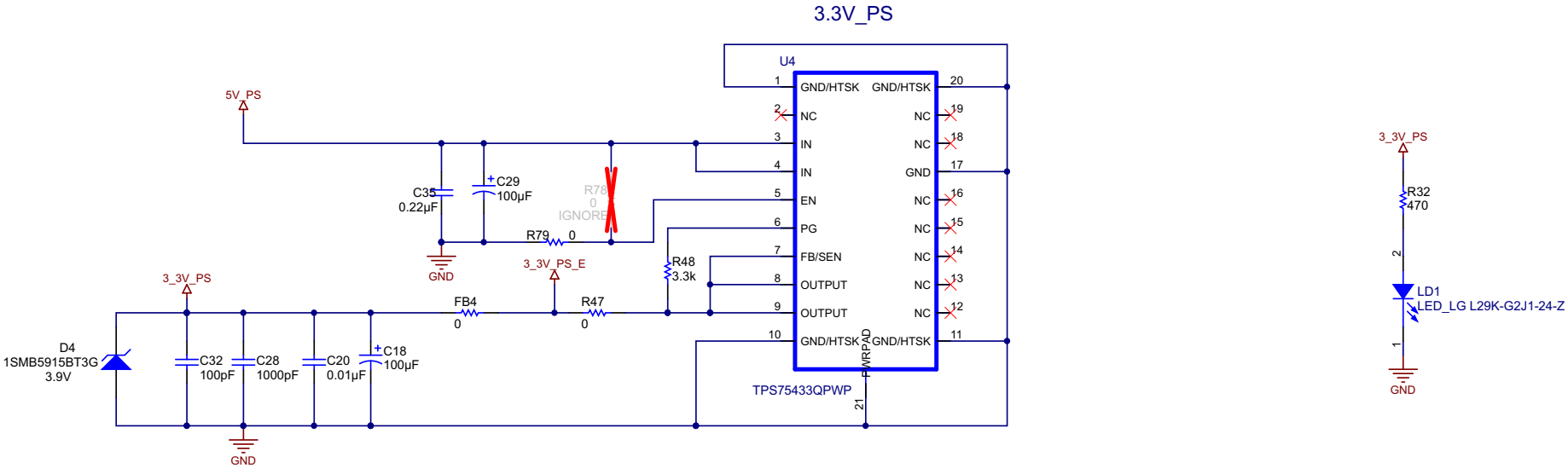

Figure 26. Schematics Page 7, Part B

Table 9. Bill of Materials

Fitted	DESCRIPTION	DESIGNATOR	MANUFACTURER	PARTNUMBER	QUANTITY	ROHS	PACKAGEREFERENCE
Fitted	Printed Circuit Board	!PCB1	Any	TIDA-00190	1	O	
Not Fitted	CAP, CERM, 1uF, 10V, +/-10%, X5R, 1206	C1, C4	MuRata	GRM319R61A105KA01D	0	Y	1206
Not Fitted	CAP, CERM, 0.22uF, 6.3V, +/-10%, X7R, 0603	C2, C7, C44	MuRata	GRM188R70J224KA88D	0	Y	0603
Not Fitted	CAP, CERM, 33pF, 50V, +/-5%, C0G/NP0, 0603	C3, C9	AVX	06035A330JAT2A	0	Y	0603
Not Fitted	CAP, CERM, 0.1uF, 16V, +80/-20%, Y5V, 0603	C5	Kemet	C0603C104Z4VACTU	0	Y	0603
Not Fitted	CAP, CERM, 10uF, 35V, +/-10%, X7R, 1206	C6, C24	Taiyo Yuden	GMK316AB7106KL	0	Y	1206
Fitted	CAP, CERM, 15pF, 50V, +/-5%, C0G/NP0, 0402	C8, C11	MuRata	GRM1555C1H150JA01D	2	Y	0402
Not Fitted	CAP, CERM, 0.01uF, 50V, +/-10%, C0G/NP0, 0402	C10, C15	MuRata	GCM155R71H103KA55D	0	Y	0402
Not Fitted	CAP, CERM, 100pF, 50V, +/-10%, X7R, 0402	C12, C14	Yageo America	CC0402KRX7R9BB101	0	Y	0402
Fitted	CAP, CERM, 10uF, 35V, +/-10%, X7R, 1206	C13	Taiyo Yuden	GMK316AB7106KL	1	Y	1206
Fitted	CAP, CERM, 33pF, 50V, +/-5%, C0G/NP0, 0603	C16, C21	AVX	06035A330JAT2A	2	Y	0603
Fitted	CAP, CERM, 100pF, 50V, +/-10%, X7R, 0402	C17, C25, C32	Yageo America	CC0402KRX7R9BB101	3	Y	0402
Fitted	CAP, TA, 100uF, 10V, +/-20%, 0.6 ohm, SMD	C18, C29	Vishay-Sprague	293D107X0010D2TE3	2	Y	7343-31
Not Fitted	CAP, CERM, 1000pF, 25V, +/-10%, X5R, 0402	C19, C42, C46	MuRata	GRM155R61E102KA01D	0	Y	0402
Fitted	CAP, CERM, 0.01uF, 50V, +/-10%, C0G/NP0, 0402	C20, C48, C54	MuRata	GCM155R71H103KA55D	3	Y	0402
Fitted	CAP, CERM, 0.1uF, 16V, +/-10%, X7R, 0603	C22, C47, C53, C55	Kemet	C0603C104K4RACTU	4	Y	0603
Fitted	CAP, CERM, 0.1uF, 10V, +/-10%, X5R, 0402	C23, C26, C36, C37	TDK	C1005X5R1A104K	4	Y	0402
Fitted	CAP, CERM, 1uF, 6.3V, +/-10%, X5R, 0603	C27, C31, C33, C34	MuRata	GRM185R60J105KE26D	4	Y	0603
Fitted	CAP, CERM, 1000pF, 25V, +/-10%, X5R, 0402	C28, C50, C52	MuRata	GRM155R61E102KA01D	3	Y	0402
Fitted	CAP, CERM, 10uF, 10V, +/-10%, X5R, 1210	C30	Kemet	C1210C106K8PACTU	1	Y	1210
Fitted	CAP, CERM, 0.22uF, 16V, +/-10%, X7R, 0603	C35	MuRata	GRM188R71C224KA01D	1	Y	0603
Fitted	CAP, CERM, 1000pF, 2000V, +/-10%, X7R, 1812	C38, C39	AVX	1812GC102KA1	2	Y	1812
Fitted	CAP, CERM, 4700pF, 2000V, +/-10%, X7R, 1812	C40	AVX	1812GC472KA1	1	Y	1812
Not Fitted	CAP, CERM, 4.7uF, 6.3V, +/-10%, X5R, 0603	C41, C43, C45	Kemet	C0603C475K9PACTU	0	Y	0603
Not Fitted	CAP, CERM, 15pF, 50V, +/-5%, C0G/NP0, 0402	C49	MuRata	GRM1555C1H150JA01D	0	Y	0402
Not Fitted	CAP, CERM, 0.1uF, 16V, +/-10%, X7R, 0603	C51	Kemet	C0603C104K4RACTU	0	Y	0603
Fitted	Diode, Schottky, 200V, 1A, PowerDI123	D1, D2	Diodes Inc.	DFLS1200-7	2	Y	PowerDI123
Fitted	Quad Channel High Speed ESD Protection Device, DCK0006A	D3	Texas Instruments	TPD4E1U06DCK	1	Y	DCK0006A
Fitted	Diode, Zener, 3.9V, 550mW, SMB	D4	ON Semiconductor	1SMB5915BT3G	1	Y	SMB
Not Fitted	FERRITE CHIP 1000 OHM 300MA 0603	FB1, FB2, FB3	TDK Corporation	MMZ1608B102C	0	Y	0603
Fitted	RES, 0 ohm, 5%, 0.1W, 0603	FB4, R17, R19, R33, R35, R41, R44, R45, R47, R51, R53, R61, R79, R84	Vishay-Dale	CRCW06030000Z0EA	14	Y	0603
Not Fitted	Fiducial mark. There is nothing to buy or mount.	FID1, FID2, FID3, FID4, FID5, FID6	N/A	N/A	0		Fiducial
Fitted	CONN TERM BLOCK 2.54MM 2POS PCB	J1	On Shore Technology Inc	OSTVN02A150	1	Y	TERM_BLK, 2pos, 2.54mm
Not Fitted	CONN HEADER 3POS 2MM VERT T/H	J2	3M	951103-8622-AR	0	Y	0.079 inch x 3
Fitted	CONN MOD JACK R/A 8P8C SHIELDED	J3	TE Connectivity	6116526-1	1		RJ45
Fitted	Receptacle, 0.8mm, 25x2, SMT	J4	Samtec	ERF8-025-05.0-L-DV-K-TR	1	Y	25x2 Socket Strip

Table 9. Bill of Materials (continued)

Fitted	DESCRIPTION	DESIGNATOR	MANUFACTURER	PARTNUMBER	QUANTITY	ROHS	PACKAGEREFERENCE
Not Fitted	Thermal Transfer Printable Labels, 0.650" W x 0.200" H - 10,000 per roll	LBL1	Brady	THT-14-423-10	0	Y	PCB Label 0.650"H x 0.200"W
Fitted	LED SmartLED Green 570NM	LD1, LD2, LD3, LD4, LD5	OSRAM	LG L29K-G2J1-24-Z	5		0603
Fitted	Mountin hole, NPTH Drill 3.2mm	MH1, MH2, MH3, MH4	N/A	N/A	4		
Fitted	RES, 100 ohm, 5%, 0.063W, 0402	R1, R2, R3, R4, R5, R6, R7, R8, R10, R11, R23, R24, R25, R26, R27, R28, R62	Vishay-Dale	CRCW0402100RJNED	17	Y	0402
Not Fitted	RES, 1.00Meg ohm, 1%, 0.063W, 0402	R9, R36	Vishay-Dale	CRCW04021M00FKED	0	Y	0402
Not Fitted	RES, 0 ohm, 5%, 0.1W, 0603	R12, R18, R29, R46, R52, R78	Vishay-Dale	CRCW06030000Z0EA	0	Y	0603
Fitted	RES, 33 ohm, 5%, 0.063W, 0402	R13	Vishay-Dale	CRCW040233R0JNED	1	Y	0402
Not Fitted	RES, 22 ohm, 5%, 0.063W, 0402	R14, R15	Vishay-Dale	CRCW040222R0JNED	0	Y	0402
Not Fitted	RES, 2.2k ohm, 5%, 0.063W, 0402	R16, R63, R68, R71, R72	Vishay-Dale	CRCW04022K20JNED	0	Y	0402
Not Fitted	RES, 0 ohm, 5%, 0.125W, 0805	R20, R37	Yageo America	RC0805JR-070RL	0	Y	0805
Fitted	RES, 0 ohm, 5%, 0.125W, 0805	R21, R30, R34, R38	Yageo America	RC0805JR-070RL	4	Y	0805
Not Fitted	RES, 4.7k ohm, 5%, 0.1W, 0603	R31, R59, R60	Yageo America	RC0603JR-074K7L	0	Y	0603
Fitted	RES, 470 ohm, 1%, 0.1W, 0603	R32, R49, R76, R80, R83	Yageo America	RC0603FR-07470RL	5	Y	0603
Fitted	RES, 49.9 ohm, 1%, 0.063W, 0402	R39, R40, R42, R43	Vishay-Dale	CRCW040249R9FKED	4	Y	0402
Fitted	RES, 3.3k ohm, 5%, 0.063W, 0402	R48	Vishay-Dale	CRCW04023K30JNED	1	Y	0402
Fitted	RES, 2.2k ohm, 5%, 0.063W, 0402	R50, R64, R65, R66, R67, R69, R70, R75, R77, R81, R82	Vishay-Dale	CRCW04022K20JNED	11	Y	0402
Fitted	RES, 75.0 ohm, 1%, 0.1W, 0603	R54, R55, R56, R57	Yageo America	RC0603FR-0775RL	4	Y	0603
Fitted	RES, 1.0Meg ohm, 5%, 0.25W, 1206	R58	Vishay-Dale	CRCW12061M00JNEA	1	Y	1206
Fitted	RES, 4.87k ohm, 1%, 0.1W, 0603	R73	Vishay-Dale	CRCW06034K87FKEA	1	Y	0603
Fitted	RES, 2.00k ohm, 1%, 0.063W, 0402	R74	Vishay-Dale	CRCW04022K00FKED	1	Y	0402
Fitted	TRANSFORMER, MDL, XFMR SGL ETHR LAN, SOIC-16	T1	Pulse electronics	HX1198FNL	1	Y	-
Not Fitted	IC REG LDO 1.8V 50MA SC70-5	U1	Texas Instruments	TPS71518DCKR	0		SOP-5 (DCK)
Not Fitted	Programmable 1-PLL VCXO Clock Synthesizer With 1.8-V, 2.5-V, and 3.3-V Outputs, PW0014A	U2	Texas Instruments	CDCE913PW	0	Y	PW0014A
Fitted	IC, INDUSTRIAL TEMP, SINGLE PORT 10/100Mbs ETHERNET PHYSICAL LAYER TRANSCEIVER, VQFN-32P	U3	Texas instruments	TLK105LRHBR	1	Y	-
Fitted	IC, Low Dropout Voltage Regulator, 3.3 V, 2.0 A	U4	Texas Instruments	TPS75433QPWP	1		PWP20
Fitted	3.3 V and 2.5 V LVCMOS High-Performance Clock Buffer Family, PW0008A	U5	Texas Instruments	CDCLVC1102PW	1	Y	PW0008A
Not Fitted	OSC 25.00 MHZ 3.3V HIGH STAB SMD	X1	Epson	HG-2150CA 25.000M-BXC3	0	Y	4-SMD, No Lead (DFN, LCC)
Not Fitted	CRYSTAL 25.0MHZ 18PF SMD	Y1	CTS-Frequency Controls	445I23D25M00000	0	Y	2-SMD
Fitted	CRYSTAL 25.0MHZ 18PF SMD	Y2	CTS-Frequency Controls	445I23D25M00000	1	Y	2-SMD

8 Layer Plots

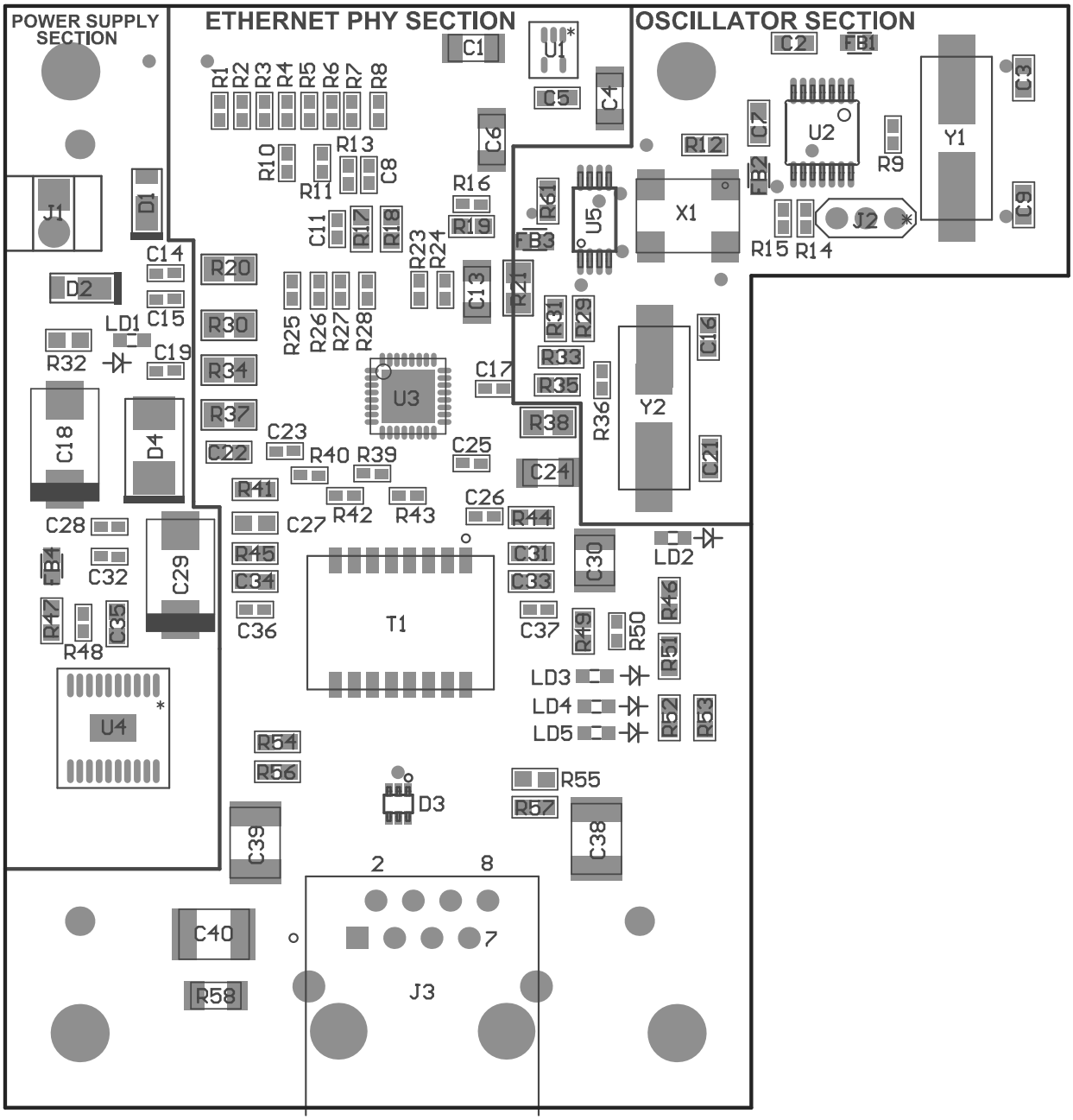

Figure 27. Layer Plots

9 Altium Project Files

For the complete set of Altium Project files, see TIDA-00190.

10 Gerber Files

To download the Gerber files for each board, see the design files at TIDA-00190.

11 References

1. *Industrial Temp, Single Port 10/100Mbs Ethernet Physical Layer Transceiver*, TLK105 Data Sheet TLK105L.
2. *TLK105/6L Customer EVM*, TLK105/6L User's Guide SLLU185.
3. *TLK1XX Design and Layout Guide*, TLK1XX Application Report SLVA531.

12 Software Files

To download the software files for the reference design, see the design files at TIDA-00190.

13 About the Author

KALLIKUPPA MUNIYAPPA SREENIVASA is a Systems Architect at Texas Instruments, where he is responsible for developing reference design solutions for the industrial segment. Sreenivasa brings to this role his experience in high-speed digital and analog systems design. Sreenivasa earned his Bachelor of Electronics (BE) in Electronics and communication Engineering (BE-E&C) from VTU, Mysore, India.

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