How to solve design challenges on interfacing Ethernet PHY with application processor or microcontrollers

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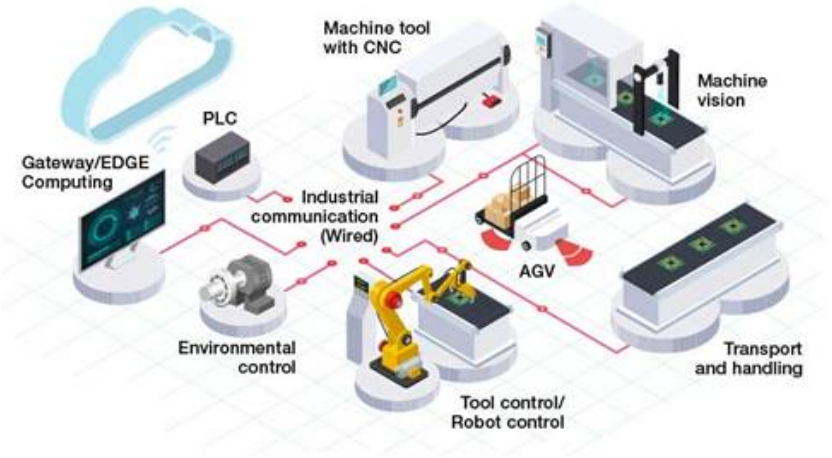
Agenda

- Introduction
- Part 1 – Ethernet design fundamentals
- Part 2 – TIDA-010010: Integration example with AM5728 with DP83867
- Part 3 – Ethernet PHY integration compression between TIDA-010010 and standard AM5728 EVM
- Summary and Outlook

Design challenges with Ethernet PHYs using MPU/MCU

- Multi-protocol industrial Ethernet (2 ports).
- Standard Ethernet for uplink, edge and cloud connection, configuration and diagnostics data.
- Ethernet speed: 10/100/1000 Gbit.
- MAC to PHY Interface.
- Ethernet topology: Line, ring, star.
- New evolution for Ethernet in Industrial
  - T1: Single twisted pair Ethernet for industrial.
  - Power of Data Line: PoDL, APL, PoE



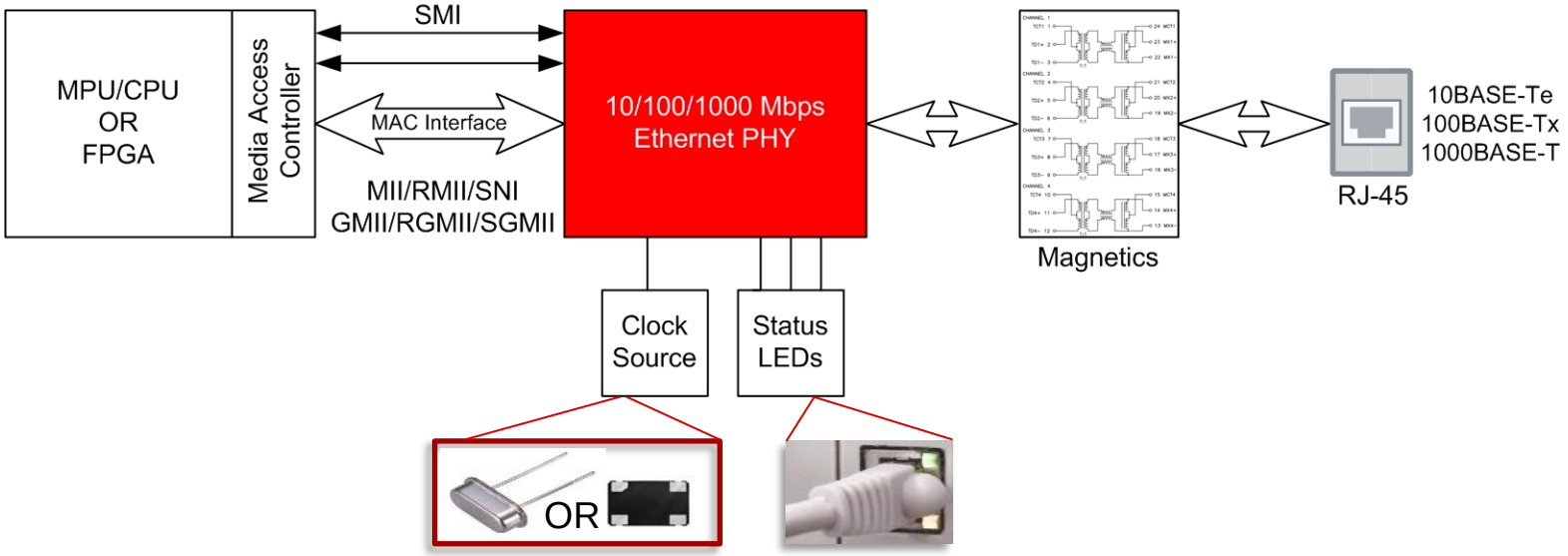
Part 1

Ethernet design fundamentals

Ethernet PHY common terminology

- PHY (Physical layer transceiver/device) provides a way to transfer digital data from one node (processor, FPGA, ASIC…) to another node via analog signaling over either copper or fiber optic cable.
- Three important processes a PHY handles:
  - PCS, physical coding sublayer.
  - PMA, physical medium attachment.
  - PMD, physical medium dependent.
- Other key terms and functions:
  - MDI, medium dependent interface (TD±/RD±).
  - MII, media independent interface (Digital pins, TX_D[3:0]/RX[3:0] etc…).
  - Start of Frame Detection (SOF) for timestamping.
  - Fast link-down detection (<15 µs)
  - Cable Diagnostics (TDR, link quality, …)

Connecting PHY to MAC: Typical application circuit



MAC interfaces – used for data transfer

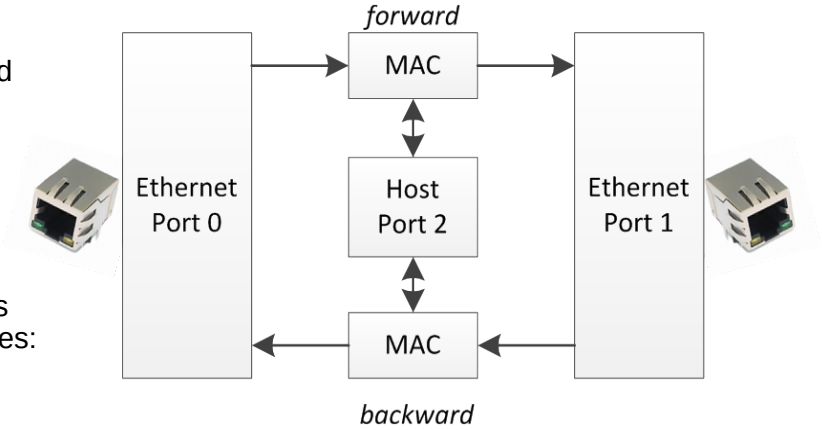
Interface Details	MII	RMII	SNI
Full Name	Media Independent Interface	Reduced-Media Independent Interface	Serial Network Interface
Pin Count	15	9	7
Clock Speed	25MHz – 100Mbps 2.5MHz – 10Mbps	50MHz – 10Mbps and 100Mbps	10MHz – 10Mbps
Transmit Pins	TX_D[3:0], TX_EN, TX_CLK	TX_D[1:0], TX_EN	TX_D[0], TX_EN, TX_CLK
Receive Pins	RX_D[3:0], RX_DV, RX_ER, COL, CRS, RX_CLK	RX_D[1:0], CRS_DV	RX_D[0], CRS, COL, RX_CLK

MAC interfaces – used for data transfer

Interface Details	GMII	RGMII	SGMII
Full Name	Gigabit Media Independent Interface	Reduced-Gigabit Media Independent Interface	Serial Gigabit Media Independent Interface
Pin Count	24	12	4
Clock Speed	125MHz – 1Gbps	125MHz – 1Gbps DDR	625MHz – 1.25Gbaud data, DDR
Transmit Pins	TX_D[7:0], TX_EN, TX_CLK, GTX_CLK, TX_ER	TX_D[4:0], TXEN_ER, TCK	TX_P, TX_N
Receive Pins	RX_D[7:0], RX_DV, RX_ER, COL, CRS, RX_CLK	RX_D[4:0], RXDV_ER, RCK	RX_P, RX_N

Industrial Ethernet MAC and frame processing

- Media Access Controller (MAC)
  - Industrial Ethernet uses 3-port switch: Two physical Ethernet ports and one host port
  - Specialized MAC is required for following frame handling methods
  - MAC requirements depend on industrial Ethernet protocol and master/slave
- Frame processing methods:
  - Cut-through: Receives the Ethernet header, performs header analyzes and takes forwarding decision; frame is not modified by MAC. Examples: Profinet, Ethernet/IP, Powerlink, Sercos in UCC/NRT channels
    - Delay Time: 3-4 µs
  - On-the-fly: Frame is forwarded to second Ethernet port; MAC can perform read and write access to the frame while its runs through MAC; CRC is updated to reflect frame modifications by MAC. Examples: EtherCAT, Sercos
    - Delay Time: <1 µs
  - Store and forward: Legacy mode used by all standard Ethernet MACs; store frame in memory, perform header analyzes first before taking forwarding decision; frame is not modified by MAC.
    - Delay Time: 6.7 µs (64 Bytes) to 125 µs (1500 Bytes)

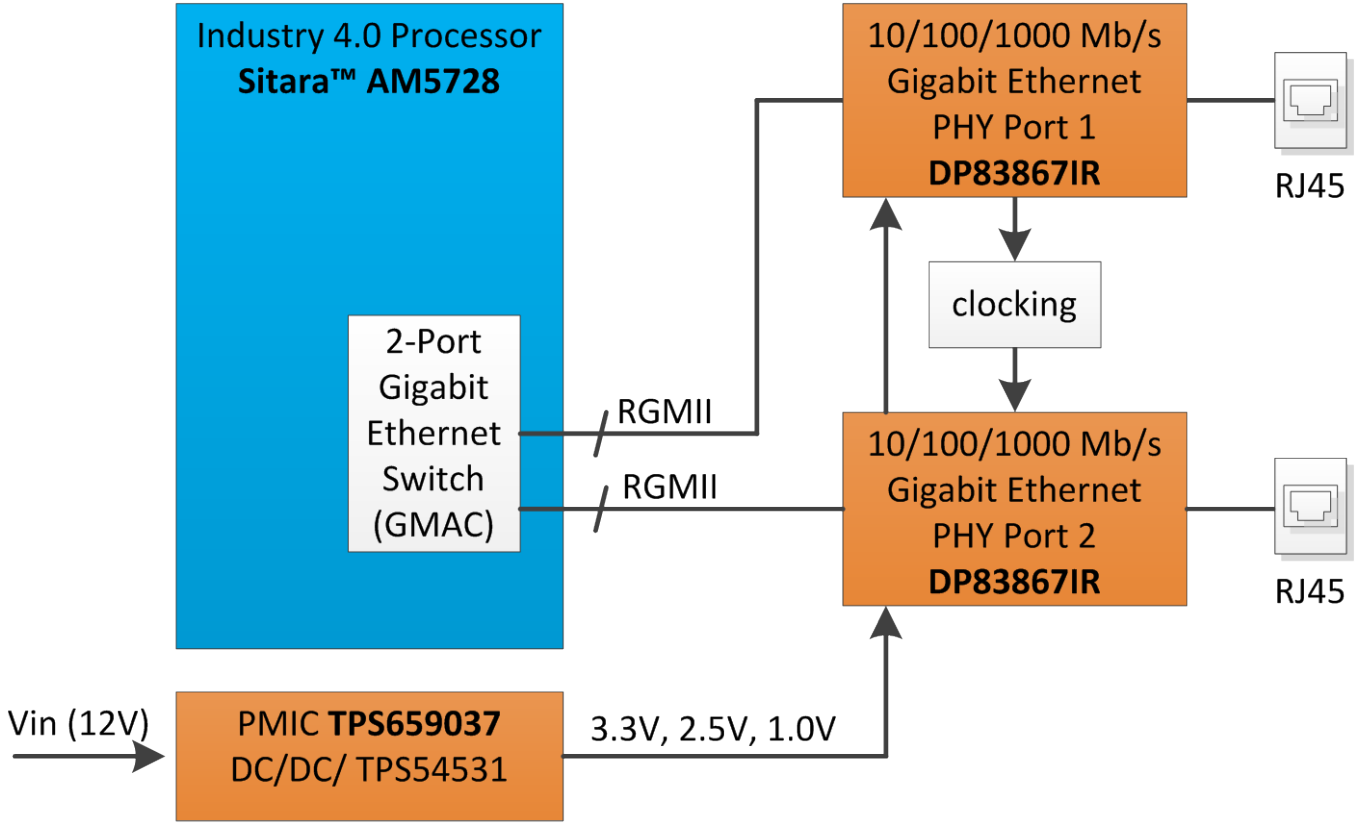


Part 2

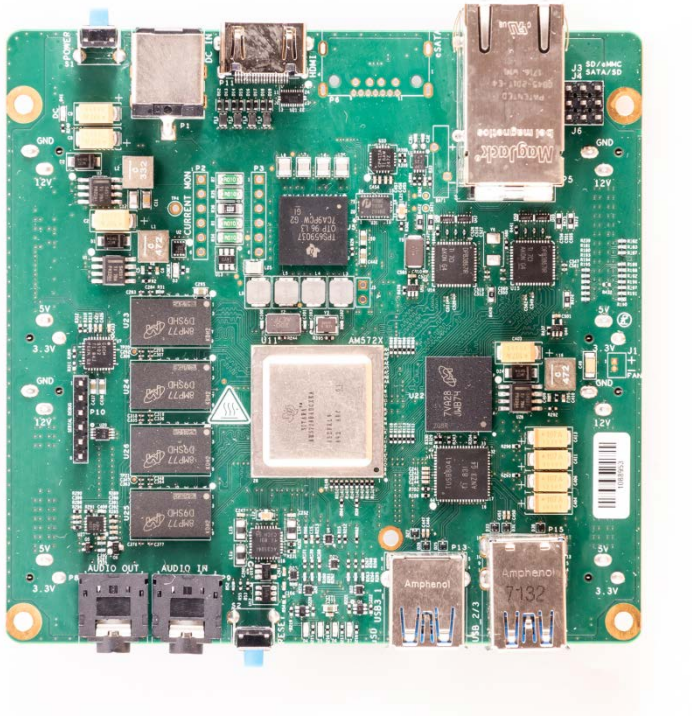
Integration example: TIDA-010010

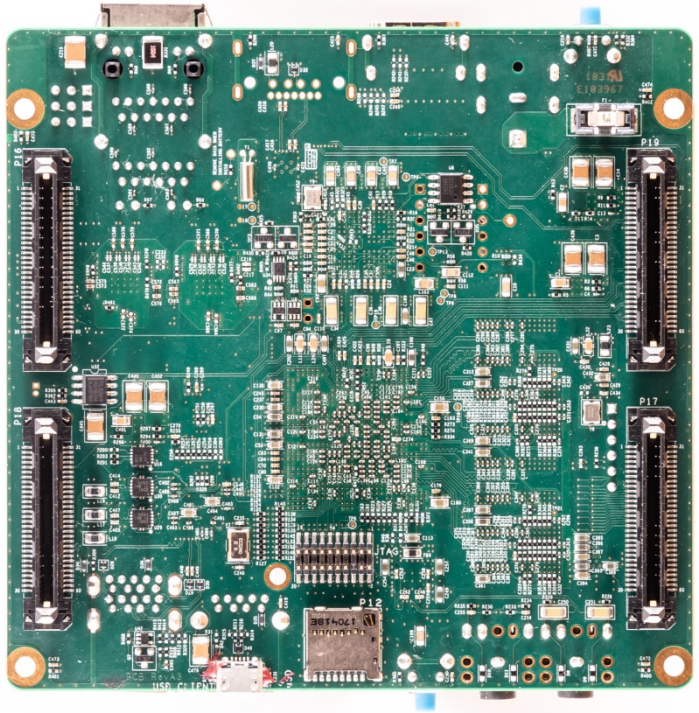
Sitara™ AM5728 processor with DP83867IR

TIDA-010010 system block diagram

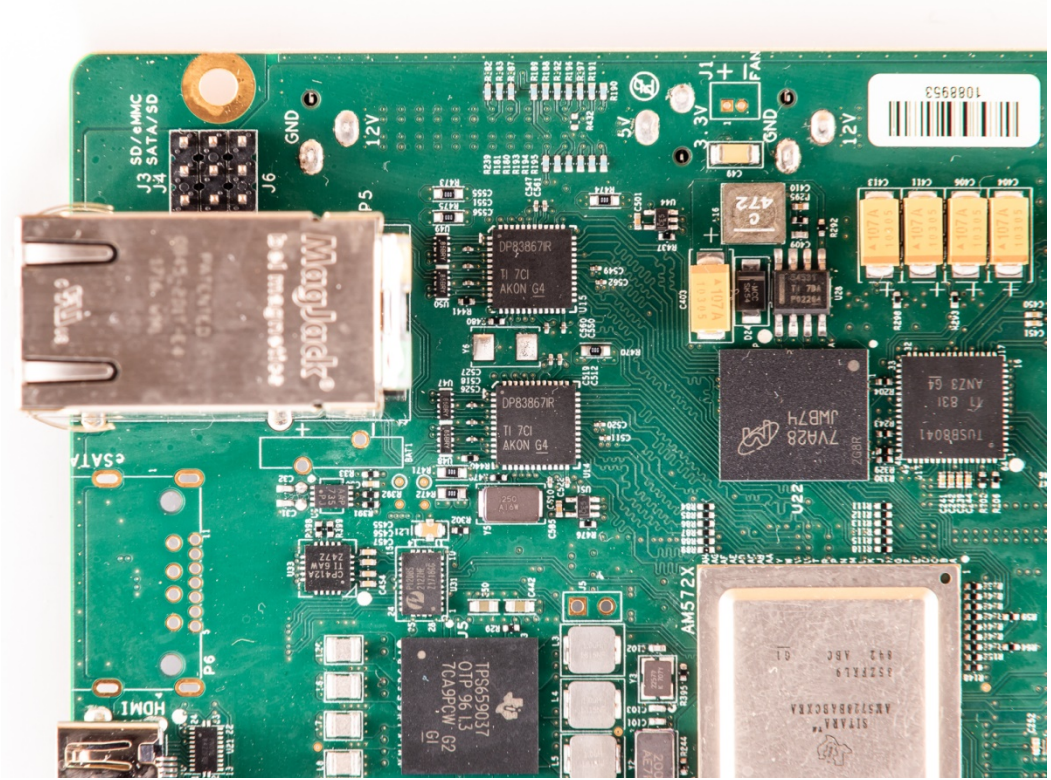


TIDA-010010 top and bottom PCB

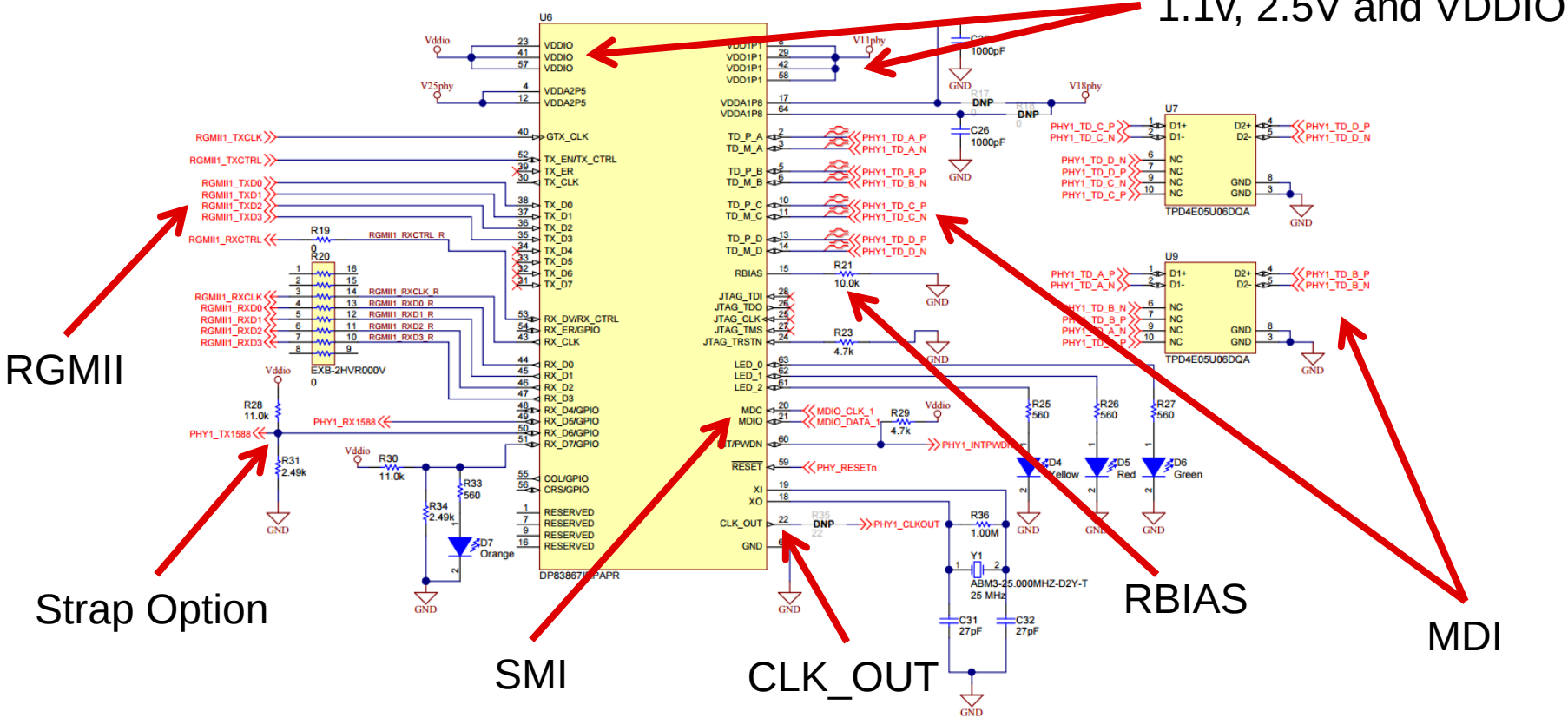




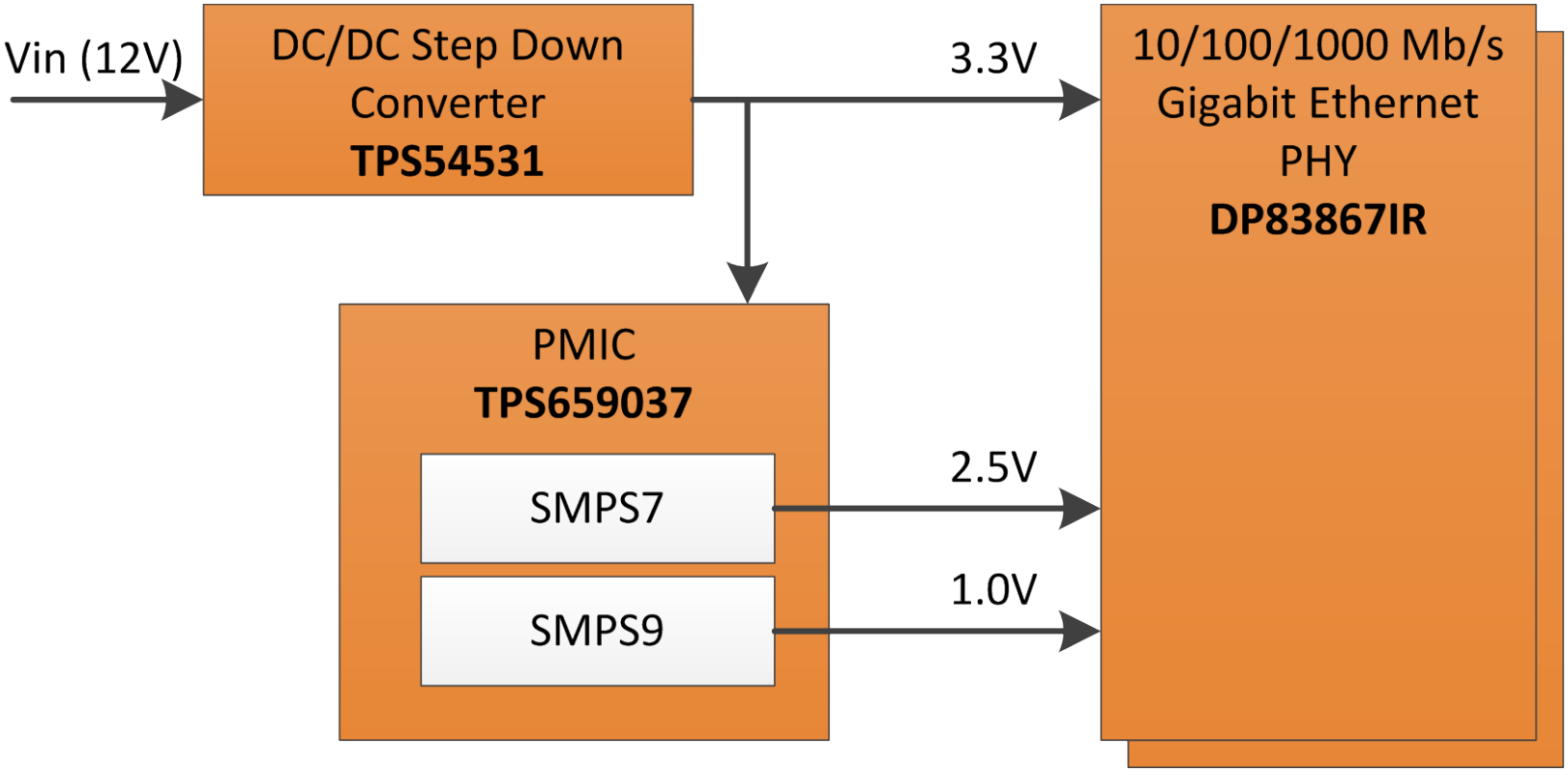
TIDA-010010 Ethernet PHY PCB section



DP83867IR PHY example design



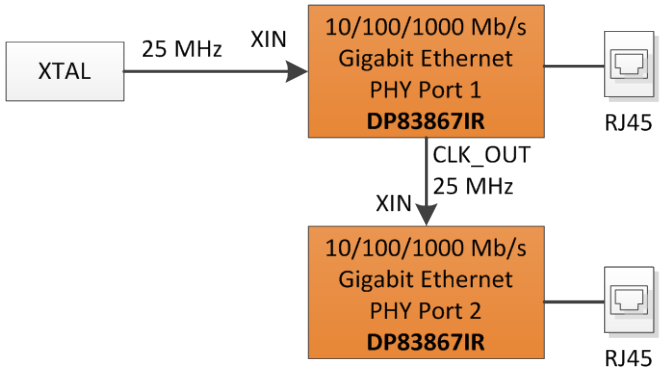
Power generation

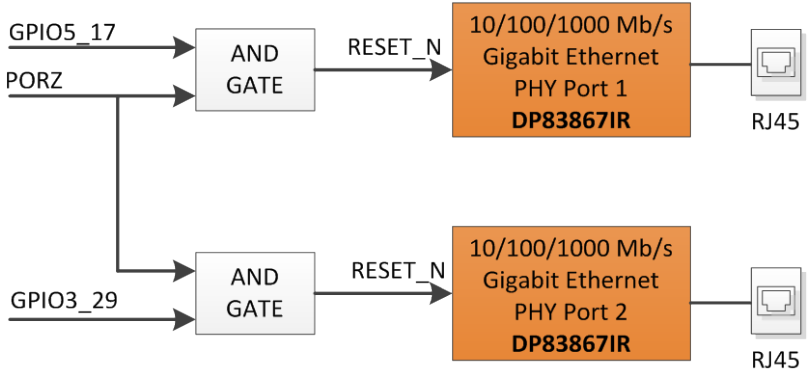


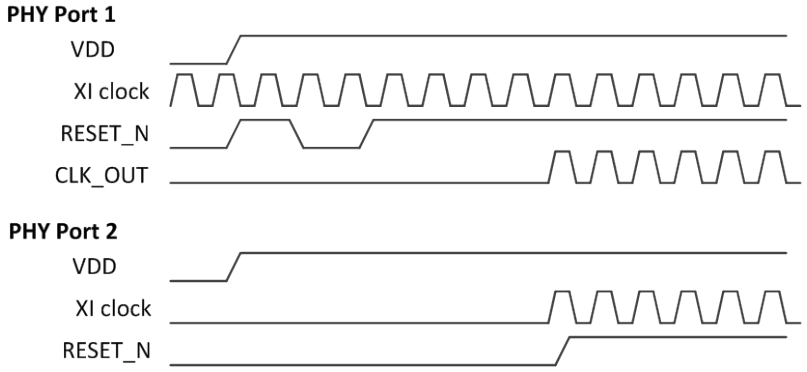
Bootstrap pins

- DP83867 configured through bootstrap during power-on-reset.
  - Examples: MDIO address, Full-duplex, RGMII mode.
  - 4 voltage levels.
    - 0 V – Mode 1
    - 1.4 V – Mode 2 (mid-voltage level)
    - 2.4 V – Mode 3 (mid-voltage level)
    - 3.3 V – Mode 4
- AM5728 should not get exposed to mid-voltage level during power up.
  - Effect on POH lifetime
- Options
  1. Configure only Mode 1 and 4, avoid Mode 2 and 3
     - Use MDIO after power up to configure the PHY
  2. Buffer to isolate signals between AM5728 and DP83867 during power up

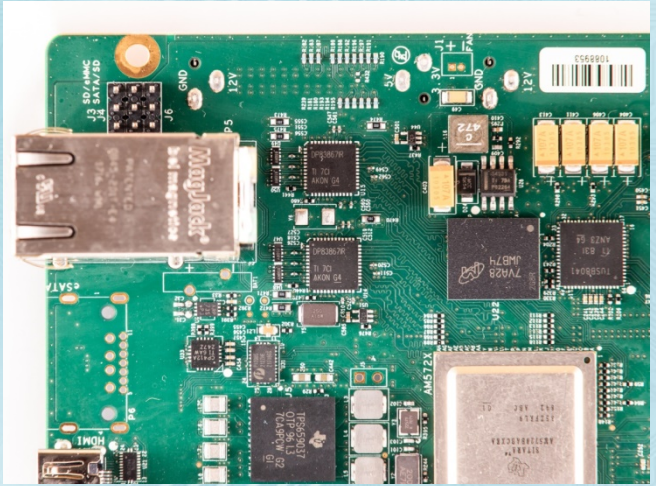
Clocking and reset generation







Part 3



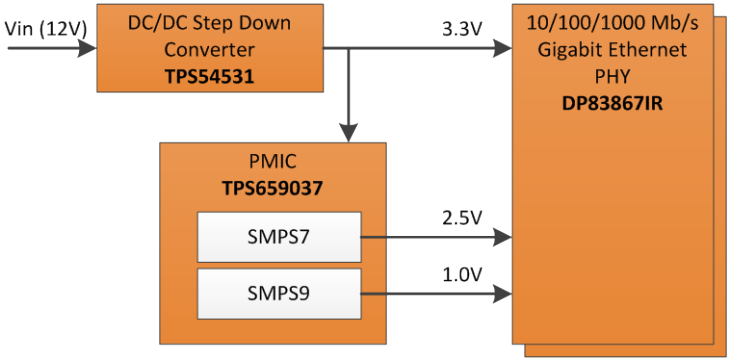
Ethernet PHY integration compression between TIDA-010010 and the standard AM5728 EVM

DP83867IR vs. Microchip/Micrel KSZ9031

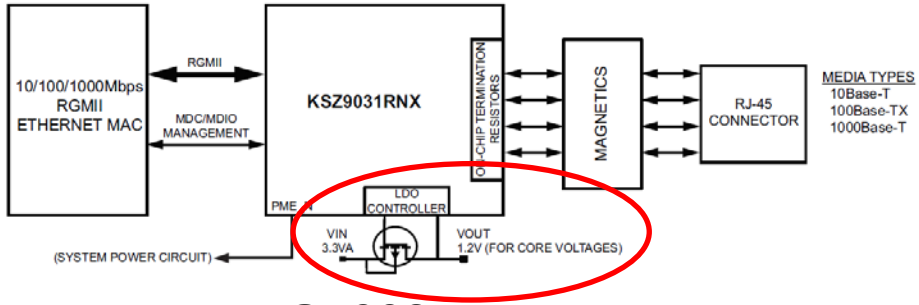
Parameter	DP83867	KSZ9031
Size	48-pin QFN, 7mm x 7mm 64-pin QFP, 10mm x 10mm	48-pin QFN, 7mm x 7mm 64-pin QFP, 10mm x 10mm
Current consumption	457mW (RGZ) 490mW (PAP)	538mW (1G, no traffic) 972mW (1G, no traffic + MOSFET losses) 621mW (1G, 100%)
Voltage Rails	3.3V, 2.5V, 1.1V or 1.0V	3.3V, 1.2V
Voltage generation	external	P-channel MOSFET for 1.2V NOTE: **Uses +441mW in MOSFET**
Temperature	-40°C to +85°C	-40°C to +85°C
Features	Fast link drop (ECAT, IE) Cable Diagnostics TDR, ALCD	n/a LinkMD Cable Diagnostics TDR
TX/RX Delay	88ns / 288ns	Not specified
PCB / BOM area	See next slides	See next slides

Power supply solution

- Using PMIC with AM5728
- Alternative suggestions from the TIDA-010010 reference design guide
- WCSP package option with 0.35-mm pitch enables smaller PCB board space area
  - From 5-V or 3.3-V source voltage to 2.5-V supply voltage: TPS62802
  - From 5-V or 3.3-V or 2.5-V source voltage to 1.0-V supply voltage: TPS62801
- QFN package option
  - From 5-V or 3.3-V voltage to 2.5-V supply voltage: TPS62230
  - 5-V or 3.3-V or 2.5-V voltage to 1.0 V: TPS62239



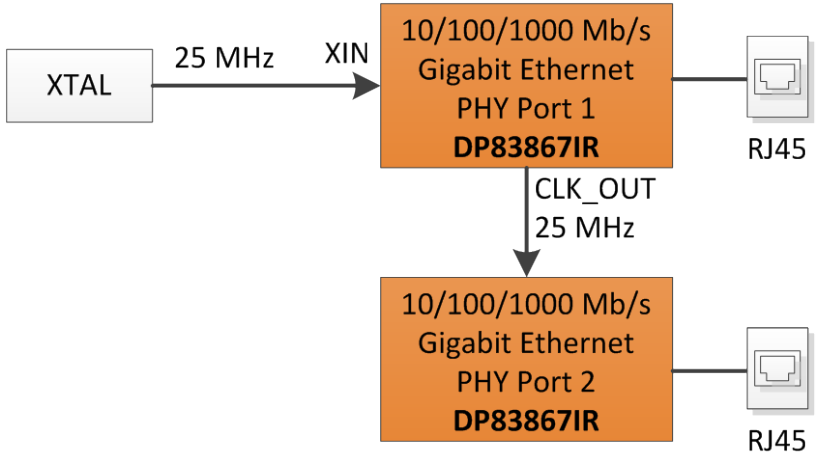
TIDA-010010



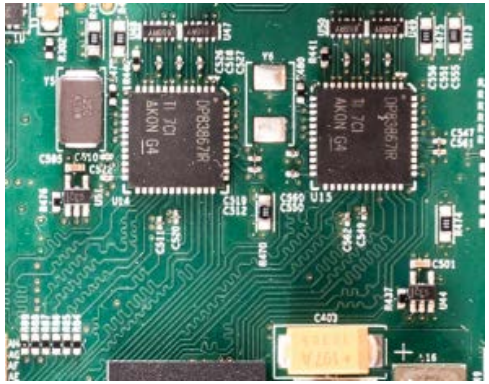
KSZ9031

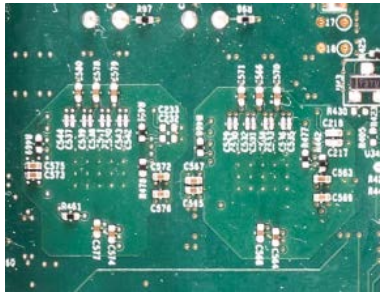
Clocking

- TIDA-010010 uses daisy chain clocking:
  - XTAL → PHY1 → PHY2
- DP83867 supports CLK_OUT pin
  - Configurable: 25MHz clock output
- KSZ9032 does not support 25 MHZ CLK_OUT

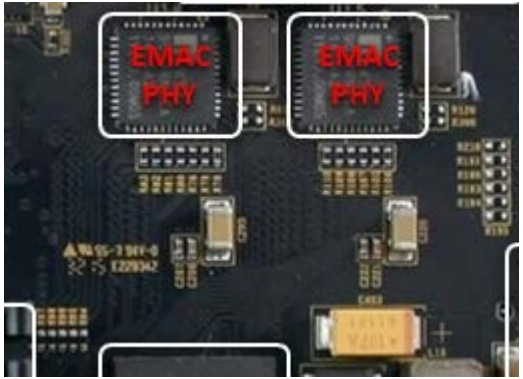


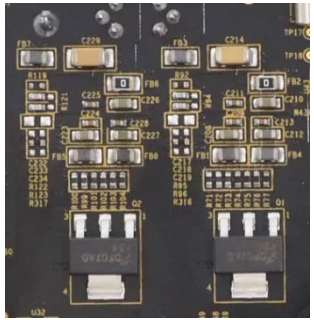
Layout area - DP83867 vs KSZ9031





DP83867





KSZ9031

Summary and outlook

Industrial Ethernet Physical Layer Transceiver (PHY)

- **Part number DP83848**
  - **“Gold Standard”** 10/100Mbps Industrial Ethernet PHY
  - Supports 100BASE-TX
- **Part number DP83822**
  - 10/100Mbps Industrial Ethernet PHY with IEEE 1588 SFD
  - Supports 100BASE-TX and 100BASE-FX
  - Fast-Link-Down detection
- **Part number DP83TC811**
  - 100Mbps Ethernet PHY for single twisted pair cable
  - Supports 100BASE-T1 Ethernet PHY
- **Part number DP83630**
  - 10/100Mbps Industrial Ethernet PHY with integrated IEEE 1588 HW Timestamping support
  - Supports 100BASE-TX and 100BASE-FX

- **Part number DP83867**
  - 10/100/1000Mbps Industrial Ethernet Gigabit PHY with IEEE 1588 SFD
  - Supports 100BASE-TX and 1000BASE-T
  - Fast-Link-Down detection
- **Part number DP83869**
  - 10/100/1000Mbps Industrial Ethernet Gigabit PHY with IEEE 1588 SFD
  - Supports IEEE 802.3 1000Base-T, 100Base-TX, 10Base-Te,1000Base-X, 100Base-FX
  - Fast-Link-Down detection

Processors with PRU-ICSS and EMAC/GMAC

PRU-ICSS (10/100Mbps)

Products

Features

- 10/100 Ethernet Speeds
- Capable of supporting Industrial Ethernet protocols, Interface protocols, and Ethernet communication protocols
  - EnDat, Hiperface DSL, BiSS, HSR, PRP, 1588, plus list below

Protocols Supported

PROFIBUS — TIDEP0002

PROFINET — TIDEP0008

EtherCAT — TIDEP0001

sercos the automation bus — TIDEP0010

ETHERNET POWERLINK

EtherNet/IP™ — TIDEP0003

PRU-ICSS-G (10/100/1000Mbps)

Products

New and Upgraded Features

- 1Gb Ethernet Speeds
- Retains FW Compatibility with previous PRU-ICSS versions
- New features enable Time Sensitive Networking (TSN), and 1Gb rates on Industrial Ethernet and redundancy protocols

Current Status

- 3x PRU_ICSS_G inside AM65xx
- Supports legacy industrial Ethernet protocols from AM3/4/5
- TSN integration into PRU-ICSS_G

Processors with PRU-ICSS and EMAC/GMAC cont'd

CPSW / EMAC / GMAC

Products

Features

- 10/100/1000 Ethernet Speeds
- Switching fabric
- Capable of supporting standard Ethernet and some industrial Ethernet protocols

Protocols Supported

TCP/IP

EtherCAT Master
TIDEP0043

EtherNet/IP
TIDEP0003

PROFINET IO

Get Started Today!

Visit links below for the latest documentation and product information

- TIDA-00204 Reference Design Page
- TIDA-00299 Reference Design Page
- TIDA-00207 Design Page
- DP83867 RGMII Linux Drivers

– Looking for a 10/100/1000 PHY Ethernet solution?
Refer to the AM5728 with DP83867 reference design

- TIDA-010010 Reference Design Page