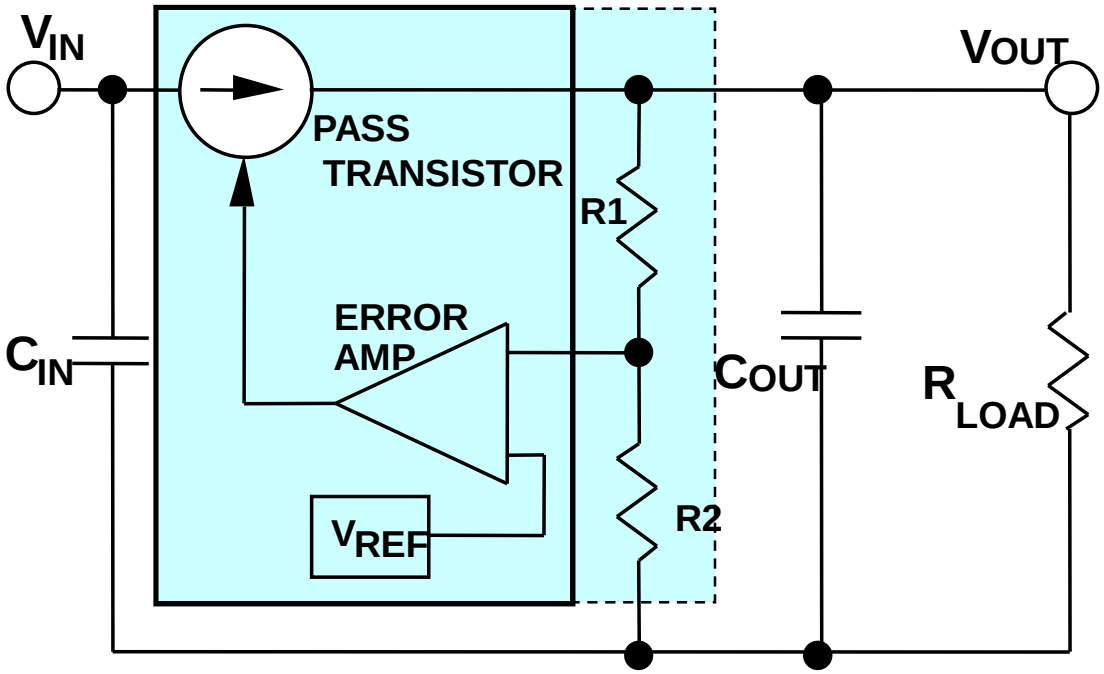
Linear Regulator Fundamentals

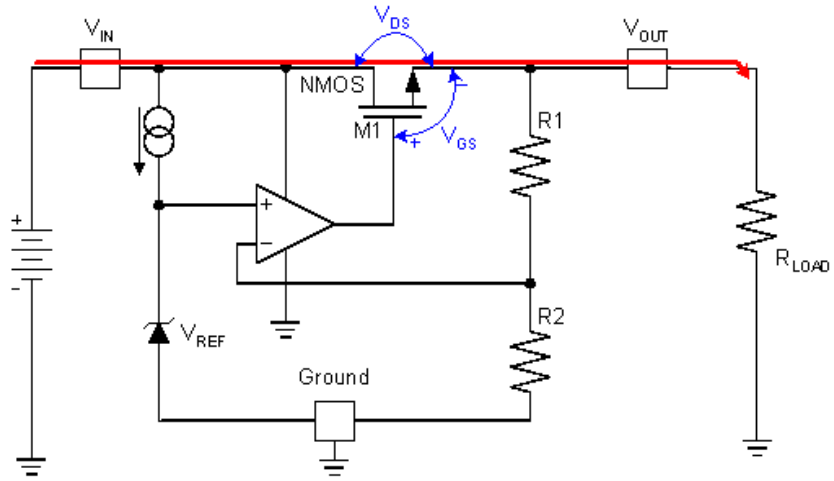
2.4 NMOS

Linear-Regulator Operation

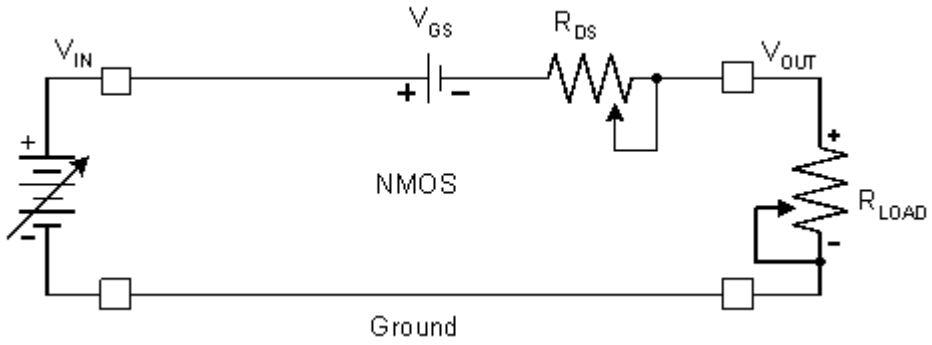
- Voltage feedback samples the output R1 and R2 may be internal or external
- Feedback controls pass transistor's current to the load



Losses in the Standard NMOS

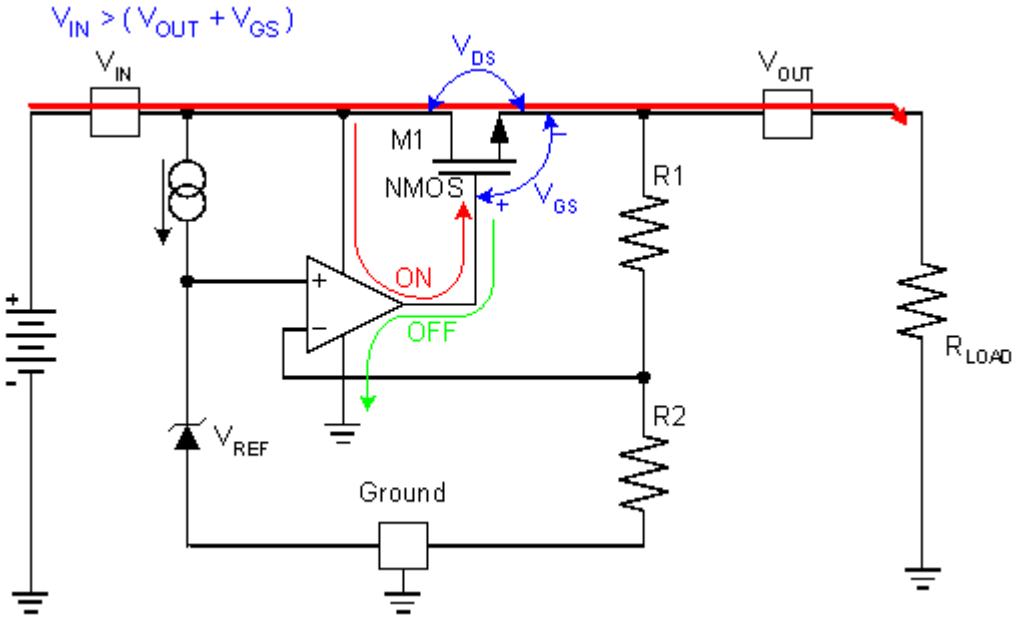


Simple Model of Losses in the NPN "Quasi-LDO"

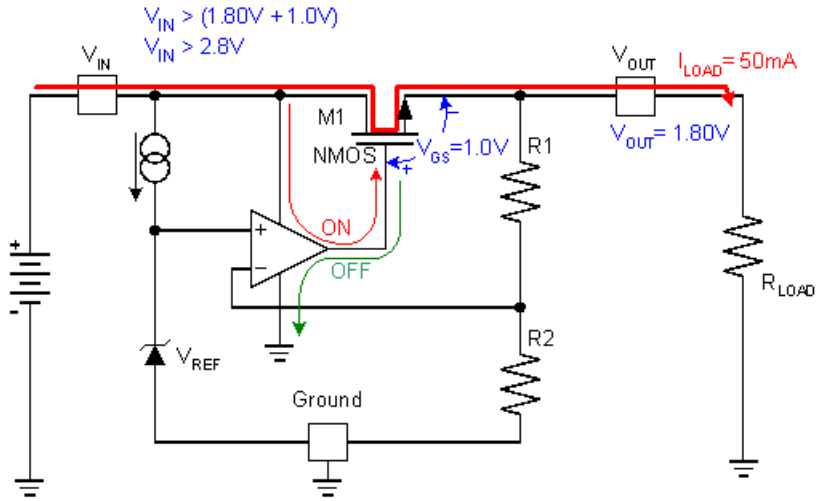


Driving the Standard NMOS Pass Element

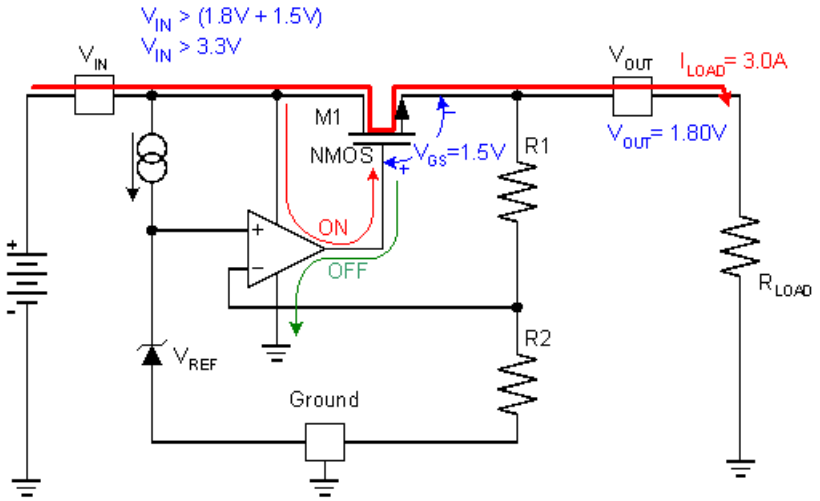
- The current flow through the NMOS pass element to the load is shown in this simplified schematic. The Gate to Source voltages (V_{GS}) used here are for illustrating the concept. Actual Gate to Source voltages will depend on the fabrication process used, as well as design considerations. A typical NMOS pass transistor will actually consist of several thousand individual transistors in parallel.



Drive Current vs. Low/High Load Current



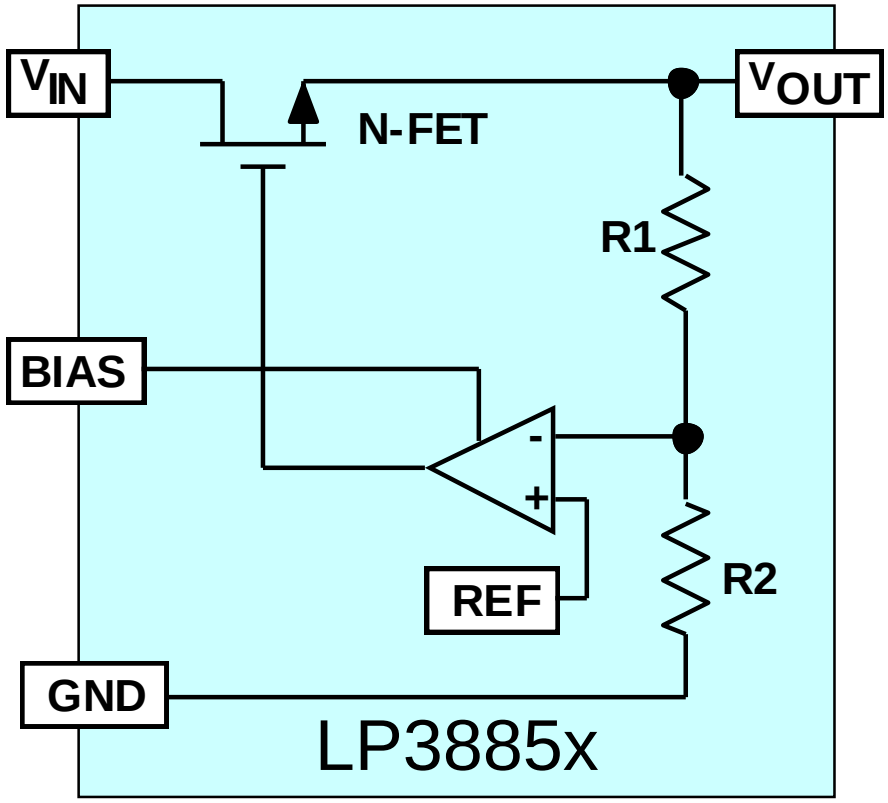
The drive current for a load current requirement of 50mA



Increasing the load current requirement
to 3A

N-FET LDO with Bias Rail

- Requires bias voltage to pull up N-FET
- Has characteristics similar to the NPN regulator



Advantages of N-FET LDO

- N-FET has lower ON resistance than P-FET
- Allows very low V_{IN} and V_{OUT} values
- Lower output impedance reduces the effect of load pole
- Stable with small external capacitors
- Low ground-pin current regardless of load
- High DC gain and good bandwidth

Summary

- The NMOS voltage regulator has the following Characteristics:
  - Requires the input voltage to be higher than the output voltage by the V_{GS} requirement of the pass transistor
    - This is not Low Drop Out
  - Ground pin current does not vary with the output load current
  - Does not require any output capacitor, (but use one anyway)

Thank you!