Slew Rate – 2
TIPL 1222
TI Precision Labs – Op Amps

Presented by Ian Williams

Prepared by Art Kay, Ian Williams, and Marek Lis
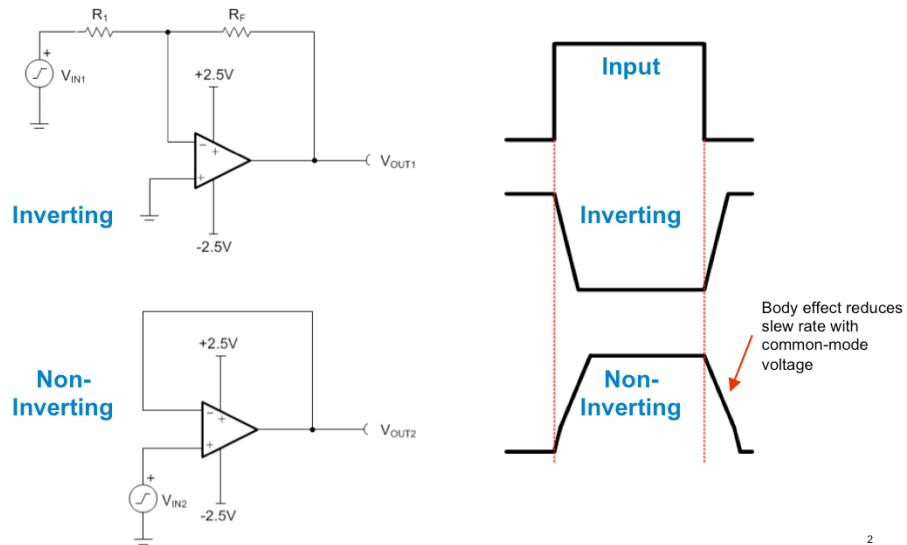
TEXAS INSTRUMENTS

Hello, and welcome to the TI Precision Lab discussing slew rate, part 2.

In this video we'll discuss the body effect's impact on slew rate, take a look at settling time, discuss the differences between an amplifier's small-signal vs. large-signal step response, and relate small-signal step response to stability.

The **body effect** is an example of a common secondary effect that influences slew rate. The body effect causes the slew rate of an amplifier to decrease with changing common mode voltage. The body effect is more pronounced in the non-inverting configuration, because in this case the common mode voltage changes with the input signal.

In this example, the non-inverting configuration shows a reduced slew rate for higher common mode voltages. The specified slew rate of an amplifier is typically measured in a non-inverting configuration, since this is the worst-case condition. In the next slide we will explain what causes the body effect inside the IC. However, the key point to understand is that the body effect is one of several secondary effects that can influence slew rate.

Body Effect on Slew Rate
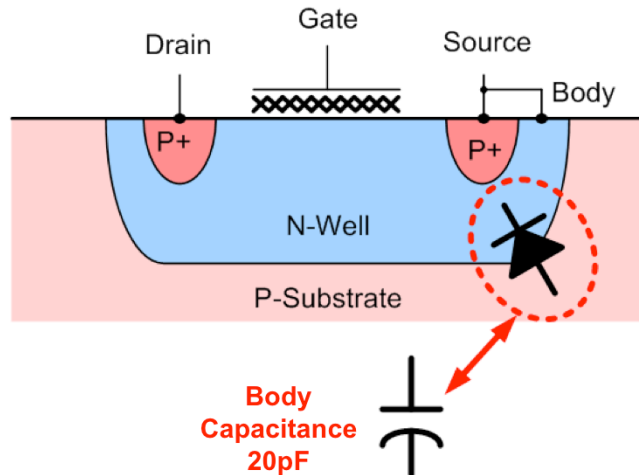
Remember from the first slew rate video that each input pin of an op-amp is connected to a transistor. Let's assume that these transistors are PMOS, or P-type MOSFET.

Looking at a cross-section of a PMOS, we see that the body is a deposit of n-type material inside the p-type substrate. A p-type drain and source are then deposited inside the n-well. A diode is formed between the body and substrate simply due to the existence of a p-n junction. The diode is normally reverse-biased and has some amount of internal capacitance. **Changing the common-mode voltage, which is the voltage across the p-n junction, will affect the amount of capacitance since the p-n junction's depletion region width will change.**

Body Effect on Slew Rate
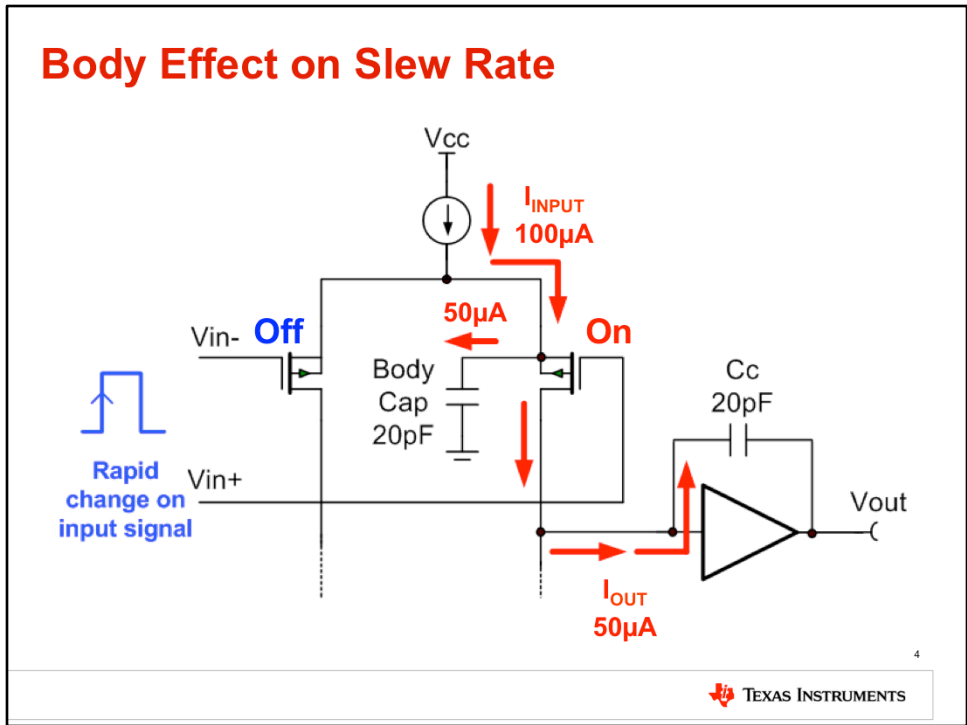
Let's go back to the input stage of an op-amp to see the implications that body capacitance has on slew rate.

Like in the previous video, we apply a large-signal step across the op-amp's input pins. The transistor on the left is off, and the transistor on the right is fully on, so all input stage current I_{INPUT} flows through the right transistor for maximum slew rate. However, the body capacitance to ground provides a new current path and reduces the amount of current I_{OUT} flowing through the Miller capacitance C_C. This reduced I_{OUT} decreases the effective slew rate of the amplifier since the voltage across a capacitor changes linearly with constant current.

In this example, the body capacitance and Miller capacitance are both equal to 20pF, so I_{OUT} will become half of I_{INPUT} as long as the common mode voltage is not constant. In this example, the effective slew rate of the amplifier is also cut in half since slew rate is equal to Iout/Cc. Note that the body capacitance will charge to the common mode voltage. Thus, if the common mode voltage is kept constant, as in the case of the inverting configuration, the body capacitance will not effect the slew rate.
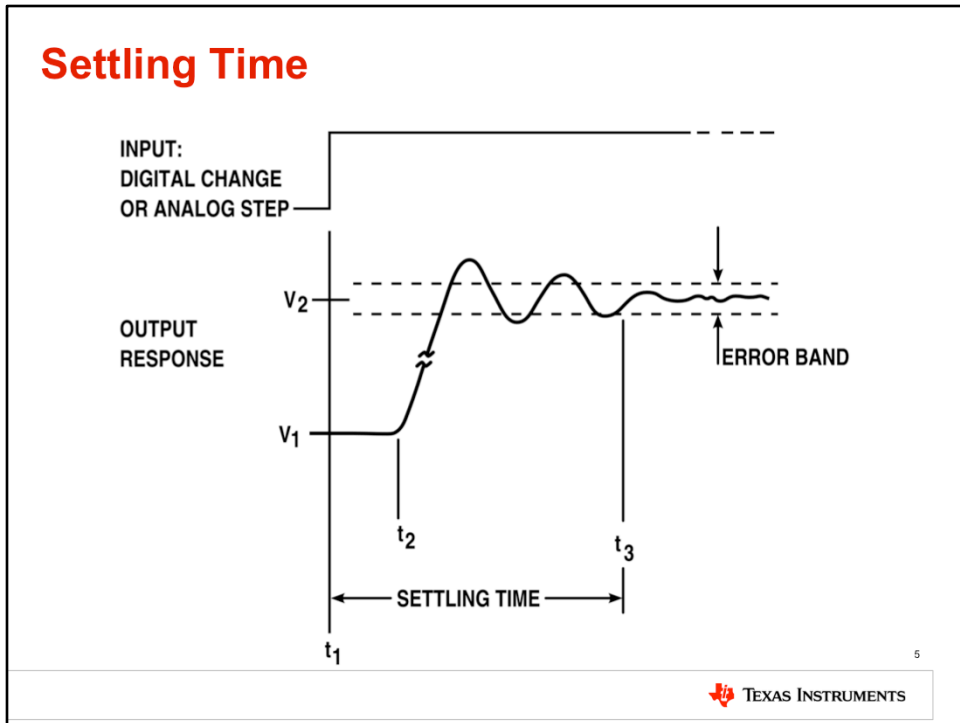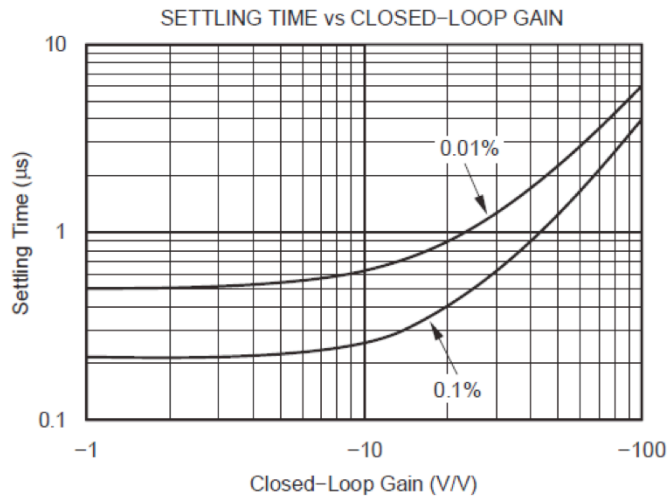
Settling Time

Let's now move on to discuss settling time.

Settling time is the time required for the amplifier's output to reach and stay within a certain error band after a large-signal step is applied to the input. The error band can either be specified in terms of percentage or number of LSBs (for an ADC with a specified number of bits).

Because the input is a large-signal step, the amplifier is in slew rate limit. The tighter the error band is (i.e. smaller error percentage), the longer the settling time will be. Capacitance, closed loop gain, and loading will also effect settling time.
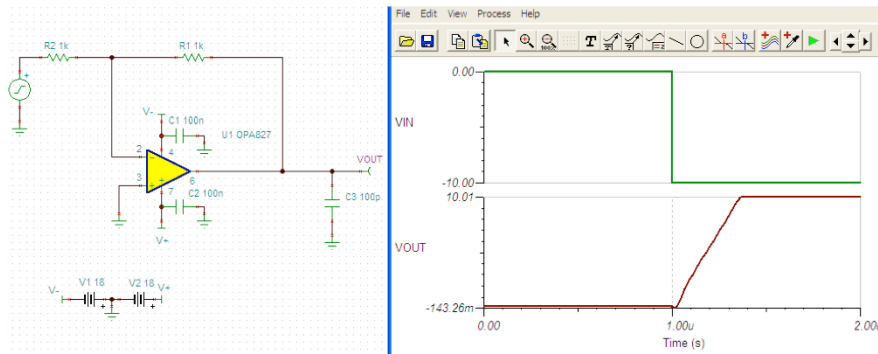
Settling Time vs. Closed-loop Gain

In many op-amp data sheets, the settling time vs. closed-loop gain is given as a plot such as the one shown here. Again, settling time is longer for a tight error band (for example, 0.01% compared to 0.1%). This should make intuitive sense.

Settling time also increases as gain increases. This is because the op-amp's loop gain decreases as closed loop gain increases. Remember, loop gain, or the difference between open-loop gain and closed-loop gain, is what's used by the op-amp to correct for errors. Having less loop gain makes it more difficult for the op-amp to settle quickly.

Simulating Settling Time – OPA827

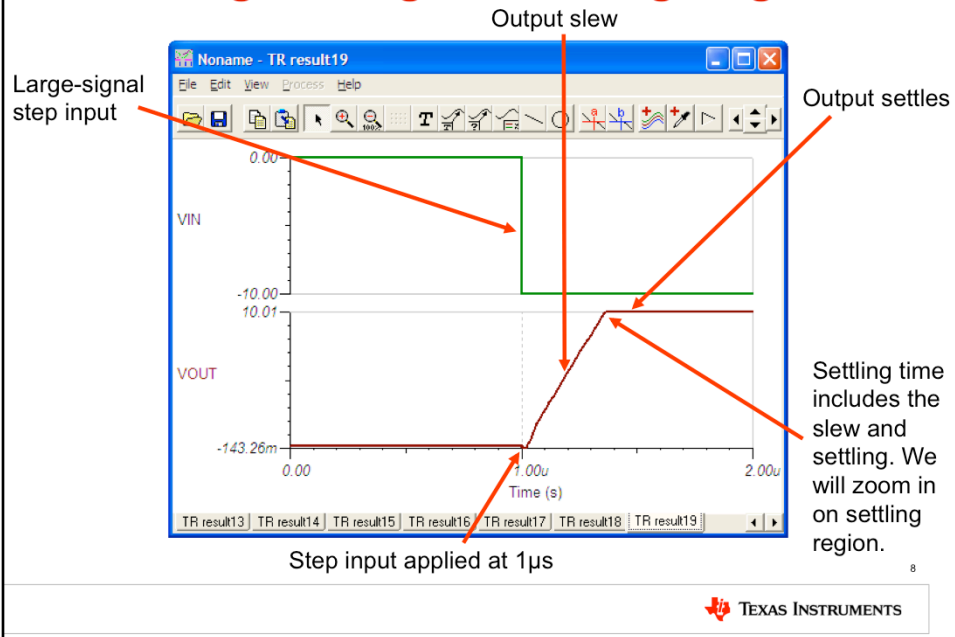| FREQUENCY RESPONSE					
Gain-Bandwidth Product	GBW	G = +1		22	MHz
Slew Rate	SR	G = −1	20	28	V/μs
Settling Time, ±0.01%	t_S	10V Step, G = −1, C_L = 100pF		550	ns

We can very easily simulate the settling time of an op-amp using TINA-TI's transient analysis function. In order to do this, it is important to closely follow the data sheet test conditions, such as the step size, gain configuration, and load capacitance.

In this case we are testing the OPA827 in a gain of -1, with a 10V step input and 100pF of load capacitance.

Simulating Settling Time – Large-signal

Output slew

Large-signal step input

Output settles

Noname - TR result19

File Edit View Process Help

VIN

0.00

-10.00

VOUT

10.01

-143.26m

0.00   1.00u   2.00u

Time (s)

Settling time includes the slew and settling. We will zoom in on settling region.

TR result13 | TR result14 | TR result15 | TR result16 | TR result17 | TR result18 | TR result19

Step input applied at 1µs

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Let's take a closer look at the transient analysis of the OPA827 settling. Please note that settling time includes both the time required for the output to slew as well as the time to settle within the specified error band. The time required to settle within of the error band (where we see the overshoot and damping oscillations) is difficult to see on this plot due to the time scale, so we will zoom in on the error band region on the next few slides.

Before we zoom in on the settling region though, let's first set up a representation of the error bands for easy visual analysis. This can be done using the TINA's post-processor function by adding horizontal lines for the V_{OUT} values at ±0.01% of the ideal. Since the ideal value is 10V, our error band values are 9.999V and 10.001V.

The settling behavior, with some overshoot and damped oscillations, can really be seen once we zoom in on the plot. In this example, the output settles after an over shoot and one cycle of ringing, for a total settling time of 400ns. This is acceptably close to the typical data sheet value of 550ns.

Small-signal Step Response
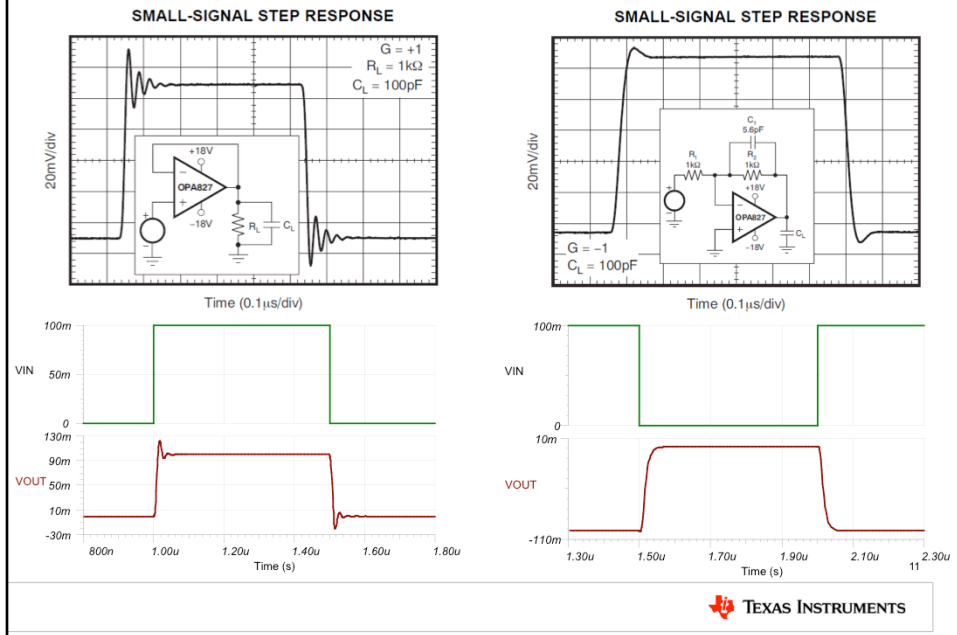
In our discussion of slew rate so far we've been dealing with large input signals, often having amplitudes of 1V or more.

Let's now take a look at an op-amp's behavior with a small-signal step response at the input, where the amplitude is 100mV or smaller. The key difference that I'll show in the next few slides is that, unlike a large-signal step input, a small-signal step input does not put the op-amp into slew rate limit.

Simulation Configuration – Small-signal
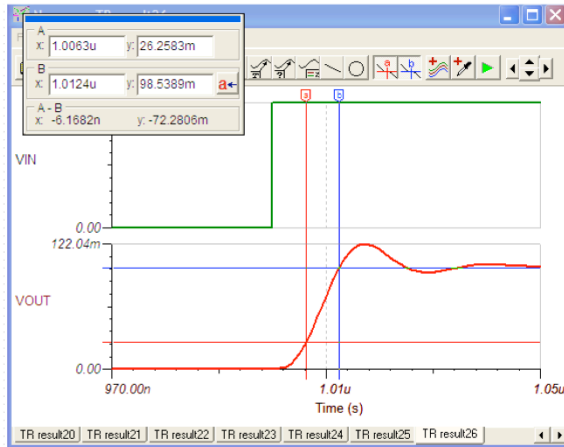
Zoom in on rising Edge
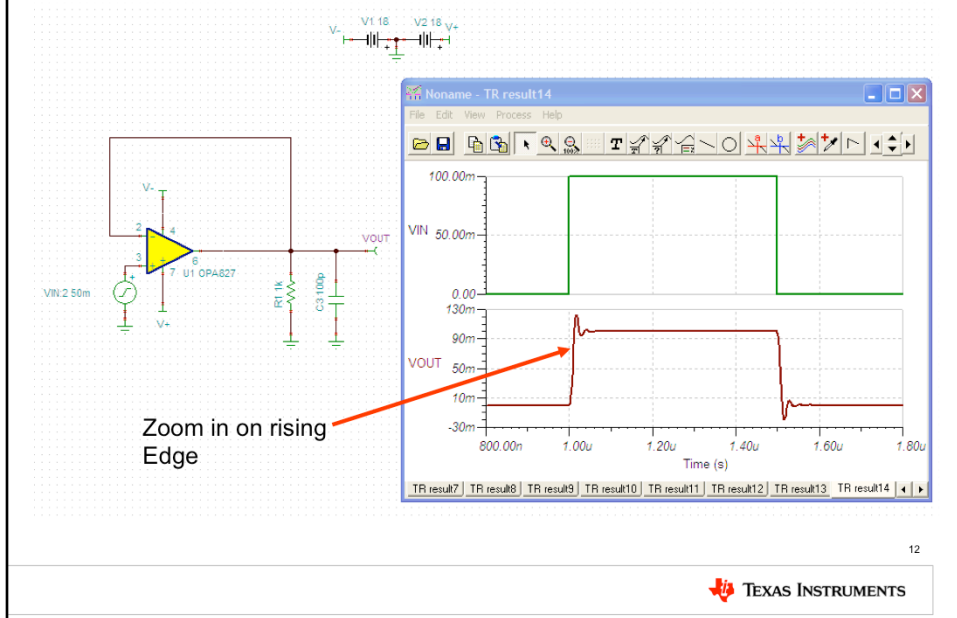
As with large-signal input steps, we can simulate the small-signal rise time of an op-amp using TINA. Here we show the simulation results for the OPA827 with a 100mV step. In the next slide we will zoom in on the rising edge so that we can accurately measure the small-signal rise time.

Simulating Settling Time – Small-signal

Rate of change of output:

- ΔV/ Δt = 72.3mV / 6.17ns
- ΔV/ Δt = 11.7V/μs
- Data sheet = 28V/μs

This is what you would expect with a real device! A small signal step will **not** put the amplifier into slew limit.

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This slide zooms in on the rising edge of the small signal step response. In this example we are computing the rise time in V/μs for comparison to the large-signal slew rate. Measuring delta V over delta T from 10% to 90% of the output swing, me get a rise time of 11.7V/μs. Compare this to the data sheet slew rate value of 28V/μs – they're quite different! Since the small-signal step input doesn't actually put the op-amp in a slew rate limit condition, the rise time does not match up with the slew rate spec.

Where does the difference in these rise times come from?

Well, as you may remember from the first slew rate video, a large-signal step input puts an op-amp in slew limit and therefore forces it outside of its normal linear operation. A small-signal step input, on the other hand, allows the op-amp to operate in its linear region and therefore the rise time is based on the op-amp's bandwidth. We can support this claim using some simple algebra.

First, let's start with the standard definition of rise time as the time required for the amplifier output voltage to move from 10% to 90% of it's ideal value. Next, we assume that the op-amp's output behavior is essentially just a capacitor charging up (known as the first order response). That allows to write an equation for V_{OUT} based on the standard charging capacitor equation. We ultimately want to solve for time, so we can say that at the times we're interested in, Vout is equal to 10% and 90% of Vfinal. We can now solve these two equations for time and substitute them back into the original rise time definition, resulting in the equation: $t_R = 2.19 \cdot tau$.

Small-signal Step Rise Time

$$f_c = \frac{1}{2\pi \cdot R \cdot C} \quad \text{and} \quad \tau_c = R \cdot C$$

$$f_c = \frac{1}{2\pi \, \tau_c} \qquad \text{(2) Closed loop bandwidth relationship with RC time constant}$$

$$f_c = \frac{1}{2\pi \left(\dfrac{t_r}{2.19} \right)} \qquad \text{Substitute 1 into 2}$$

$$t_r = \frac{0.35}{f_c} \qquad \text{Rise time relationship to closed loop bandwidth}$$

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Continuing the derivation, we recall that the f_C, or cutoff frequency of the amplifier's closed-loop bandwidth, is equal to 1/(2*pi*RC). Well, tau = RC, so we can substitute that in. Plugging in our result from the previous page that t_R= 2.19*tau, we can now solve for t_R and ultimately conclude that the small-signal step rise time is equal to 0.35/(f_c).

Calculation vs. Simulation

$$t_r := \frac{0.35}{2\text{MHz}} = 175 \times 10^{-9}\ s$$

simulated $=$ 138ns
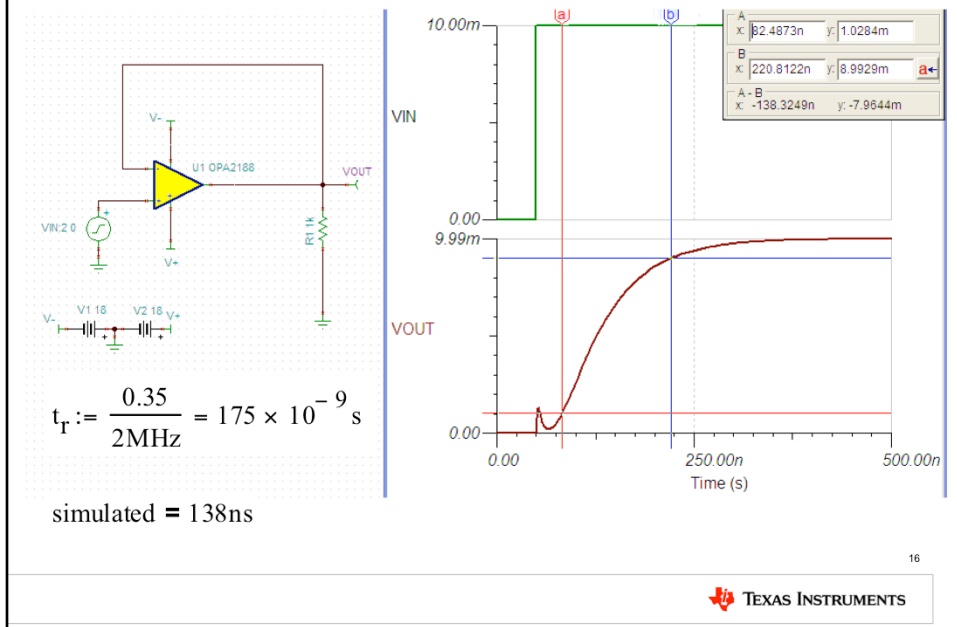
Let's test this result against simulation data. Looking at the OPA2188 data sheet, we see that the op-amp has a gain bandwidth of 2 MHz. Our equation from the last slide gives us a calculated rise time of 175ns. The simulation results in a rise time of 138ns, which is an error of about 20%. This is decent enough for our approximation, since the real op-amp is not just a first-order system (which we assumed to simplify the derivation) and the simulation model has limits on its overall accuracy.
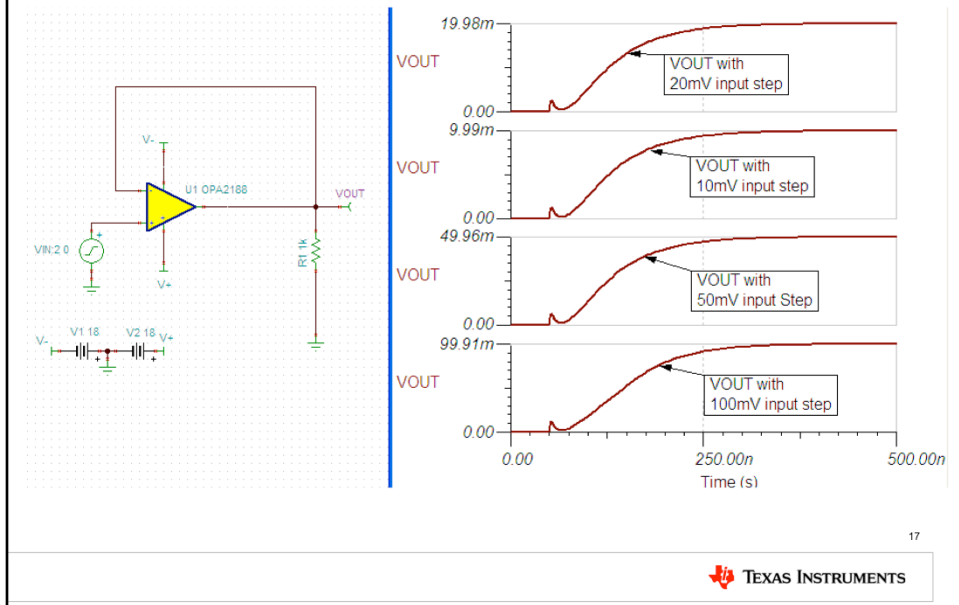
An interesting point to make is that our small-signal rise time equation is that the only variable is the amplifier's bandwidth. This implies that the rise time of a small-signal step is independent of the step amplitude. Of course, the amplitude must not exceed 100mV or the input is no longer considered small-signal.

Of course, we can test this in simulation, which was done by measuring rise time with different input step amplitudes from 10mV to 100mV. As you can see, the rise time for each case is the same!

Rise Time vs. Step Size – Large-signal
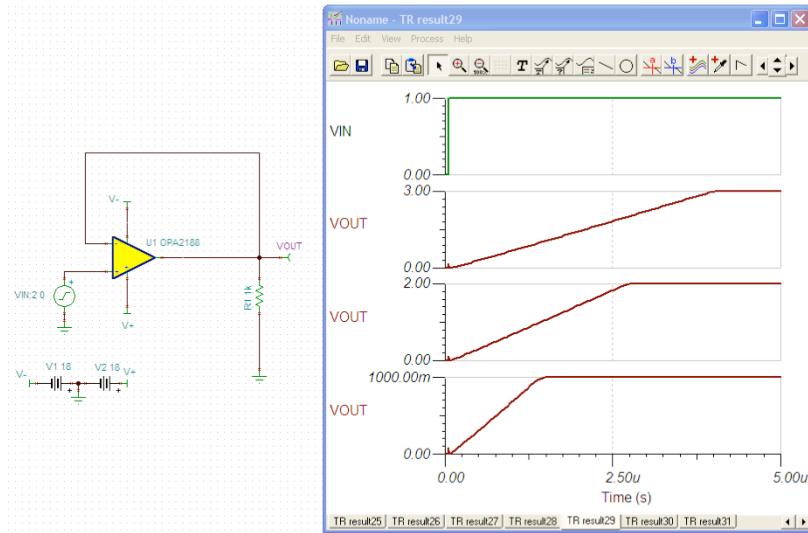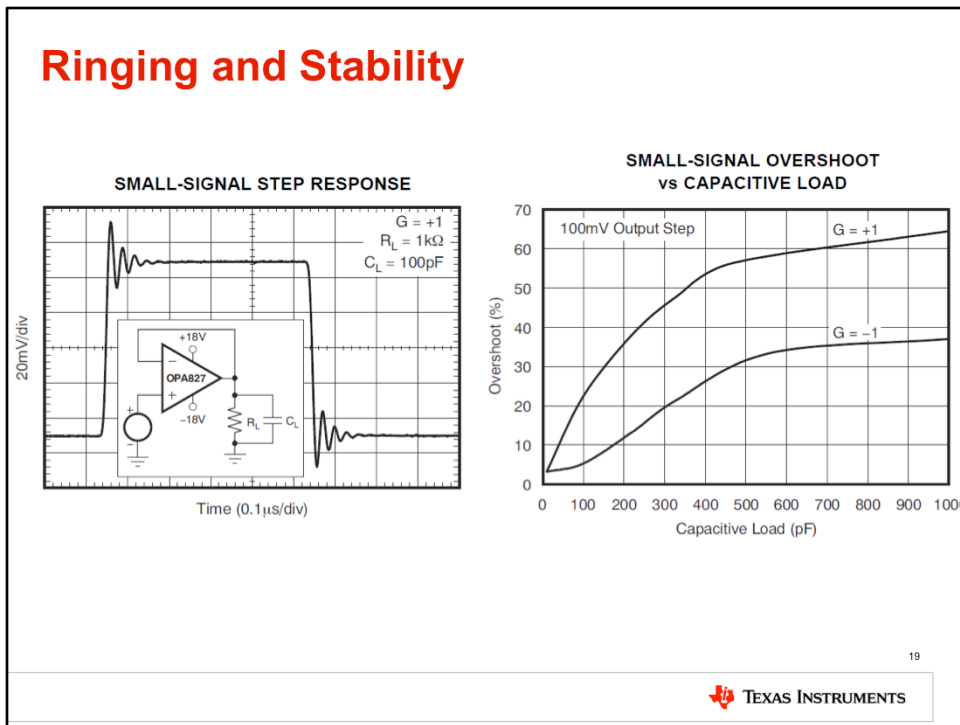
However, for a large-signal step the rise time **is** dependent on the input step size. This is because the op-amp is in its slew rate-limited operation and can only change its output voltage at a fixed rate. In this example, the slew rate is equal to 0.8V/µs, and we can see that the rise times increase as the input step size increases.

Ringing and Stability

SMALL-SIGNAL STEP RESPONSE

G = +1
R_L = 1kΩ
C_L = 100pF

+18V

OPA827

−18V

R_L C_L

20mV/div

Time (0.1µs/div)

**SMALL-SIGNAL OVERSHOOT
vs CAPACITIVE LOAD**

100mV Output Step

G = +1

G = −1

Overshoot (%)

Capacitive Load (pF)

19

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The small signal step response can be used to judge the stability of the system. In general, any second or third order system response, such as an op-amp, can be tested for stability by applying a square wave at the input and observing the output behavior.

In the case of the op-amp, care must be taken to ensure that the op-amp is linearly amplifying the signal. This means that a large-signal input step cannot be used, since the op-amp will be in slew limit and will not be operating linearly. Rather, a small-signal input step should be used.

As a general rule, a larger overshoot on the output implies that the op-amp is less stable. In this example using the OPA827, the maximum capacitance for a stable response is 1000pF; this corresponds to a 60% overshoot.
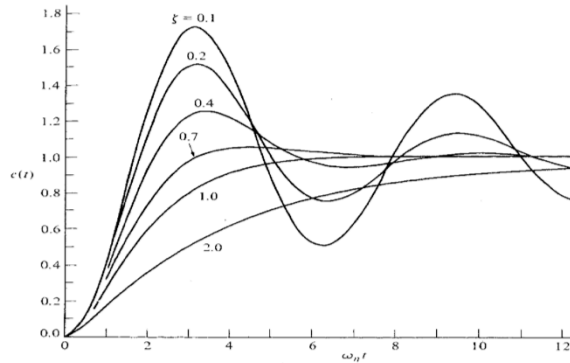
Ringing and Stability

Transfer function for second order system

$$G(s) = \frac{\omega_n^2}{s^2 + 2\zeta \cdot \omega_n + \omega_n^2}$$

Time domain response dampened oscillations

$$c(t) = 1 - \frac{1}{\sqrt{1 - \zeta^2}} \cdot e^{-\zeta \omega_n \cdot t} \cdot \cos\left(\omega_n \cdot \sqrt{1 - \zeta^2} \cdot t - \varphi\right)$$

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This final slide gives a little bit more detail on overshoot and stability, showing equations for the transfer function of a second-order system in both the frequency domain and time domain. Plugging in different values of zeta, or the "damping factor," into the time-domain equation gives the plot on the right which predicts the system's overshoot .

Stability is a deep concept which is covered in depth by later videos, so I won't go into more detail in this module.

Thanks for your time! Please try the quiz.

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That concludes this video – thank you for watching! Please try the quiz to check your understanding of this video's content.

Slew Rate 2

Multiple Choice Quiz

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Quiz: Slew Rate 2

1. The body effect is an example of ___.
a. a secondary effect that changes slew rate.
b. a circuit that boosts slew rate.
c. a stability consideration.
d. None of the above.

2. The body effect is not a problem when _____.
a. common mode voltage changes with the input signal.
b. common mode voltage is held constant.
c. a unity gain buffer is used.
d. None of the above.

3. Settling time is the _____.
a. rise time from 10% to 90% of the waveform.
b. time starting when the input step is applied until the output is within an error guard band.
c. the time from the overshoot peak to the final dampened oscillation.

Quiz: Slew Rate 2

4. Settling time will _____.
a. increase when closed loop gain increases.
b. decrease when closed loop gain increases.
c. remain the same when closed loop gain increases.

5. Is the settling time longer for a 0.1% or 0.01% error band?
a. 0.1%
b. 0.01%

6. In order for a signal to be considered a small signal step, its amplitude must be less then ____.
a. 1V
b. 100mV
c. 10mV
d. 100µV

Quiz: Slew Rate 2

7. Assume a small signal step is applied to the input of an op amp, the rise time of the output signal will be _____.
a. Dependent on slew rate
b. Dependent on bandwidth
c. Dependent on the load resistance.
d. Dependent on bias current.

8. Assume a small signal step is applied to the input of an op amp, the rise time of the output signal will be _____.
a. Dependent on the input signal's amplitude.
b. Independent of the input signal's amplitude.

9. Assume a large signal step is applied to the input of an op amp, the rise time of the output will be ___.
a. Dependent on the input signal's amplitude.
b. Independent of the input signal's amplitude.

TEXAS INSTRUMENTS

Quiz: Slew Rate 2

10. Assume a small signal step is applied to the input of an op amp, overshoot is an indicator of ____.
a. The amplifier's bandwidth.
b. The amplifier's slew rate.
c. The amplifier's settling time.
d. The amplifier's stability

11. Assume a small signal step is applied to the input of an op amp, overshoot and ringing on an amplifier will ____.
a. Increase with increasing capacitive load
b. Decrease with increasing capacitive load.
c. Be unaffected by capacitive load.

12. What is the difference between small signal and large signal step response?
a. Small signal shows the amplifier in slew rate limit and large signal shows linear response.
b. Small signal shows linear response and large signal the amplifier in slew rate limit.

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Slew Rate 2

Multiple Choice Quiz: Solutions

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TEXAS INSTRUMENTS

Quiz: Slew Rate 2

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b. a circuit that boosts slew rate.
c. a stability consideration.
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Quiz: Slew Rate 2

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b. decrease when closed loop gain increases.

c. remain the same when closed loop gain increases.

5. Is the settling time longer for a 0.1% or 0.01% error band?

a. 0.1%

b. 0.01%

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b. 100mV

c. 10mV

d. 100µV

TEXAS INSTRUMENTS

Quiz: Slew Rate 2

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12. What is the difference between small signal and large signal step response?
a. Small signal shows the amplifier in slew rate limit and large signal shows linear response.
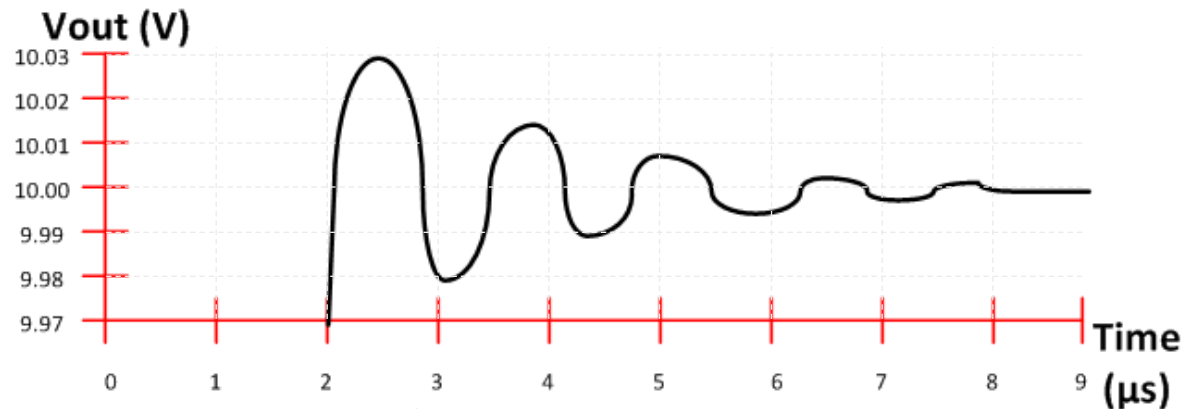b. Small signal shows linear response and large signal the amplifier in slew rate limit.

Slew Rate 2

Exercises

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![Texas Instruments logo] TEXAS INSTRUMENTS
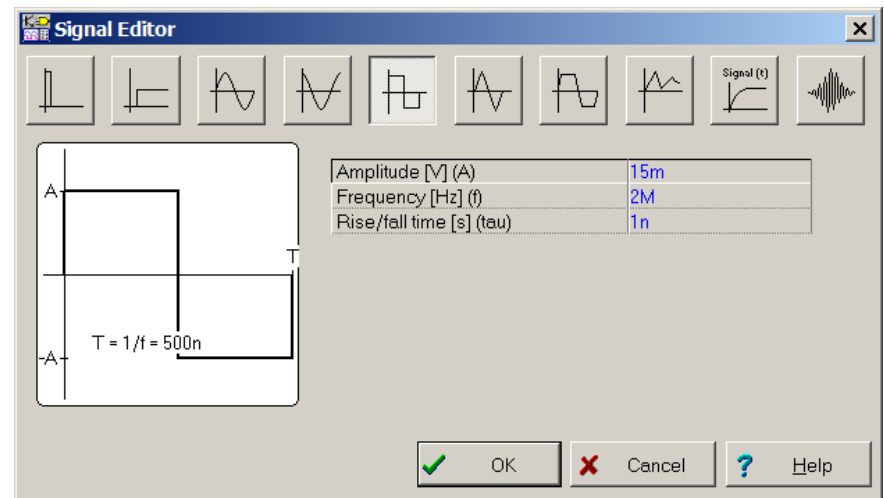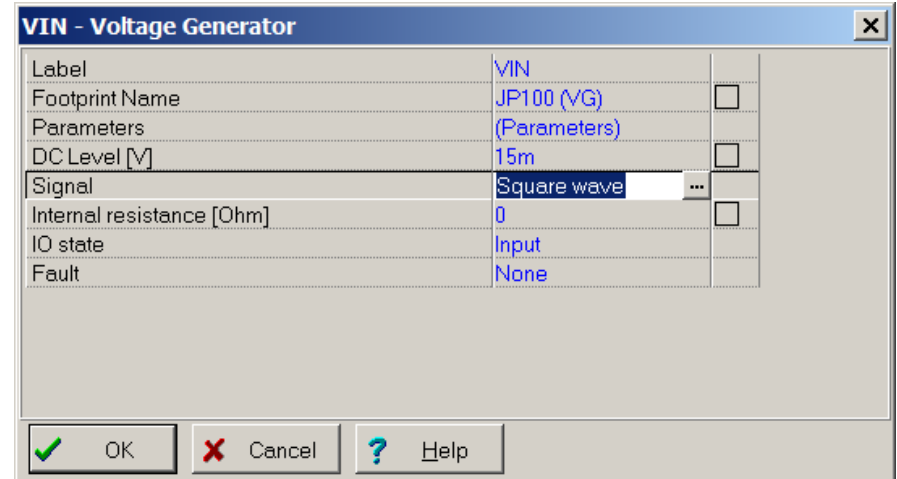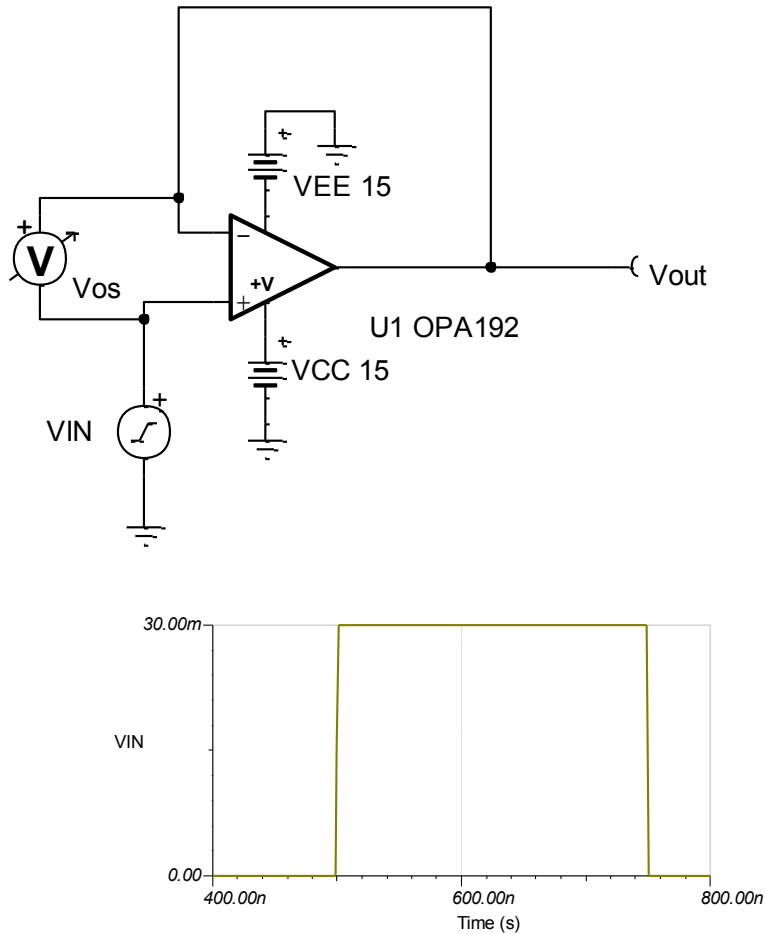
1. The waveforms below show the input step and the output response for an amplifier. The waveform at the top shows zoomed in detail on the output waveform. What is the 0.2%, and 0.1% settling times.

2. Simulate the 0.001% settling time for the circuit below. Why does the output waveform have two different slopes?
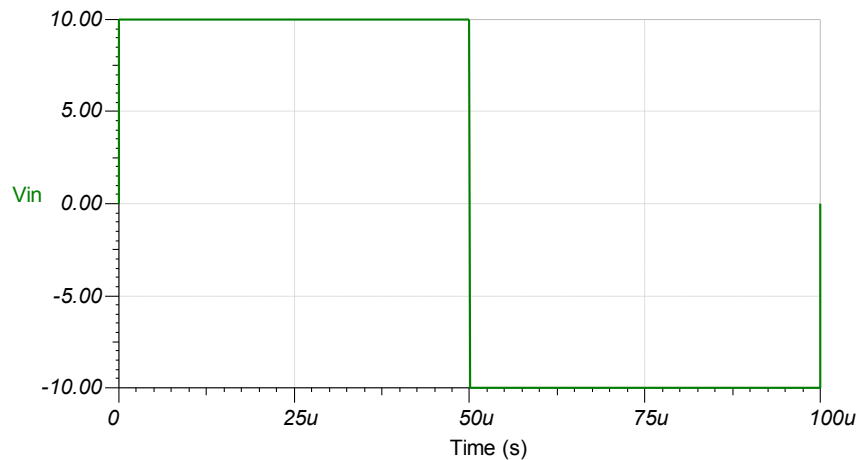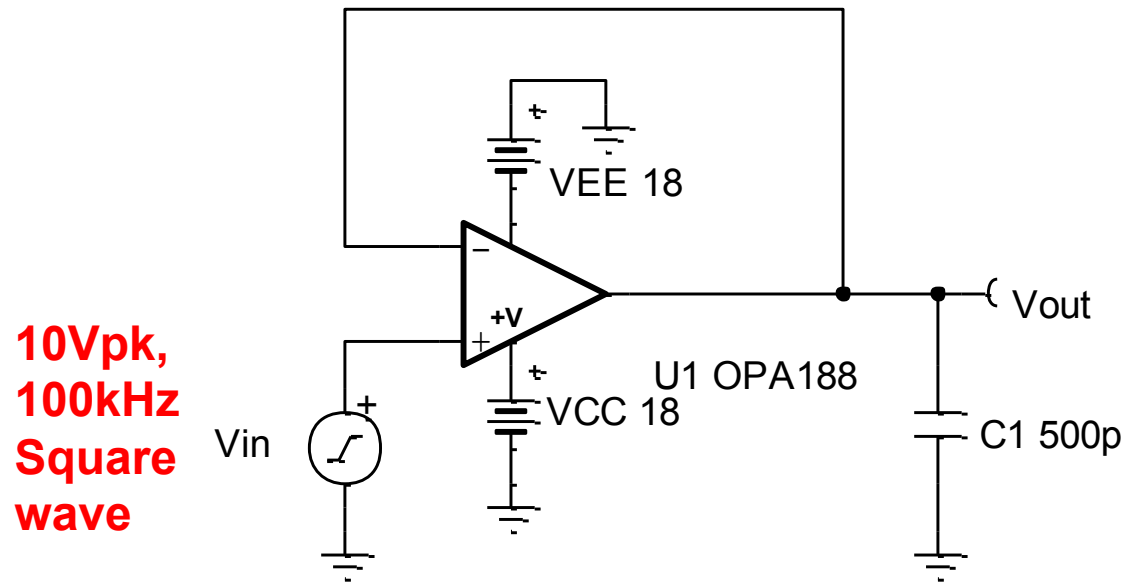
10Vpk, 100kHz Square wave

Vin

VEE 18

+V
−

U1 OPA188

VCC 18

Vout

C1 500p

3. Calculate and simulate the rise time for the circuit below for a 10mV, 20mV, and 30mV input step.

VEE 15

Vos

+v

Vout

U1 OPA192

VCC 15

VIN

VIN - Voltage Generator

Label	VIN
Footprint Name	JP100 (VG)
Parameters	(Parameters)
DC Level [V]	15m
Signal	Square wave
Internal resistance [Ohm]	0
IO state	Input
Fault	None

OK   Cancel   Help

Signal Editor

Amplitude [V] (A)	15m
Frequency [Hz] (f)	2M
Rise/fall time [s] (tau)	1n

A

T

T = 1/f = 500n

-A

OK   Cancel   Help

30.00m

VIN

0.00

400.00n   600.00n   800.00n

Time (s)

4. Calculate and simulate the rise time for the circuit below for a 1V, 2V, and 3V input step. What is the fundamental difference between problem 3 and 4
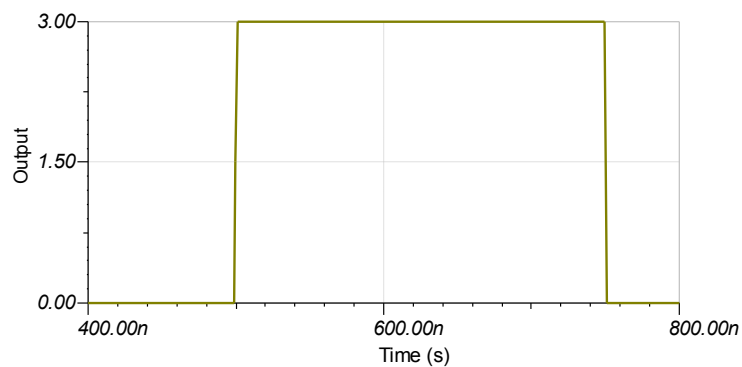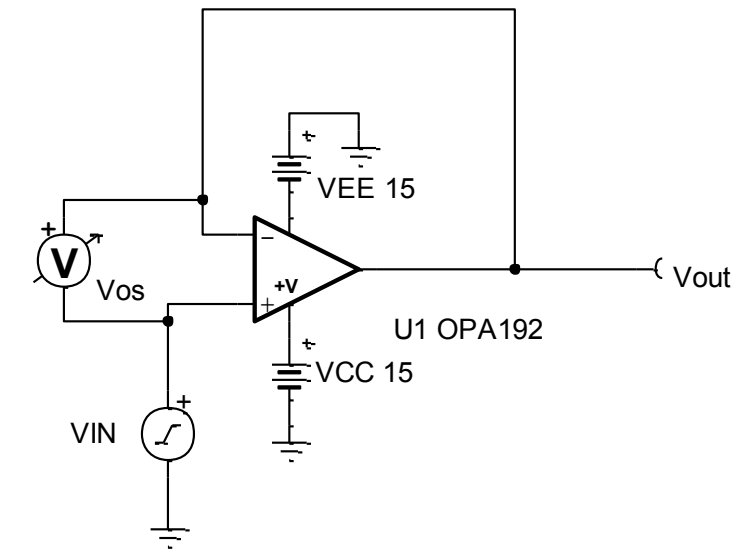
VIN – Voltage Generator

Label	VIN
Footprint Name	JP100 (VG)
Parameters	(Parameters)
DC Level [V]	1.5
Signal	Square wave
Internal resistance [Ohm]	0
IO state	Input
Fault	None

15m

✔ OK   ✘ Cancel   ? Help

Signal Editor

Amplitude [V] (A)	1.5
Frequency [Hz] (f)	2M
Rise/fall time [s] (tau)	1n

T = 1/f = 500n

✔ OK   ✘ Cancel   ? Help

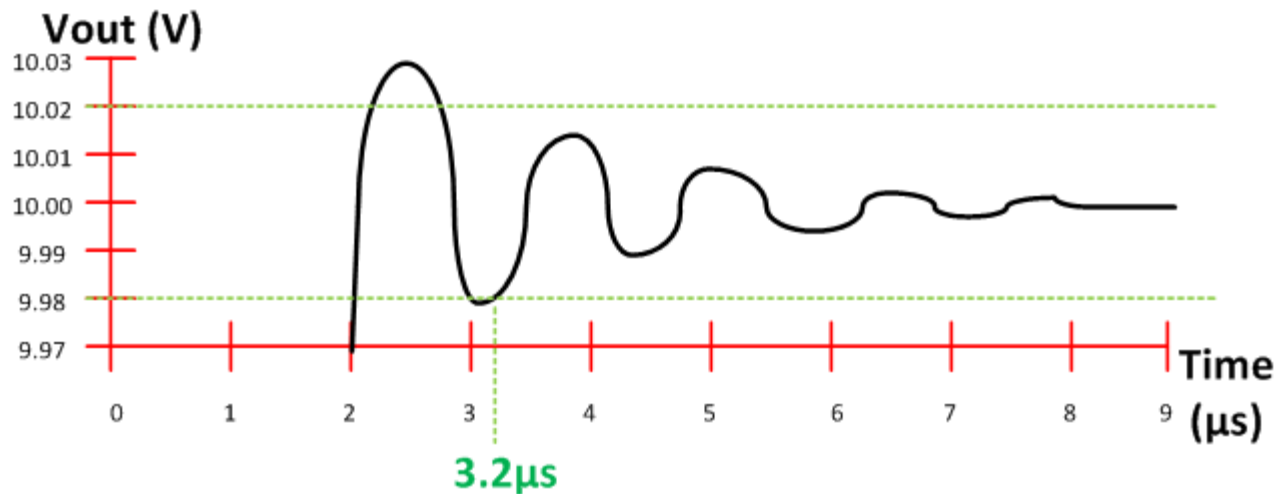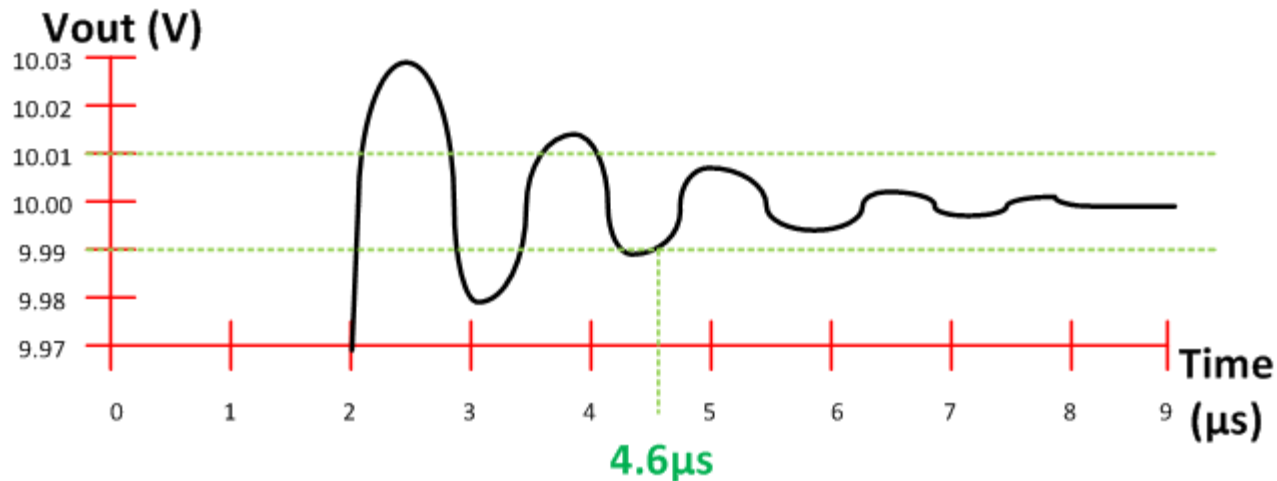U1 OPA192

VEE 15

VCC 15

Vout

Vos

VIN

Slew Rate 2

Solutions

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1. The waveforms below show the input step and the output response for an amplifier. The waveform at the top shows zoomed in detail on the output waveform. What is the 0.2%, and 0.1% settling times. **0.1% settling time is 4.6µS and 0.2% settling time is 3.2µS**
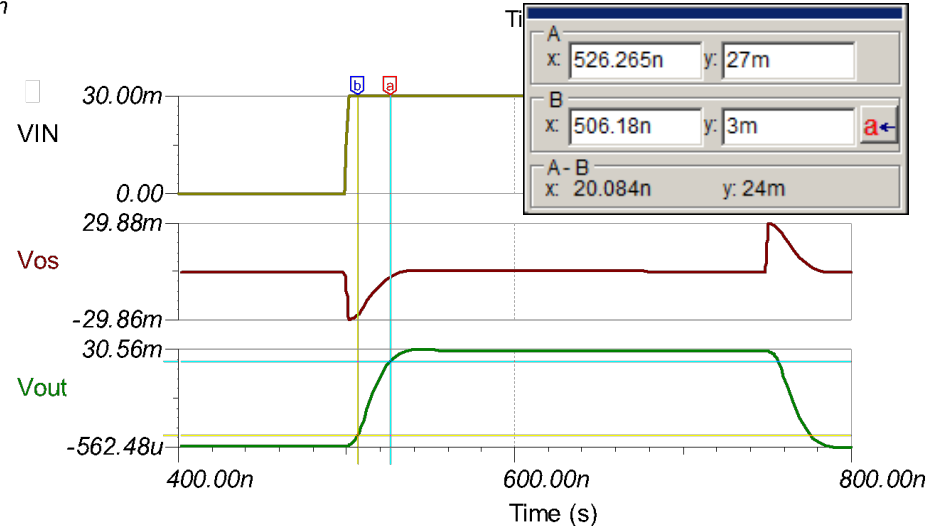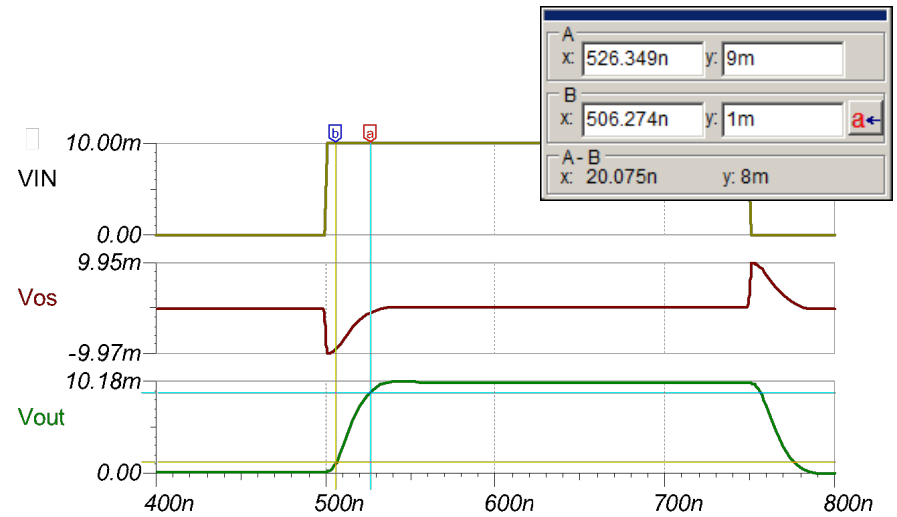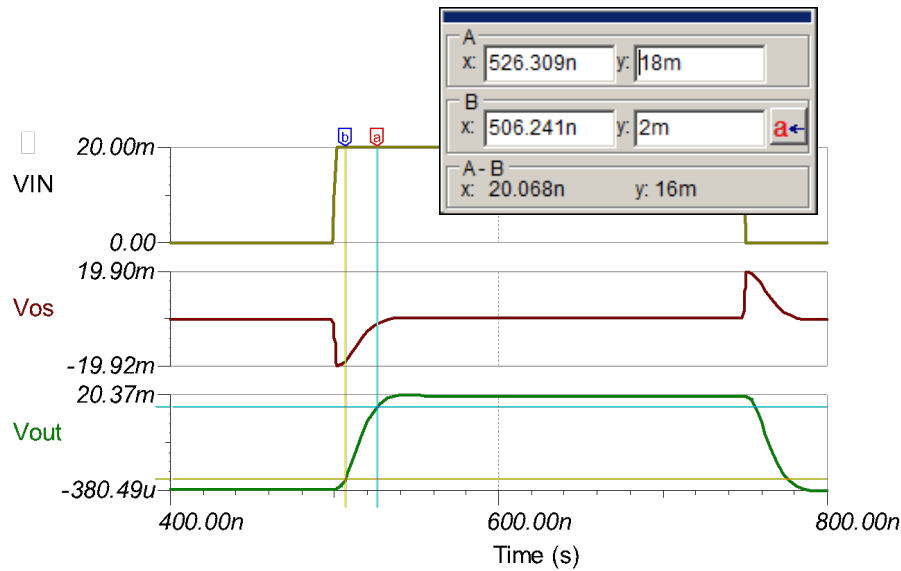
2. Why does the output waveform below have two different slopes?
This amplifier has slew boost. The output rise time reduces as the signal approaches its final value.
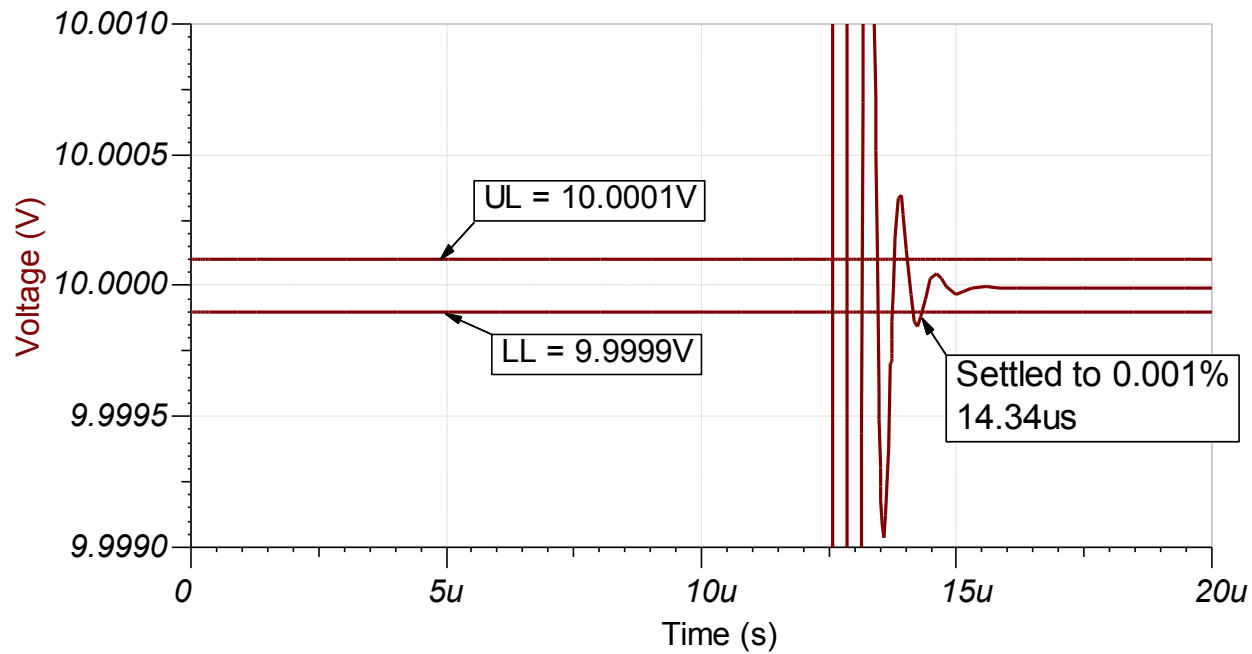
1222-SR 2-Problem 2.TSC

TEXAS INSTRUMENTS

3. Calculate and simulate the rise time for the circuit below for a 10mV, 20mV, and 30mV input step. The rise time is 20ns for each case, calculation results 35ns.

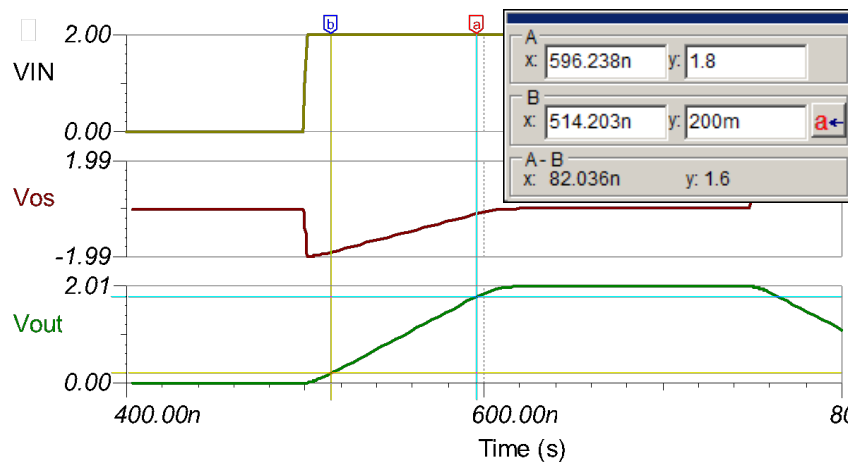**1222-SR 2-Problem 3.TSC**

$$t_r = 0.35/f_c = 35ns$$

GBW	Unity gain bandwidth	10	MHz

TEXAS INSTRUMENTS

4. Calculate and simulate the rise time for the circuit below for a 1V, 2V, and 3V input step. Rise time is 43ns, 82ns, and 122ns. Slew rate is the same in each case (about 20V/µS). What is the fundamental difference between problem 3 and 4? In problem 3 the rise time is constant because it is in small signal response. In problem 4 rise time depends on the output signal's amplitude because it is in slew limit.

$$\frac{1.8V - 0.2V}{0.5962\mu s - 0.5142\mu s} = 19.5 \frac{V}{\mu s}$$

1222-SR 2-Problem 4.TSC

TEXAS INSTRUMENTS