Redefining high resolution and low noise in Delta-Sigma ADC applications

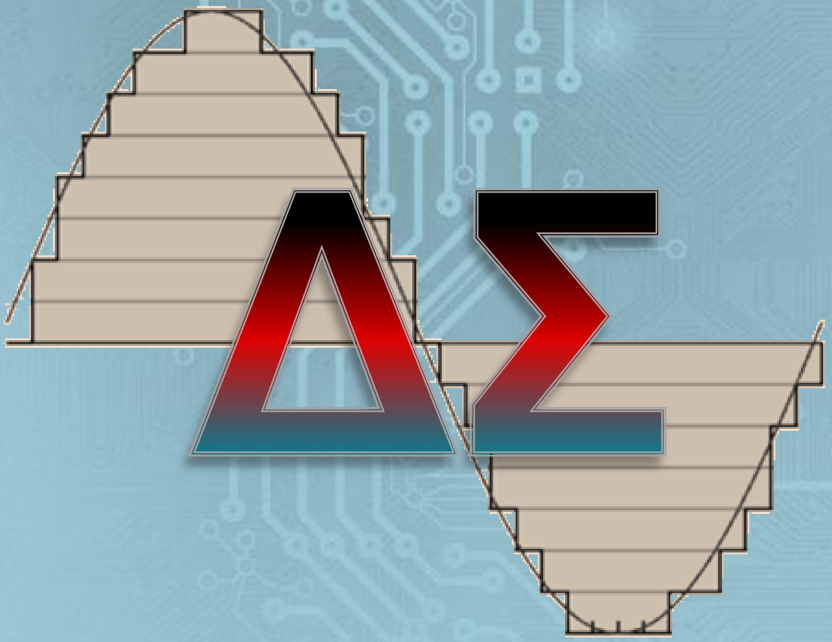
Agenda

Redefining high resolution and low noise in Delta-Sigma ADC applications

- **How do Precision Delta-Sigma (ΔΣ) ADCs work?**
- **Introduction to the ADS1262 & ADS1263**
- **Common Application Circuits using the ADS126xEVM**
  - 3-/4-Wire RTDs
  - 3-/4-Wire RTD Pitfalls
  - Load Cells
  - Load Cell Pitfalls
- **How to use the ADS1262 and ADS1263 monitoring and diagnostic features**
- **Coming Soon… PLC reference design**
- **Additional Information**

Precision Delta-Sigma ADC Basics

Why is this a high resolution, low noise ADC architecture?



First, what do Precision ΔΣ ADCs do?

Temperature Measurement

Vibration / Flow Measurement

Pressure Measurement

Power / Harmonics Measurement

- High resolution + low noise
- Offer wide dynamic range
- Measure slow-moving signals
- Often application-specific

PLC / DCS Systems

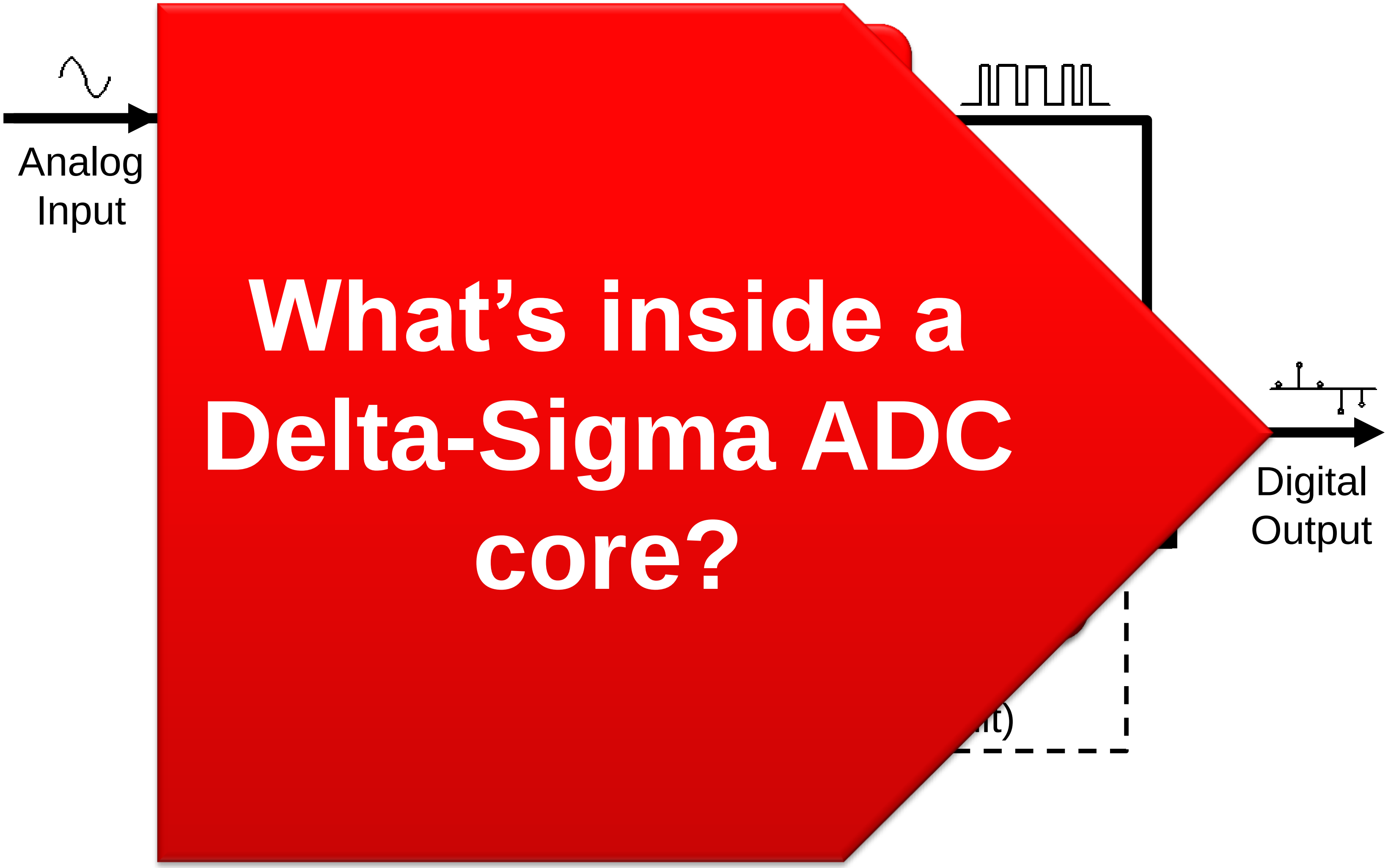
Test & Measurement

Seismic Data Acquisition

Medical

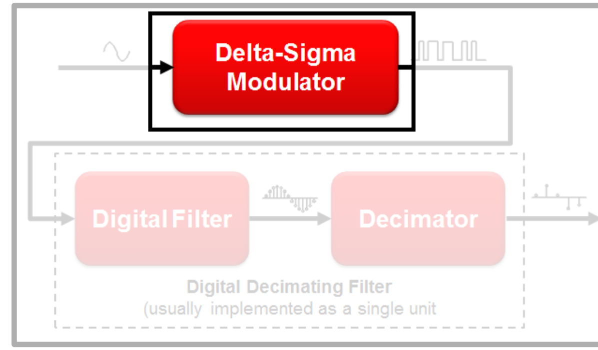
How Do Precision Delta-Sigma ADC's Work?

ADC Architecture Overview

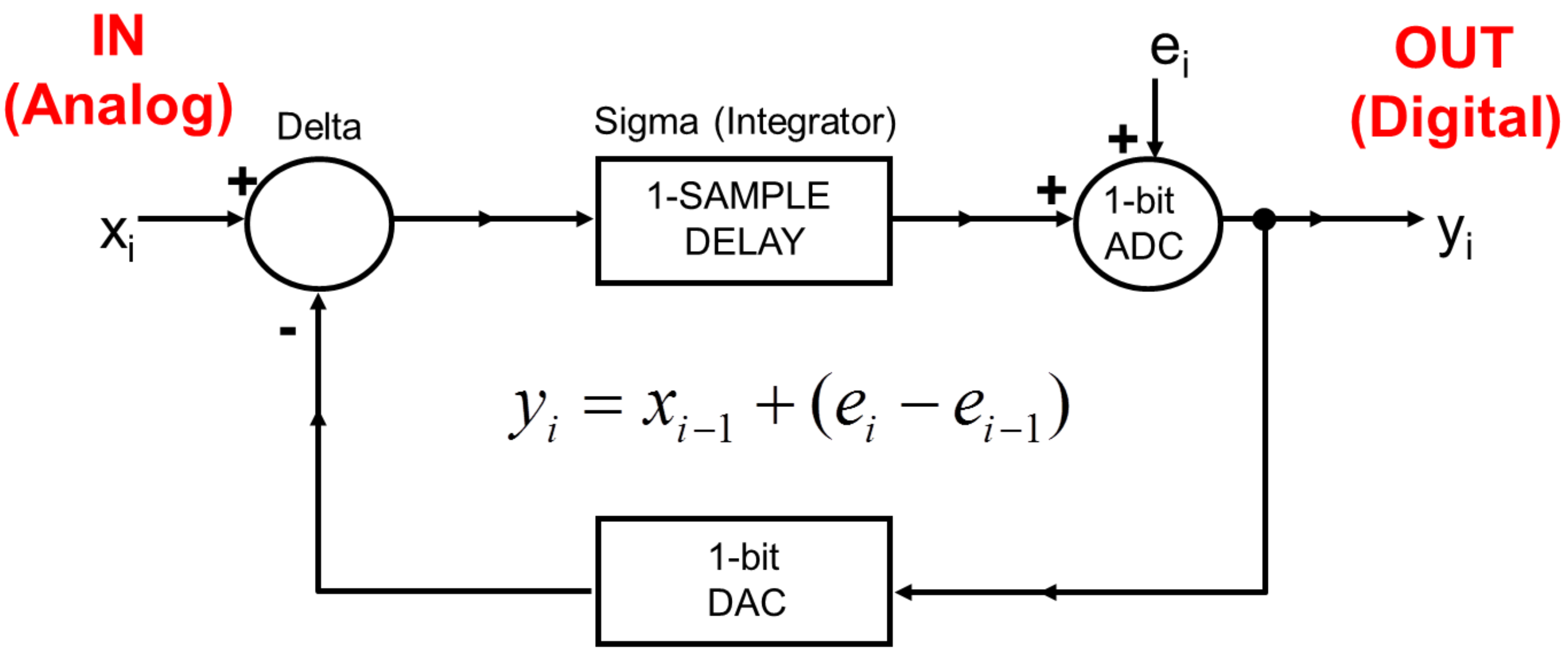


How Do Precision Delta-Sigma ADC's Work?

The Delta-Sigma Modulator – Time Domain



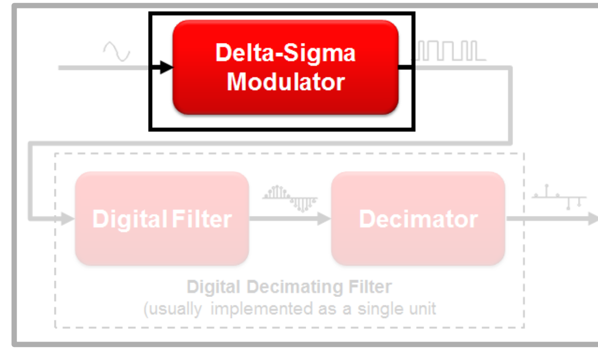
- Digital output is equal to the input plus the quantization noise
- Goal is to minimize error due to quantization noise



$$y_i = x_{i-1} + (e_i - e_{i-1})$$

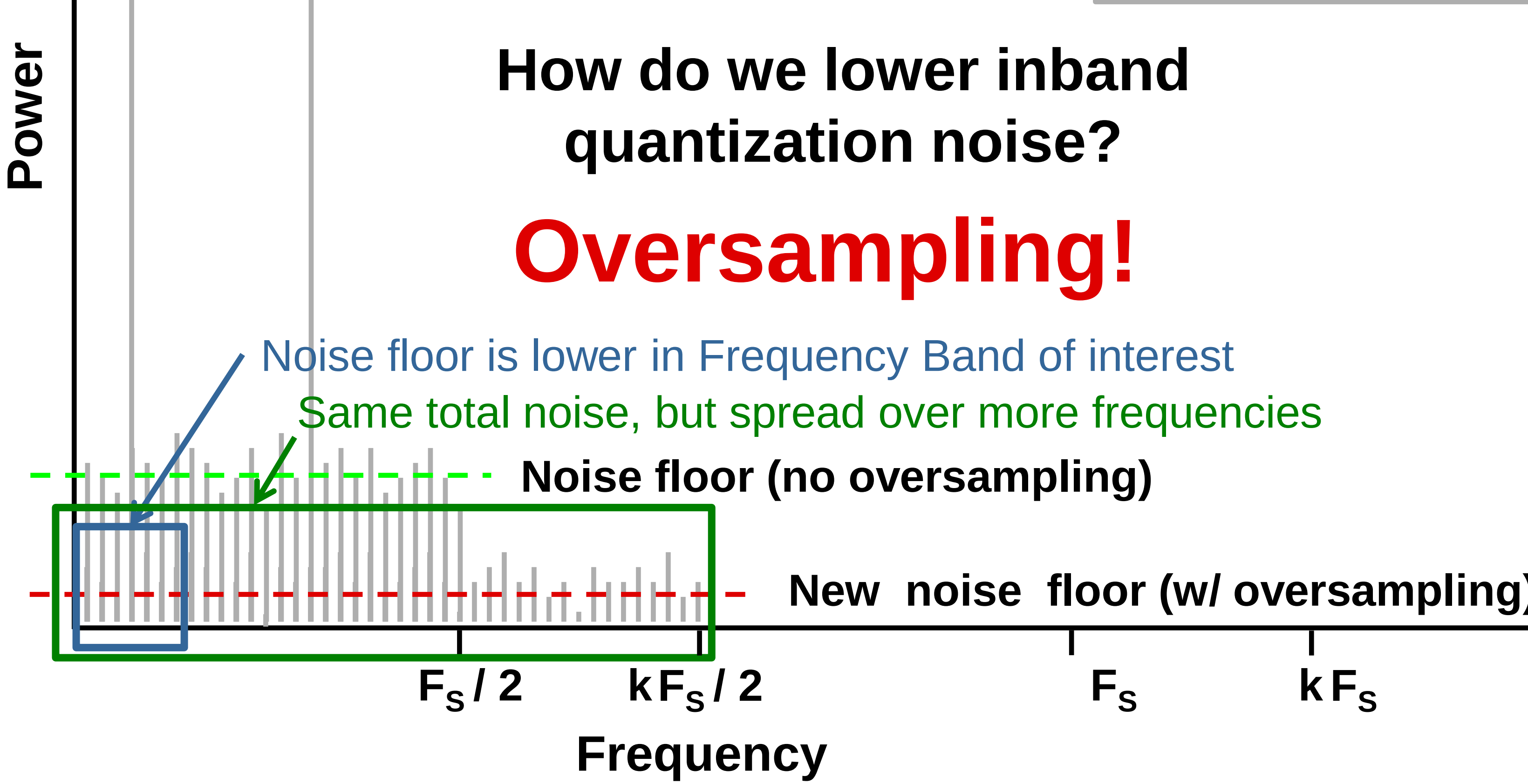
How Do Precision Delta-Sigma ADC's Work?

The Delta-Sigma Modulator – Frequency Domain



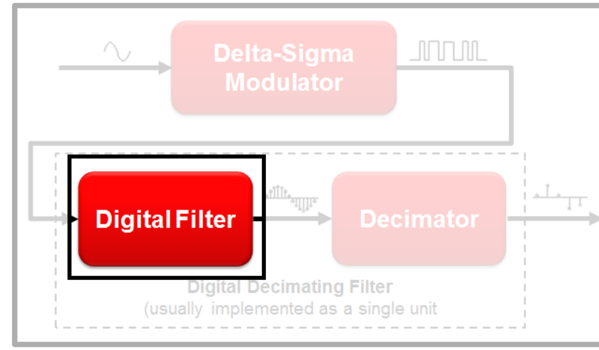
How do we lower inband quantization noise?

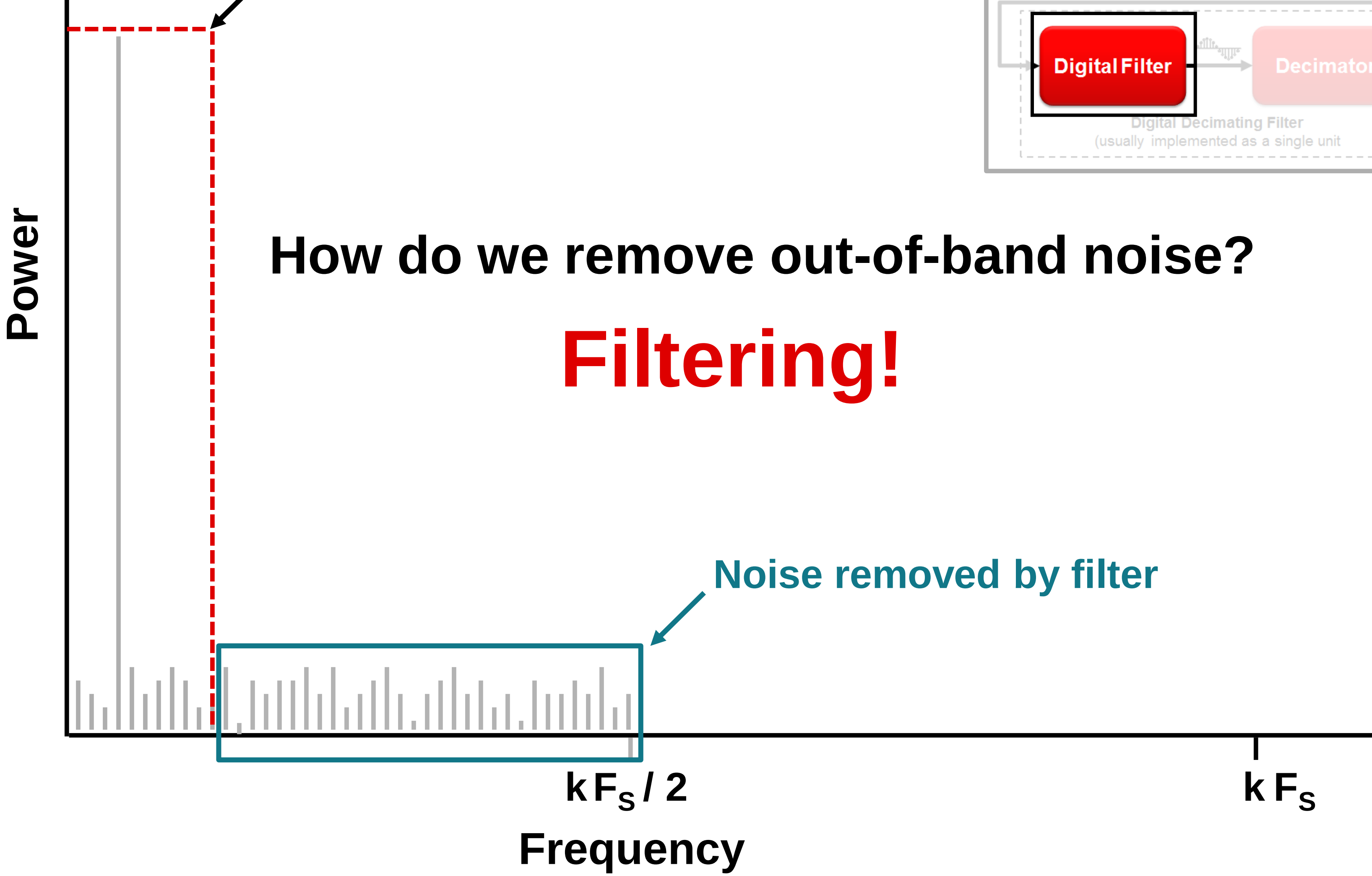
Oversampling!



How Do Precision Delta-Sigma ADC’s Work?

The Digital Filter – Ideal Response



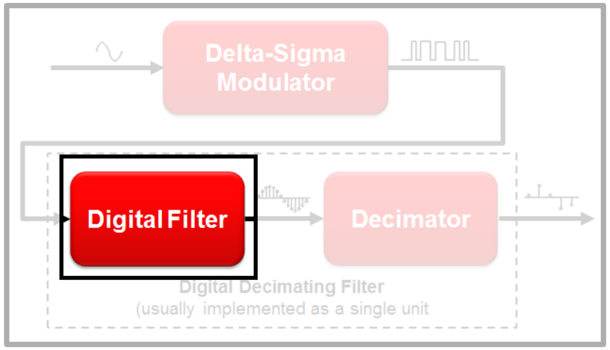


How do we remove out-of-band noise?

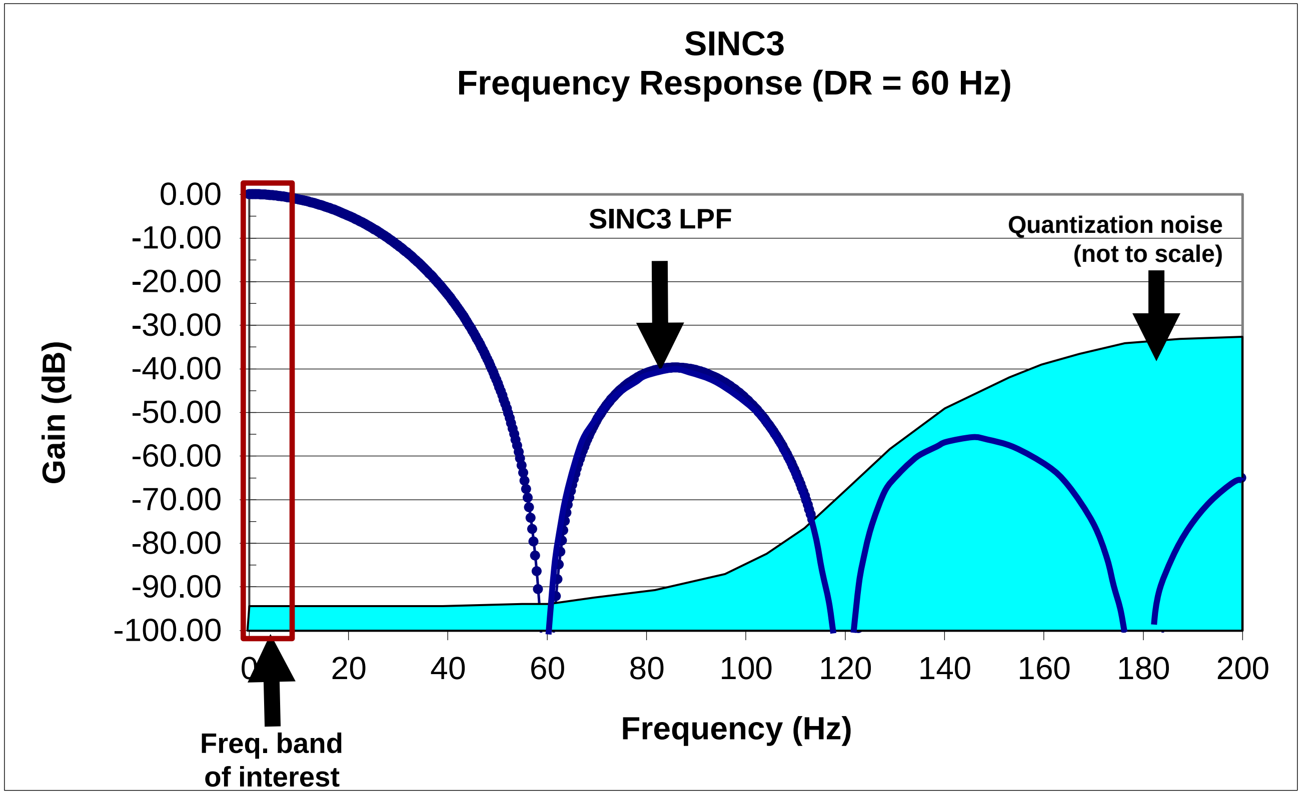
Filtering!

How Do Precision Delta-Sigma ADC's Work?

The Digital Filter – Actual Response

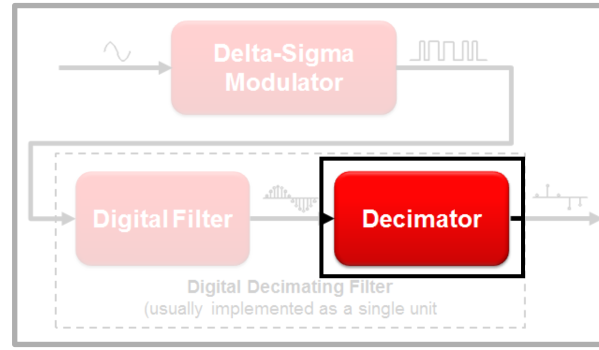


For a real-world SINC^3 filter, the actual response and noise attenuation looks like this:

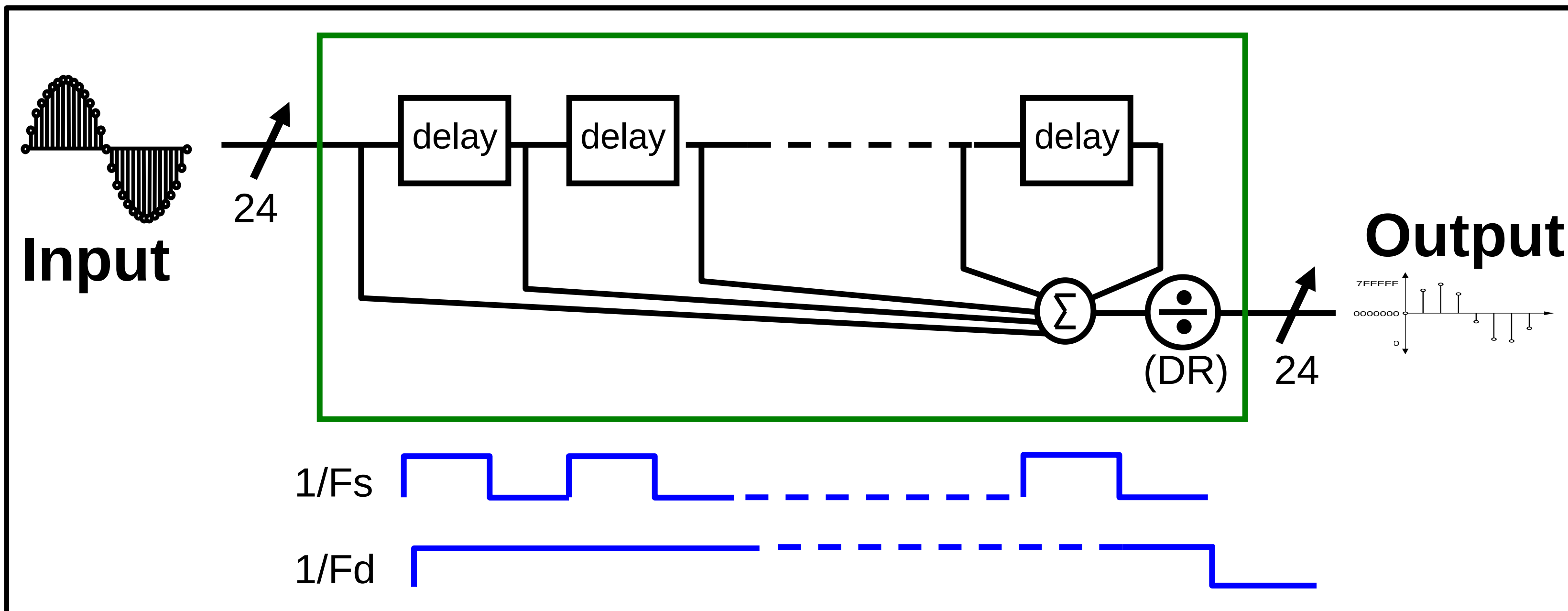


How Do Precision Delta-Sigma ADC's Work?

The Decimator

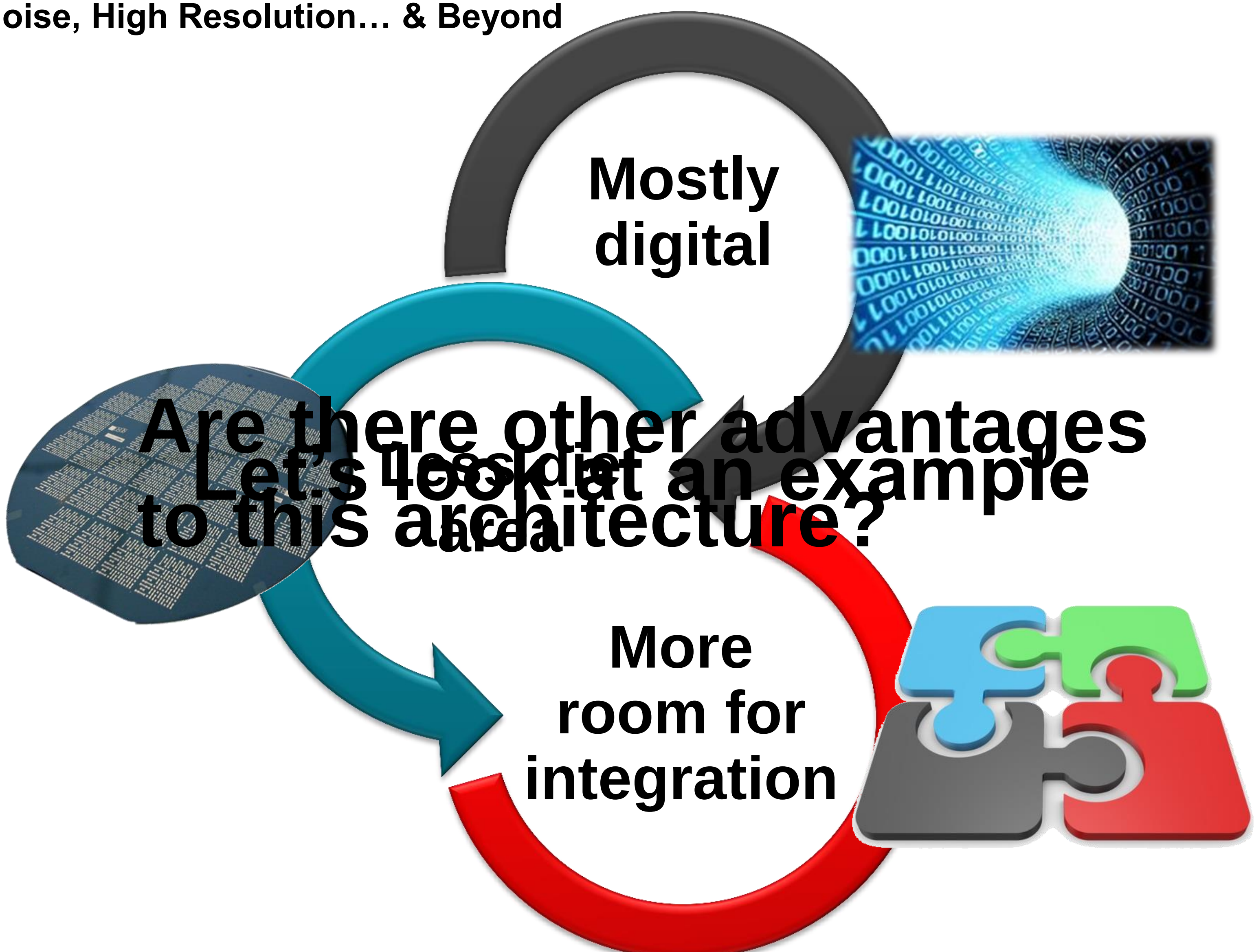


- Decimate the output by averaging several samples
- Often accomplish both filtering & decimation with SINC filter



How Do Precision Delta-Sigma ADC's Work?

Low Noise, High Resolution… & Beyond

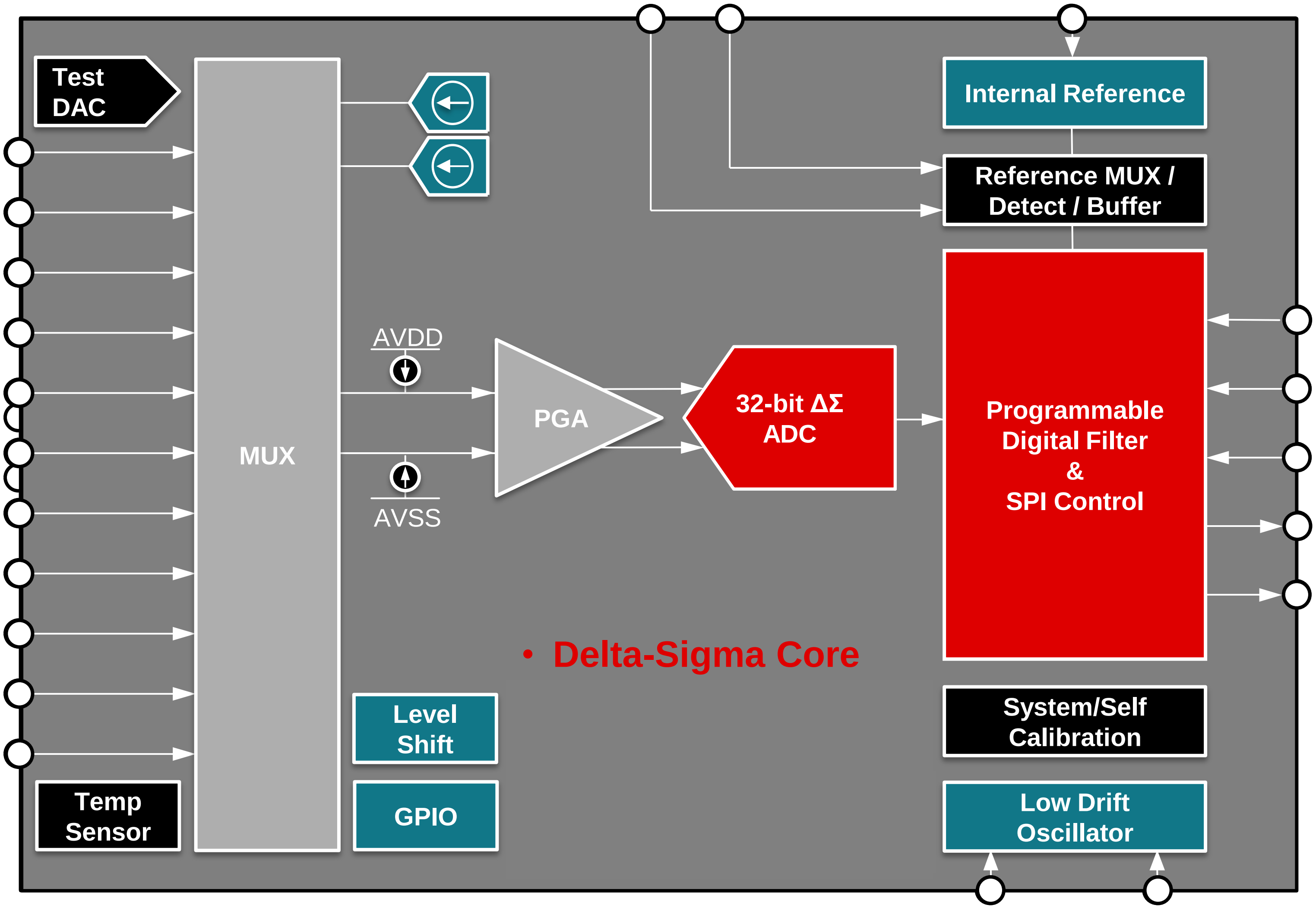


Are there other advantages to this architecture?

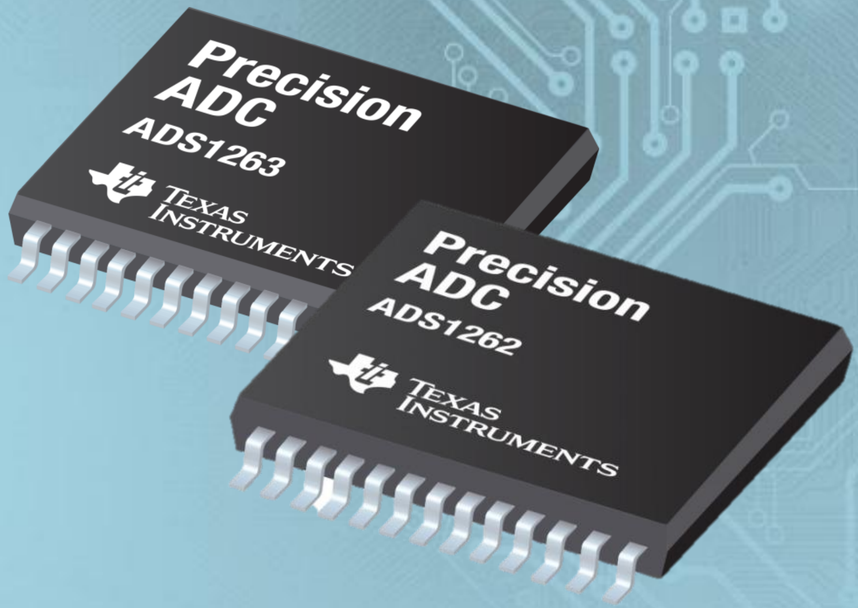
Let's look at an example

How Do Precision Delta-Sigma ADC's Work?

Lots of digital = lots of room for integration!



ADS1262
and
ADS1263



ADS1262/3

Best-in-class Industrial ΔΣ ADC w/ Ultra Low Noise| 32-bit | 10/5 SE/Diff Channels

Features

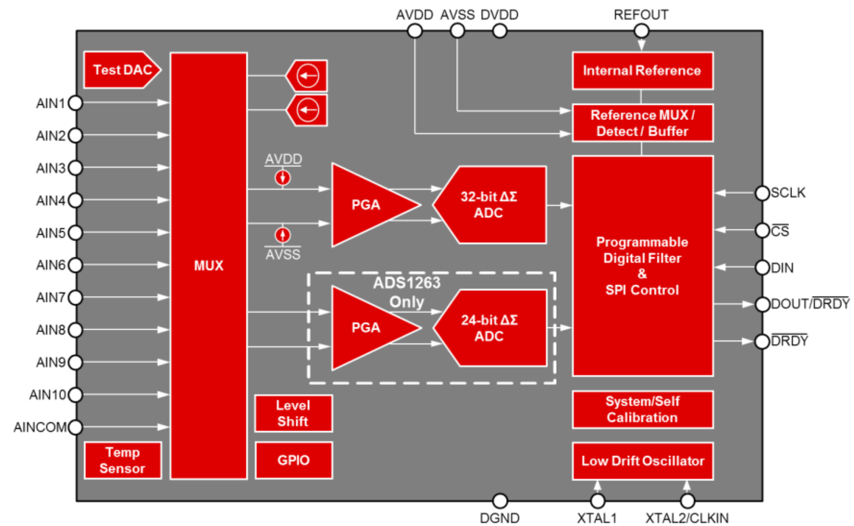
- **Highest Resolution ADC**:
  - **27 bit ENOB, 7nV Noise** (@2.5SPS)
- **11 Flexible, Multiplexed Inputs:**
  - 10 Single-Ended **OR** 5 Differential
- **Highly Specified Performance:**
  - Offset Drift: **1nV/°C**
  - Gain Drift: **0.5ppm/°C**
  - INL: **3ppm**
- **Highly Integrated Device:**
  - Low Drift Internal Reference: **2.5V**
  - GPIOs (8)
  - Internal Clock: **7.3728MHz**
  - High Impedance PGA: **1/2/4/8/16/32**
  - SINC + 50/60Hz Digital Filter
- **Fault Detection/Input Diagnostics**

Applications

- Industrial PLC
- High-End Panel Meters and Process Controllers
- High Precision Weigh Scales
- Industrial Strain Gauge Analyzers
- Analytical Equipment
- RTD Measurement

Benefits

- Wide dynamic range 32-bit ADC enables direct digitization of low level sensors
- High-resolution, low-drift architecture provides the industry's best performing ADC
- A high level of integration eliminates the need for several typical discrete components, decreasing necessary PCB space and reducing costs
- Wide sample rate allows this device to be adaptable to a variety of applications
- On-chip sensor bias current sources make the ADS1262 RTD-ready
- Fault detection improves system reliability

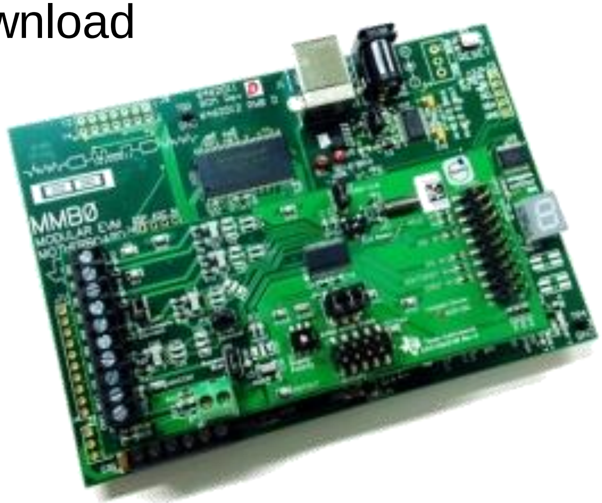


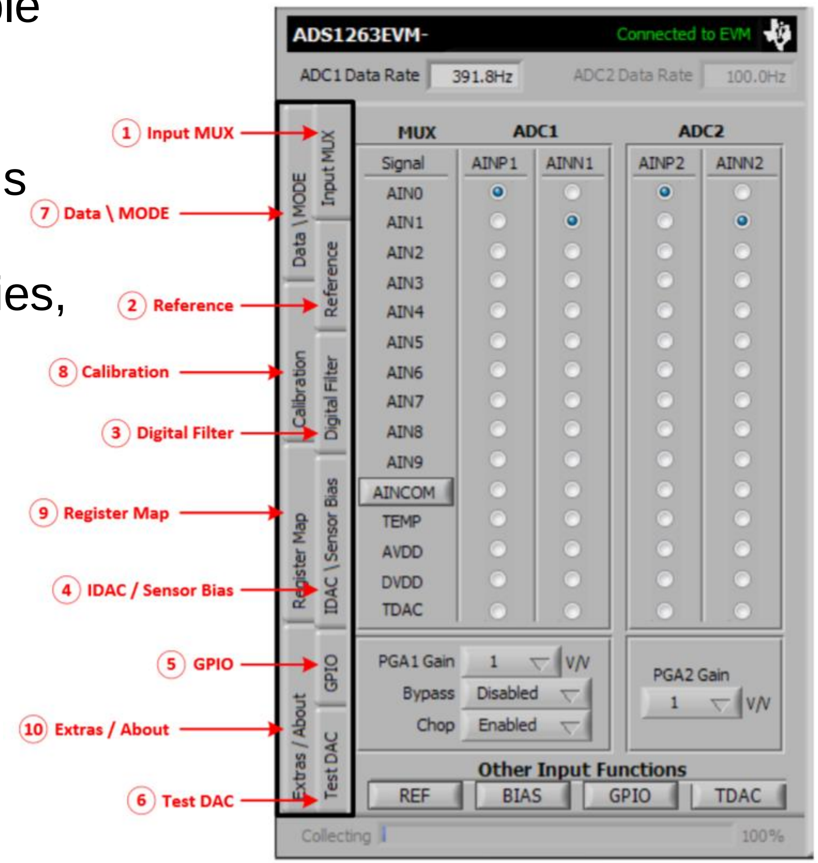
ADS1262/3 – Performance Development Kit

PDK

Performance development kits (PDKs)

- Daughter card, motherboard, USB cable and power supply.
- ADCPro[TM] evaluation software for Microsoft Windows with built-in analysis tools.
- Configurable inputs, references, supplies, and clock sources
- Getting started software available for download



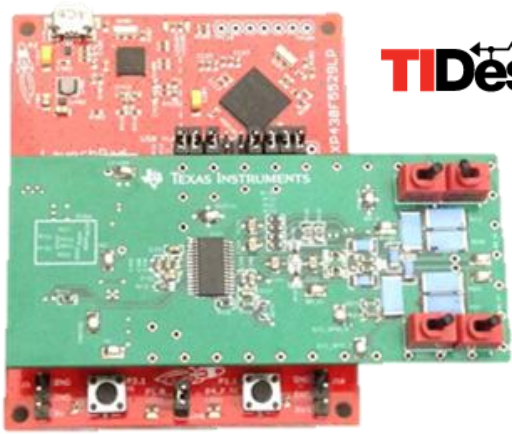


ADS1262/3 – More Tools for Faster Design

Precision Weigh Scale Reference Design | Excel Configuration Calculator

TI Designs reference design for high resolution, low drift, precision weigh scale measurements with AC bridge excitation (TIPD188)

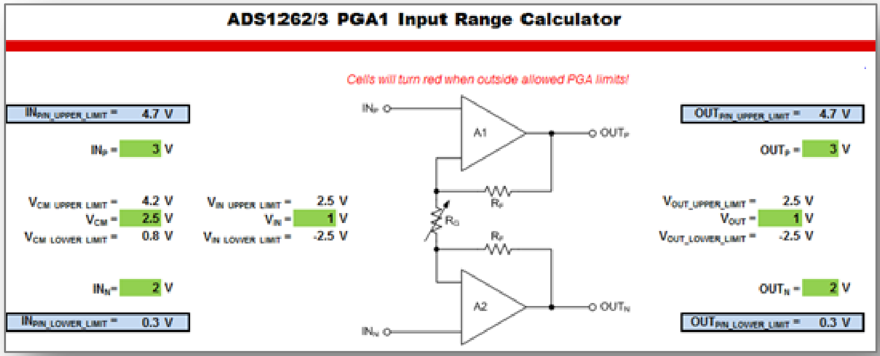
- Improve offset and offset drift performance for bridge measurements
- Accelerates time to market.
- Includes schematics, BOM and design files



TIDesigns

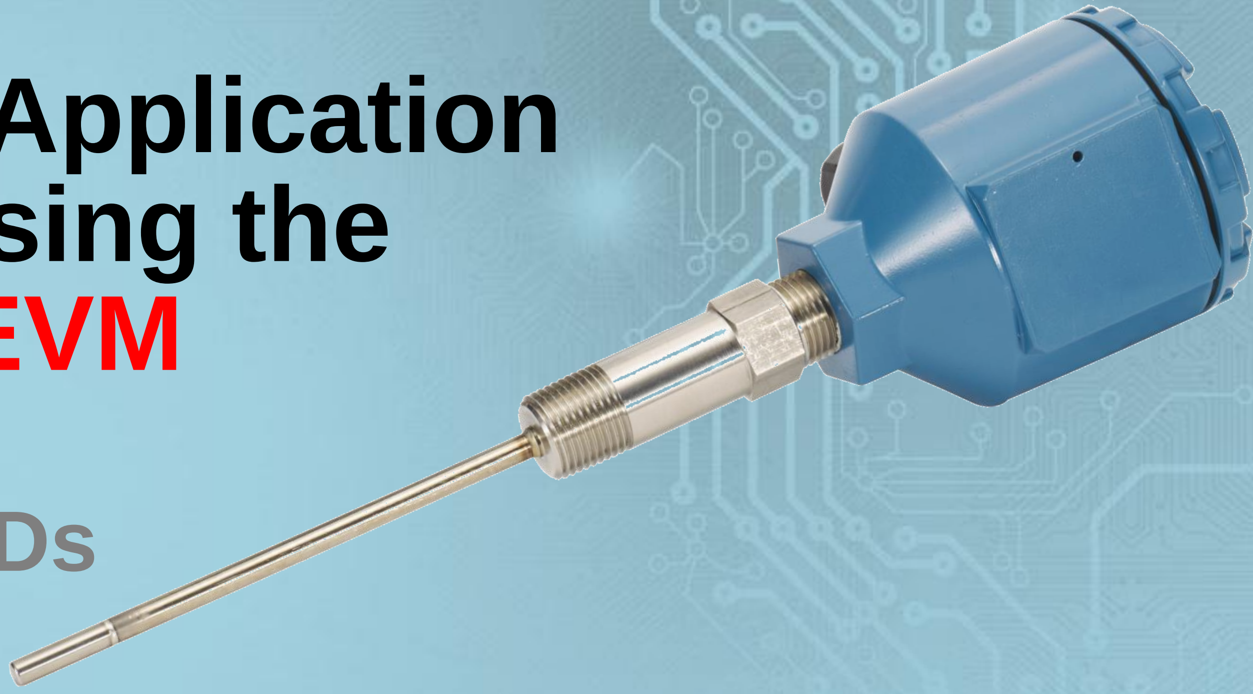
Excel-based calculator for device configuration

- Check PGA input range requirements.
- Calculate CRC/checksum values.
- Evaluate different SINC filter responses.
- View a register map.



Common Application Circuits using the ADS126xEVM

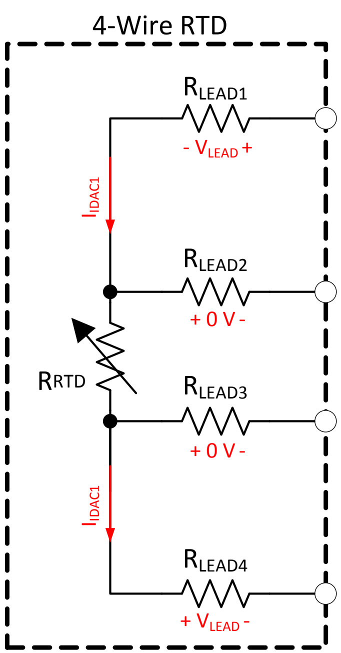
3-/4-Wire RTDs

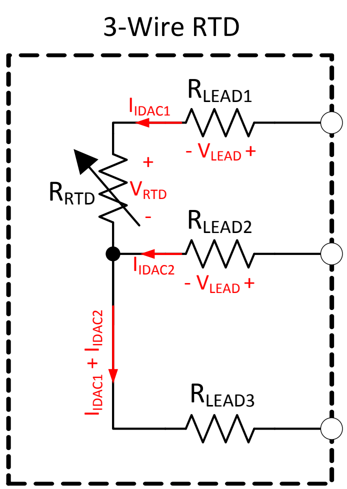


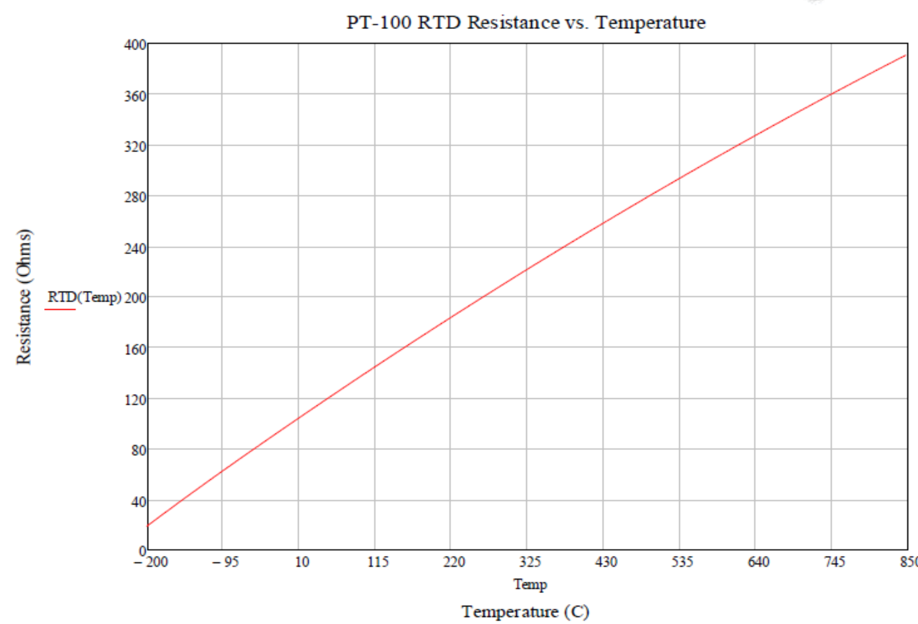
Common Apps – 3-/4-Wire RTDs

Resistance Temperature Detector (RTD) Overview

- Predictable resistance change
- Mostly made of platinum
- PT100 most common device used in industry
- High accuracy, stability and repeatability
- 2-, 3-, 4-wire types



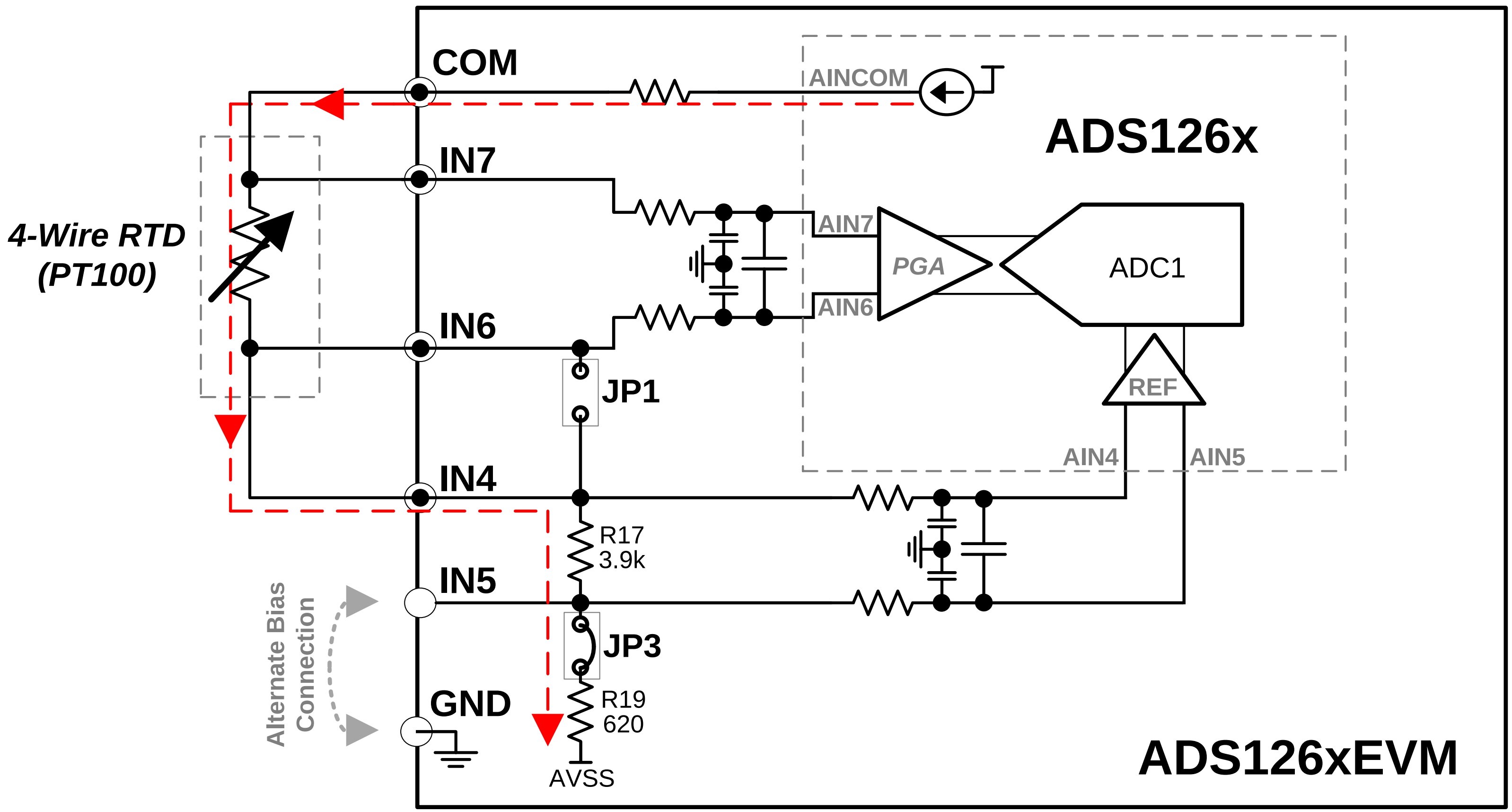




Common Apps – 3-/4-Wire RTDs

4-Wire RTD Connections

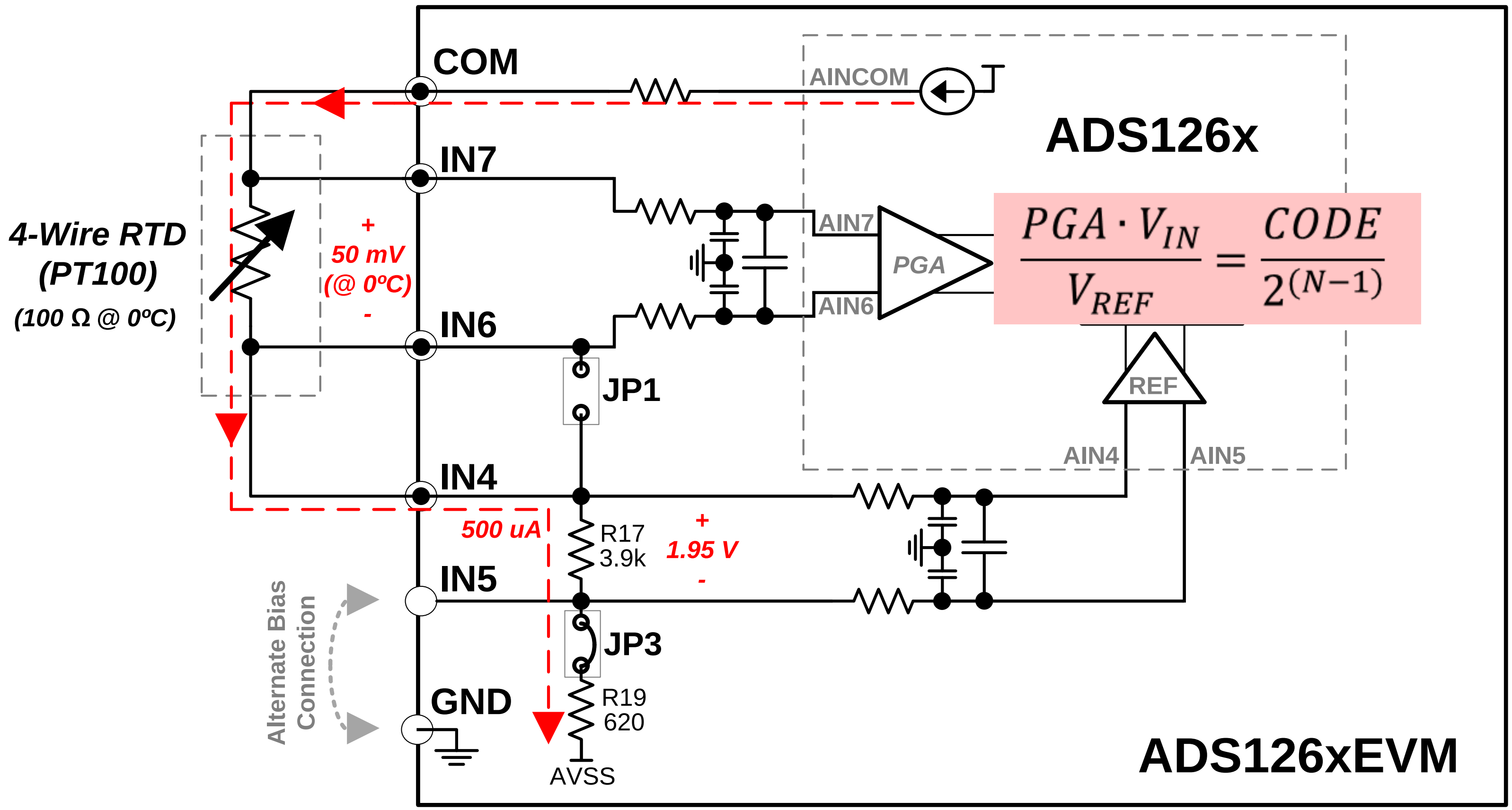
- IDAC is used to excite the RTD and generate the reference voltage ***("ratiometric")***



Common Apps – 3-/4-Wire RTDs

4-Wire RTD Connections

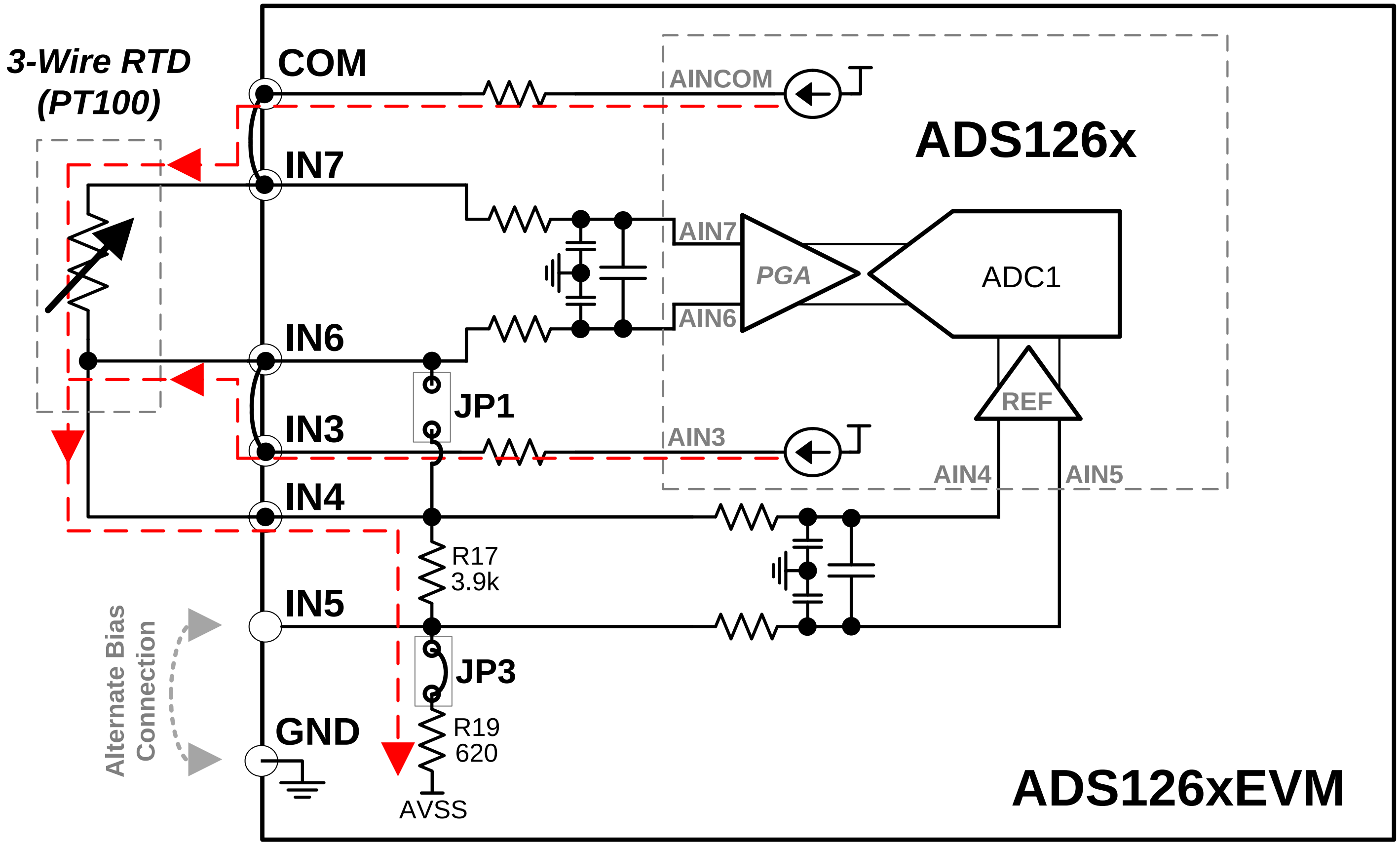
- Ratiometric configuration is unaffected by changes in IDAC current.



Common Apps – 3-/4-Wire RTDs

3-Wire RTD Connections

- A second **(matched)** IDAC current source is used to remove the effect of RTD lead resistance from the measurement.



Common Apps – 3-/4-Wire RTDs

3-Wire RTD Connections

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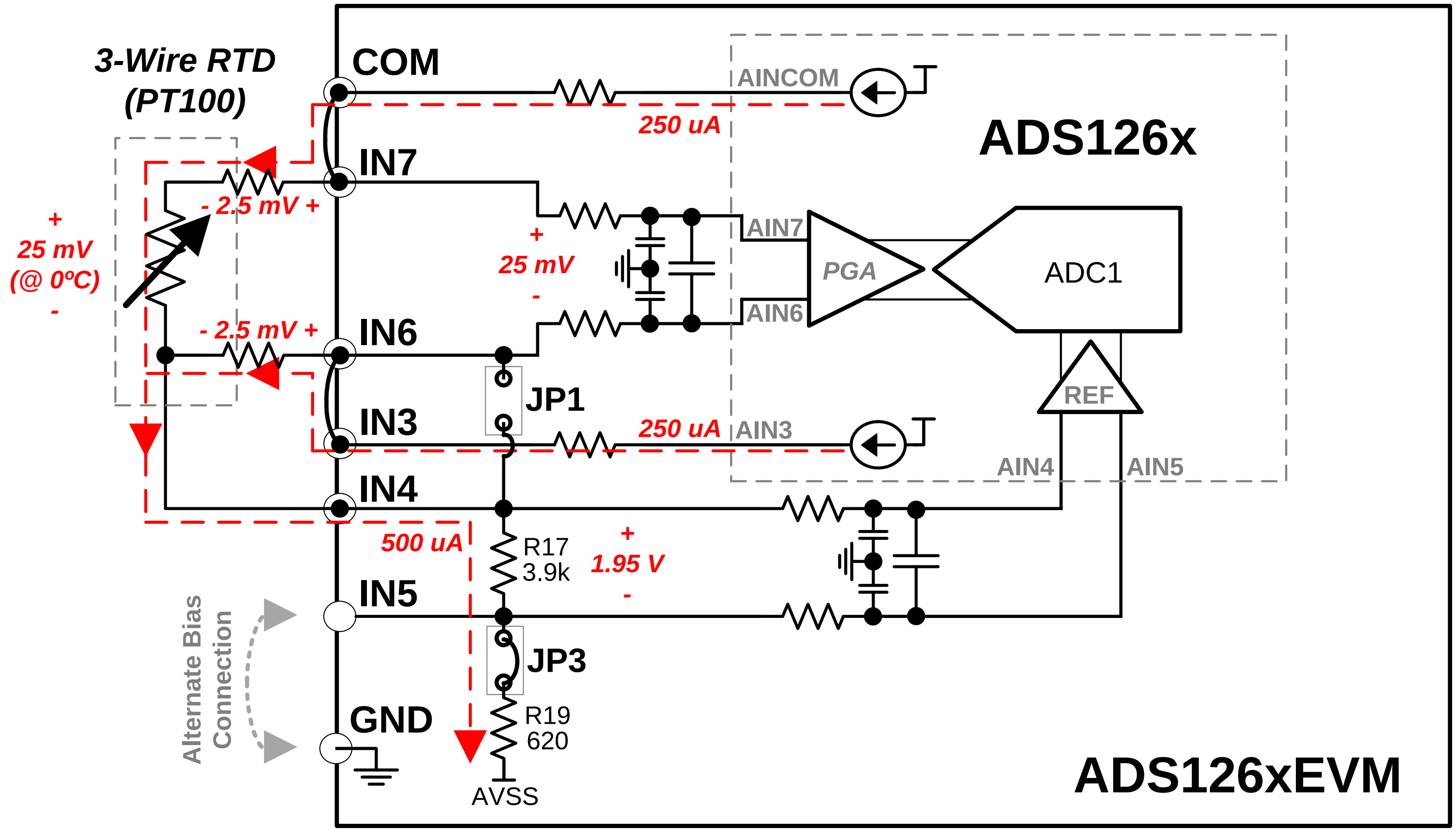
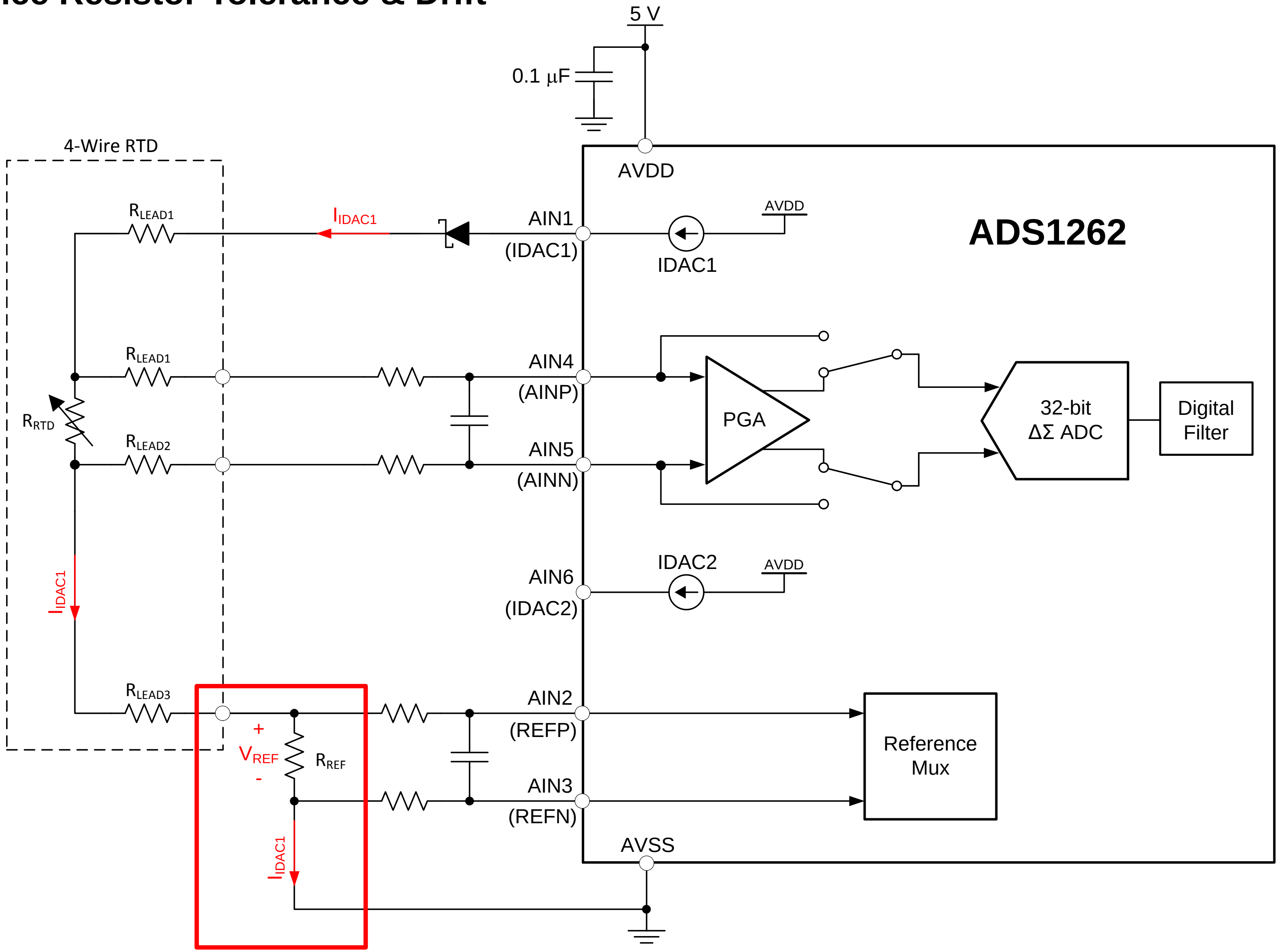


Common Application Circuits using the ADS126xEVM

3-/4-Wire RTD Pitfalls

Common Apps – 3-/4-Wire RTD Pitfalls

Reference Resistor Tolerance & Drift



Common Apps – 3-/4-Wire RTD Pitfalls

Reference Resistor Tolerance & Drift

- $\Delta R_{REF} \rightarrow$ Gain Error (GE)

1. **Resistor Tolerance** Gain Error (removed by calibration):

$$GE\ (ppm) = 10{,}000 \cdot Tolerance\ (\%) \cdot FSR\ Utilization\ (\%)$$

2. **Resistor Temperature Coefficient** Gain Error (remains after cal):

$$GE\ (ppm) = Temp\ Co.\left(\frac{ppm}{°C}\right) \cdot Temp\ Range\ (°C) \cdot FSR\ Utilization\ (\%)$$

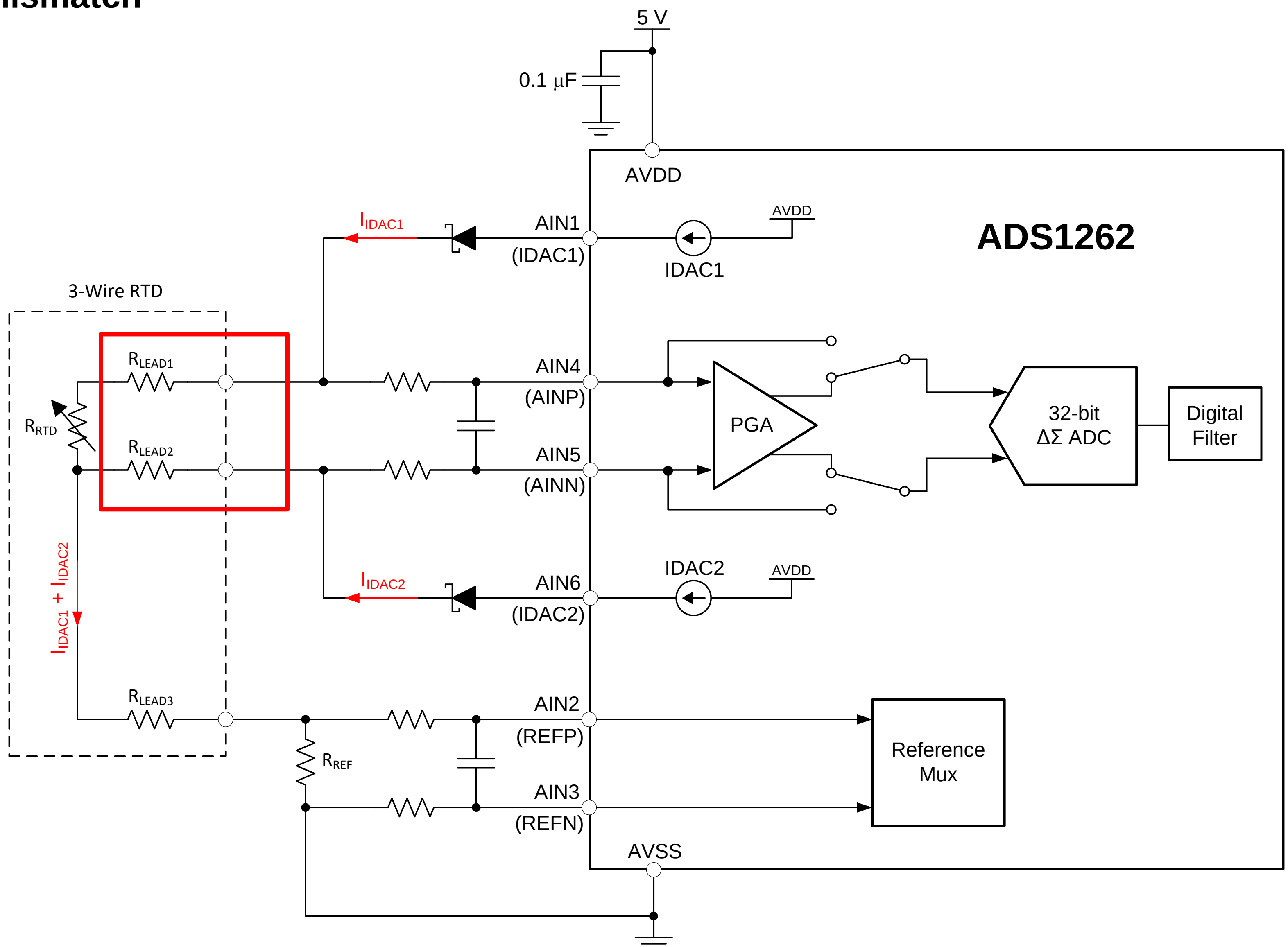
   – Example:

$$25\ \frac{ppm}{°C} \cdot 50\ °C \cdot 90\%\ Utilization = \mathbf{1125\ ppm\ (9.8\ bits\ accuracy)}$$

Use a reference resistor with a temperature coefficient ≤ 1 ppm/ºC

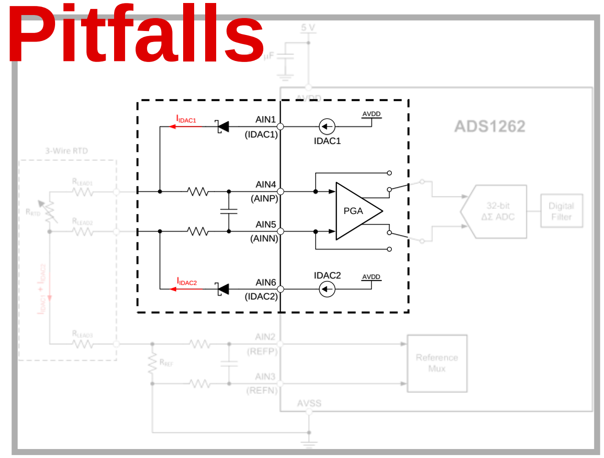
Common Apps – 3-/4-Wire RTD Pitfalls

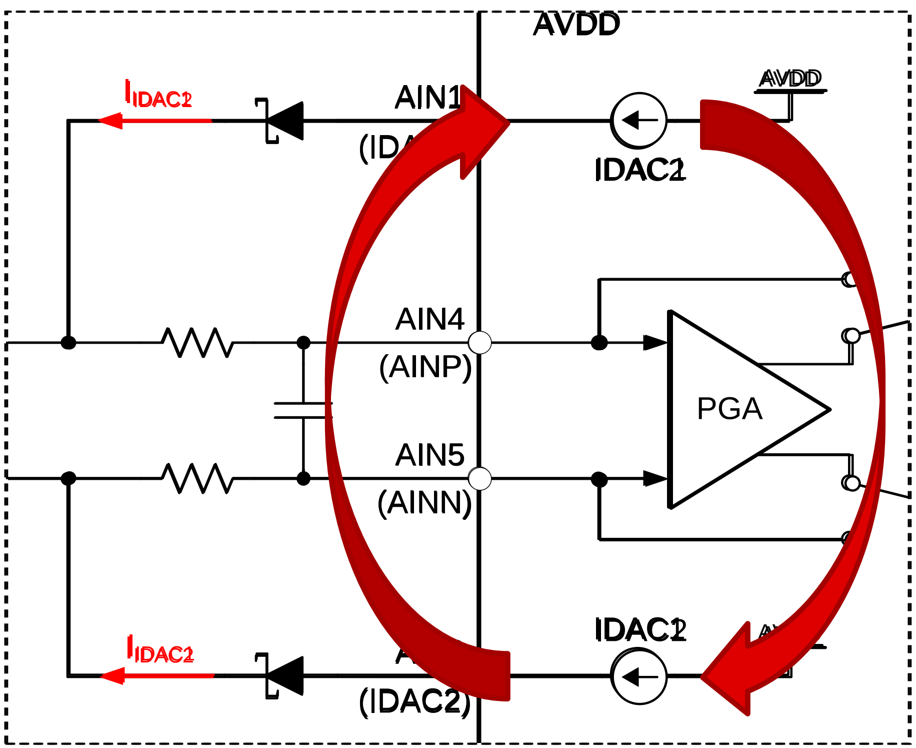
IDAC Mismatch



Common Apps – 3-/4-Wire RTD Pitfalls

IDAC Chopping using the ADS1262/3





1) $V_{IN1} = V_{RTD} + \Delta V_{LEAD}$

2) $V_{IN2} = V_{RTD} - \Delta V_{LEAD}$

AVE: $\frac{1}{2}\cdot(V_{IN1} + V_{IN2}) = V_{RTD}$

Common Apps – 3-/4-Wire RTD Pitfalls

Error Improvements using IDAC Chopping

- (Neglecting R_{REF} & RTD errors)

			Before Calibration		After Calibration	
System Temperature Range	50	(Δ°C)				
IDAC CHOPPING = OFF						
IDAC Match Error	0.1%	(%)	500	(ppm)	0	(ppm)
IDAC Match Drift	5	(ppm/°C)	125	(ppm)	125	(ppm)
...			...		...	
TOTAL ADC ERROR			556	(ppm)	127	(ppm)
IDAC CHOPPING = ON						
IDAC Match Error	0.0%	(%)	0	(ppm)	[illegible]	(ppm)
IDAC Match Drift	0	(ppm/°C)	0	(ppm)	[illegible]	(ppm)
...			...		...	
TOTAL ADC ERROR			210	(ppm)	23	(ppm)

5x Accuracy Improvement!

Common Apps – 3-/4-Wire RTD Pitfalls

3-Wire RTD Error Analysis

- Neglects RTD errors
- Assume all errors are linear
- Errors added as the "root-sum-of-squares" (uncorrelated errors)
- **ADS1262 data sheet provides this characterization data!**

System Temperature Range	50	(Δ°C)						
ADS1262 Errors								
FSR	0.45	(V)		Before Calibraion			After Calibraion	
Noise RTI (@ 20 SPS, FIR)	266.01	(nV_{P-P})		0.84	(ppm)		0.84	(ppm)
Offset	43.75	(uV)		97.22	(ppm)		0.21	(ppm)
Offset Drift	13.75	(nV/°C)		1.53	(ppm)		1.53	(ppm)
Gain Error	50	(ppm)		43	(ppm)		0.18	(ppm)
Gain Error Drift	0.5	(ppm/°C)		21.69	(ppm)		22	(ppm)
INL	3	(ppm)		3	(ppm)		3	(ppm)
IDAC Absolute Error	0.7%	(%)		0	(ppm)		0	(ppm)
IDAC Absolute Drift	50	(ppm/°C)		0	(ppm)		0	(ppm)
IDAC Match Error (Offset)	0.0%	(%)		0	(ppm)		0	(ppm)
(Gain Error)				0	(ppm)		0	(ppm)
IDAC Match Drift (Offset)	0	(ppm/°C)		0	(ppm)		0	(ppm)
(Gain Error)				0	(ppm)		0	(ppm)
I_{REFP} Abs. Bias Current	100	(nA)		174	(ppm)		0	(ppm)
I_{REFP} Abs. Bias Current V Coeff	50	(nA/V)		0	(ppm)		0	(ppm)
I_{REFP} Abs. Bias Current Drift	0.03	(nA/°C)		3	(ppm)		3	(ppm)
I_{REF} Diff. Bias Current	25	(nA)		45	(ppm)		0	(ppm)
I_{REF} Diff. Bias Current V Coeff	6	(nA/V)		0	(ppm)		0	(ppm)
I_{REF} Diff. Bias Current Drift	0.06	(nA/°C)		5	(ppm)		5	(ppm)
$I_{AINP/N}$ Abs. Bias Current	2	(nA)		7	(ppm)		0	(ppm)
$I_{AINP/N}$ Abs. Bias Current V Coeff	0.75	(nA/V)		0	(ppm)		0	(ppm)
$I_{AINP/N}$ Abs. Bias Current Drift	0.01	(nA/°C)		0	(ppm)		0	(ppm)
I_{AIN} Diff. Bias Current	0.1	(nA)		0.11	(ppm)		0	(ppm)
I_{AIN} Diff. Bias Current V Coeff	0.20	(nA/V)		0.04	(ppm)		0.04	(ppm)
I_{AIN} Diff. Bias Current Drift	0.01	(nA/°C)		0.67	(ppm)		0.67	(ppm)
TOTAL ADC ERROR				210	(ppm)		23	(ppm)
R_{REF} Errors								
Tolerance	0.05%	(±%)		434	(ppm)		0	(ppm)
Temp Drift	0.1	(±ppm/°C)		4	(ppm)		4	(ppm)
TOTAL R_{REF} ERROR				434	(ppm)		4	(ppm)

TOTAL ERROR					
Total Uncorrelated System Error		482	(ppm)	23	(ppm)
		0.434	(±Ω)	0.021	(±Ω)
		1.127	(±°C)	0.054	(±°C)

Common Apps – 3-/4-Wire RTD Pitfalls

Temperature Resolution

- Resolution = Measurement Repeatability or smallest discernable unit

ADS1262 Configuration		
PGA GAIN	8	(V/V)
Data Rate	20 SPS	(SPS)
Filter	FIR	-

↓

ADC Noise RTI	376.20	(nV_{P-P})

RTD (PT100 type)		
T_H(°C) - T_L(°C):	1050	(°C)
VRTD (@ -200°C):	9.260	(mV)
VRTD (@ +850°C):	195.241	(mV)

↓

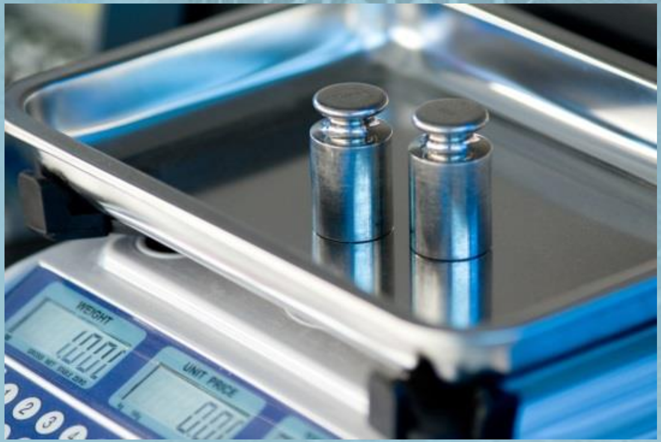
ΔVin	185.981	(mV)

↓ ↓

Noise-Free Bits	18.9	(nV_{P-P})
Temperature Resolution	0.002	(°C_{P-P})

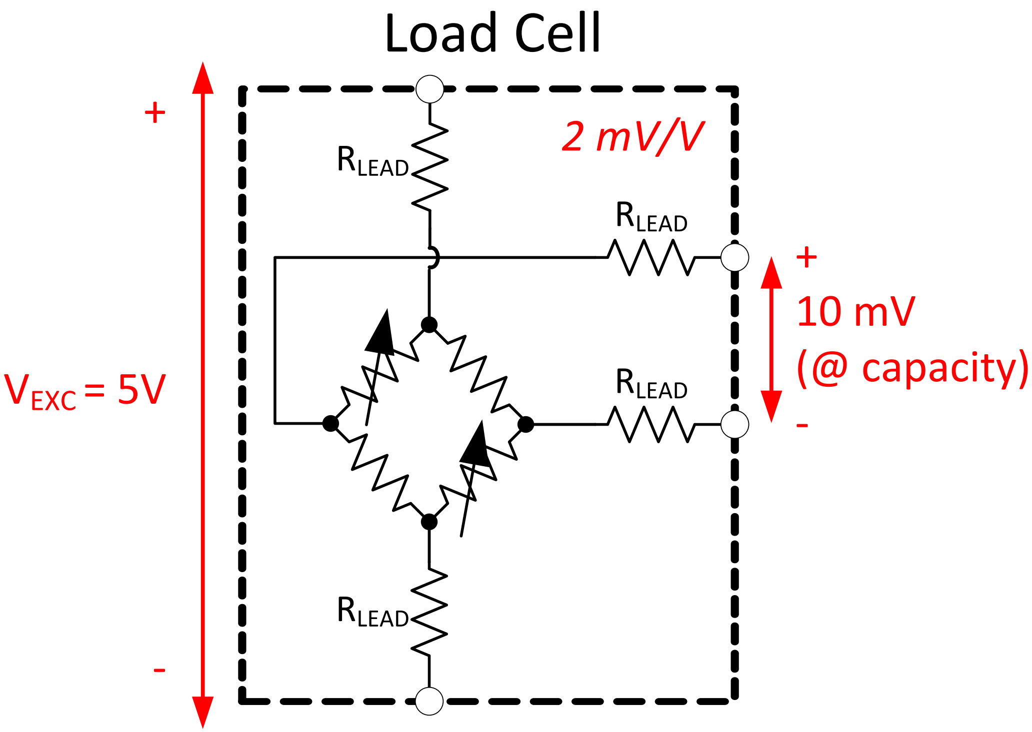
Common Application Circuits using the ADS126xEVM

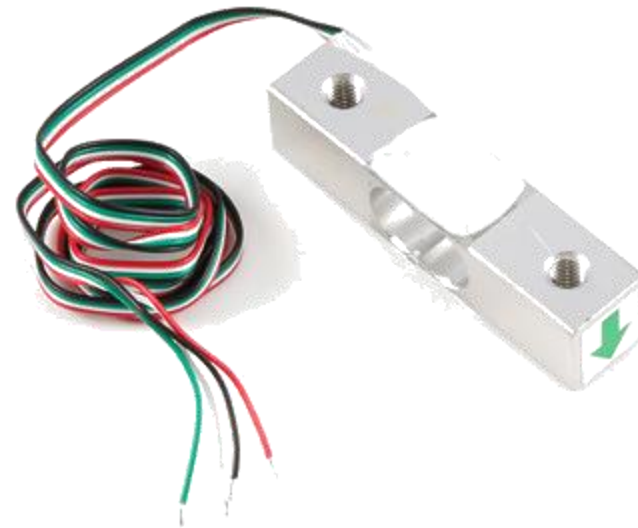
Load Cells



Common Apps – Load Cells

Introduction to Load Cells

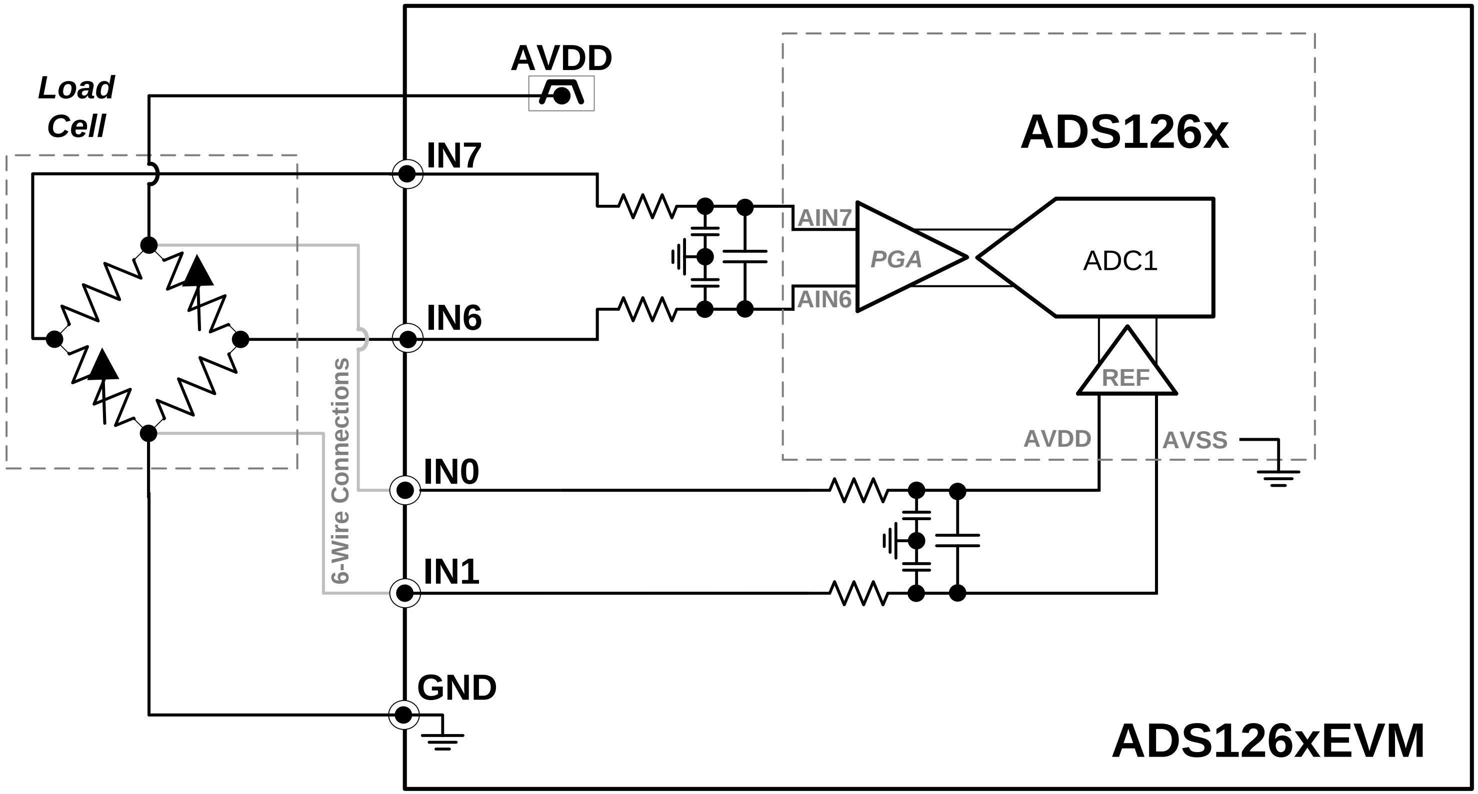




Common Apps – Load Cells

Connecting a Load Cell to the ADS126xEVM

- 4-/6-Wire Load Cell Connections
- ADS126x can internally use the analog supply as the reference voltage

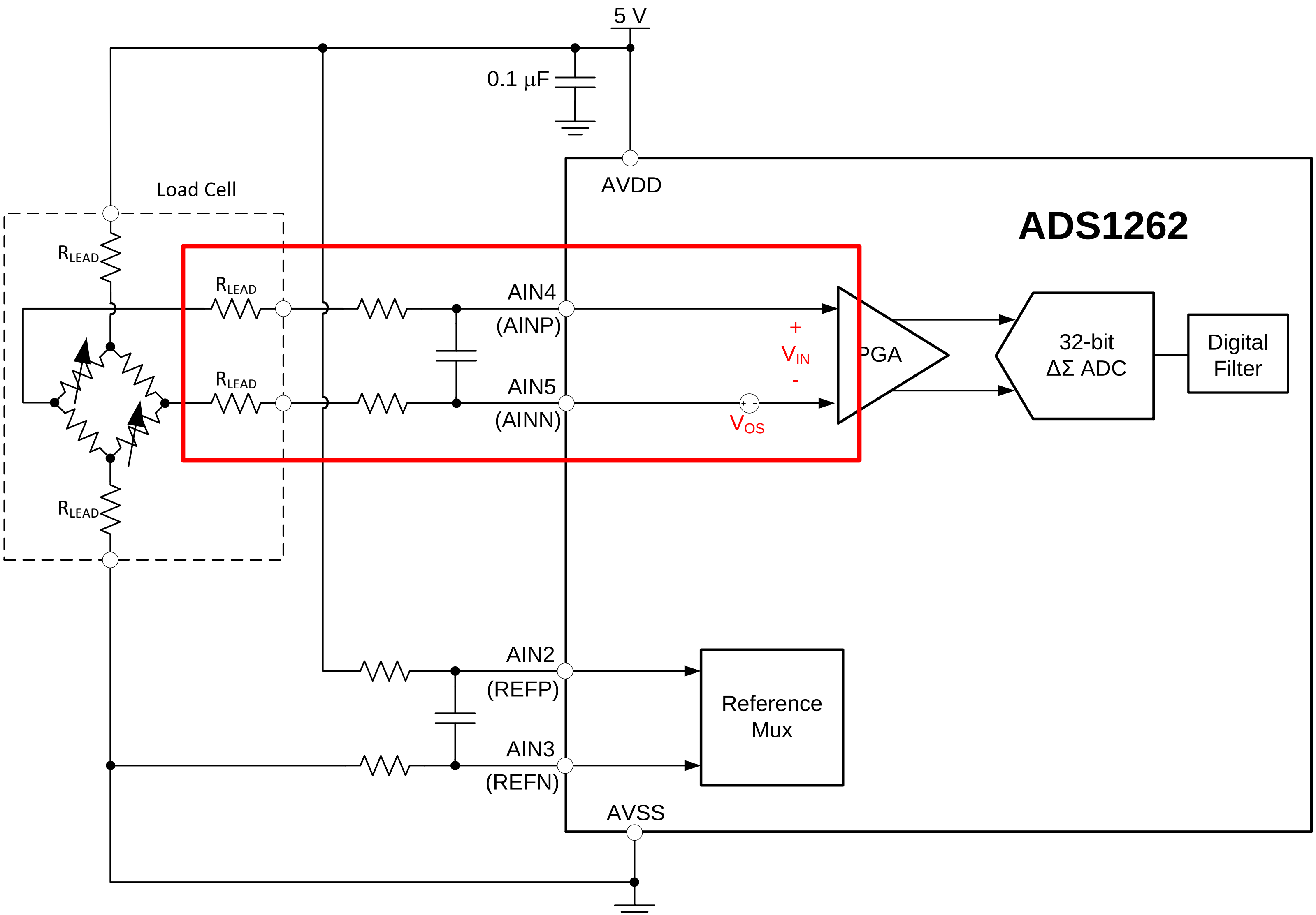


Common Application Circuits using the ADS126xEVM

Load Cell Pitfalls

Common Apps – Load Cell Pitfalls

Offset Drift

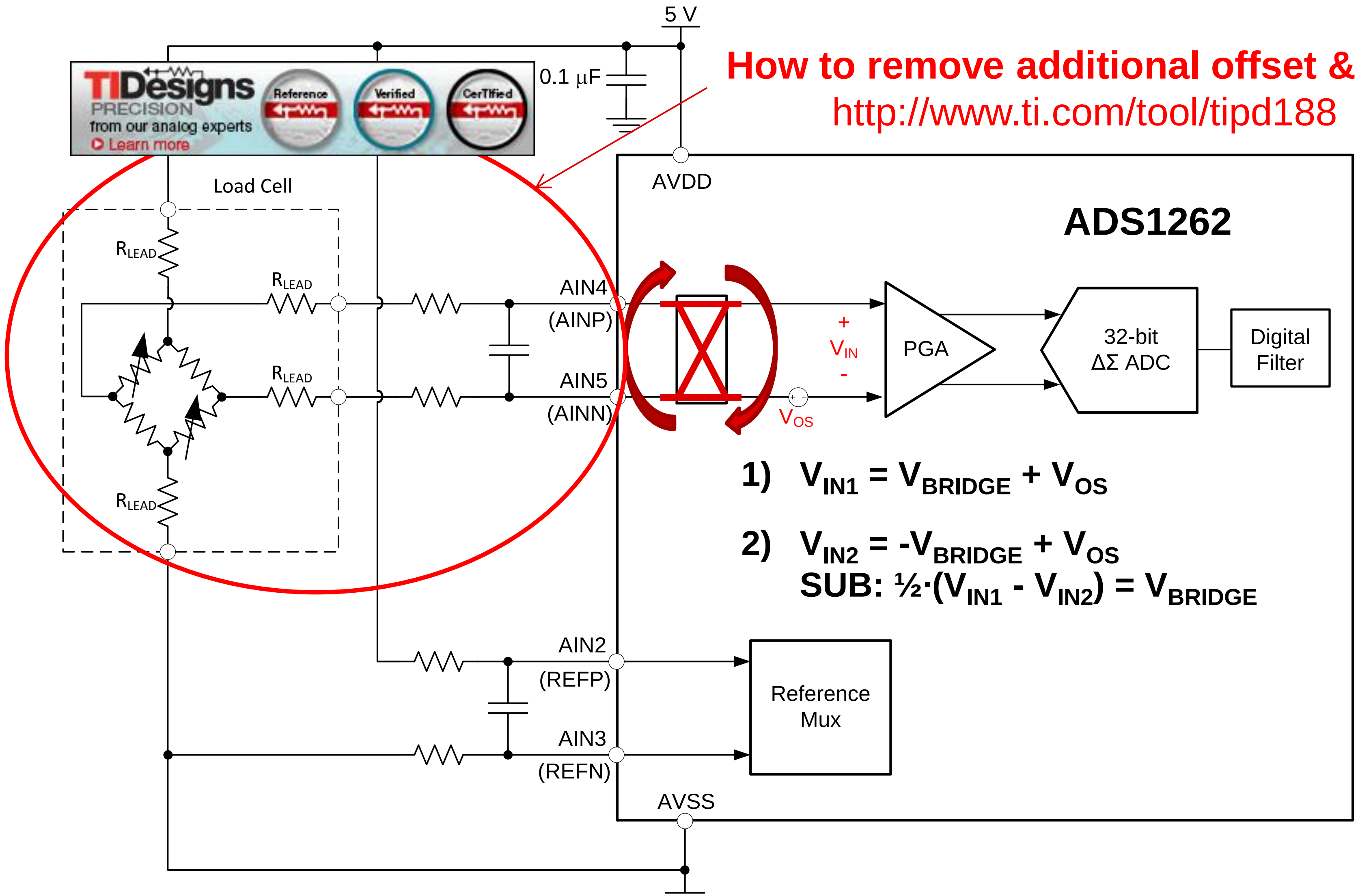


Common Apps – Load Cell Pitfalls

Input Chopping to Remove Offset Drift using the ADS1262/3

How to remove additional offset & drift

http://www.ti.com/tool/tipd188



1) $V_{IN1} = V_{BRIDGE} + V_{OS}$

2) $V_{IN2} = -V_{BRIDGE} + V_{OS}$

SUB: $\frac{1}{2} \cdot (V_{IN1} - V_{IN2}) = V_{BRIDGE}$

Common Apps – Load Cell Pitfalls

Error Analysis

- Neglects load cell errors

System Temperature Range	165	(Δ°C)				
ADS1262 Errors						
FSR	0.3125	(V)	Before Calibraion		After Calibraion	
Noise RTI (@ 20 SPS, FIR)	198.00	(nV_{P-P})	0.63	(ppm)	0.63	(ppm)
Offset	10.938	(uV)	35	(ppm)	0.16	(ppm)
Offset Drift	10.9	(nV/°C)	5.78	(ppm)	5.78	(ppm)
Gain Error	50	(ppm)	3	(ppm)	0.01	(ppm)
Gain Error Drift	0.5	(ppm/°C)	4.99	(ppm)	4.99	(ppm)
INL	3	(ppm)	3	(ppm)	3	(ppm)
I_{REFP} Abs. Bias Current	100	(nA)	0	(ppm)	0	(ppm)
I_{REFP} Abs. Bias Current V Coeff	50	(nA/V)	0	(ppm)	0	(ppm)
I_{REFP} Abs. Bias Current Drift	0.03	(nA/°C)	0	(ppm)	0	(ppm)
I_{REF} Diff. Bias Current	200	(nA)	0.23	(ppm)	0	(ppm)
I_{REF} Diff. Bias Current V Coeff	6	(nA/V)	0	(ppm)	0	(ppm)
I_{REF} Diff. Bias Current Drift	0.30	(nA/°C)	0.06	(ppm)	0.06	(ppm)
$I_{AINP/N}$ Abs. Bias Current	2	(nA)	0.15	(ppm)	0	(ppm)
$I_{AINP/N}$ Abs. Bias Current V Coeff	0.75	(nA/V)	0	(ppm)	0	(ppm)
$I_{AINP/N}$ Abs. Bias Current Drift	0.01	(nA/°C)	0	(ppm)	0	(ppm)
I_{AIN} Diff. Bias Current	0.1	(nA)	0.260	(ppm)	0	(ppm)
I_{AIN} Diff. Bias Current V Coeff	0.20	(nA/V)	0.002	(ppm)	0.002	(ppm)
I_{AIN} Diff. Bias Current Drift	0.01	(nA/°C)	5.16	(ppm)	5.16	(ppm)
TOTAL ADC ERROR			36	(ppm)	10	(ppm)

TOTAL ERROR				
Total Uncorrelated System Error	36	(ppm)	10	(ppm)
	11.39	(±µV)	3.04	(±µV)
	0.365	(±g)	0.097	(±g)

Common Apps – Load Cell Pitfalls

Weight Resolution

- Resolution = Measurement Repeatability or smallest discernable unit

ADS1262 Configuration		
PGA GAIN	32	(V/V)
Data Rate	20 SPS	(SPS)
Filter	FIR	-

↓

ADC Noise RTI	198.00	(nV_{P-P})

Load Cell		
Max Load Capacity	10	(kg)
Sensitivity	2	(mV/V)
Excitation	5	(V)

↓

ΔVin	10	(mV)

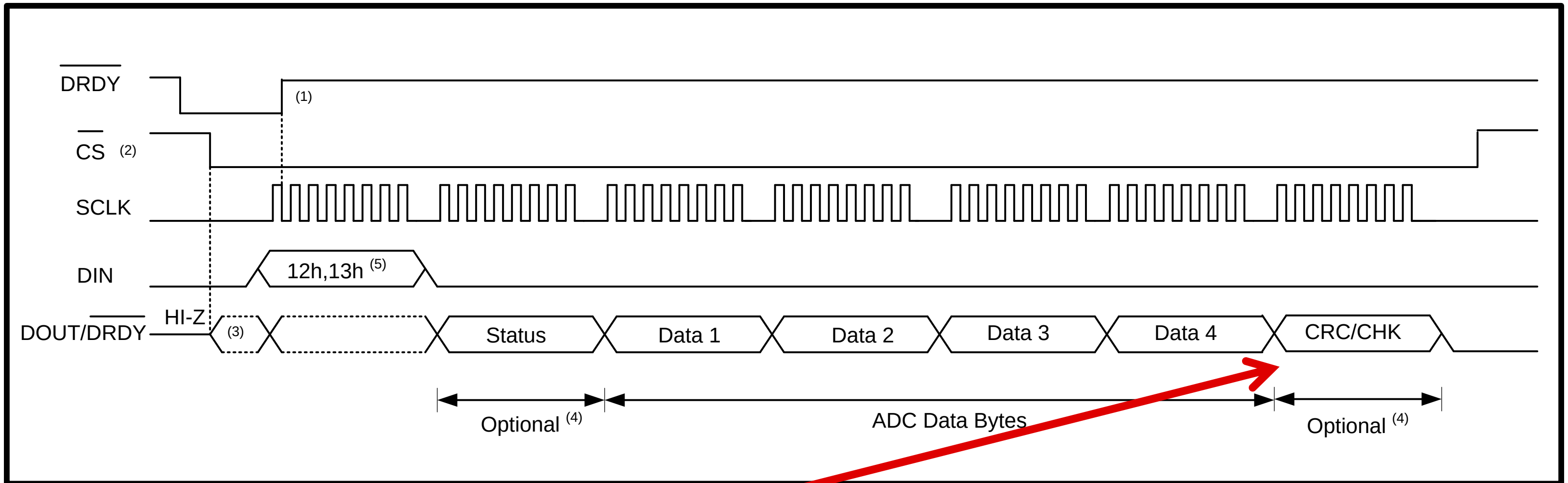
↓ ↓

Noise-Free Bits	15.6	(nV_{P-P})
Weight Resolution	0.198	(g_{P-P})

How to Use the **ADS126x Monitoring and Diagnostic** Features

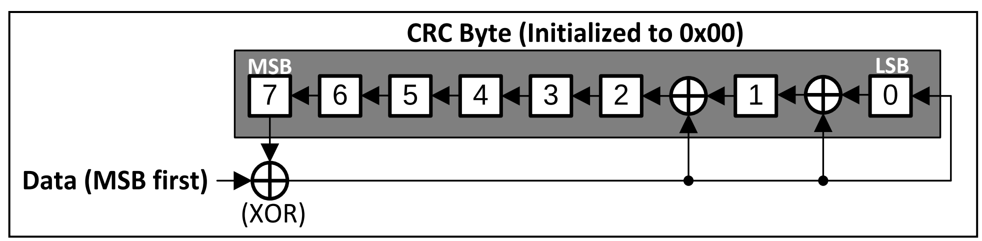
ADS126x Monitoring & Diagnostics

Communication Error Checking



Checksum/CRC

	Data byte 1
+	Data byte 2
+	Data byte 3
+	Data byte 4
+	9Bh
=	checksum byte



ADS126x Monitoring & Diagnostics

Fault Monitoring

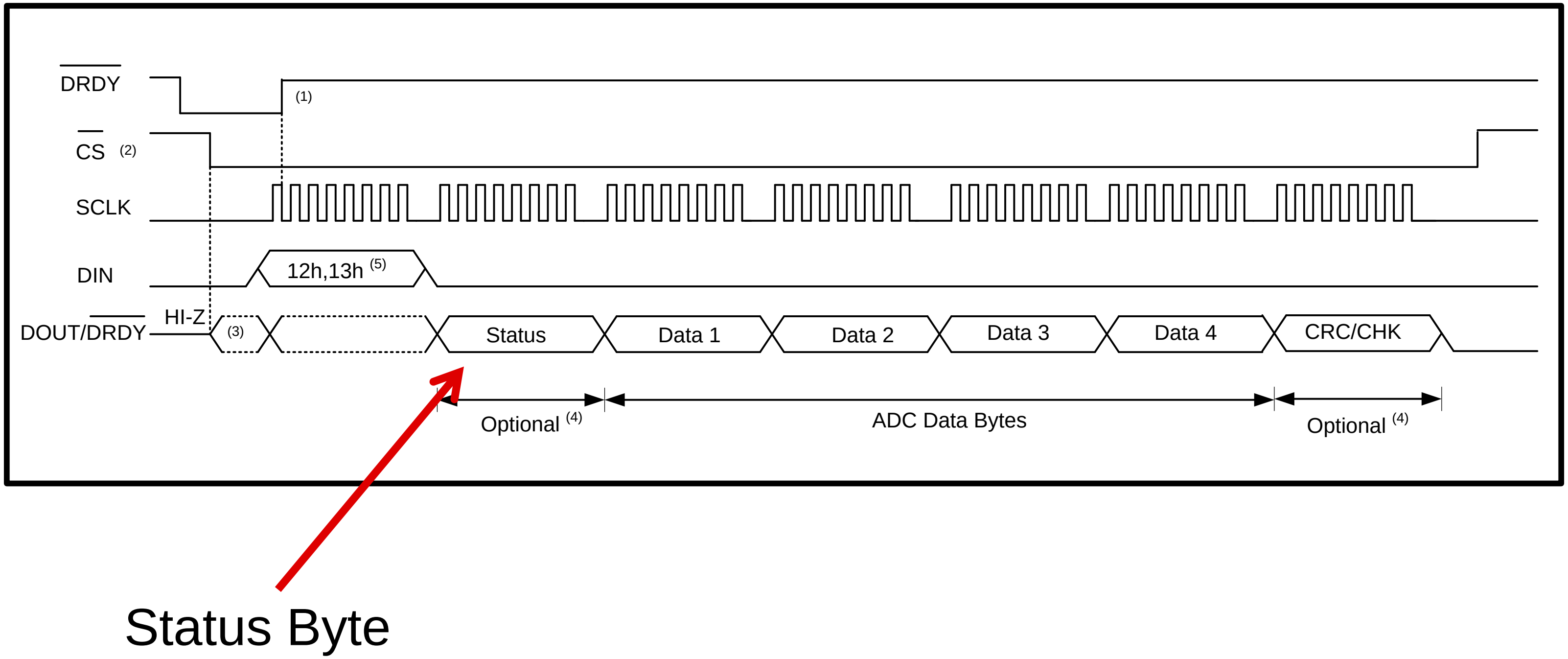
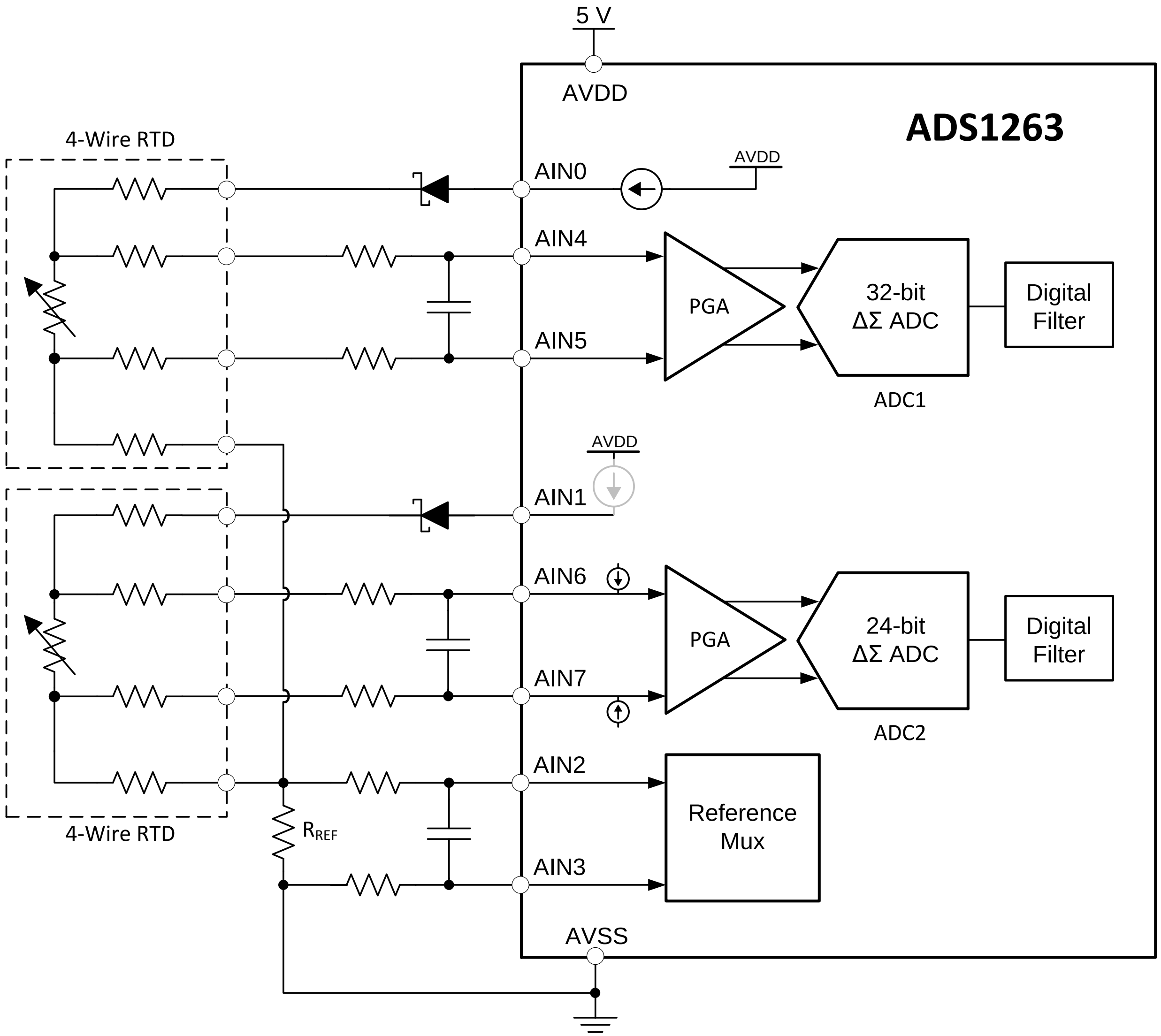


Figure 92. Status Byte (STATUS)

7	6	5	4	3	2	1	0
ADC2	ADC1	EXTCLK	REF_ALM	PGAL_ALM	PGAH_ALM	PGAD_ALM	RESET

ADS126x Monitoring & Diagnostics

Burnout Detection with ADC2



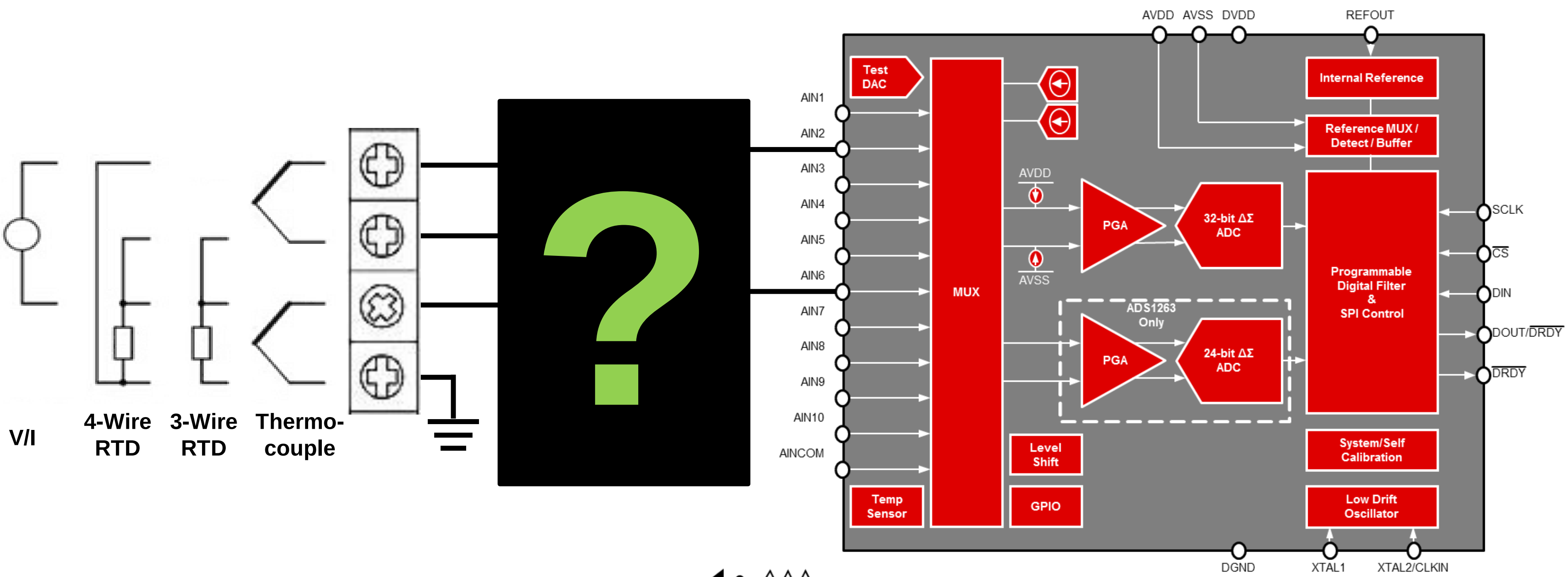
Universal Input for Programmable Logic Controllers using the ADS1262

Upcoming Universal Input Module for PLC

Best-in-class Industrial ΔΣ ADC w/ Ultra Low Noise| 32-bit | 10/5 SE/Diff Channels

New Reference Design for Programmable Logic Controllers (PLC)

Coming soon…



TI Designs

Additional Information

Redefining high resolution and low noise in Delta-Sigma ADC applications

General Delta-Sigma ADC information:

- Understanding the Delta-Sigma modulator
- Delta-Sigma basics: how the digital filter works
- How Delta-Sigma ADCs work (Part 1)
- How Delta-Sigma ADCs work (Part 2)

ADS1262 & ADS1263 Information:

- ADS1262 Product Folder
- ADS1262EVM
- ADS1262/3 precision weigh scale reference design
- ADS1262/3 configuration calculator
- Buy or sample the ADS1262/3

Thanks!

Any Questions?