WEBENCH® Clock Architect

Design And Simulate Clock Circuits And Complex Clocking Trees

Clocks are Everywhere

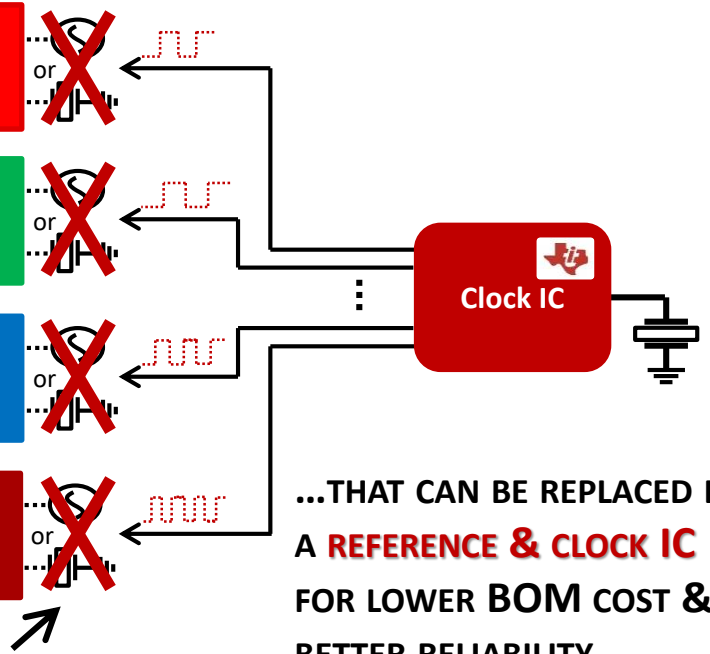
If a system has….

Processors
(FPGA, DSP, ASIC, ARM/MIPS-based processor, etc.)

I/O
(USB controller, backplane SERDES, etc.)

Connectivity
(Switch ASIC, Ethernet MAC/PHY, WiFi, 3G/LTE modem, etc.)

Data Converters
(High speed & precision ADC, DAC, Analog Front-Ends)



…THAT CAN BE REPLACED BY A REFERENCE & CLOCK IC FOR LOWER BOM COST & BETTER RELIABILITY

… there are certainly multiple crystals or oscillators used as clock sources

General Purpose Clocking Application

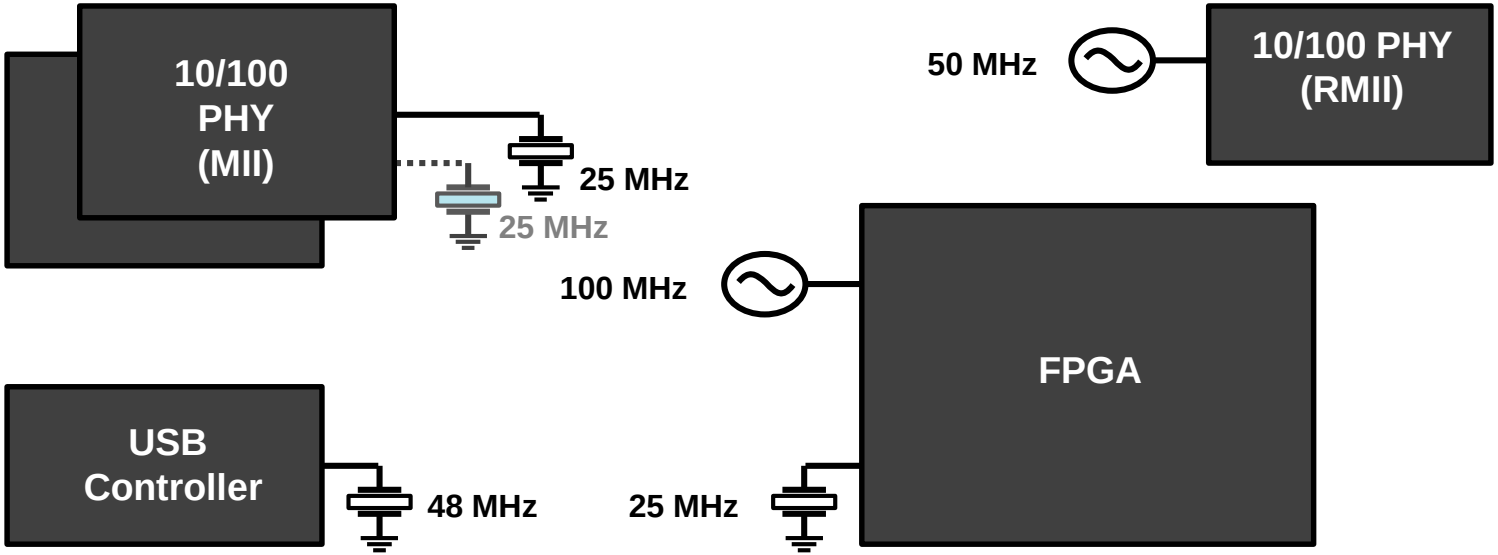
Industrial & Consumer Crystal & Oscillator Replacement

Crystals + Oscillators

Crystals: 4

Oscillator: 2

Clock: None



Example Case

General Purpose Clocking Application

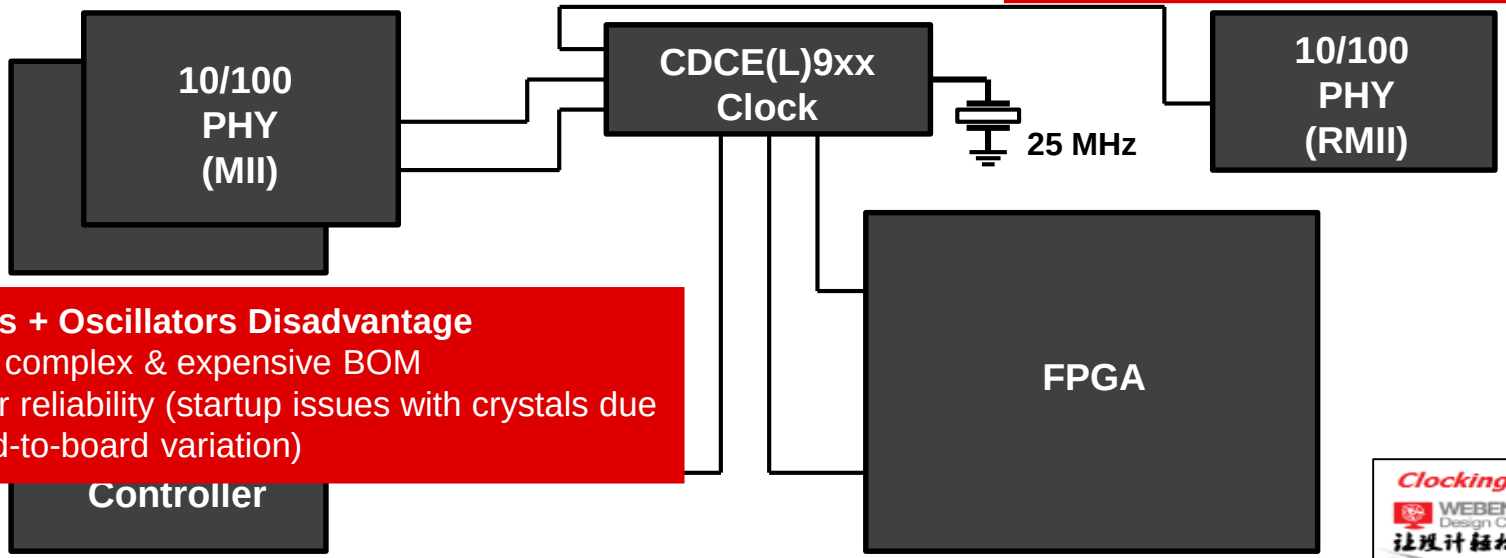
Industrial & Consumer Crystal & Oscillator Replacement

Crystals + Oscillators

Crystals: 4
Oscillator: 2
Clock: None

1 x Crystal + 1 x Clock

Crystals: 1
Oscillator: None
Clock: 1



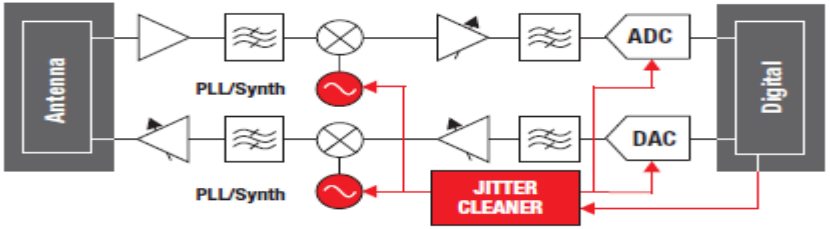
Crystals + Oscillators Disadvantage
→More complex & expensive BOM
→Lower reliability (startup issues with crystals due to board-to-board variation)

Example Case

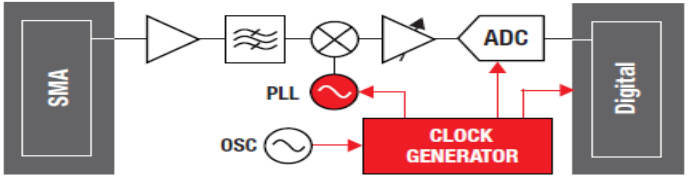
Performance Clocking Applications

Wireless/Wired/Optical Comms, Networking, and Test & Measurement

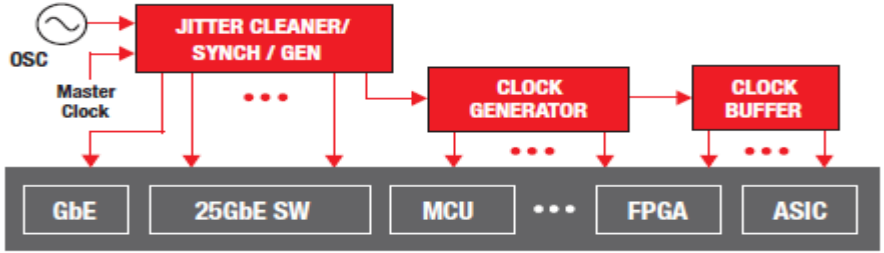
Wireless RRU



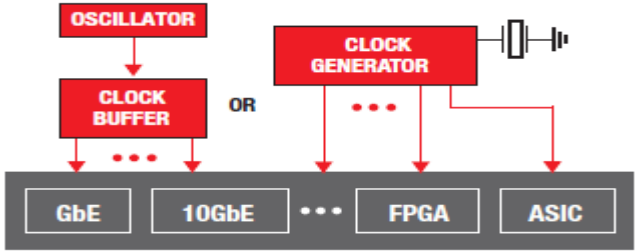
Test & Measurement



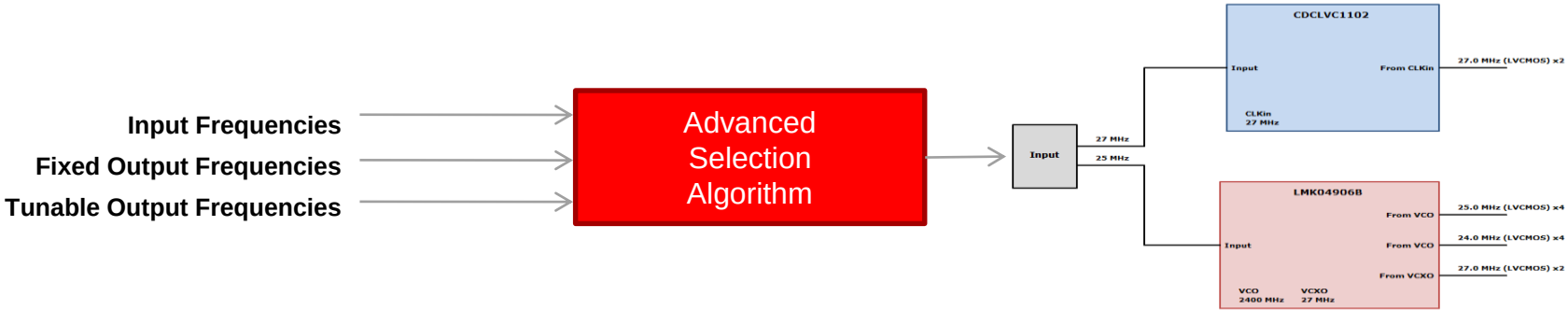
Wired/Optical Communications

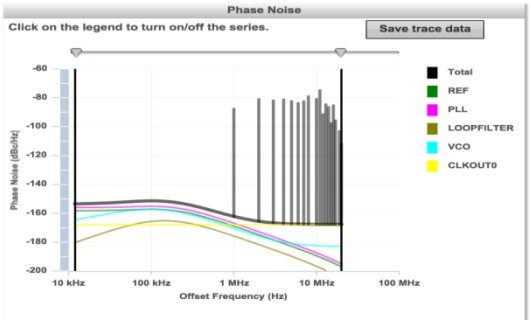


Networking

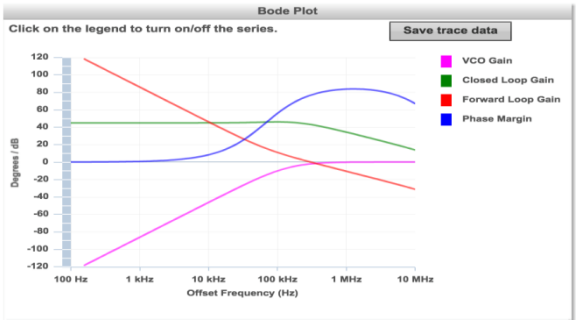


Overview of WEBENCH® Clock Architect

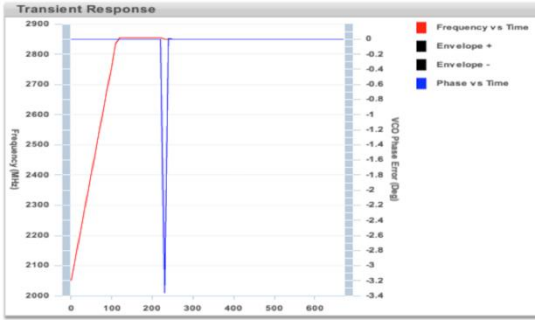




Phase Noise



Bode Plot



Lock Time

Tool Capabilities

Industry's first Clock & Timing tool that does it all

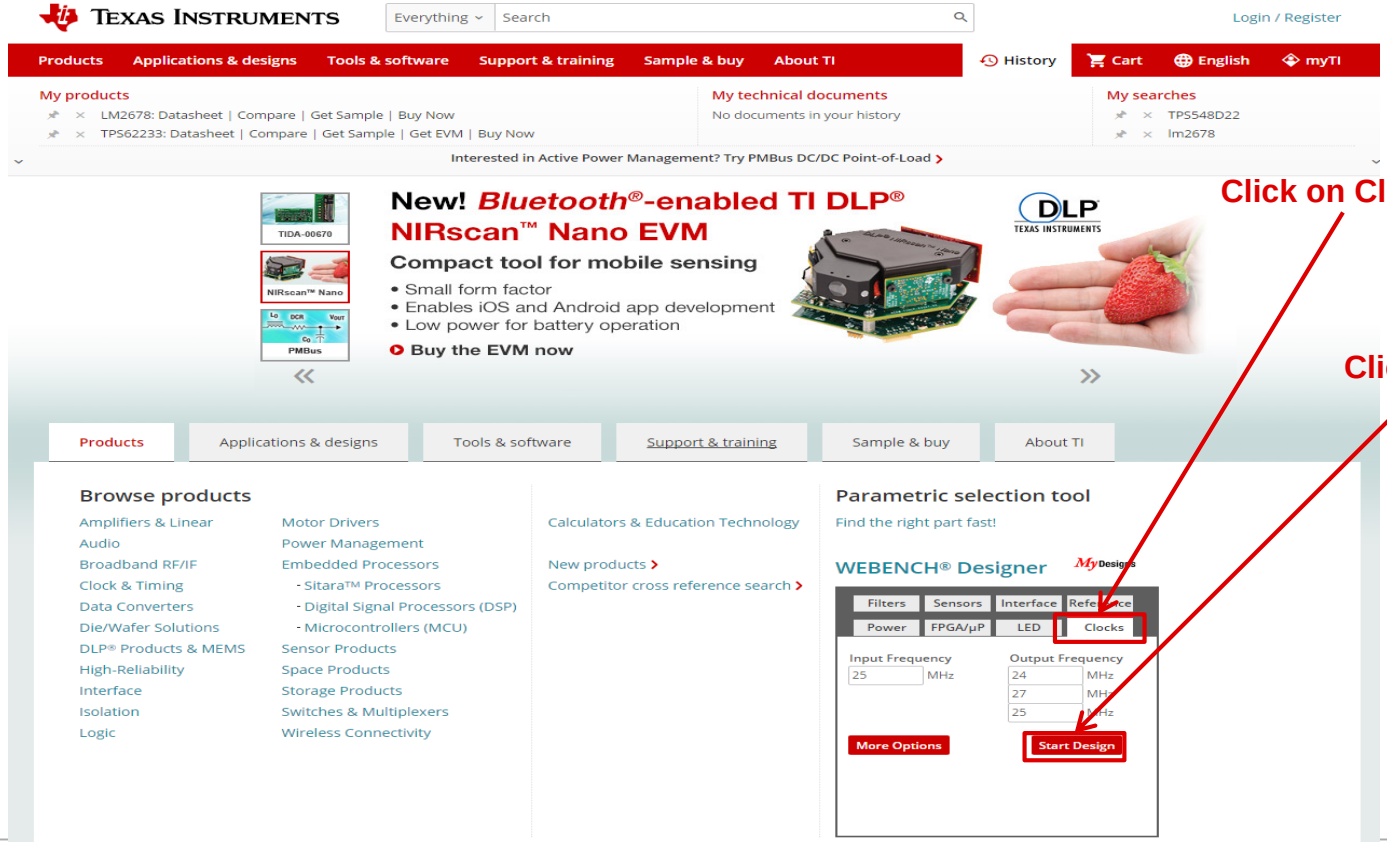
- Recommends a system clock tree solution with one or more parts
- Allows users to customize PLL Loop Filter Design
- Simulates phase noise, spurs, and lock time
- Cascades noise from a device upstream in the clock tree solution to a downstream device

Provides quick and hassle-free experience for a user looking for an optimized clock tree solution. Output clock phase noise simulations match real silicon performance

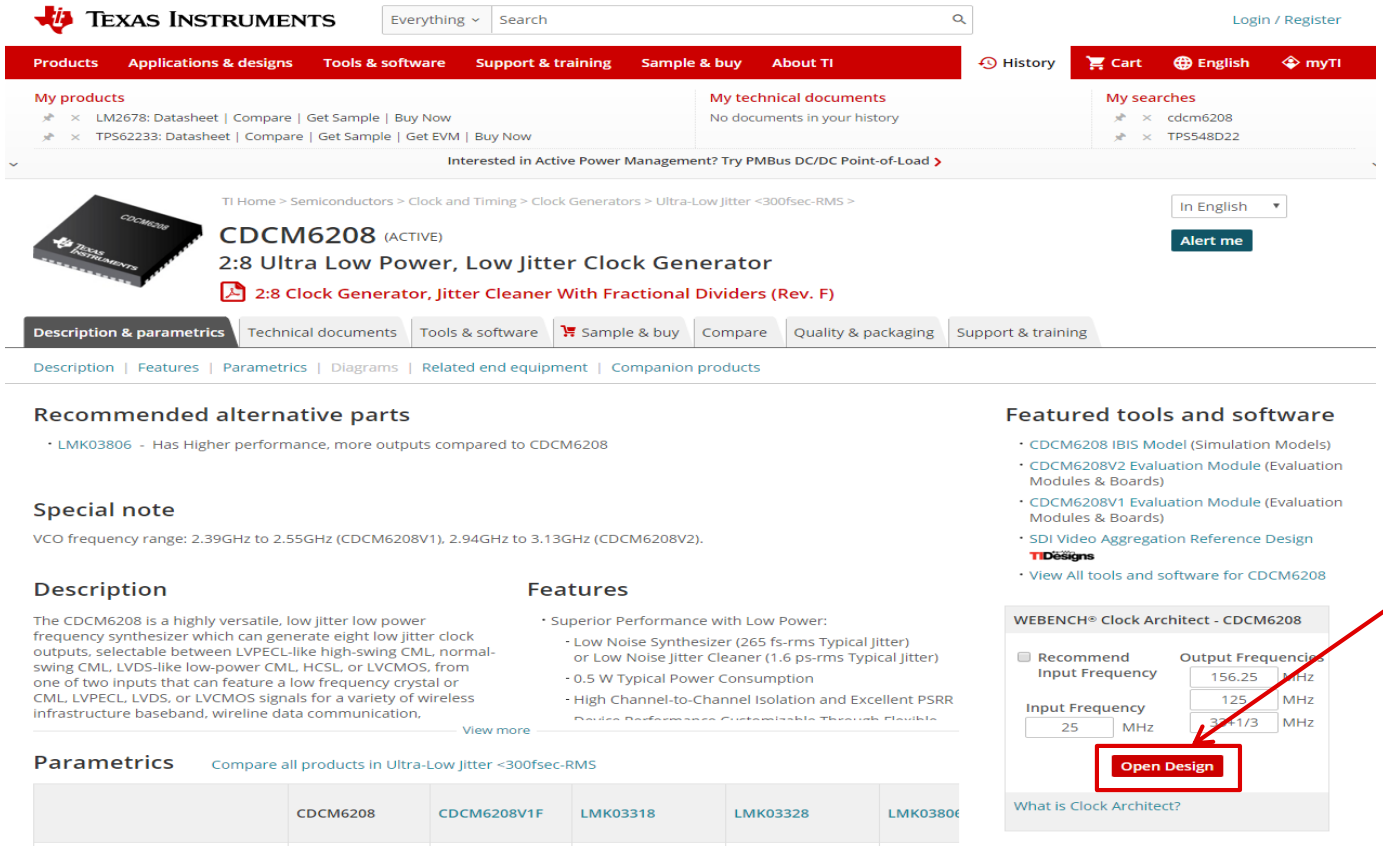
New Features

- Custom Phase Noise Profile for XOs, VCOs, and VCXOs
- Part Filters
- Spurs & Lock Time
- Share Design
- Advanced Loop Filter Configuration
- Active Filters

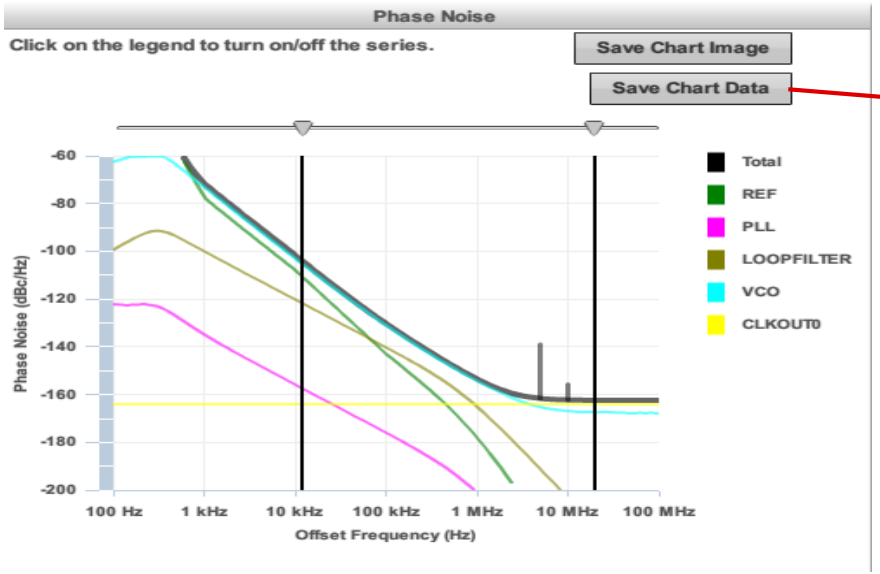
Accessing from TI.com Launch Panel



Accessing from Product Folder



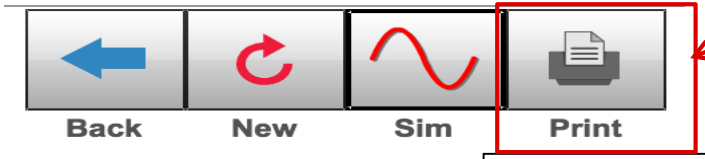
Save Trace Data



	A	B	C	D	E	F	G
1	Offset(Hz	Total	OSCin	PLL	LOOPFILTI	VCO	Y0
2	12000	-132.915	-143.793	-134.501	-150.93	-139.774	-159.024
3	12924.08	-133.033	-144.409	-134.679	-150.469	-139.57	-159.024
4	13919.33	-133.14	-145.022	-134.85	-150.027	-139.382	-159.024
5	14991.21	-133.237	-145.631	-135.015	-149.607	-139.211	-159.024
6	16145.64	-133.324	-146.236	-135.173	-149.209	-139.058	-159.024
7	17388.96	-133.404	-146.837	-135.325	-148.834	-138.924	-159.024
8	18728.03	-133.479	-147.433	-135.471	-148.482	-138.808	-159.024
9	20170.22	-133.549	-148.024	-135.61	-148.154	-138.711	-159.024
10	21723.47	-133.617	-148.609	-135.744	-147.85	-138.634	-159.024
11	23396.32	-133.682	-149.187	-135.872	-147.57	-138.574	-159.024
12	25198	-133.746	-149.758	-135.995	-147.313	-138.533	-159.024
13	27138.42	-133.811	-150.322	-136.113	-147.079	-138.509	-159.024
14	29228.27	-133.875	-150.876	-136.225	-146.866	-138.501	-159.024
15	31479.05	-133.94	-151.42	-136.332	-146.674	-138.508	-159.024
16	33903.15	-134.006	-151.953	-136.435	-146.501	-138.529	-159.024
17	36513.93	-134.073	-152.474	-136.534	-146.347	-138.562	-159.024
18	39325.75	-134.14	-152.981	-136.627	-146.209	-138.606	-159.024
19	42354.11	-134.208	-153.473	-136.717	-146.087	-138.66	-159.024
20	45615.67	-134.276	-153.948	-136.803	-145.979	-138.721	-159.024

PDF Design Report

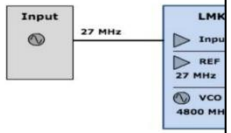
Click Print



WEBENCH® Clock Architect

Project Report

Project: 238809/1582 Project 1582 - [LMK03318]
Created: 1/29/16 10:35:00 AM



Block Diagram

System Specification and Parameters

Fixed Outputs

Name	Freq (MHz)	Format	Count
fixed0	24	Any	1
fixed1	27	Any	1
fixed2	25	Any	1

Options

Name	Design Value
Automatically Select Input Frequencies	Yes

TEXAS INSTRUMENTS

WEBENCH® Clock De

Loop Filter: LMK03318 L

Preferences

Name	Desig
Filter Type	Pass
Filter Order	3rd O
Op Amp Gain	1.00
Charge Pump Gain	6.40
VCO Gain	45.00
VCO Input Capacitance	0.00
VCO Frequency	4800
Phase Det. Frequency	27.00
Filter type	desig
Brickwall Bandwidth	308.0392425793467 kHz
Delta Sigma Order	3
Randomization Factor	0.0 %
PLL Whole Part	177

WEBENCH® Clock Architect Project

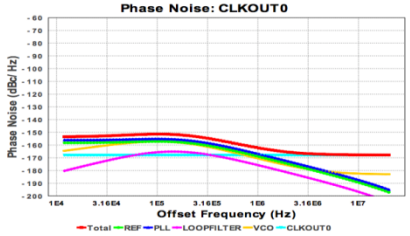
Output Block: LMK03318 LMK03318 : CLKOUT0 as LVCMOS output, 25.0 MHz

Integrated Noise Info 12000.0 Hz - 2.0E7 Hz

Name	Design Value
Calculated Area	0.00
Equivalent Flat Noise	-165.063 dBc/Hz
RMS Jitter	224.704 fs
RMS Phase Error (deg)	0.002 deg
RMS Phase Error	0.035 mrad
EVM	0.004%
SNR	89.045 dB
Spur	-92.045 dBc
Jitter (Pk-Pk)	1602.249 fs
Jitter (Cycle to Cycle Pk)	3204.499 fs
Jitter (Cycle to Cycle RMS)	317.779 fs
A/D ENOB	14.506 bits
TIE (Time Interval Error)	-0.286
UI (Unit Interval)	0.00
Lower Integration Limit	12.00 kHz
Upper Integration Limit	20.00 MHz

Phase Noise Values (dBc/Hz)

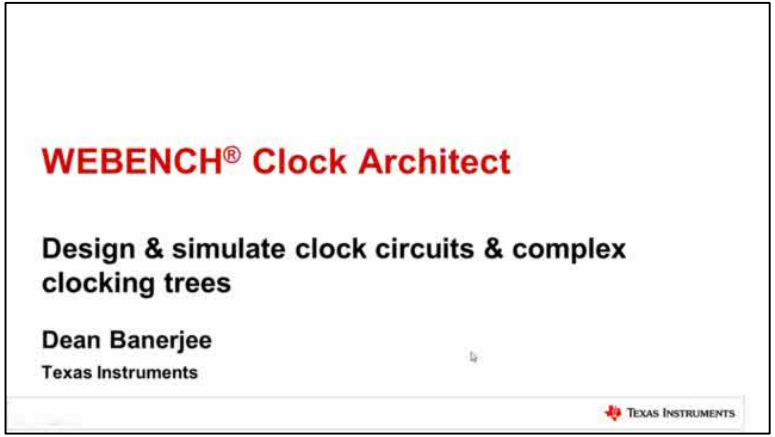
Offset	Total	REF	PLL	LOOPFILTER	VCO	CLKOUT0
12 kHz	-153.45	-158.25	-156.03	-180.24	-164.51	-167.95
100 kHz	-151.43	-157.26	-155.2	-165.67	-157.29	-167.95
20000 kHz	-167.8	-197.05	-195.03	-204.82	-182.92	-167.95



TEXAS INSTRUMENTS

Resources

- Try the WEBENCH Clock Architect tool **ti.com/clockarchitect**
- Find out more about TI clock and timing products, applications tools and support, visit **ti.com/clocks**
- **Visit ti.com**
- **Video**



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