Fixed Frequency Control vs Constant On-Time Control of Step-Down Converters

Voltage-mode/Current-mode vs D-CAP2™/D-CAP3™

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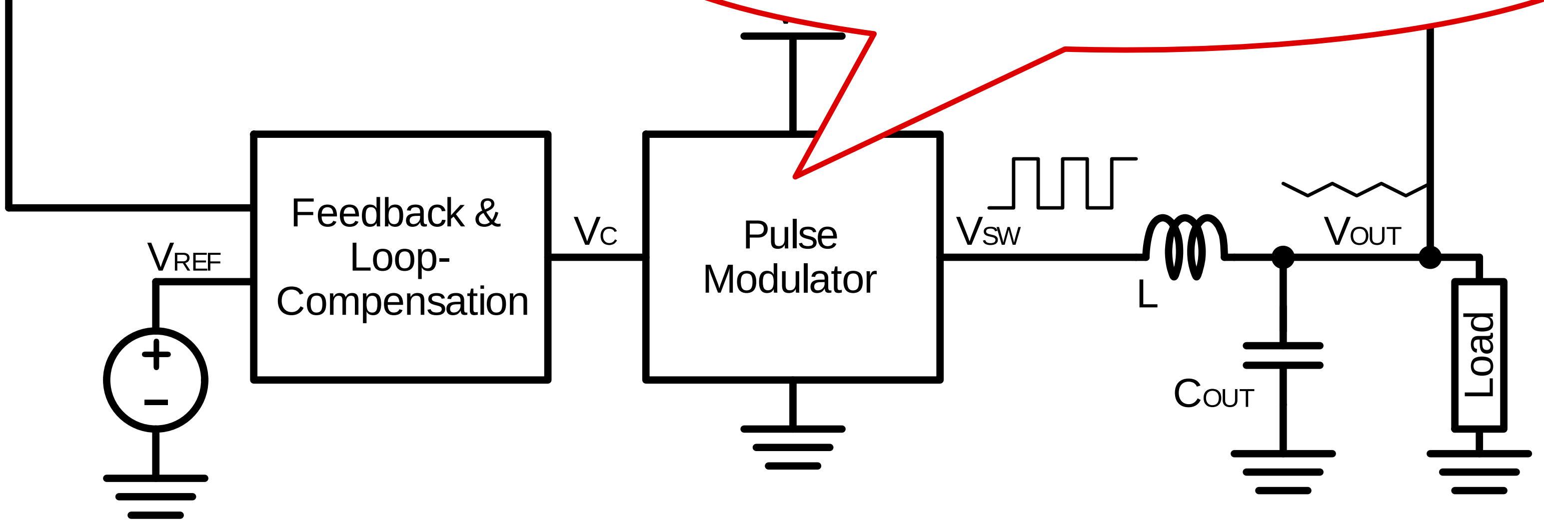
Contents

- Abbreviation/Acronym
- Quick history
- How each control mode works
- Large signal transient response
- Line transient response
- Loop stability (VM / CM / HM)
  - Bode plot
  - Output impedance plot
  - Small signal transient response
- Output voltage noise

BUCK CONVERTER BASIC

Common Operation of Step-Down (Buck) Converters

VM/CM: PWM Generator
HM: ON pulse Generator

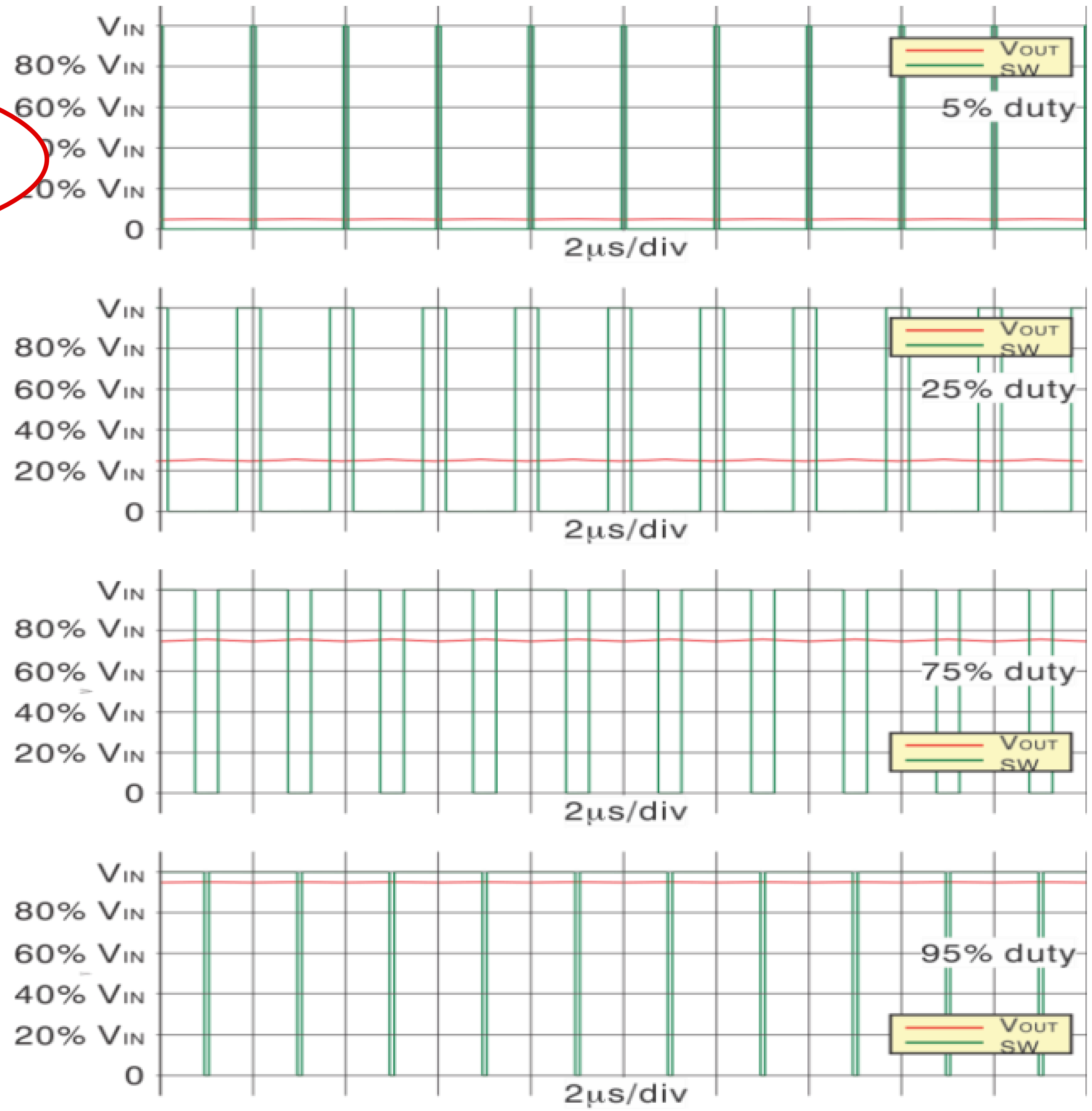


Equation at Stable Condition

$$D \times V_{IN} = V_{OUT}$$

With HM, Take “D” as pulse “Density”

Simulation Waveform



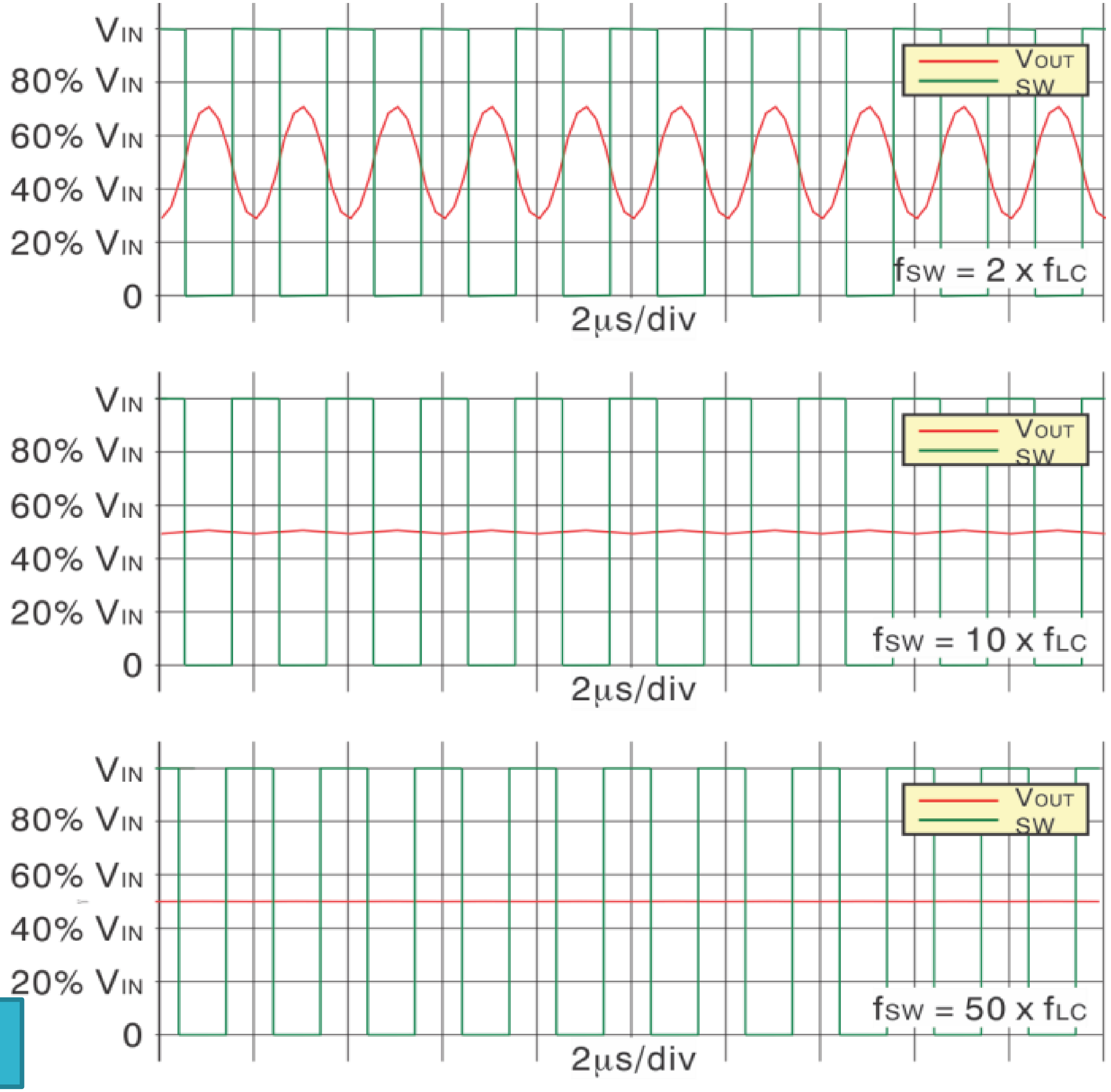
TEXAS INSTRUMENTS

Buck Conv. Common Operation: Switching Frequency

$$f_{LC} = \frac{1}{2 \cdot \pi \cdot \sqrt{L \cdot C_{OUT}}}$$

$f_{SW} > 10 \times f_{LC}$ $\quad \ldots OK$

$f_{SW} \approx 50 \times f_{LC}$ $\quad \ldots Recommended$



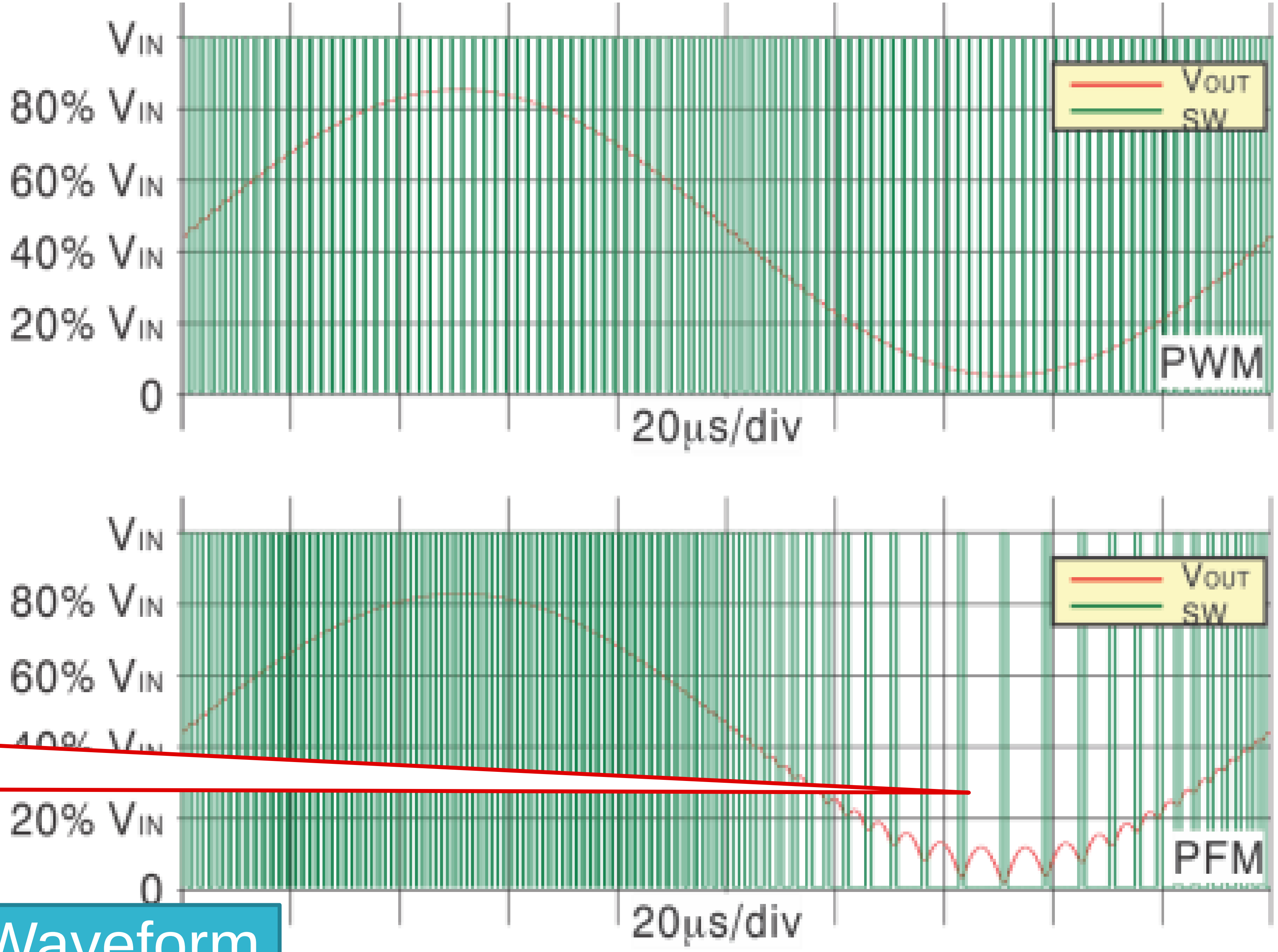
Simulation Waveform

Texas Instruments

Duty/Density Change VM/CM vs HM

- Force changing "D" control signal to monitor V_{OUT} response.
- V_{OUT} will just follow "D" over constant V_{IN}.

$$D \times V_{IN} = V_{OUT}$$



f_{SW} goes down approaching to f_{LC}

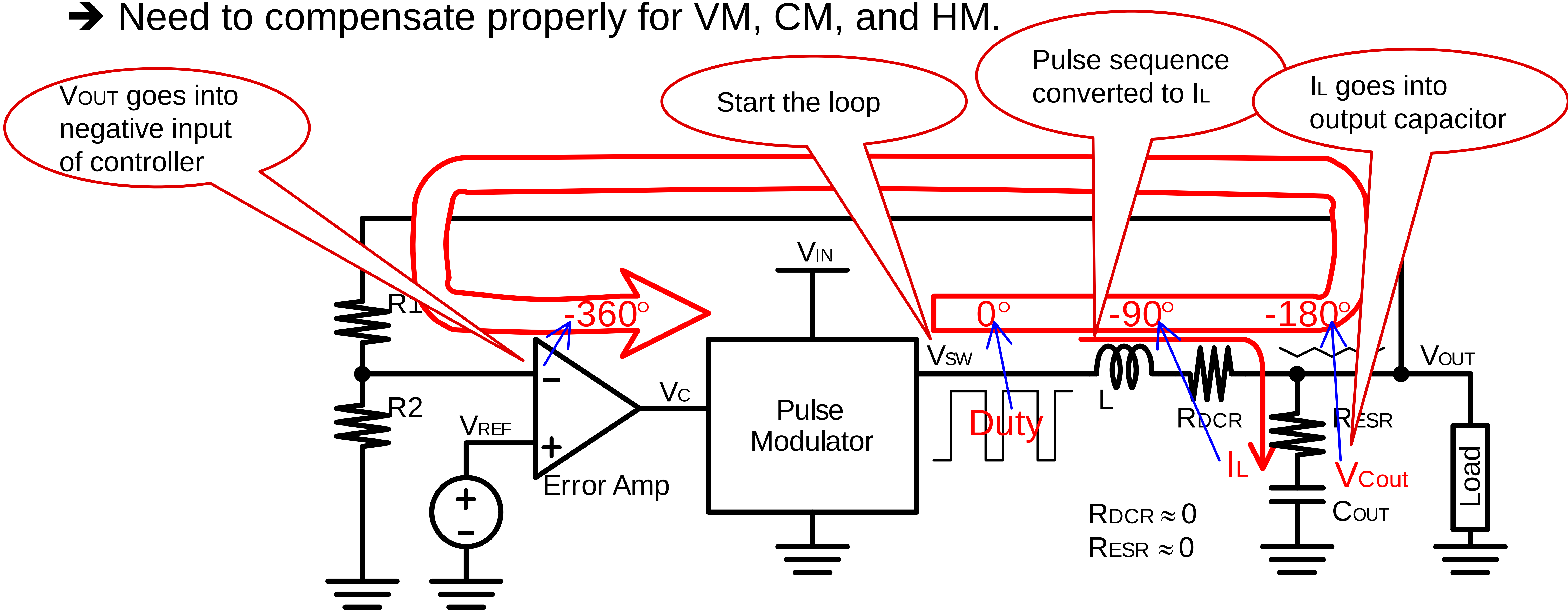
Simulation Waveform

BUCK CONVERTER COMPENSATION

TEXAS INSTRUMENTS

Buck Conv. Common without any Loop Compensation

- All buck-converter without any loop compensation is guaranteed to oscillate
  ➔ Need to compensate properly for VM, CM, and HM.



TEXAS INSTRUMENTS

Loop Compensation: Voltage Mode

$$f_{p0} \approx \frac{1}{2\pi \times R_1 C_1}$$

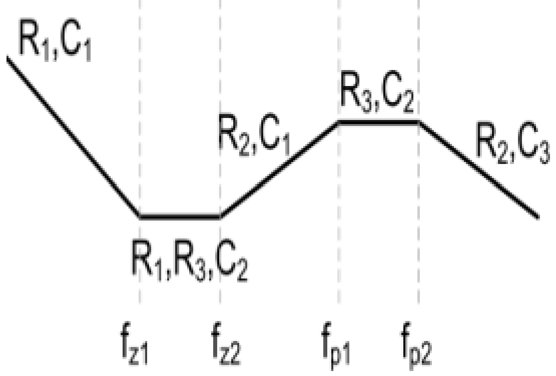
$$f_{p1} = \frac{1}{2\pi \times R_3 C_2}$$

$$f_{p2} \approx \frac{1}{2\pi \times R_2 C_3}$$

$$f_{z1} = \frac{1}{2\pi \times (R_1 + R_3) C_2}$$

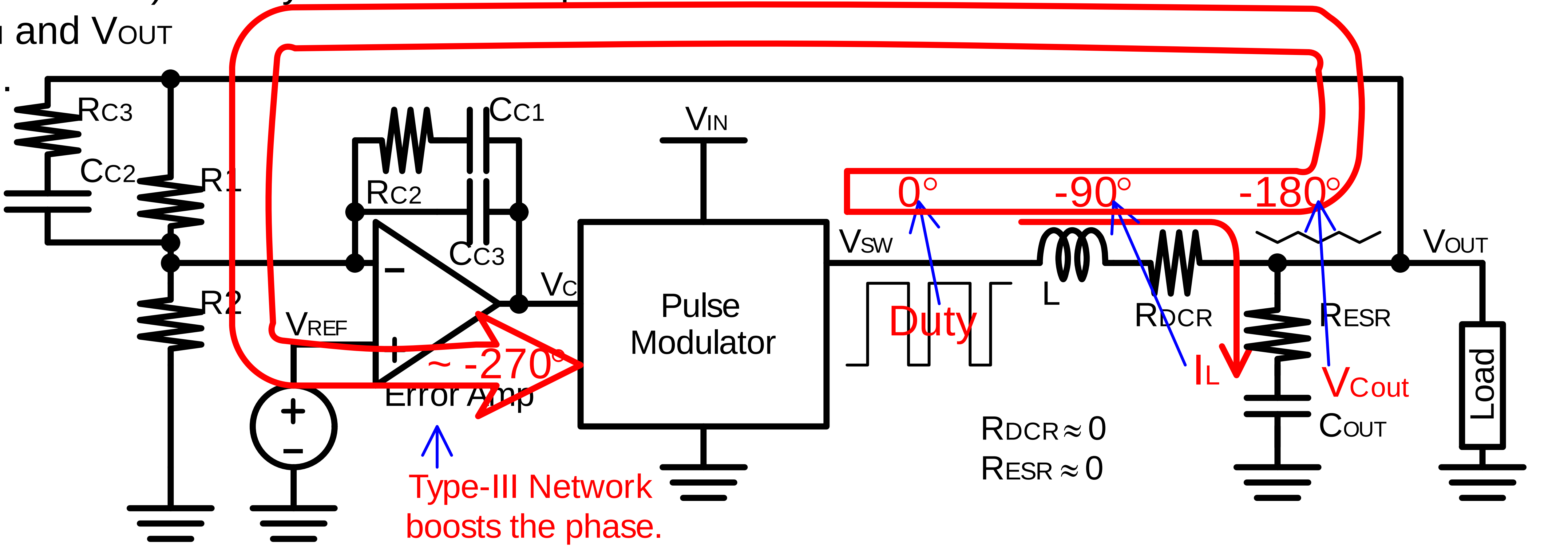
$$f_{z2} = \frac{1}{2\pi \times R_2 C_1}$$

Figure 7,
TI Apps Note
SLVA662



- Type-III compensation is popular, but tough to design
- The compensator re-shape feedback signal to boost phase back.

  ➔Completely free from handling output current information (unlike CM or HM). Always the same response over the same V_{IN} and V_{OUT} condition.



TEXAS INSTRUMENTS

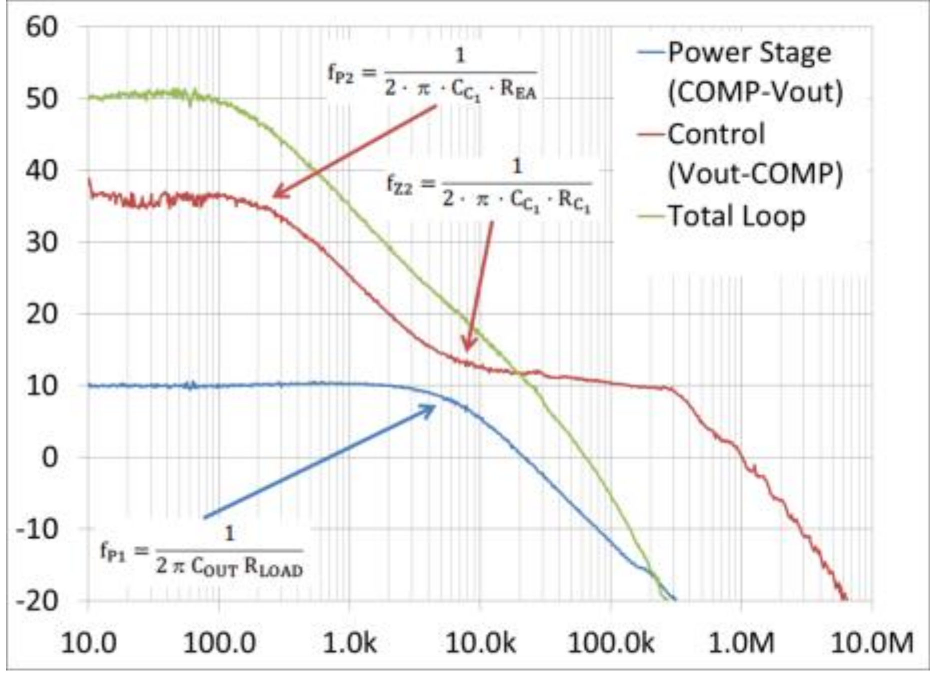
Loop Compensation: Current Mode

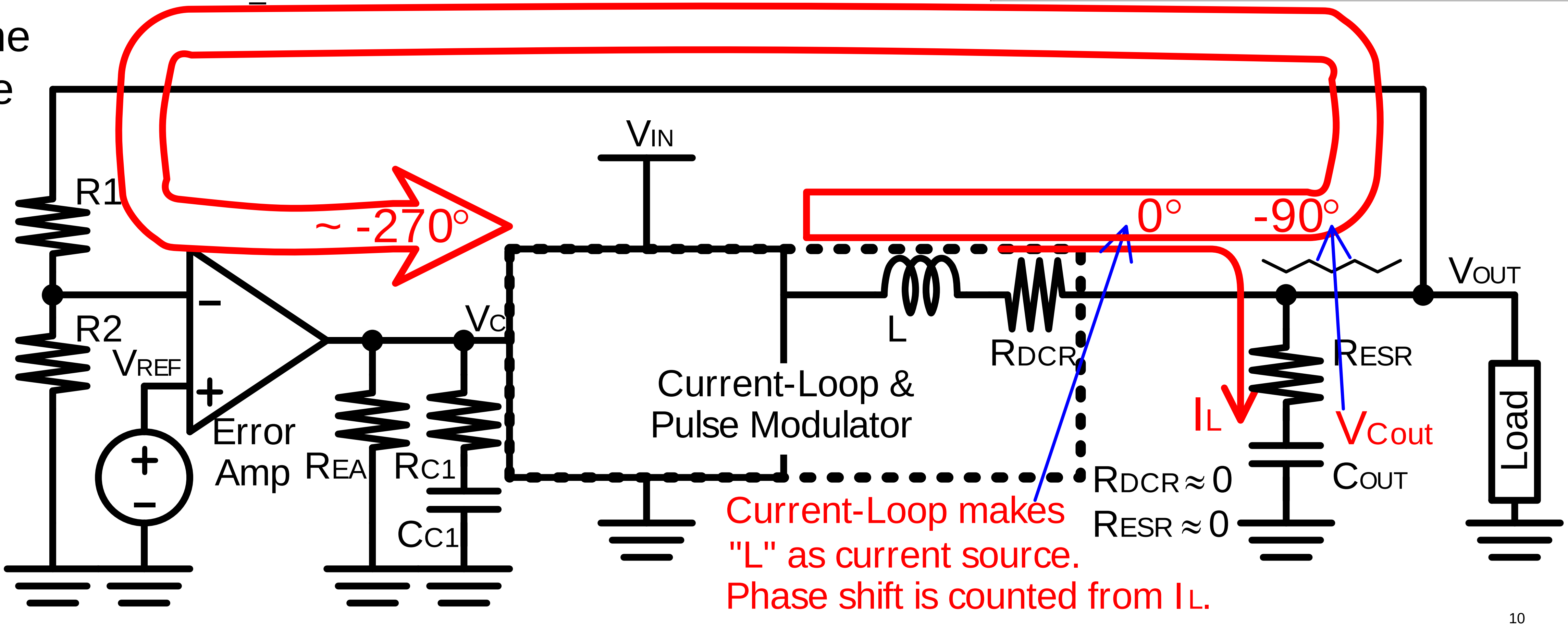
- Double-loop structure: the inner current-loop masks inductor from the main voltage-loop.
  - ➔Easy to calculate compensation component
  - ➔The loop is a heavy function of output current.
  - ➔Double-loop limits freq. configuration:

    $f_{SW} > f_{CURRENT\_LOOP} > f_{VOLTAGE\_LOOP}$

    With x10 rule, the main loop will be x100 slower than f_{SW}

TI Apps Note SLVA352A

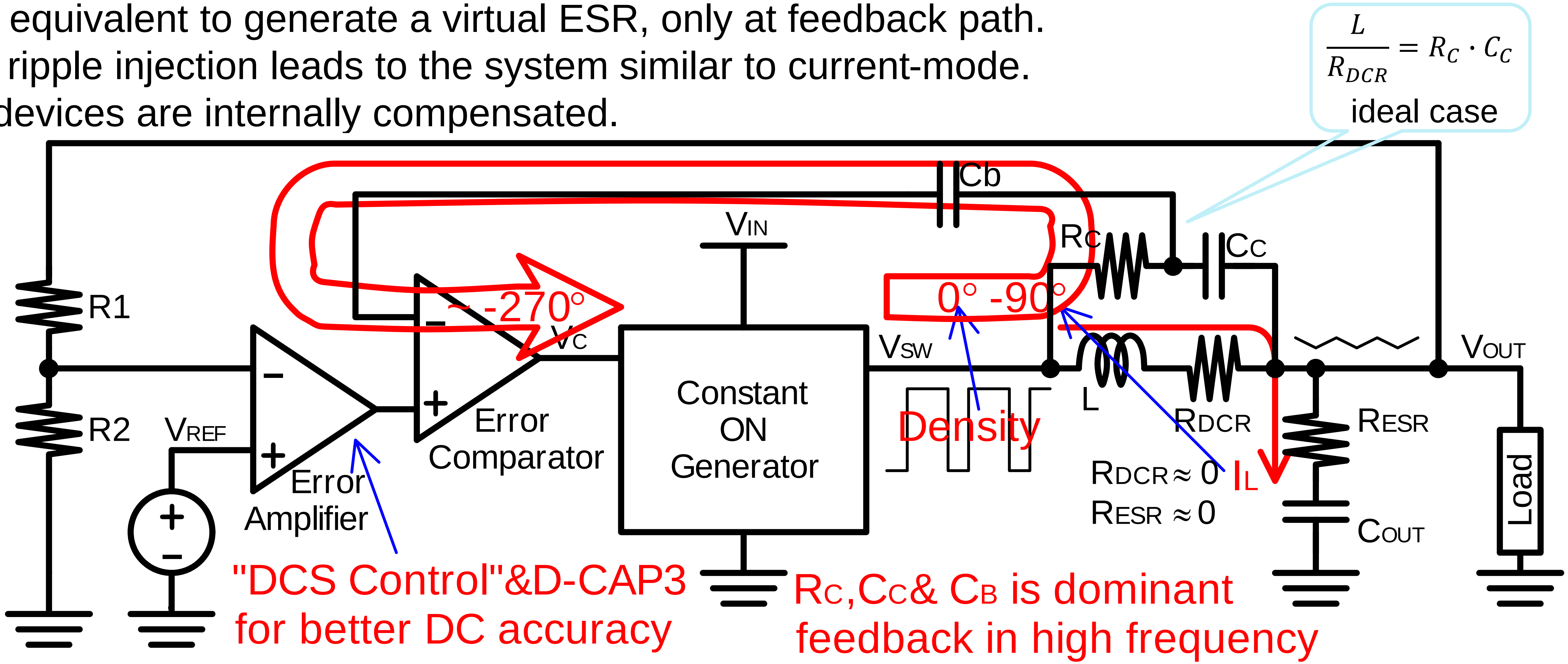




Texas Instruments

Loop Compensation: Hysteretic Mode

- Ripple injection method is popular to compensate.
- Basic idea is override feedback signal (could oscillate) with an output current "ripple" information.
  - ➔This is equivalent to generate a virtual ESR, only at feedback path.
  - ➔Heavy ripple injection leads to the system similar to current-mode.
  - ➔Many devices are internally compensated.

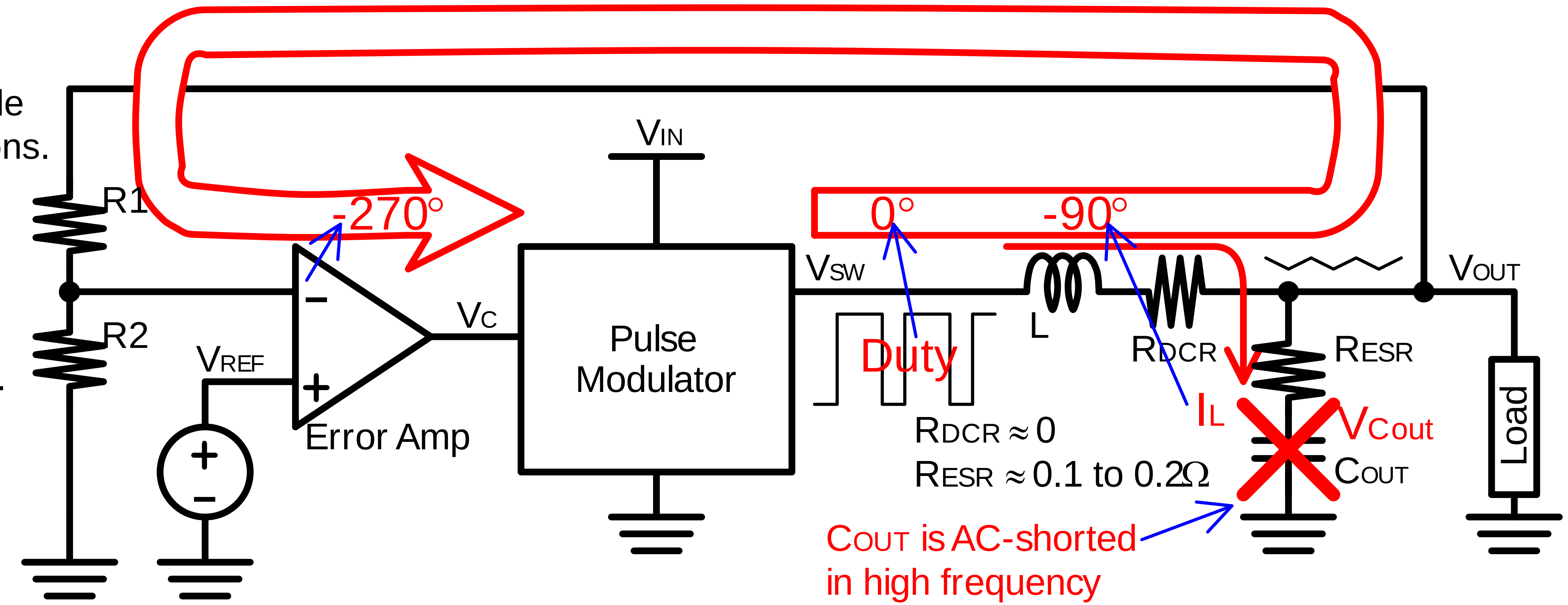


Almighty Loop Compensation (Debugging Only)

- Disregarding all other factors, old-days electrolytic capacitors or Tantalum capacitors will bring ultimate stability due to their high ESR.
- Frequency region above R_{ESR} and C_{OUT} resonant frequency, the output capacitor turns into resistor, so no 90° shift.

➔High ESR system generates huge amount of ripple that is not acceptable in most of applications. …not practical…

➔This method is very good for a debugging of unknown oscillation.



APPLE-TO-APPLE COMPARISON

Comparison Condition / Representative Parts

Parameter	Value	Note
Input Voltage Range (V_{IN})	5V to 12V	Select a device to work at both 5V and 12V
Output Voltage (V_{OUT})	1.2V	Popular voltage rail for many logic ICs
Maximum Output Current (I_{OUT})	5A	
Temperature	Room Temp	Just an ease of comparison, don't take high- or low-temperature data in this document
Switching Frequency (f_{SW})	Range of 600kHz to 700kHz	Analog ICs can't hit completely the same frequency. Set samples in narrow enough range.

Mode	Voltage-mode	Current-mode		Hysteretic-mode
Referred as	VM-IC	CM-IC	CM-IC2	HM-IC
Control mode detail	Voltage-Mode with Input Voltage Feed-forward	Peak-Current-Mode		D-CAP2
Compensation	Type-III	Type-II		Internal Ripple Injection
Input Voltage Range	4.5V to 16V	4.5V to 17V		4.5V to 18V
Output Current Max	6A	6A		6A
High-side FET	26mΩ (Integrated)	26mΩ (Integrated)		36mΩ (Integrated)
Low-side FET	13mΩ (Integrated)	19mΩ (Integrated)		28mΩ (Integrated)
Frequency	600kHz	633kHz	1.2MHz	688kHz
Inductor	1uH	3.3uH	3.3uH	1.5uH
Output Capacitor	22uF × 5 (Ceramic)	200uF (Ceramic)	220uF (Tantalum)	22uF × 2 (Ceramic)
L x Cout Resonant Freq.	15.2kHz	6.20kHz	5.91kHz	19.6kHz
Input Capacitor	To eliminate input impedance impact on the measurements, wide (frequency) range of bypass capacitors are connected at each board edge.			

Kept the original EVM design as much as possible

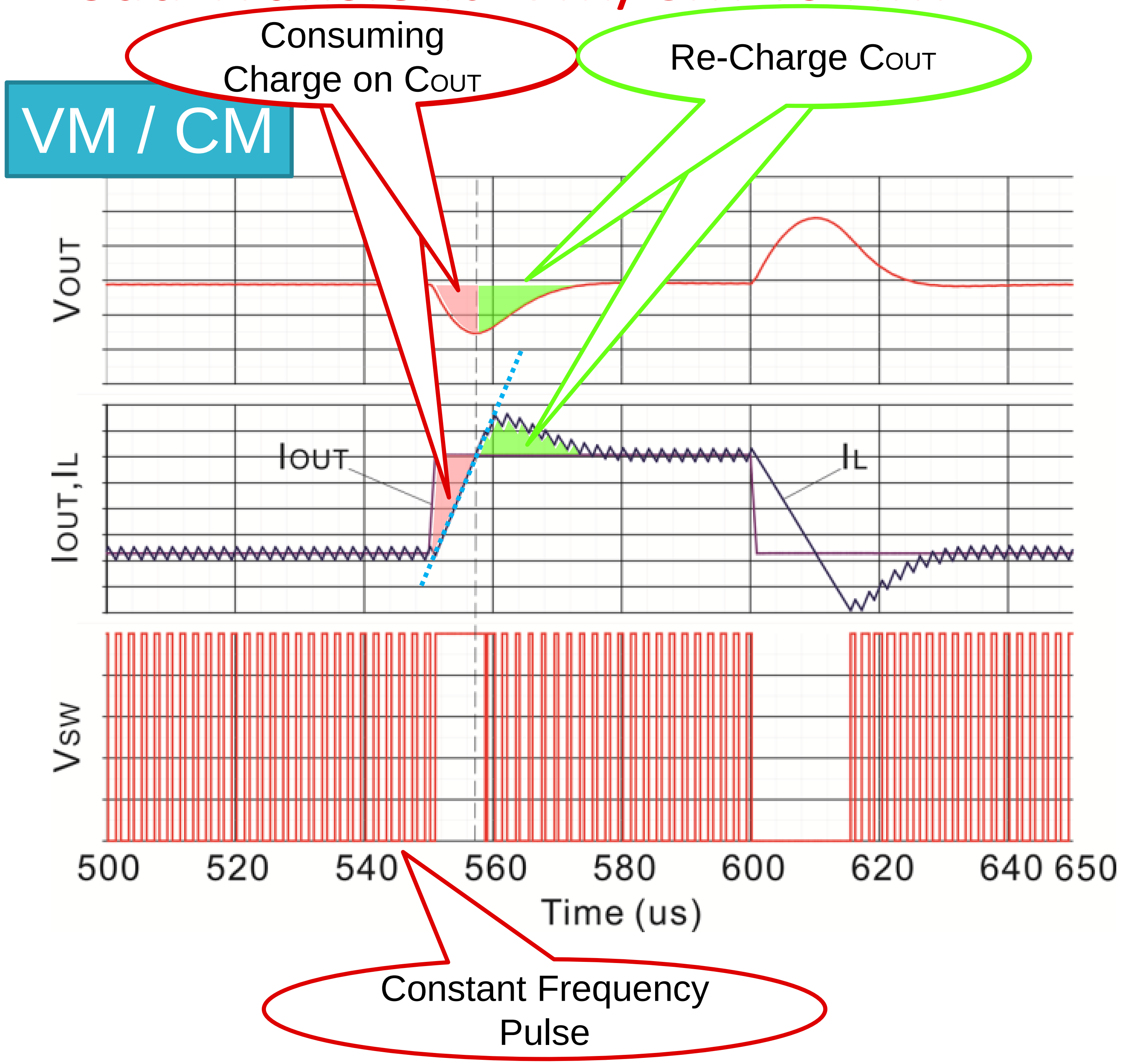
*1: for further comparisons, 2nd configuration of CM-IC is prepared whose EVM has a higher switching frequency setting.

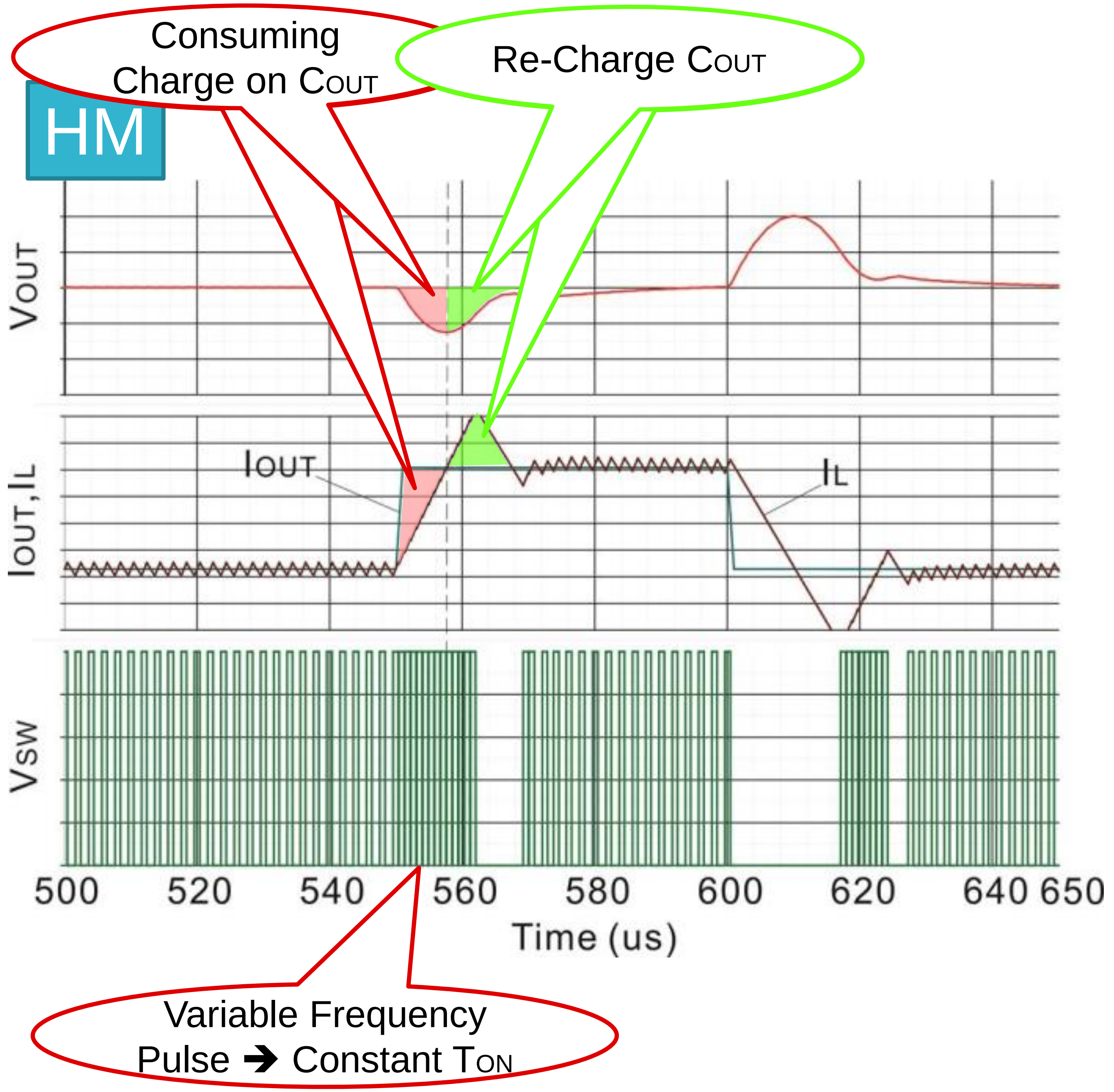
Apple-to-apple comparison

LARGE SIGNAL LOAD TRANSIENT RESPONSE PART 1: BASIC COMPARISON

Load Transient VM/CM vs HM

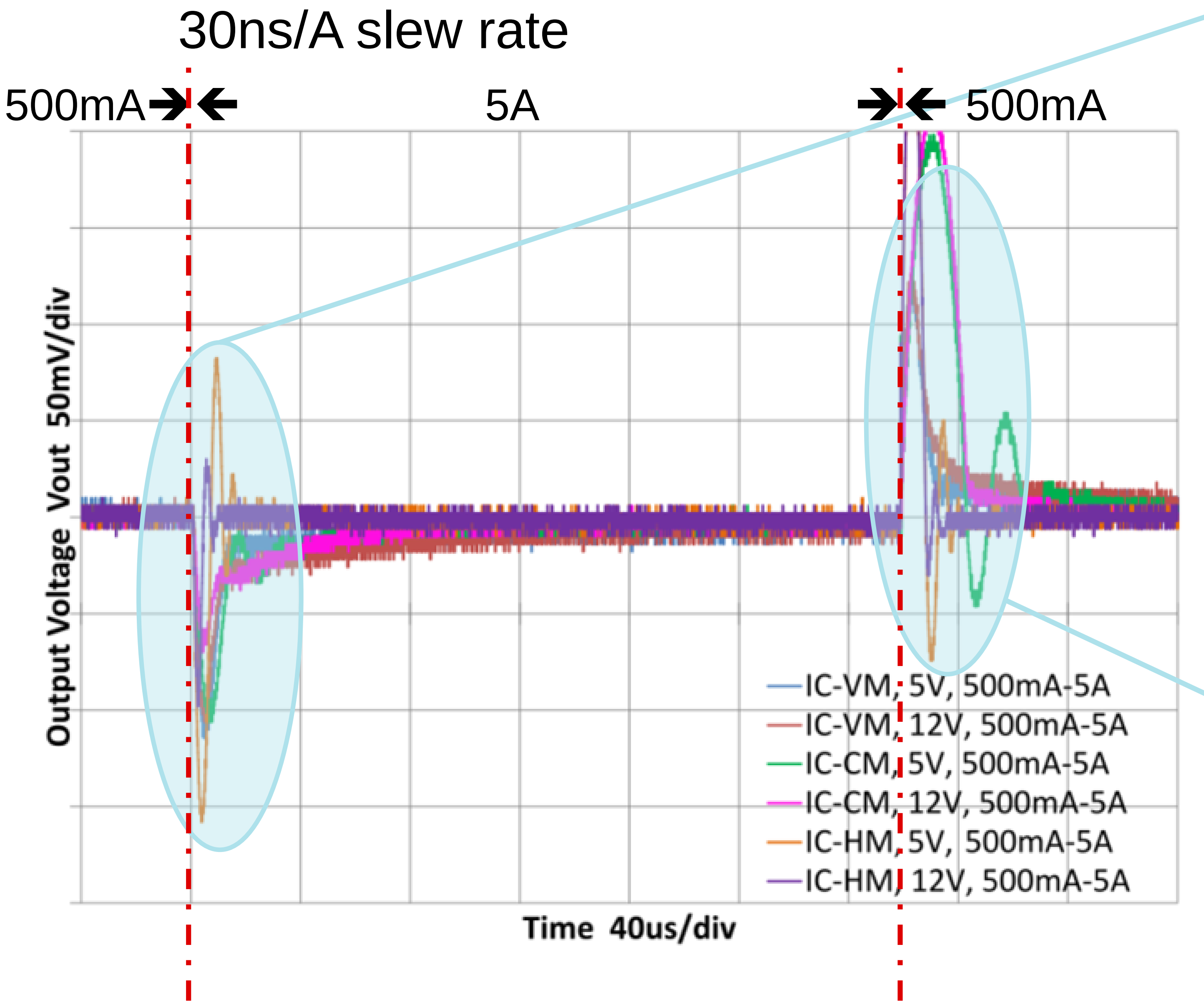
Simulation Waveform

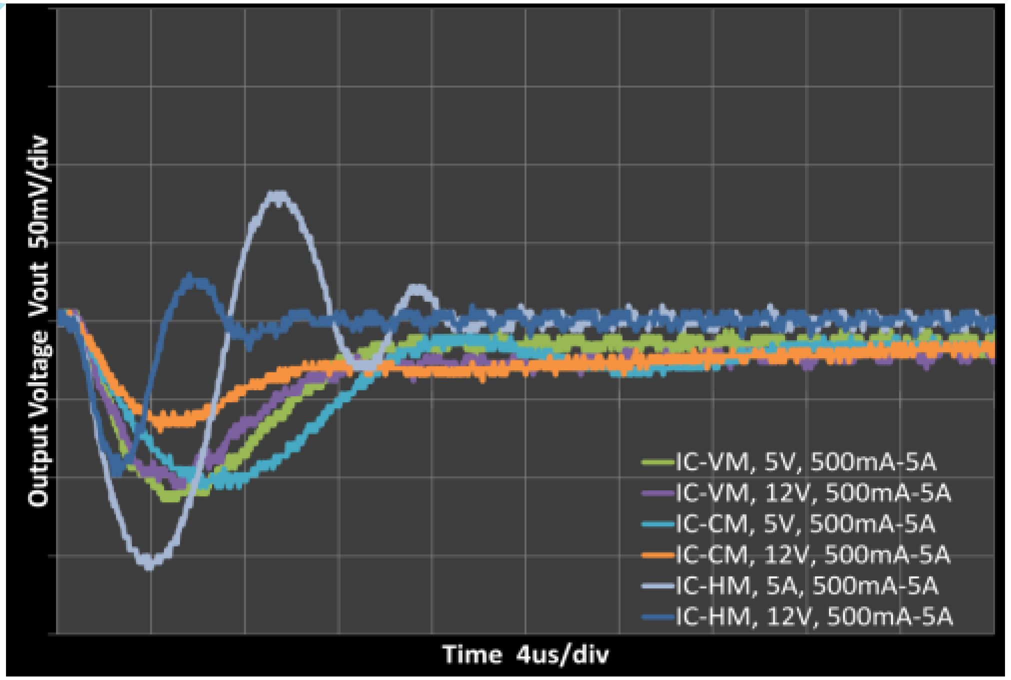


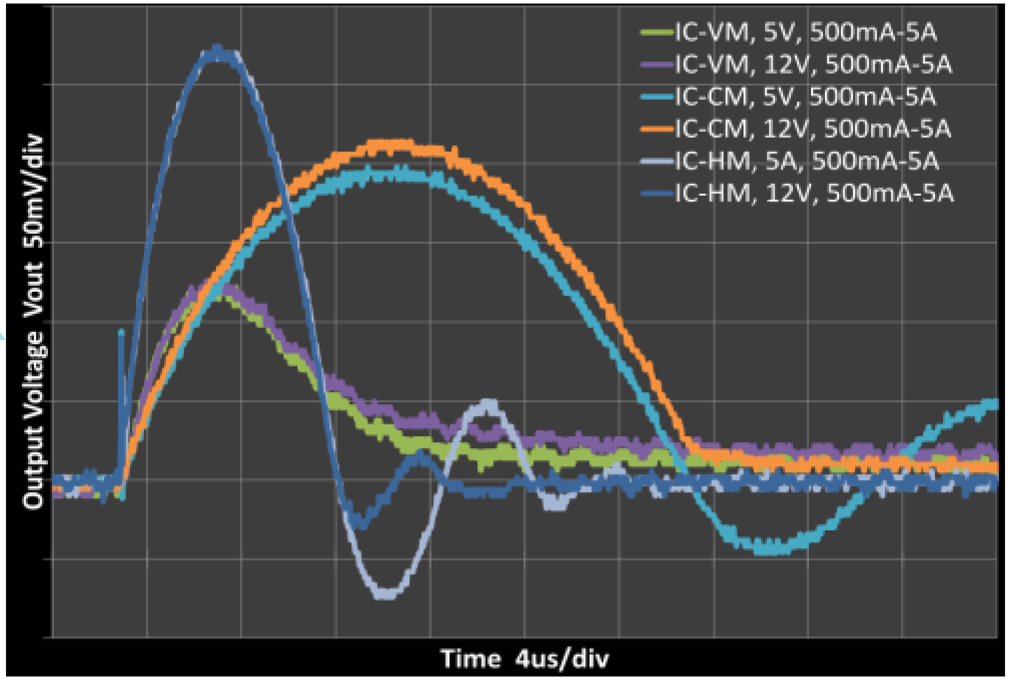


TEXAS INSTRUMENTS

Large Signal Load Transient Response







See next slide

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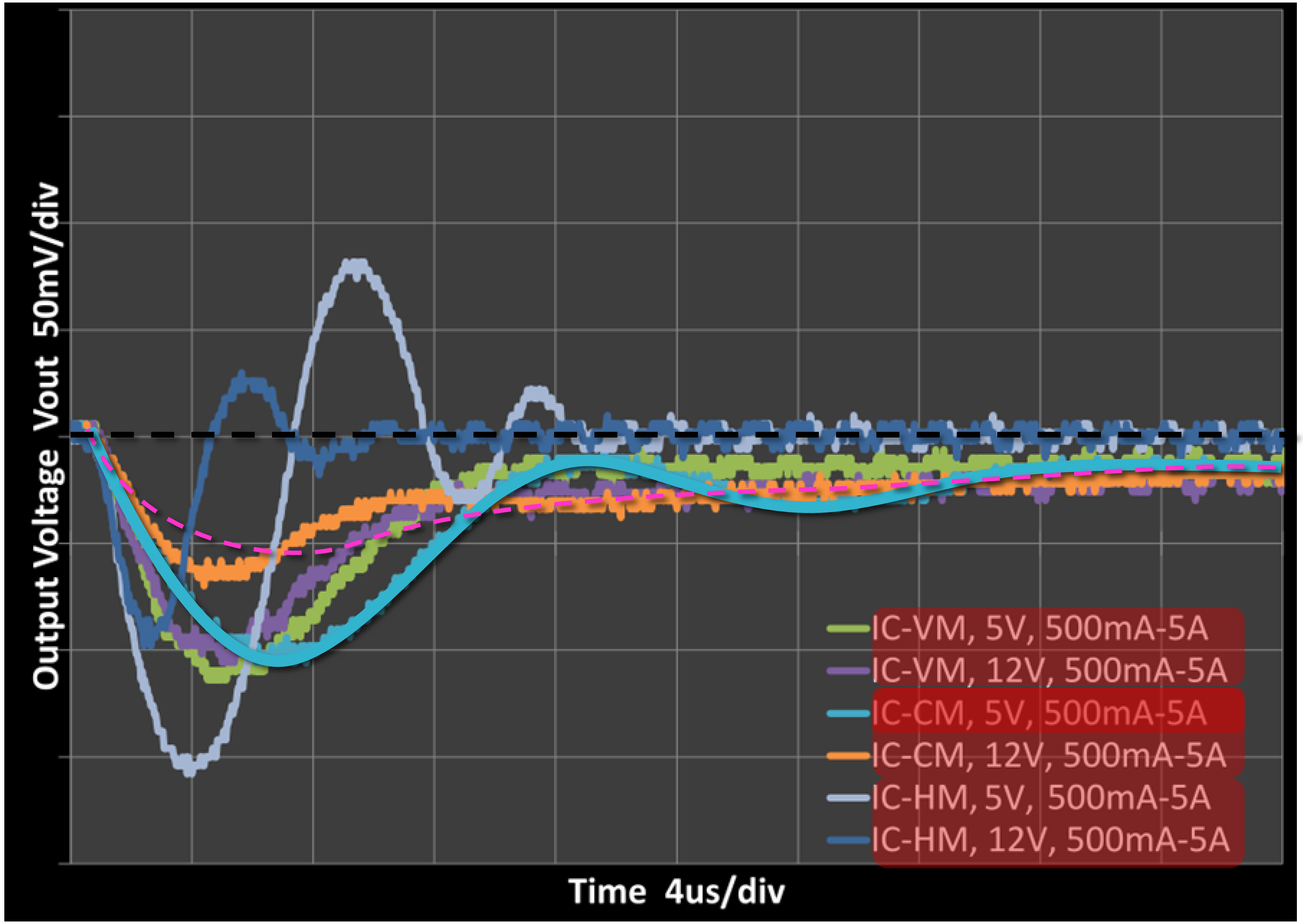
Large Signal Load Transient Response: Undershoot



V_{IN} Feed-forward,
$D \times V_{IN} = V_{OUT}$

VM-IC:

No V_{IN} difference, no ringing.

Recovery time ~ 15us

2 loops: V_{ERR} ➔ I_L ➔ V_{OUT}

$$\frac{dI_L}{dt} = \frac{V_{IN} - V_{OUT}}{L}$$

CM-IC:

Inner current-loop ringing before V_{OUT} recovery.

Recovery time ~ 15us

Only Comparator
$V_{OUT} > V_{TARGET}$

HM-IC:

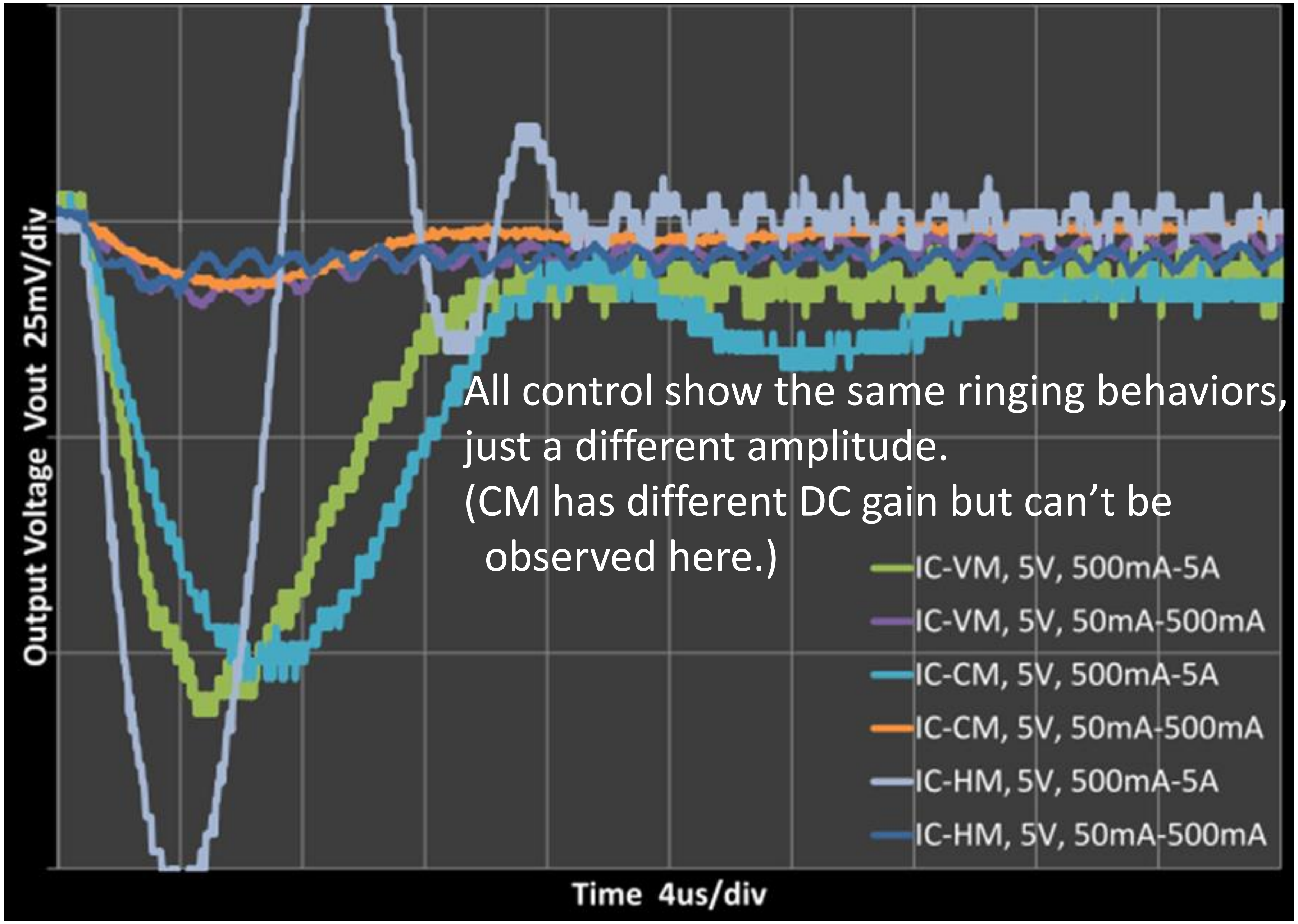
Ringing and bigger undershoot (less C_{OUT})

Recovery time ~ 5us-10us

Apple-to-apple comparison

LARGE SIGNAL LOAD TRANSIENT RESPONSE PART 2: COMPARISONS VARIOUS PARAMETERS

Large Signal Load Transient Response: IOUT Dependency



VM-IC:

No IOUT difference, only amplitude changes.

Recovery time ~ 15us

CM-IC:

Inner current-loop ringing before VOUT recovery.

Recovery time ~ 15us

HM-IC:

DC voltage error (light-load mode)

Recovery time ~ 4us

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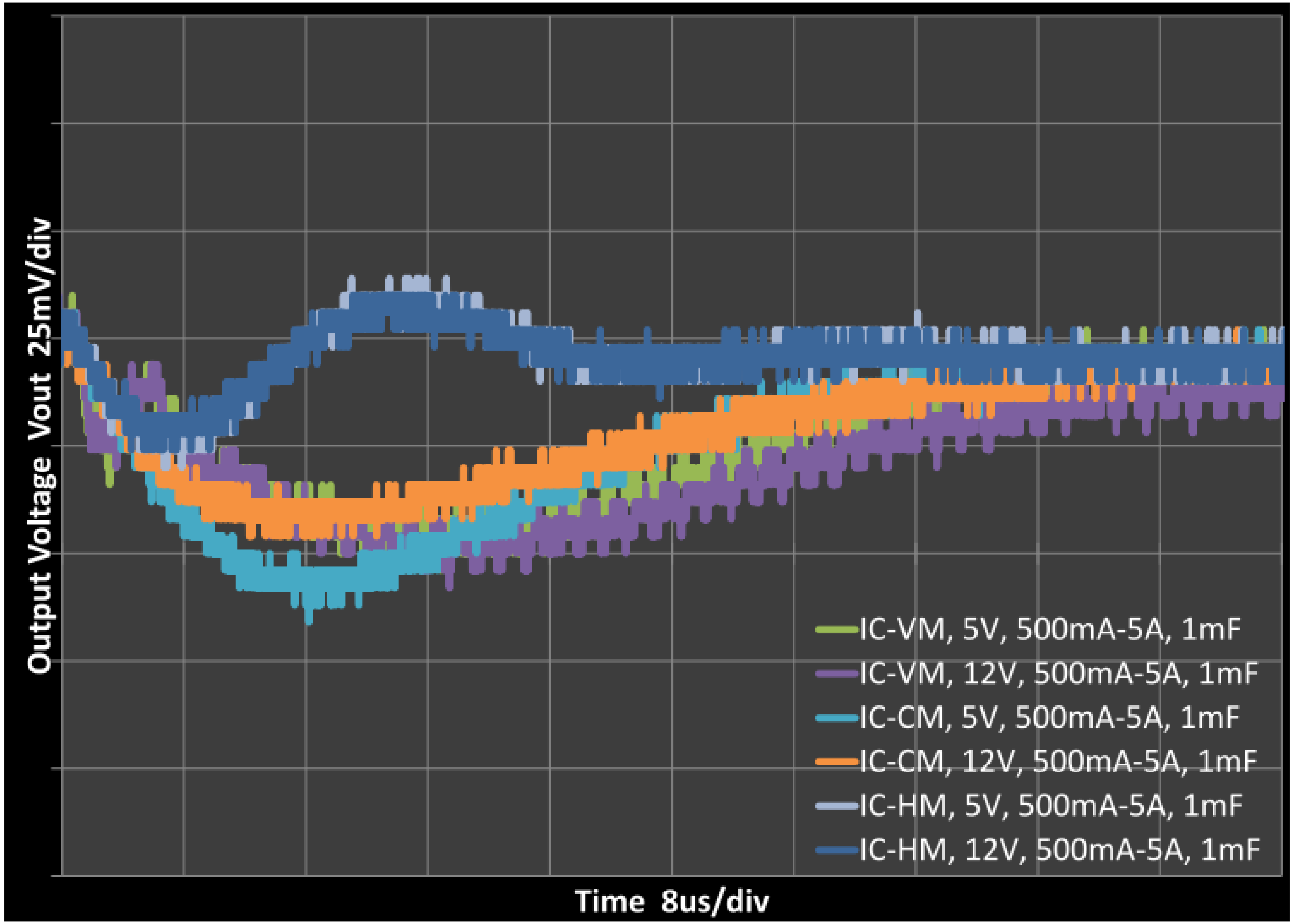
Large Signal Load Transient Response: C_{OUT} = 1mF



VM-IC:

Recovery time ~ 60us

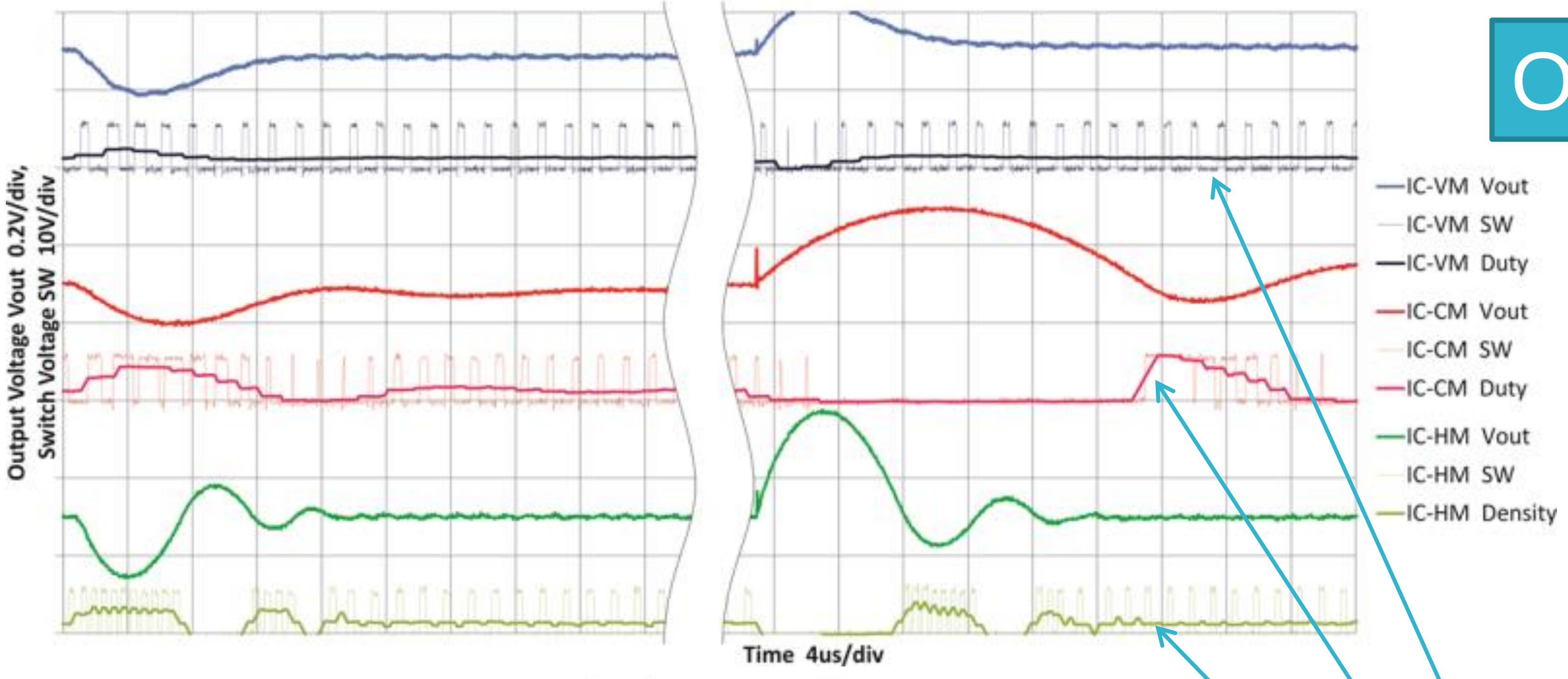
CM-IC:

Recovery time ~ 50us

HM-IC:

Recovery time ~ 30us

Large Signal Load Transient Response: Pulse Behavior



Original Board

VM-IC:

Very slow and smooth duty control

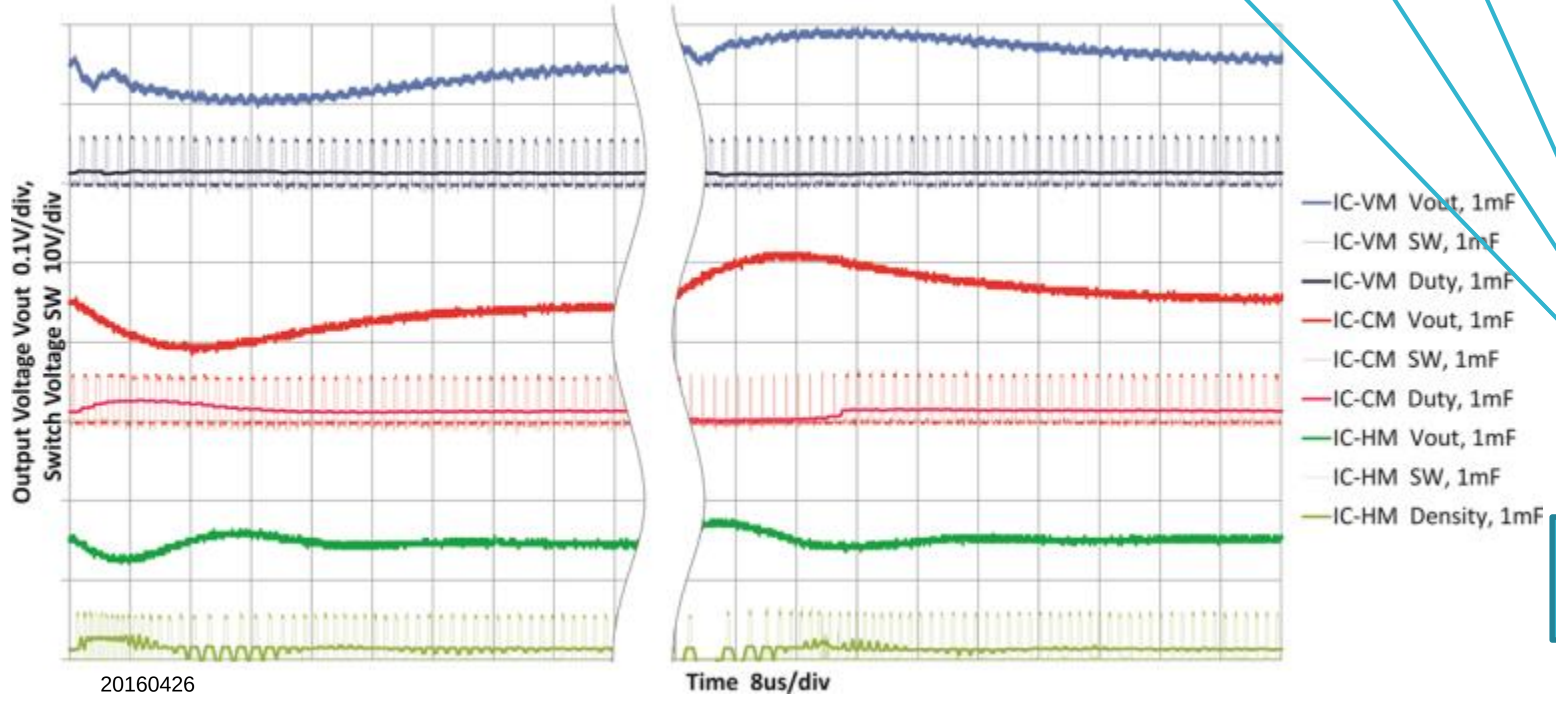
CM-IC:

Moderately fast duty control

HM-IC:

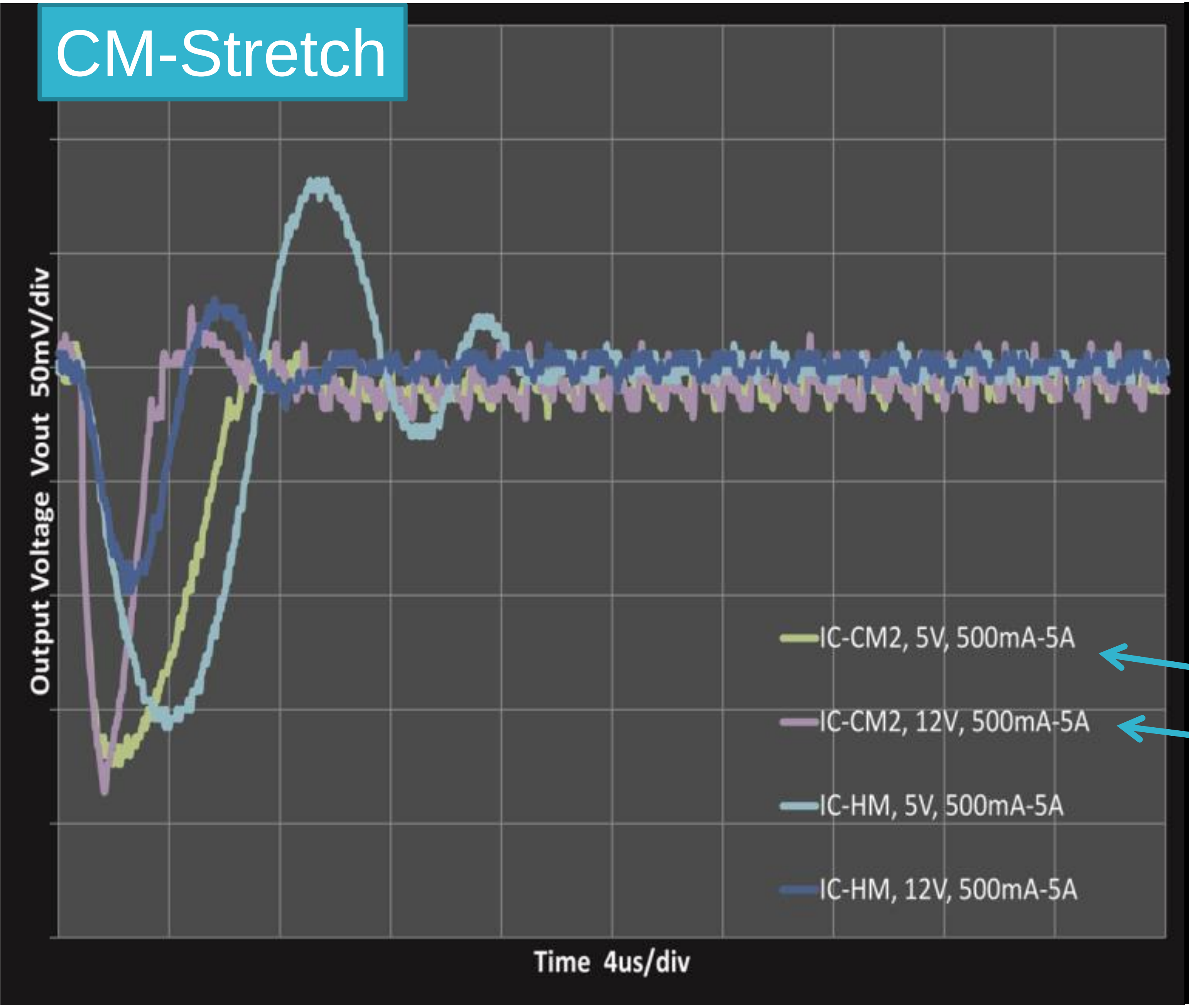
Very fast and aggressive pulse-density control → <u>Variable switching frequency: work harder only when needed</u>.

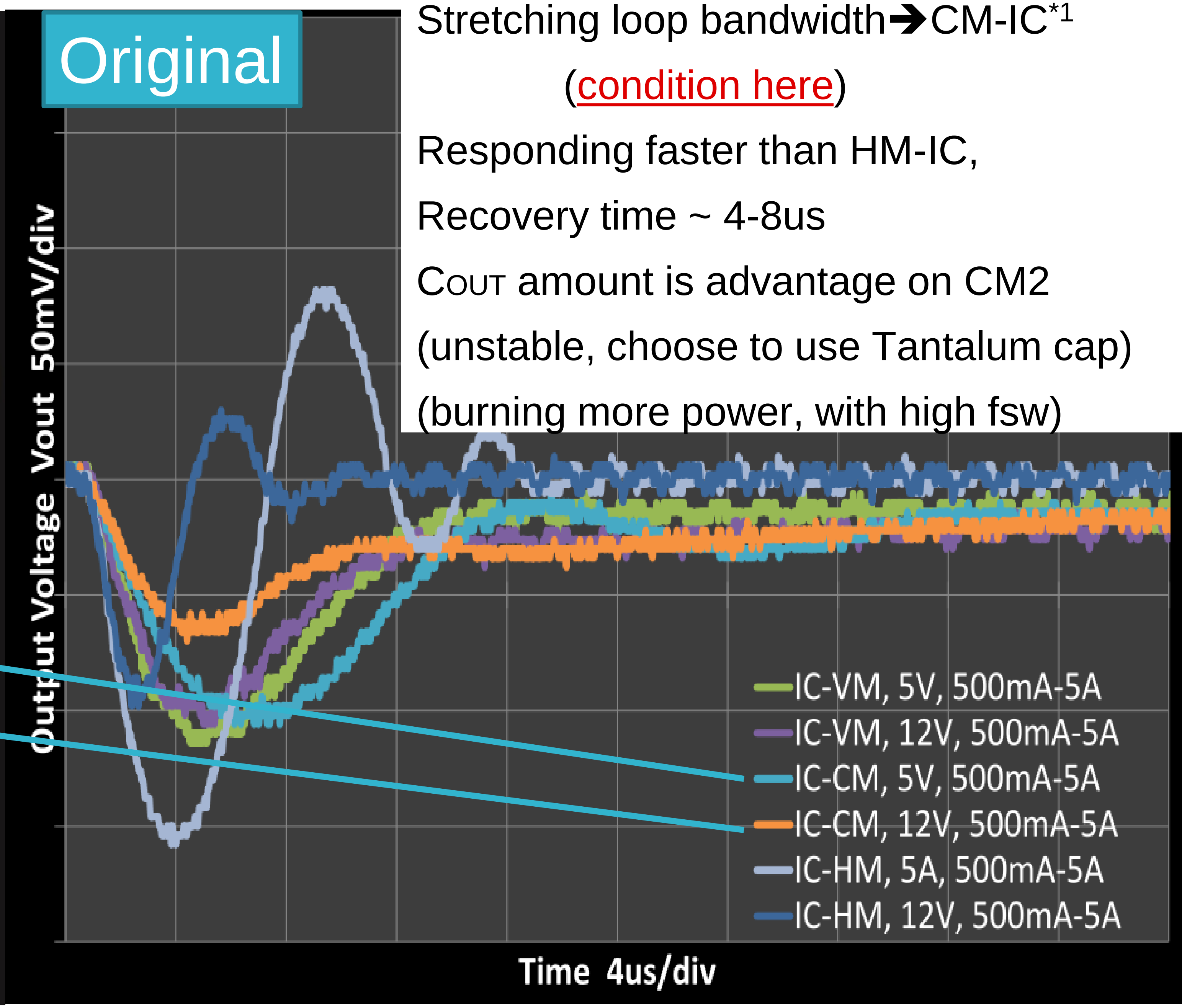
Per cycle averaged duty



1mF COUT

Large Signal Load Transient Response: Stretched CM-IC





Stretching loop bandwidth➔CM-IC*1

(condition here)

Responding faster than HM-IC,

Recovery time ~ 4-8us

C_{OUT} amount is advantage on CM2

(unstable, choose to use Tantalum cap)

(burning more power, with high fsw)

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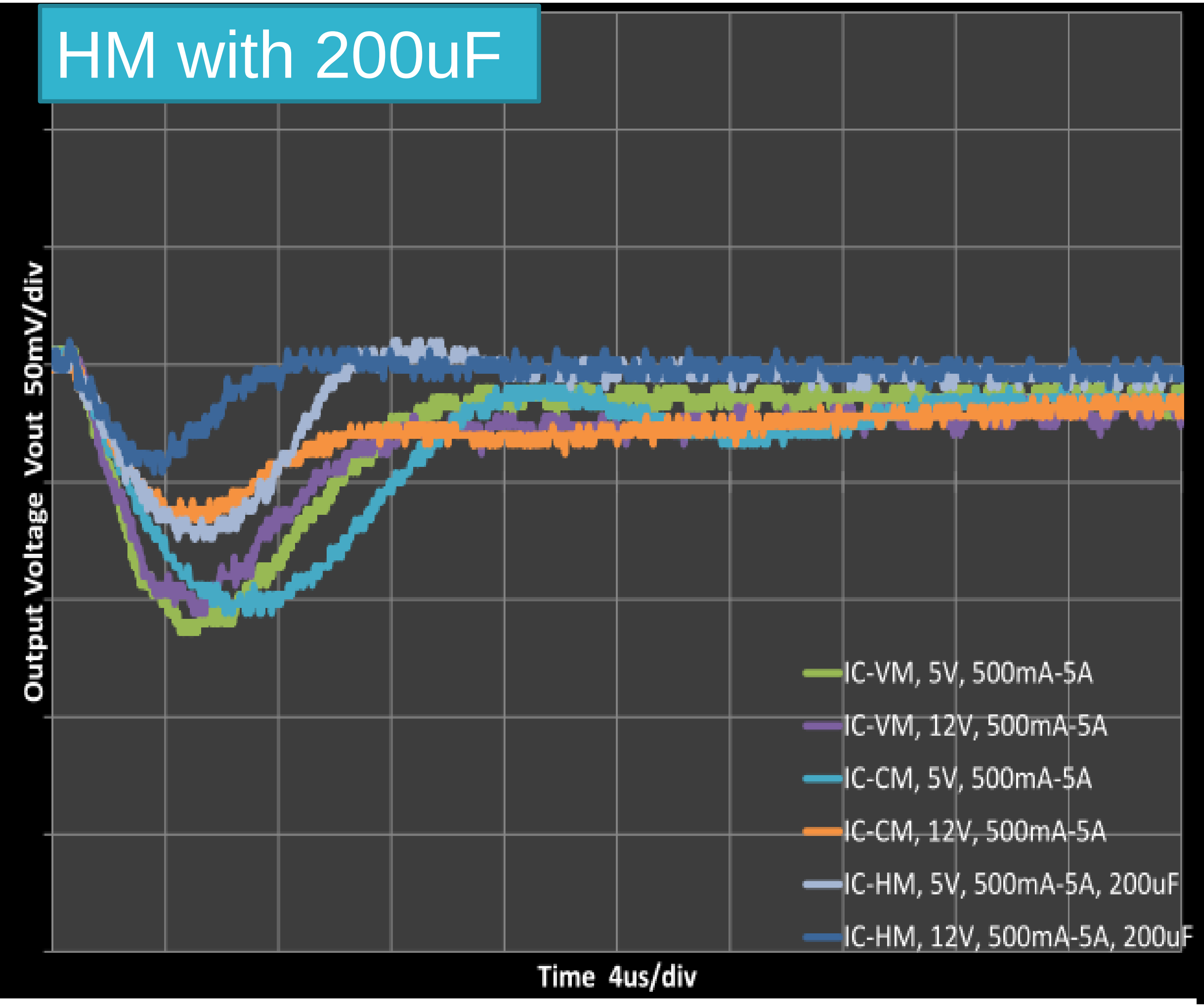
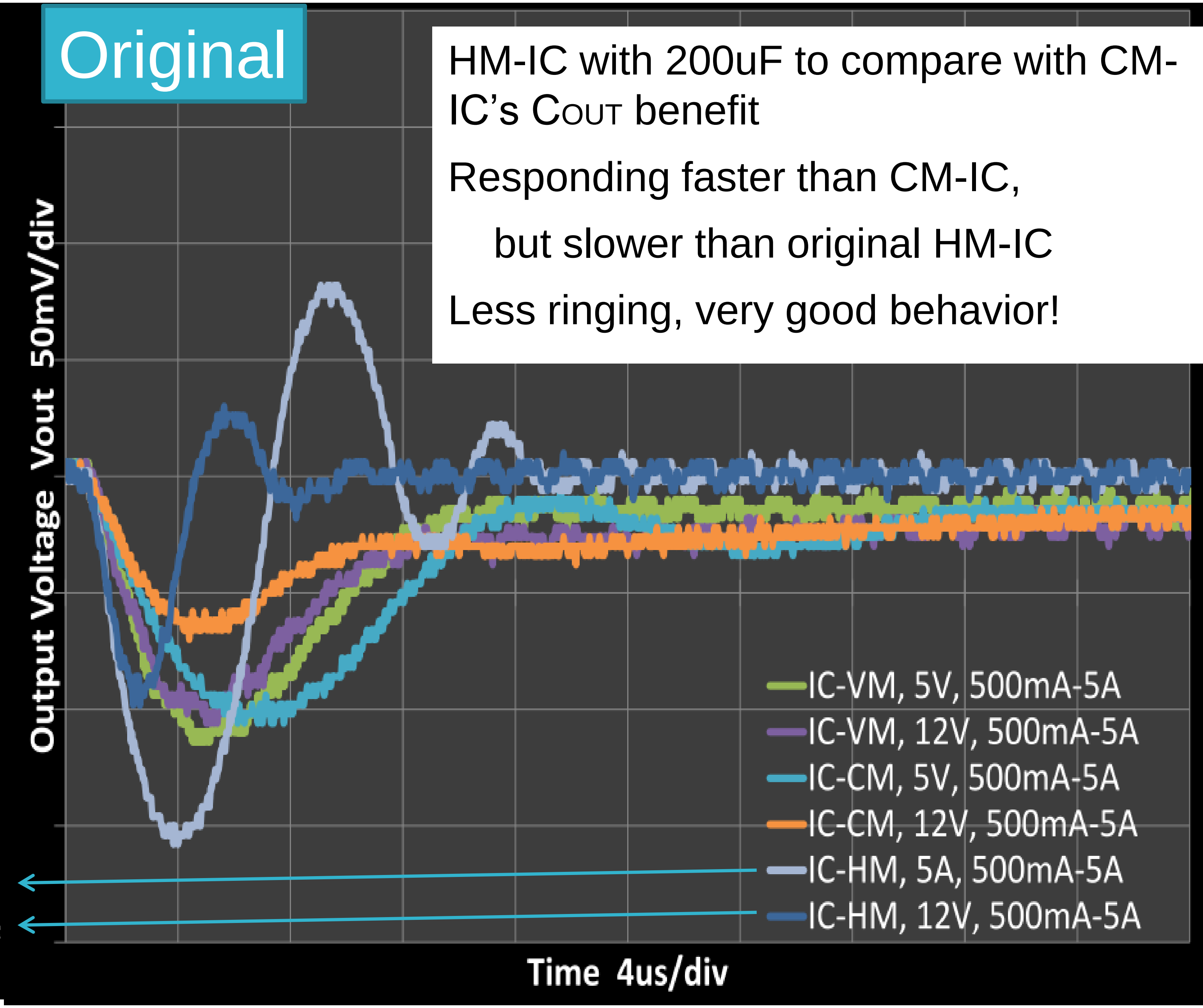
Large Signal Load Transient Response: HM-IC Bigger COUT





HM-IC with 200uF to compare with CM-IC's COUT benefit

Responding faster than CM-IC,

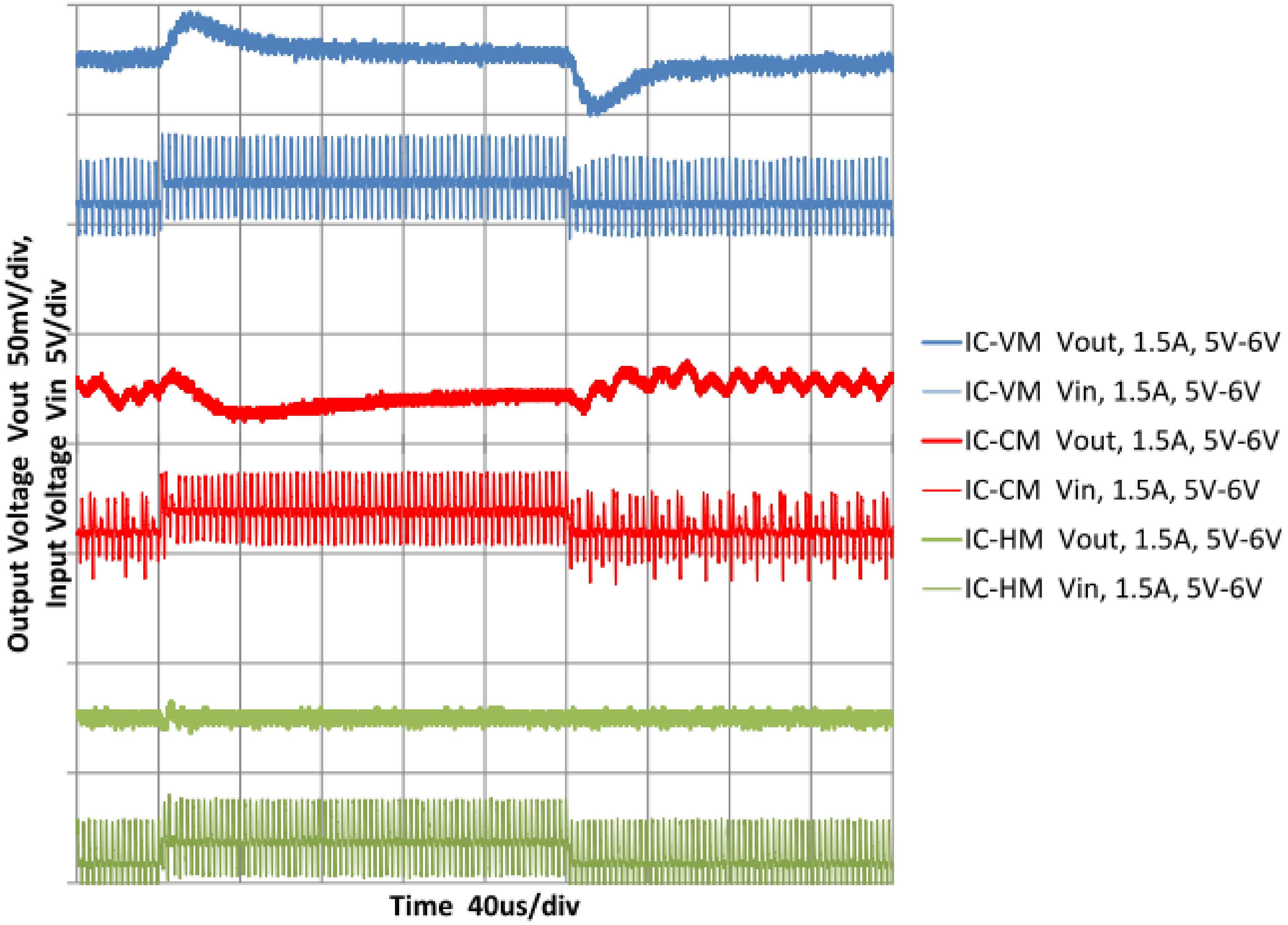
but slower than original HM-IC

Less ringing, very good behavior!

Apple-to-apple comparison

LINE TRANSIENT RESPONSE

Line Transient Response



VM-IC:

Smooth waveforms

Recovery time ~ 40us

CM-IC:

Edge of stability (0.1uF input cap)

Recovery time ~ 80us

HM-IC:

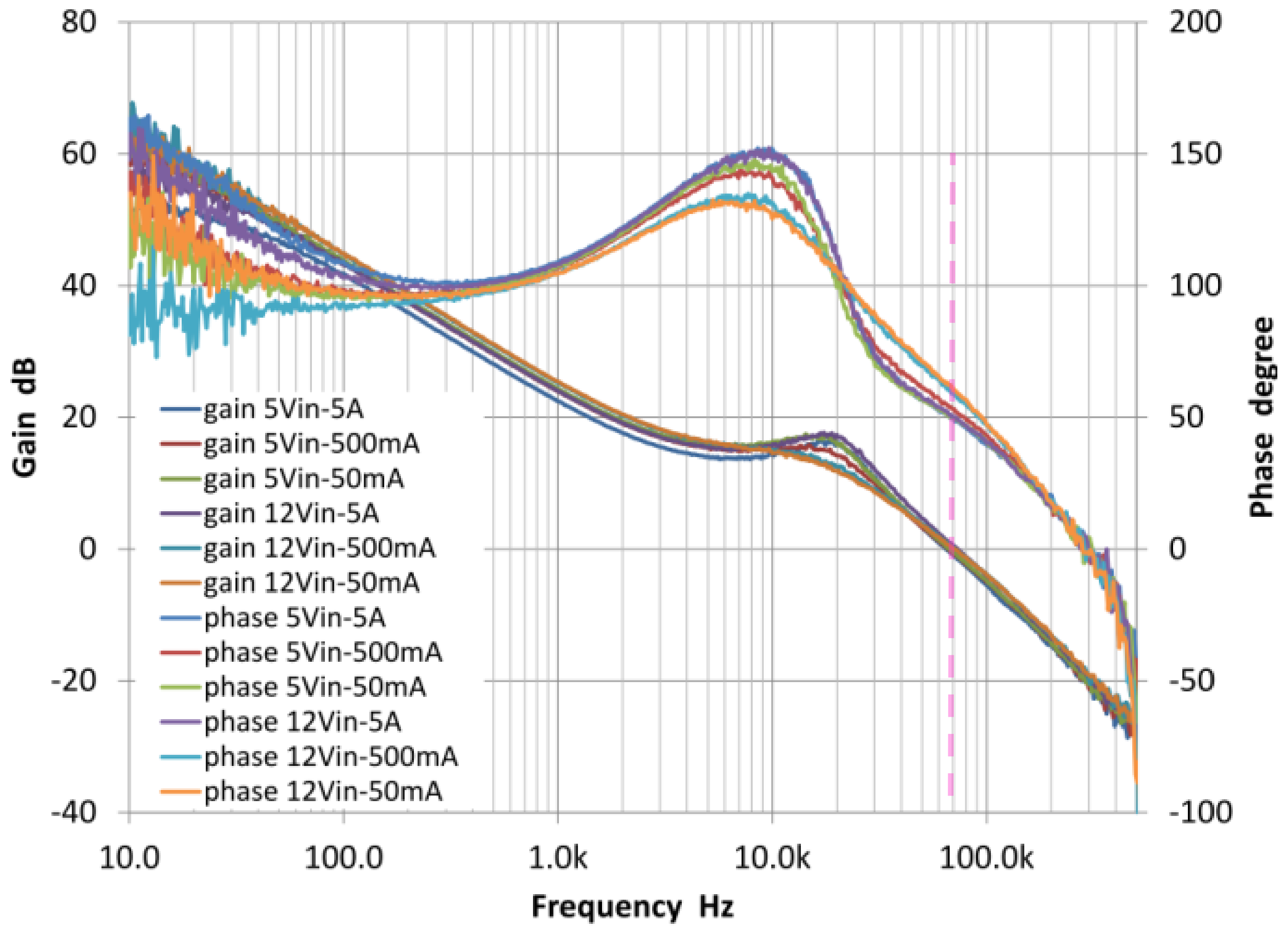
Perfect response

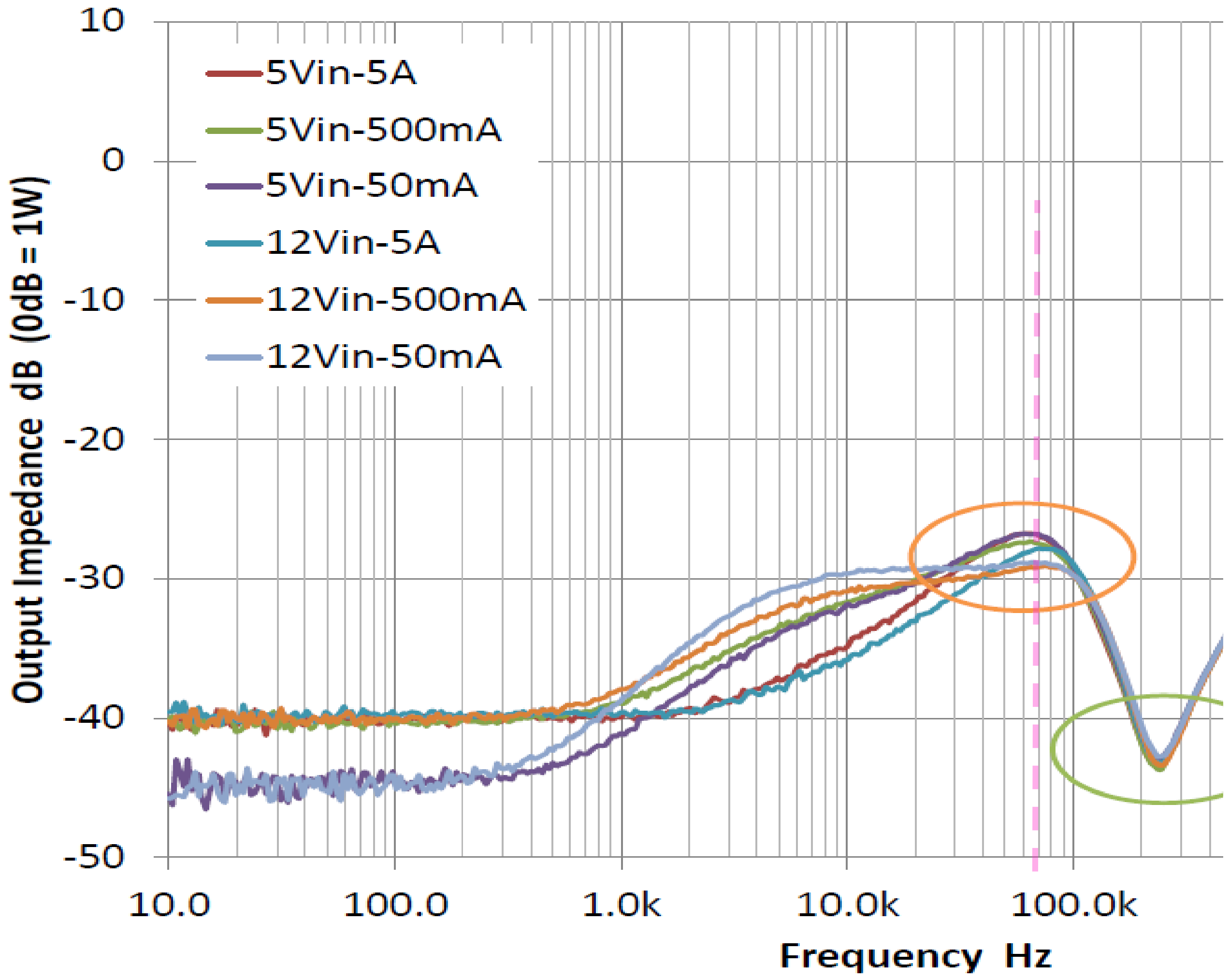
Recovery time (can't observe glitches)

Apple-to-apple comparison

LOOP STABILITY / SMALL SIGNAL STUDY VOLTAGE-MODE

Stability (Bode/ZOUT): VM-IC





Compared with CM-IC (shown later), very consistent gain & phase curves over VIN and IOUT. Harder to design type-III compensation but consistent response once it's designed.

See next slide for phase margin values

Texas Instruments

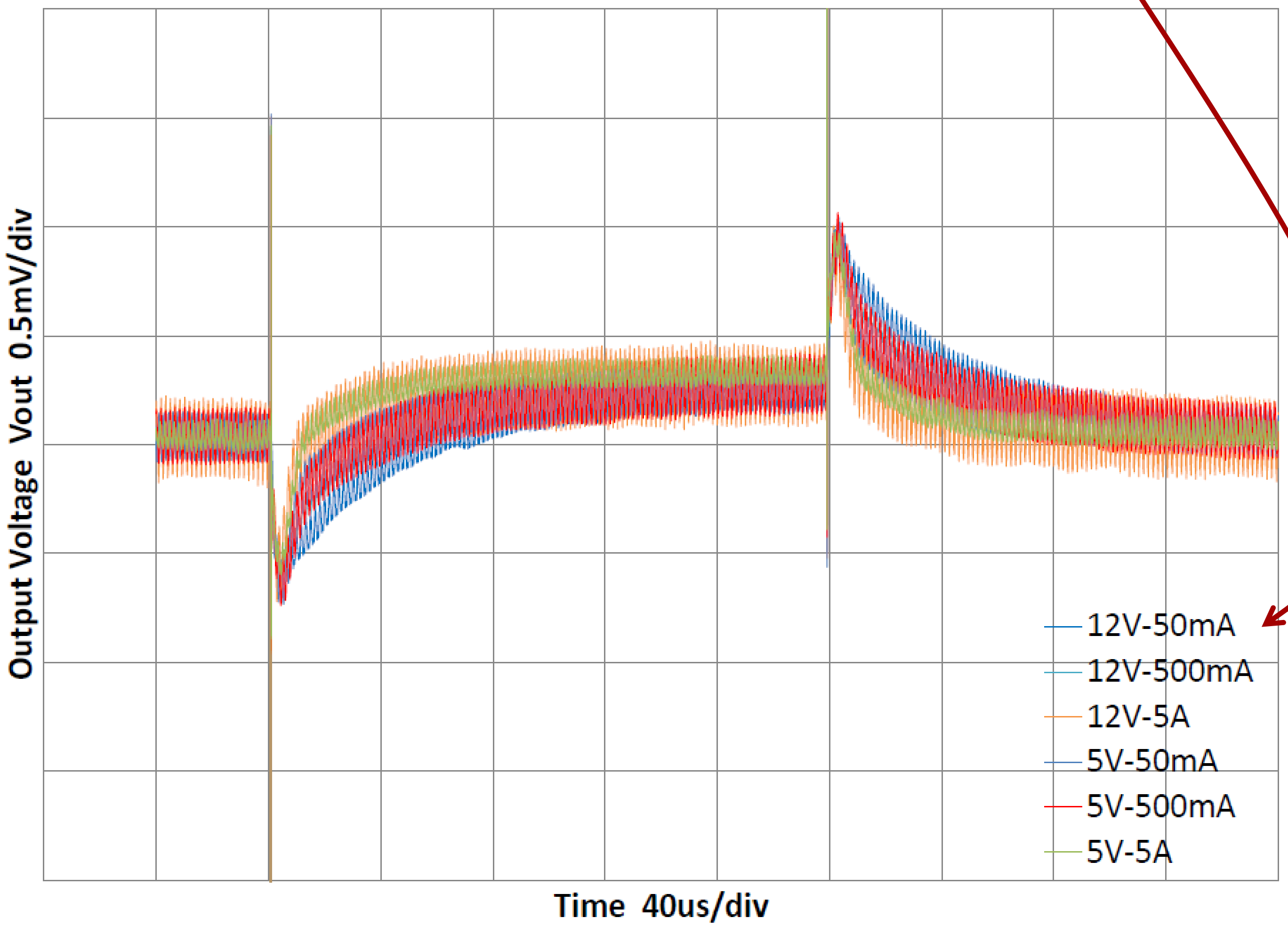
Stability (PM, Small-Signal Transient): VM-IC

Condition	Phase Margin	
	from Bode-plot	from Output Impedance
5Vin-5A	51.3° at 65.0kHz	61.0° at 86.5kHz
5Vin-500mA	54.0° at 67.3kHz	66.1° at 75.8kHz
5Vin-50mA	50.3° at 67.3kHz	62.5° at 82.0kHz
12Vin-5A	49.5° at 72.3kHz	58.4° at 92.2kHz
12Vin-500mA	57.6° at 72.3kHz	68.6° at 112kHz
12Vin-50mA	59.6° at 72.3kHz	> 71°

Phase Margin (Degrees)	Ringing (Bumps)
80.88	0
60.75	0
57.64	0
54.08	0
50.16	1
45.7	1.5
40.61	2
34.72	3
27.78	4
19.43	6
9.09	17

Table 1,
TI Apps Note SLVA381B

10mA load transient over DC current load

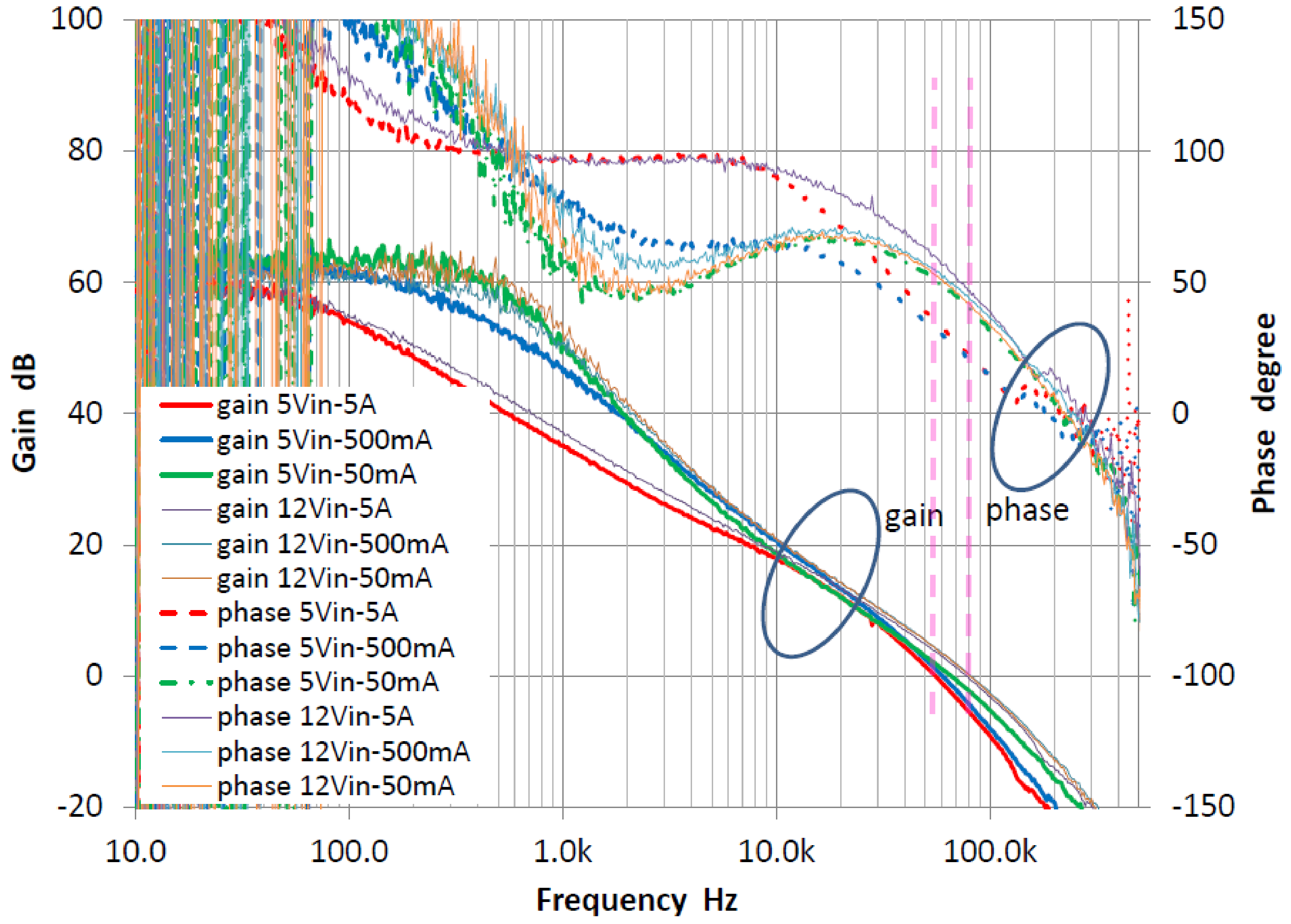


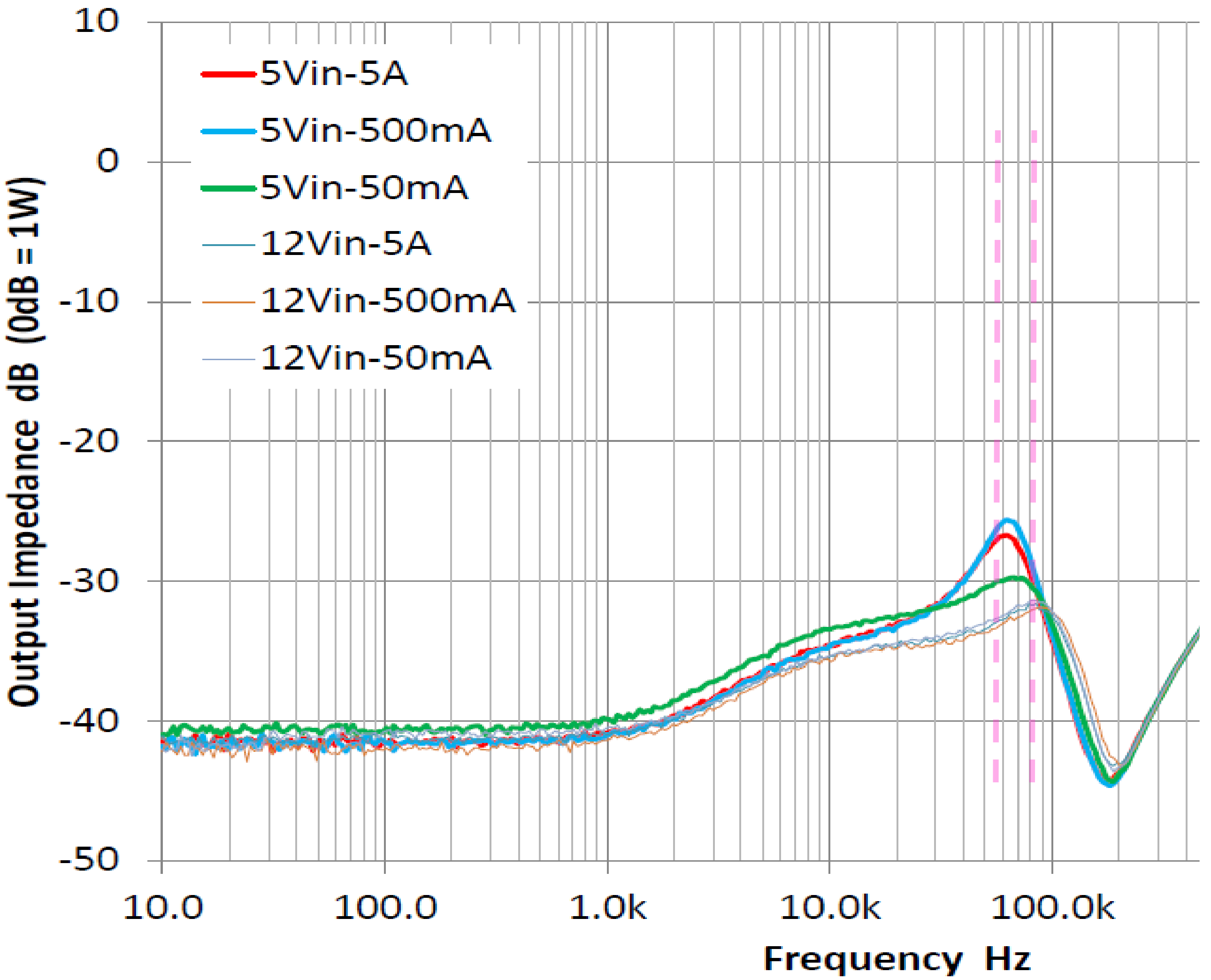
No ringing observed.

Apple-to-apple comparison

LOOP STABILITY / SMALL SIGNAL STUDY CURRENT-MODE

Stability (Bode/ZOUT): CM-IC





Loop response changes a lot by VIN, IOUT.

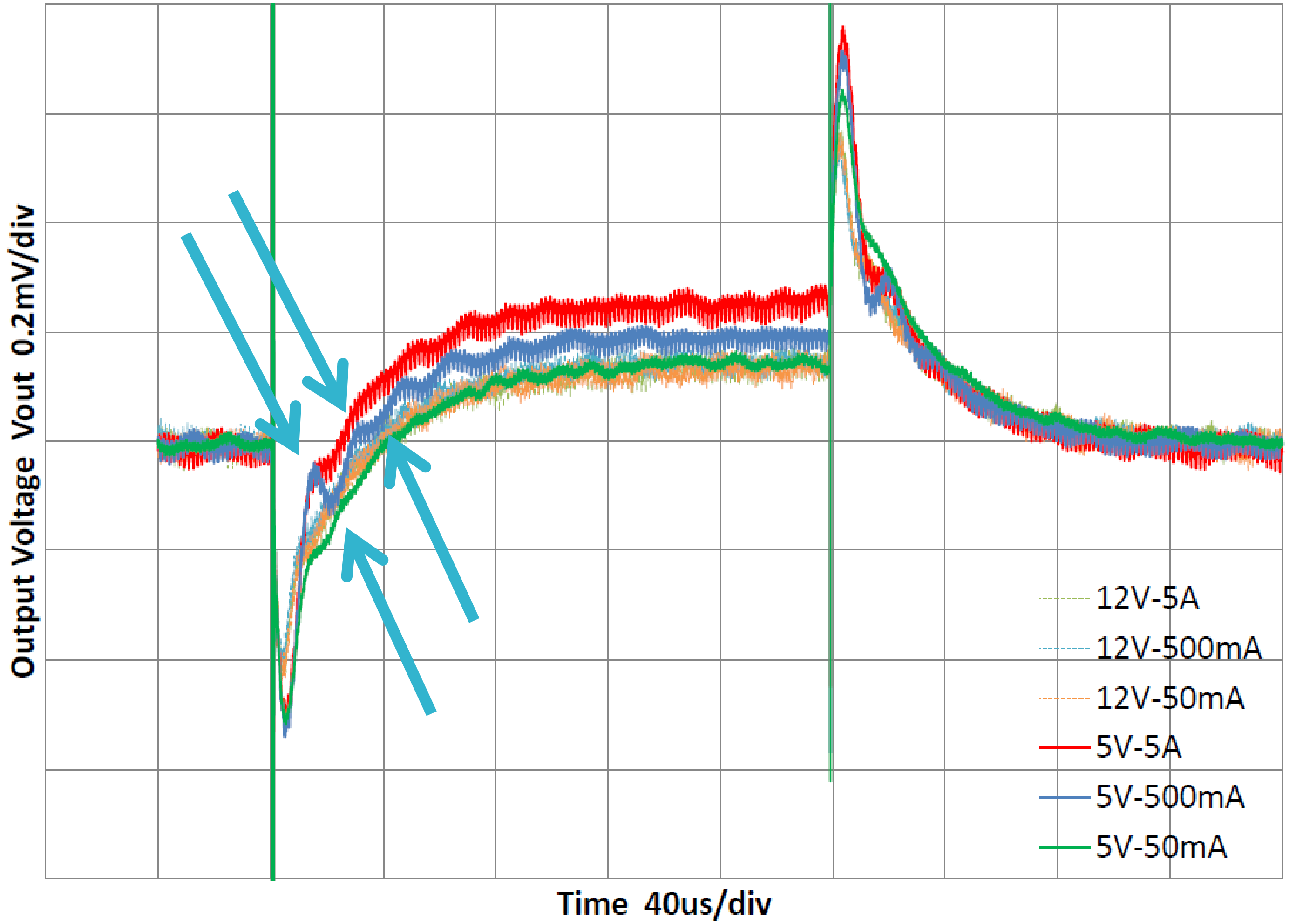
It's challenging to support wide changing operation range.

See next slide for phase margin values

TEXAS INSTRUMENTS

Stability (PM, Small-Signal Transient): CM-IC

Condition	Phase Margin	
	from Bode-plot	from Output Impedance
5Vin-5A	35.0° at 55.7kHz	36.7° at 64.8kHz
5Vin-500mA	29.8° at 60.4kHz	31.4° at 70.1kHz
5Vin-50mA	46.2° at 67.3kHz	50.8° at 82.0kHz
12Vin-5A	48.1° at 77.7kHz	56.4° at 88.6kHz
12Vin-500mA	43.7° at 80.6kHz	56.8° at 112kHz
12Vin-50mA	42.1° at 80.6kHz	54.2° at 99.7kHz



Phase Margin (Degrees)	Ringing (Bumps)
80.88	0
60.75	0
57.64	0
54.08	0
50.16	1
45.7	1.5
40.61	2
34.72	3
27.78	4
19.43	6
9.09	17

Table 1,
TI Apps Note
SLVA381B

It is optimized at 12Vin/6A…
5Vin/500mA is not good…

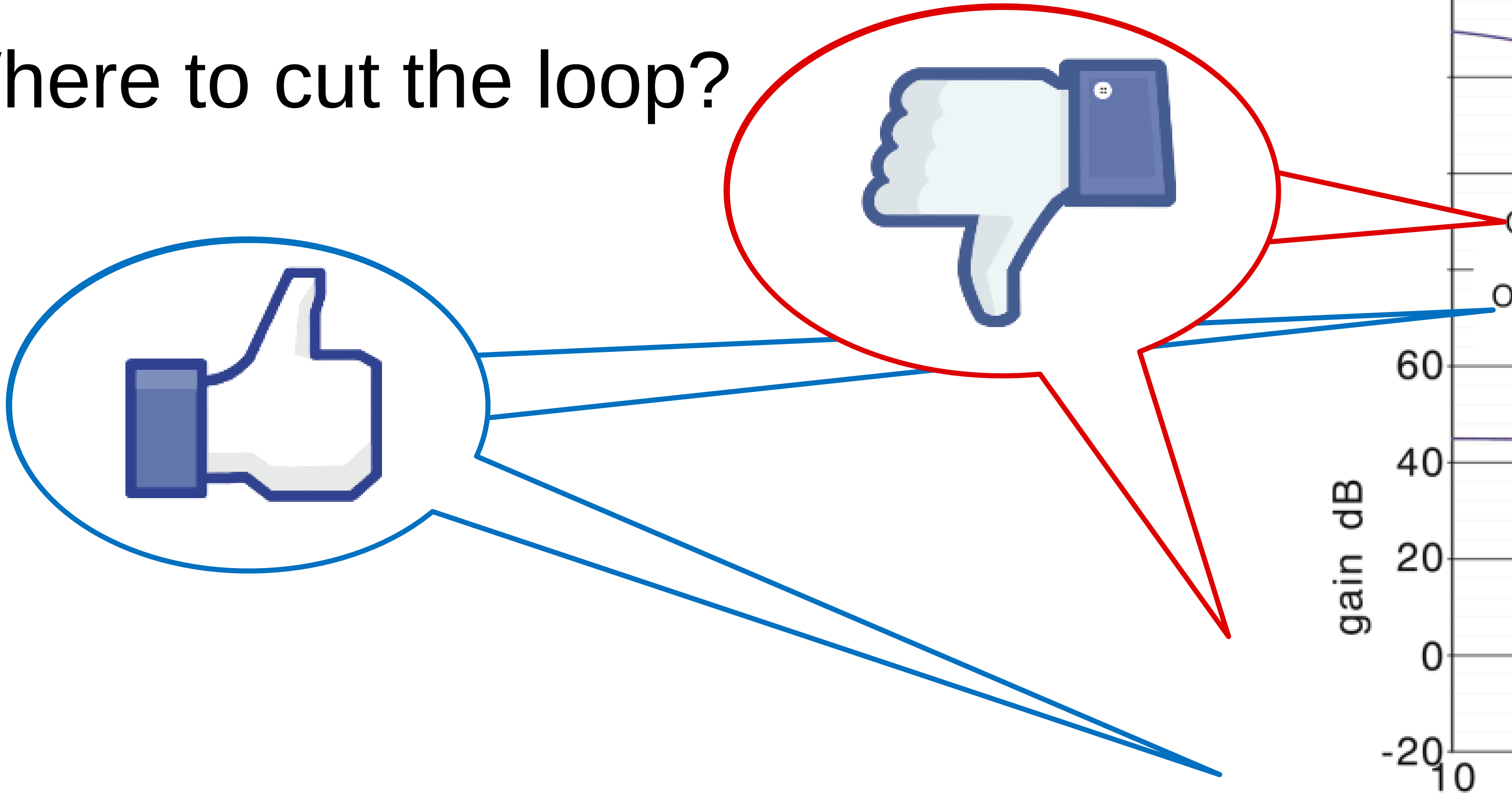
Apple-to-apple comparison

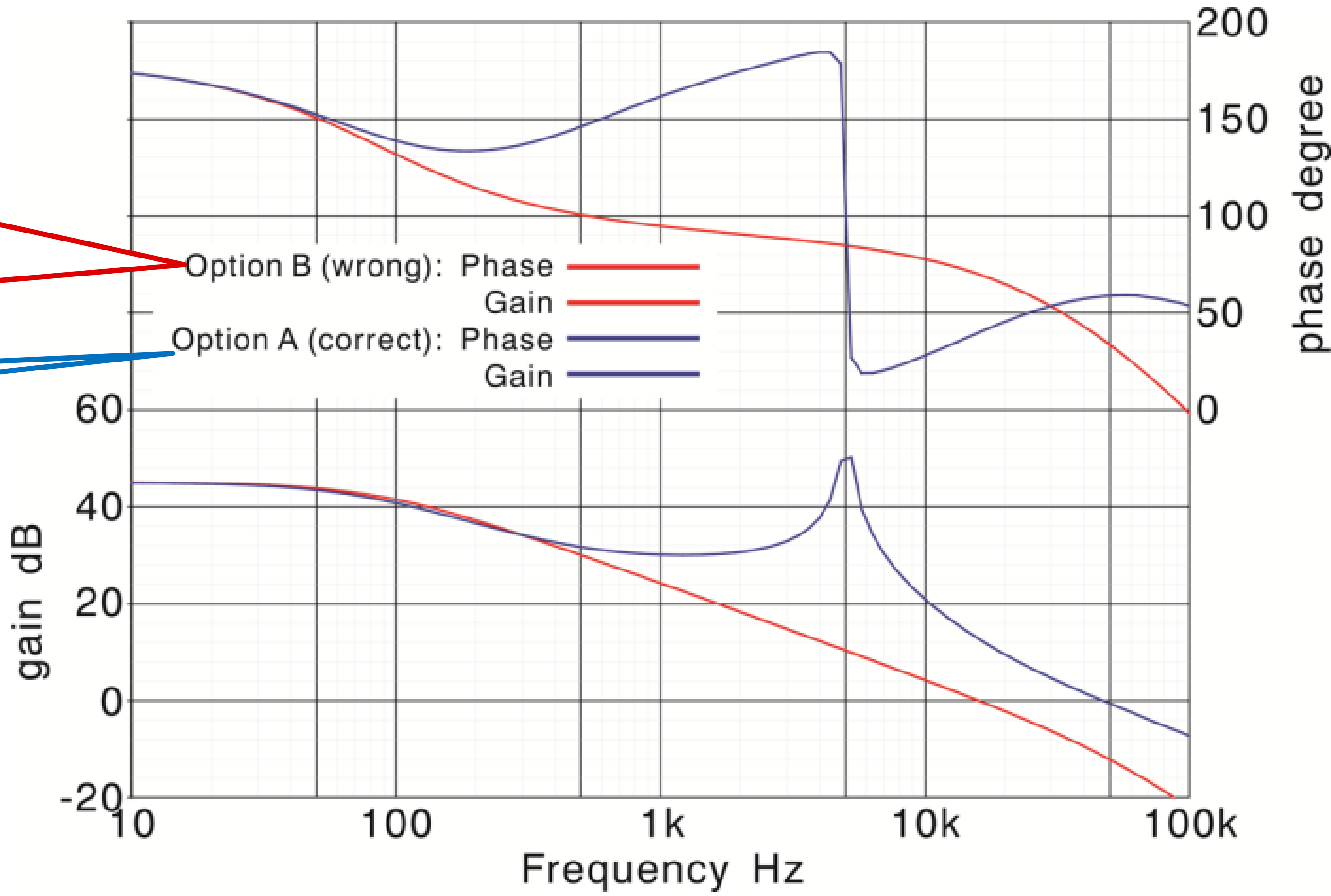
LOOP STABILITY / SMALL SIGNAL STUDY HYSTERETIC-MODE

Bode-plot Measurement: Hysteretic-mode

Simulation Waveform

- Where to cut the loop?



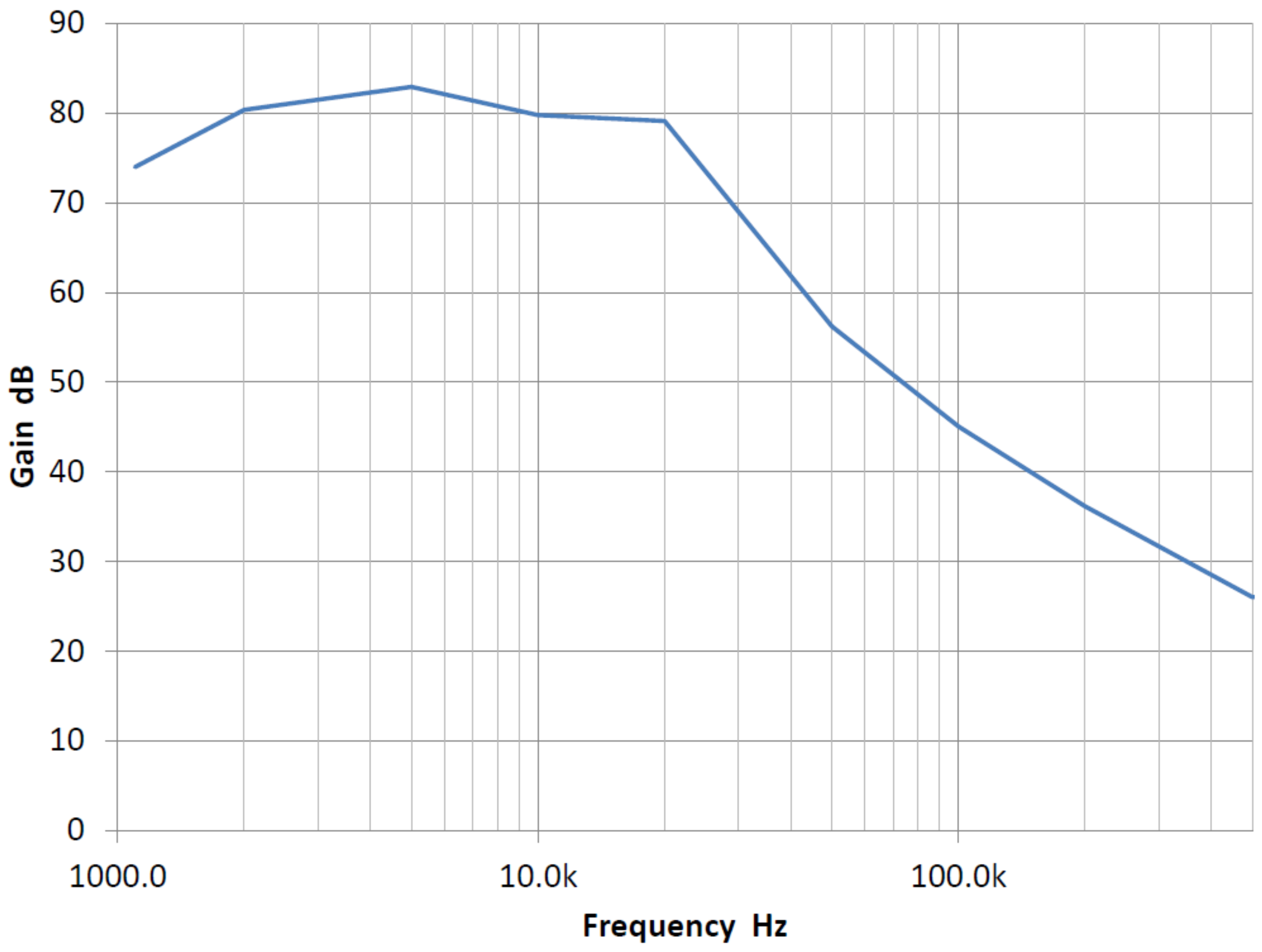


Note:

HM-IC is a D-CAP2™ IC doesn't have VOUT terminal for the ripple injection. Modified ripple injection RC circuit is used which makes tough to take right Bode plot (detail in later slide).

Bode-plot: Hysteretic-mode w/o Compensation

- Without any loop compensation (ripple injection) circuit, nor without using high ESR capacitors, a hysteretic mode device has infinite gain until frequency of f_{LC}, after f_{LC}, the gain decline with 40dB/dec LC filter slope.
- In a real application, this gain will be "2 x V_{IN} / (smallest perturbation you can inject)".
  ➔Without any compensation, it will end up with rail-to-rail (V_{IN}-GND amplitude) oscillation at V_{IN} at worst.



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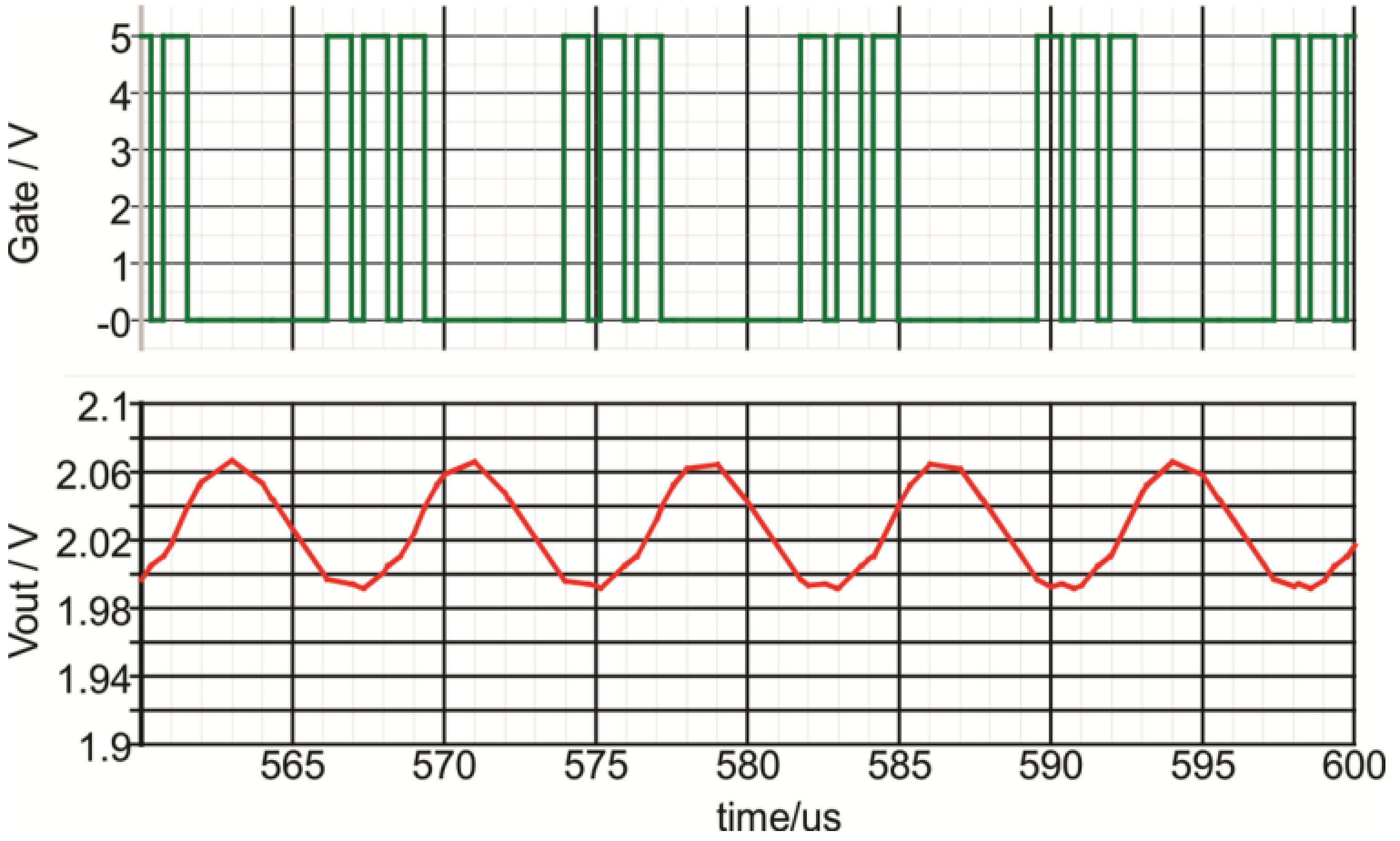
Bode-plot: Hysteretic-mode with a poor Compensation

- With a poor compensation, a hysteretic mode device falls into a double-pulse to multiple-pulse situation.
- In case of just double-pulse, there's a high chance of failure to capture this situation if only its output voltage is monitored.

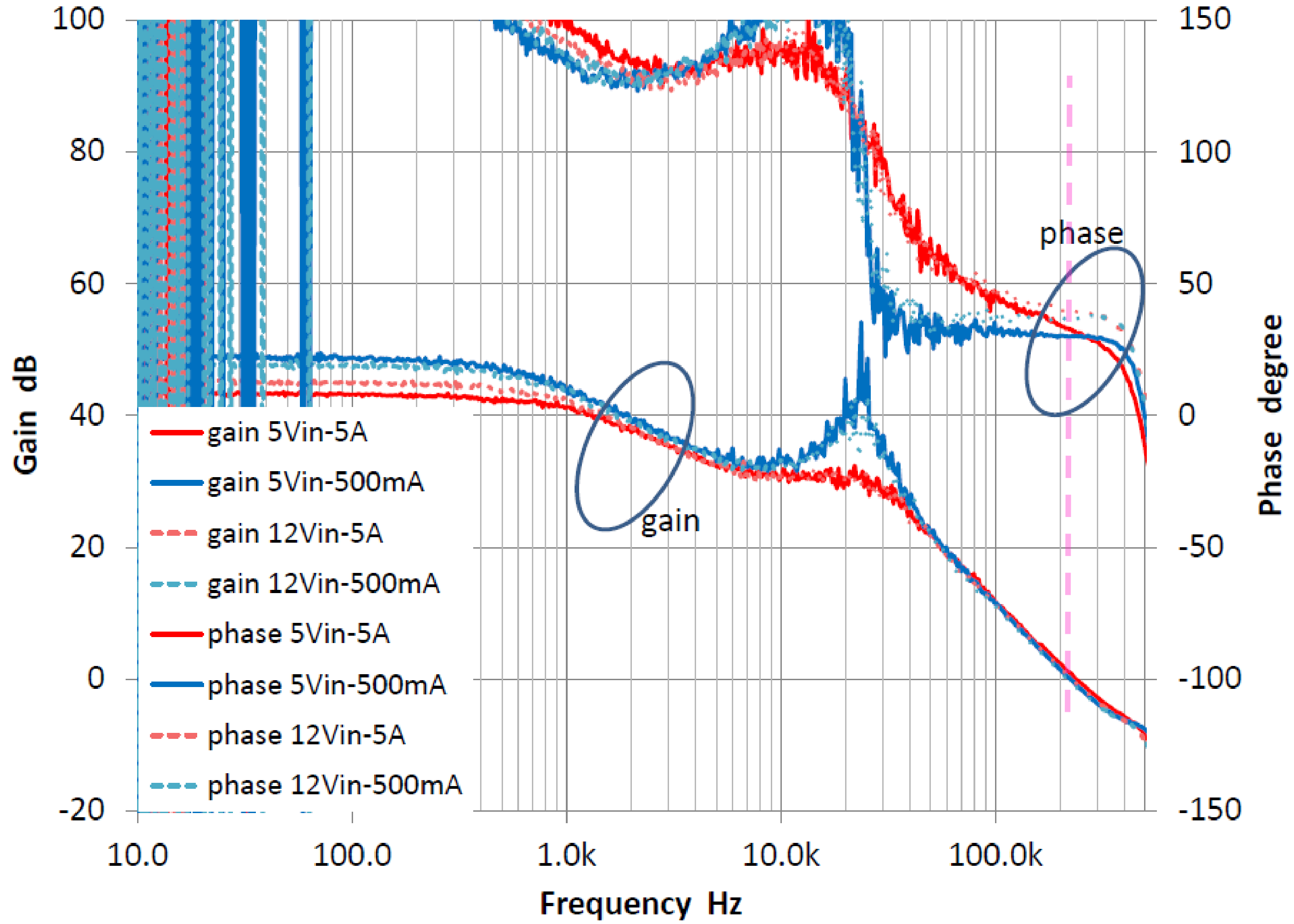
  ➔Having a double pulse situation only at a worst condition, not a big issue. Missing double pulse situation at a center condition is not good as it gets worse by sweeping conditions.

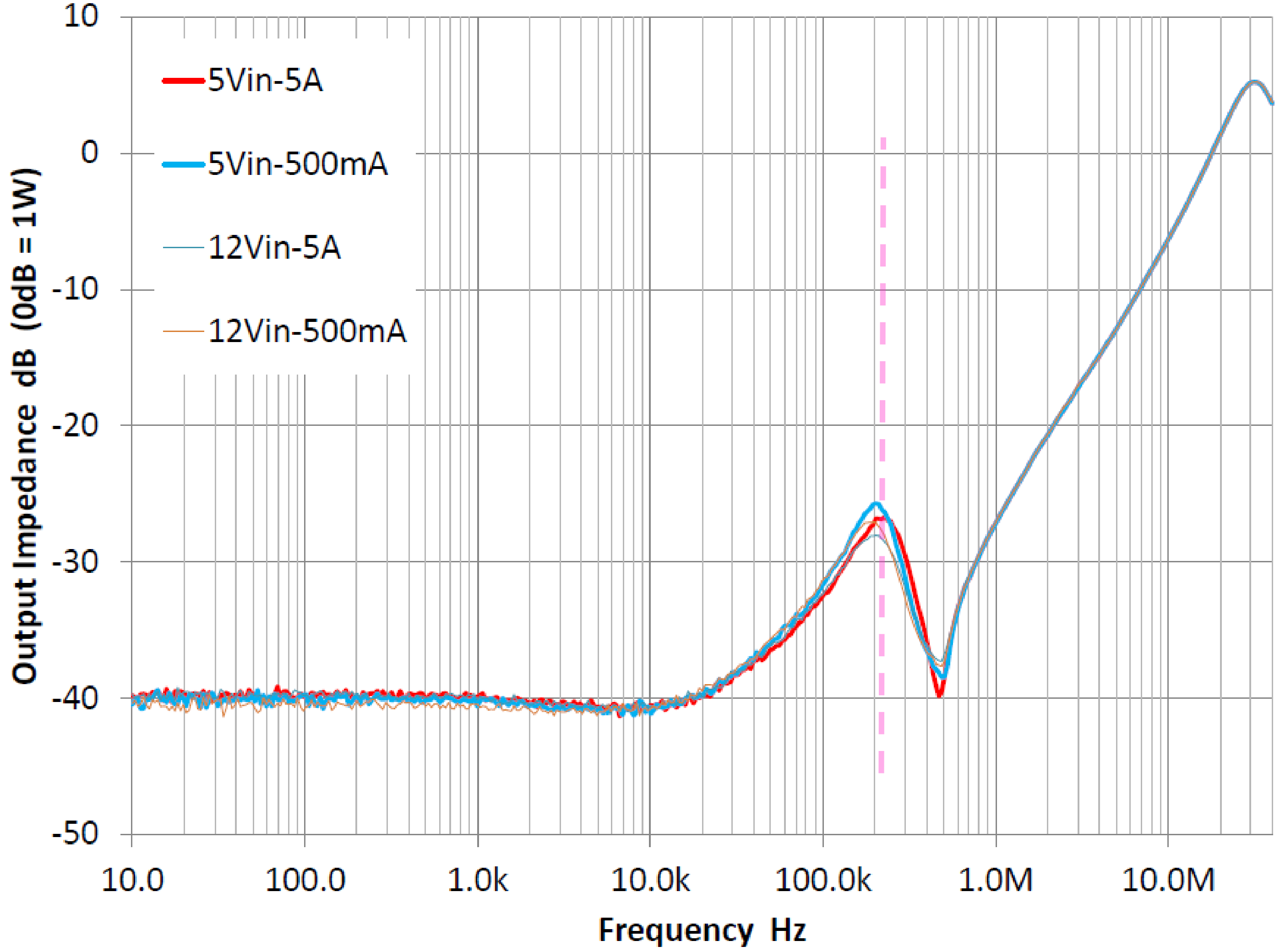


Simulation Waveform

Stability (Bode/ZOUT): HM-IC

HM-IC is an Eco-mode™ (skip-mode) IC. 50mA load data excluded.





IOUT change = RLOAD change

Smaller RLOAD decreases Q-factor of LC resonant.

See next slide for phase margin values

Texas Instruments

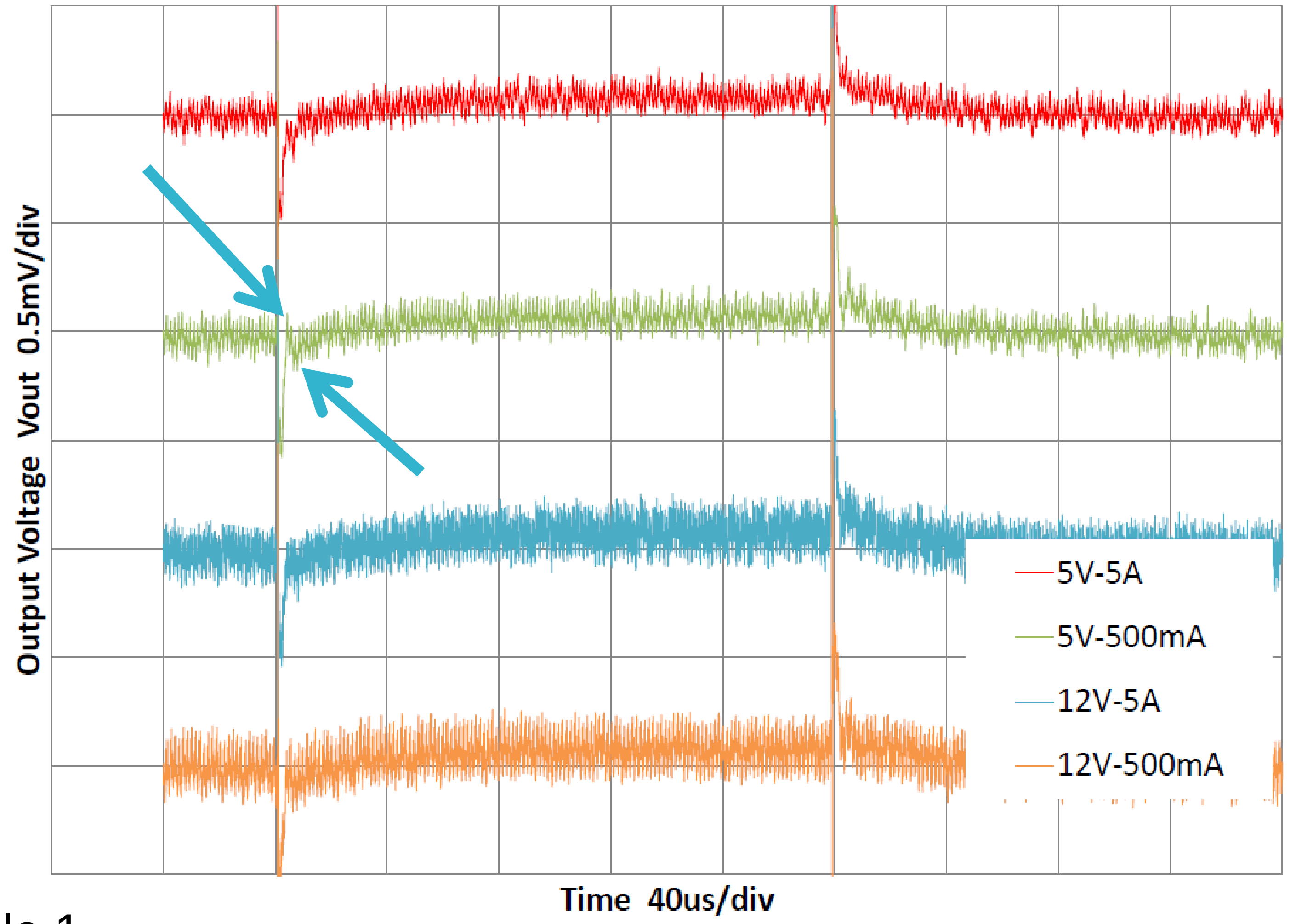
Stability (PM, Small-Signal Transient): HM-IC

Condition	Phase Margin	
	from Bode-plot	from Output Impedance
5Vin-5A	31.4° at 237kHz	43.6° at 236kHz
5Vin-500mA	29.8° at 221kHz	41.1° at 201kHz
12Vin-5A	40.3° at 229kHz	49.1° at 201kHz
12Vin-500mA	36.7° at 213kHz	47.9° at 201kHz

Output impedance gives accurate PM result…let's see➔

Phase Margin (Degrees)	Ringing (Bumps)
80.88	0
60.75	0
57.64	0
54.08	0
50.16	1
45.7	1.5
40.61	2
34.72	3
27.78	4
19.43	6
9.09	17

Table 1, TI Apps Note SLVA381B



Because of un-breakable inner-loop, output impedance (non invasive) measurement gives more accurate phase margin here.

Texas Instruments