Basics of Analog Multiplexers 1

TIPL 2601
TI Precision Labs – Op Amps

Created by Abhijeet Godbole, Art Kay

Presented by Peggy Liska

Analog Multiplexer Parameters Summary

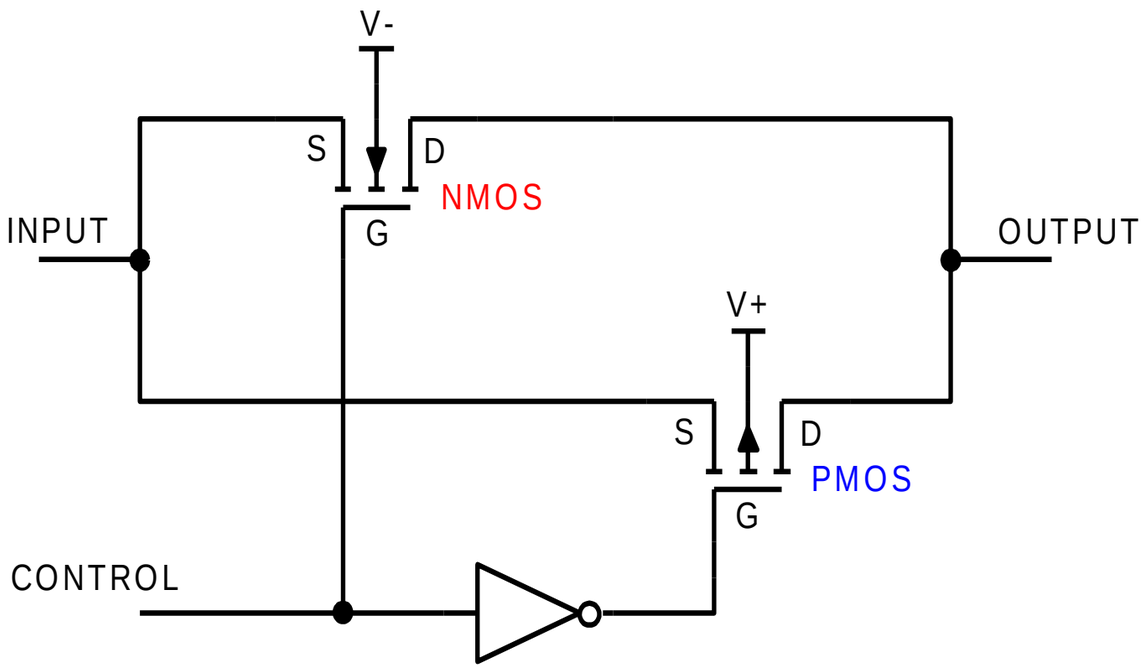
- Part 1: Understanding Basic Construction of CMOS Switch
- Part 2: Understanding DC Performance parameters of Multiplexer

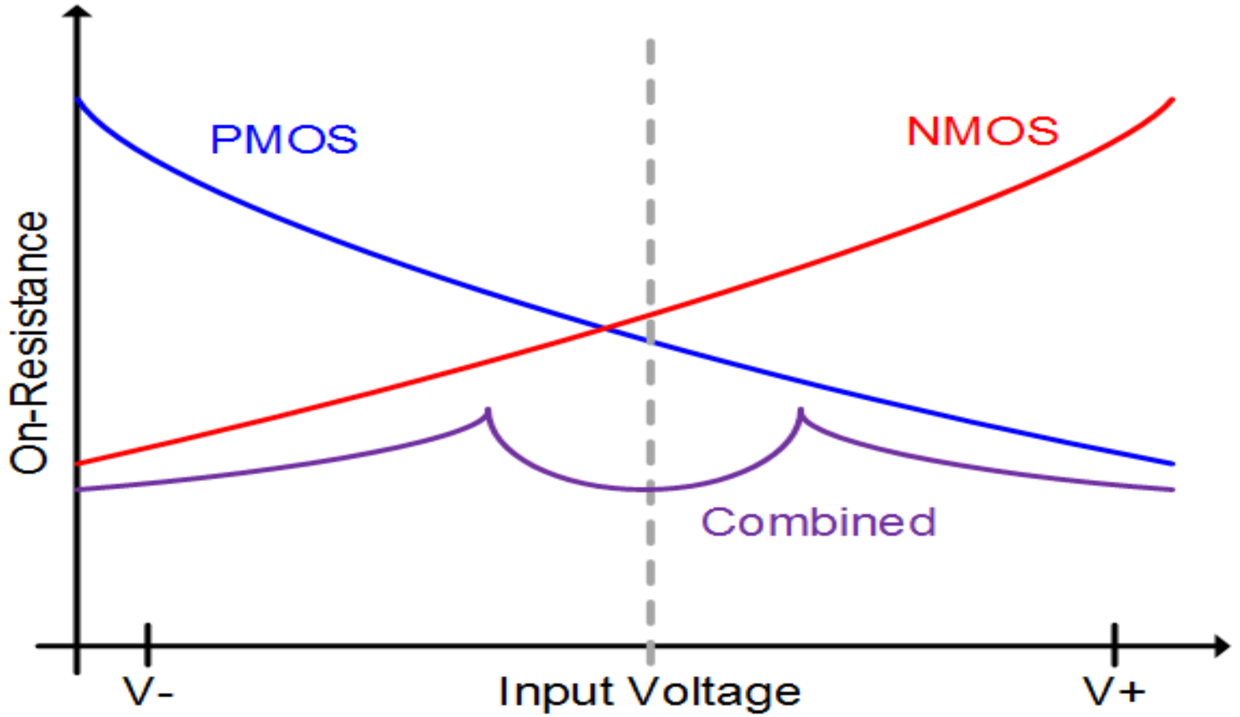
  1) ON Resistance
  - ON Resistance and it’s dependence on input Signal of MUX
  - ON resistance effect on Gain Error

  2) On Capacitance
  - Terminology for capacitance related with Multiplexer
  - Effect of ON capacitance on Multiplexer Settling Behavior

- Goals:
  - 1. To understand DC parameters of multiplexers
  - 2. Understand their importance while designing data acquisition system

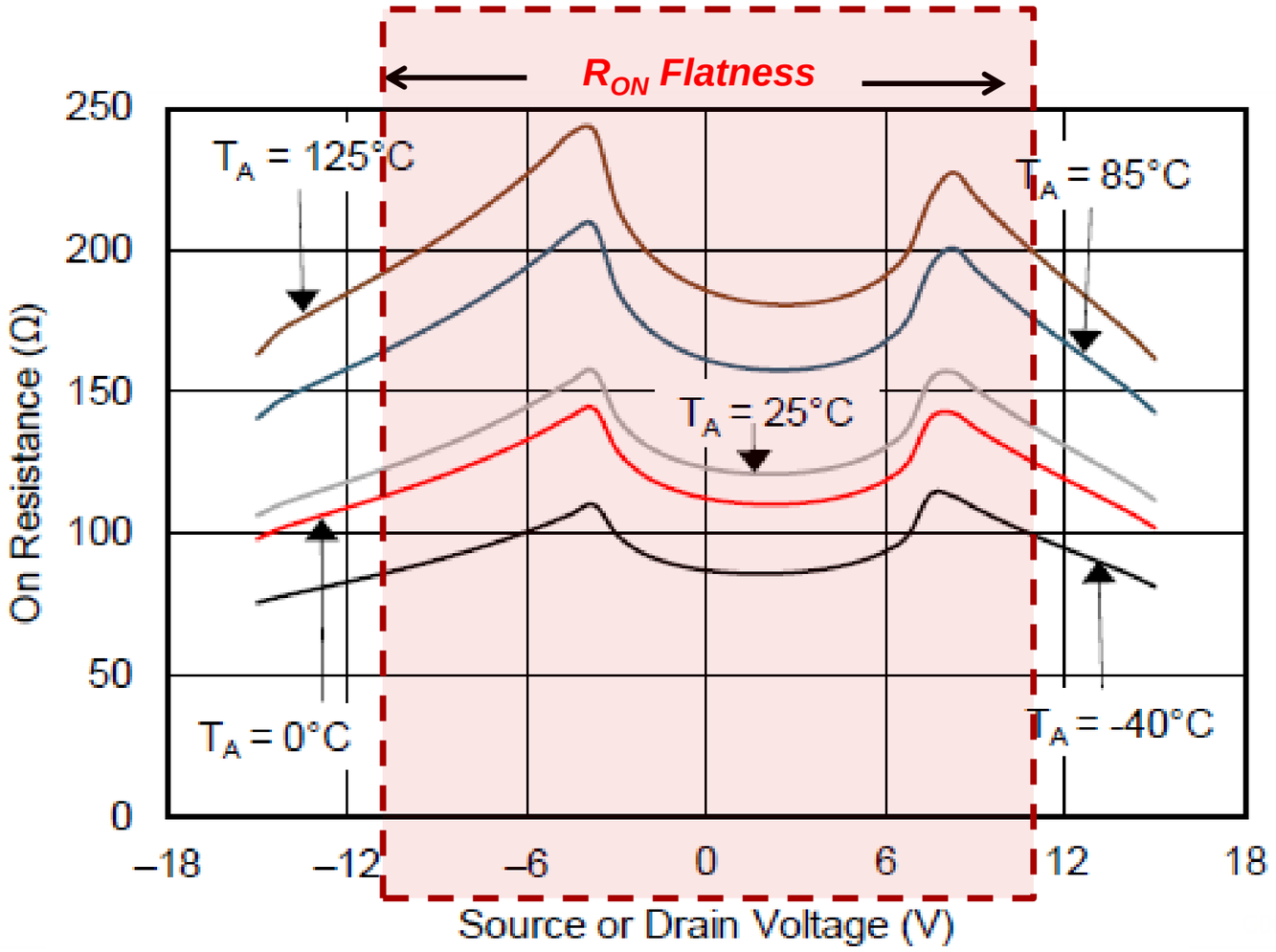
Basic Construction of CMOS Switch





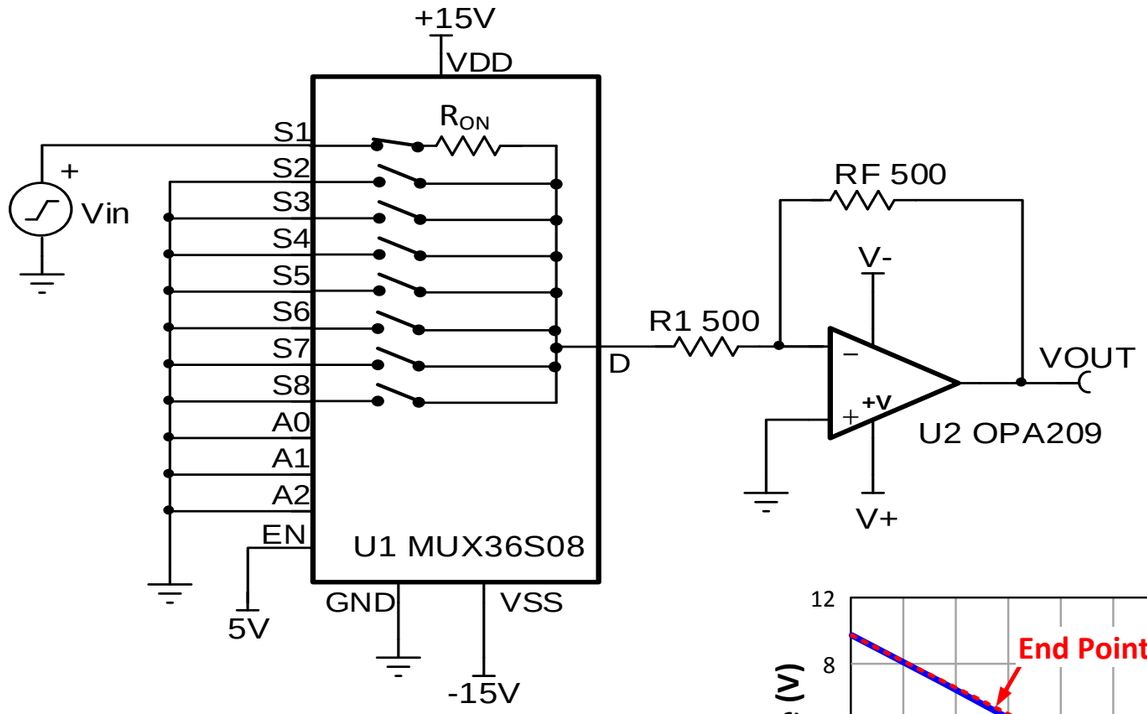
- Parallel combination of N channel and P channel FET
- Control Signal determines state of the switch
- **PMOS** conducts for positive input voltage and **NMOS** conducts for Negative Input Voltage

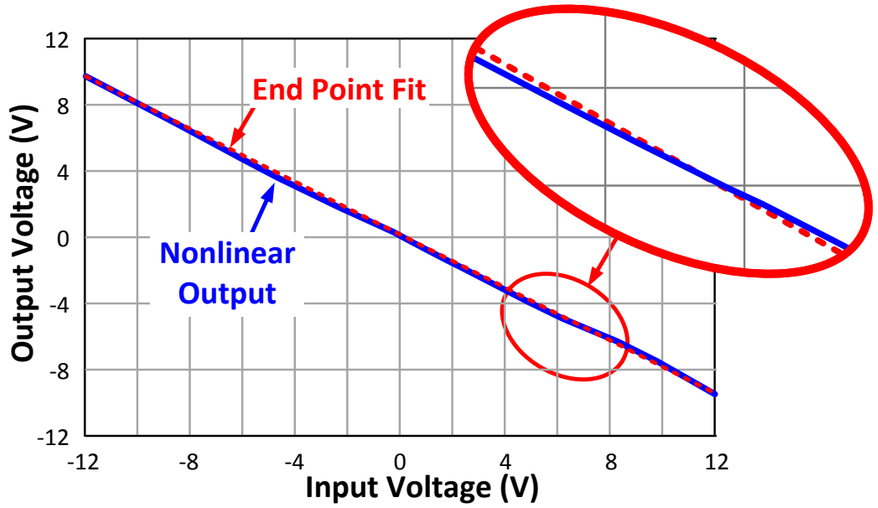
MUX ON Resistance (R_{ON})

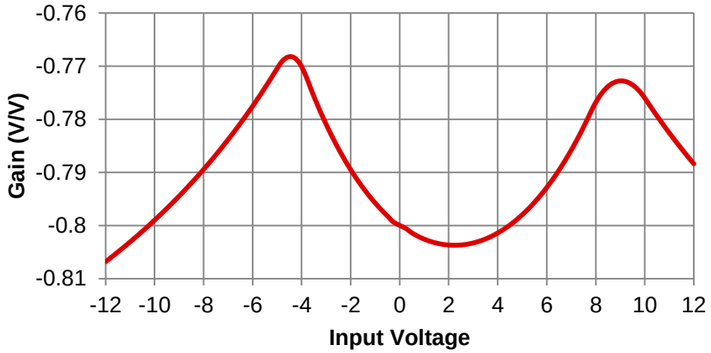


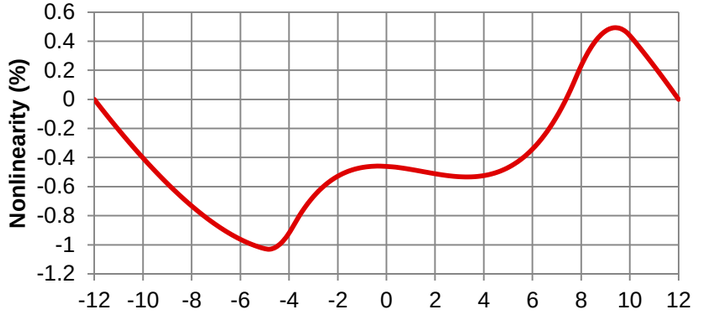
- R_{ON} = Resistance between source to drain terminal when switch is closed.
- Switch on resistance varies with input voltage.
- Difference between maximum and minimum value of on resistance over specified input range is termed as ***"R_{ON} Flatness".***

Input Signal Dependent Distortion Due to MUX R_{ON} Variation





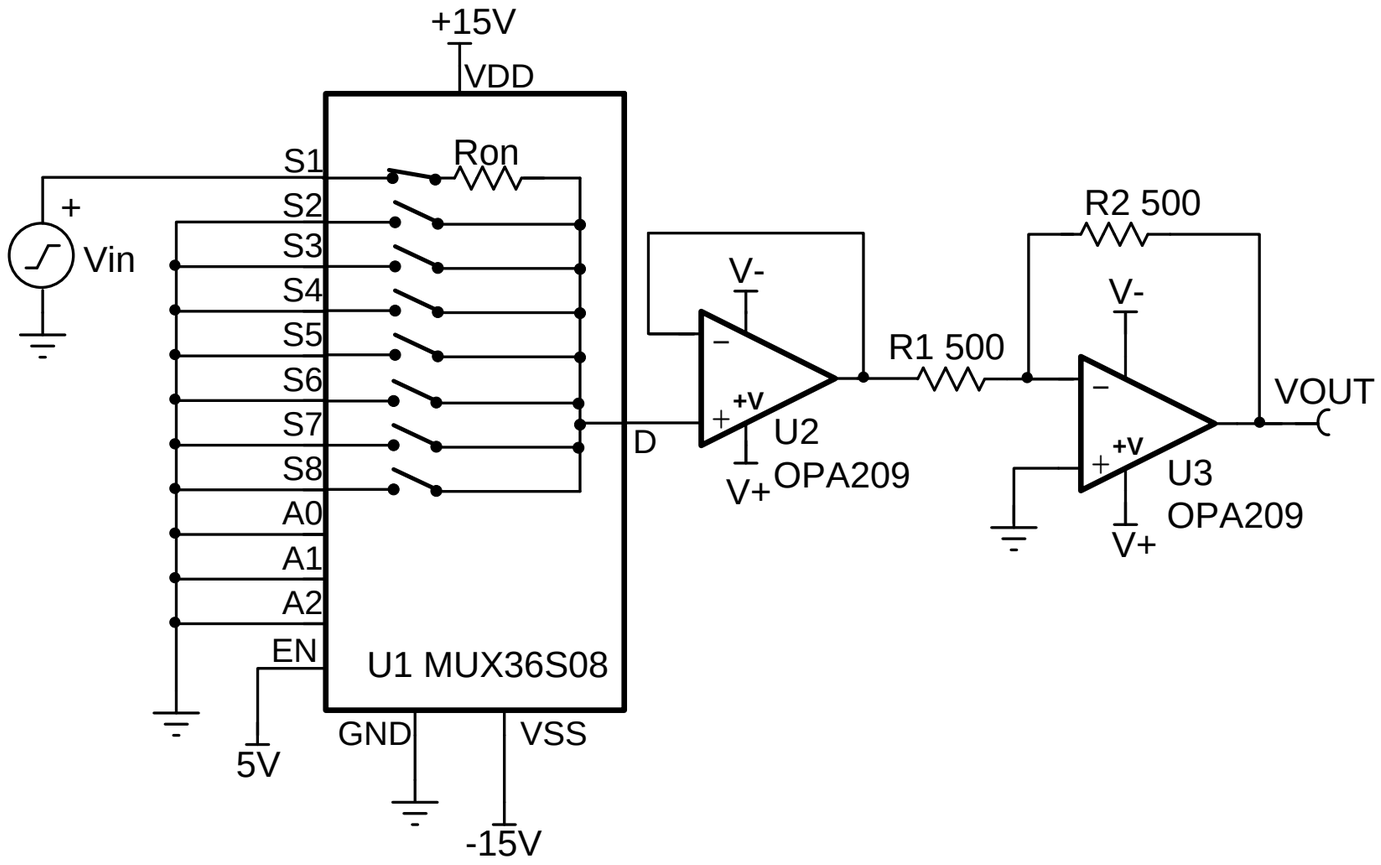




Effective MUX R_{ON} is:

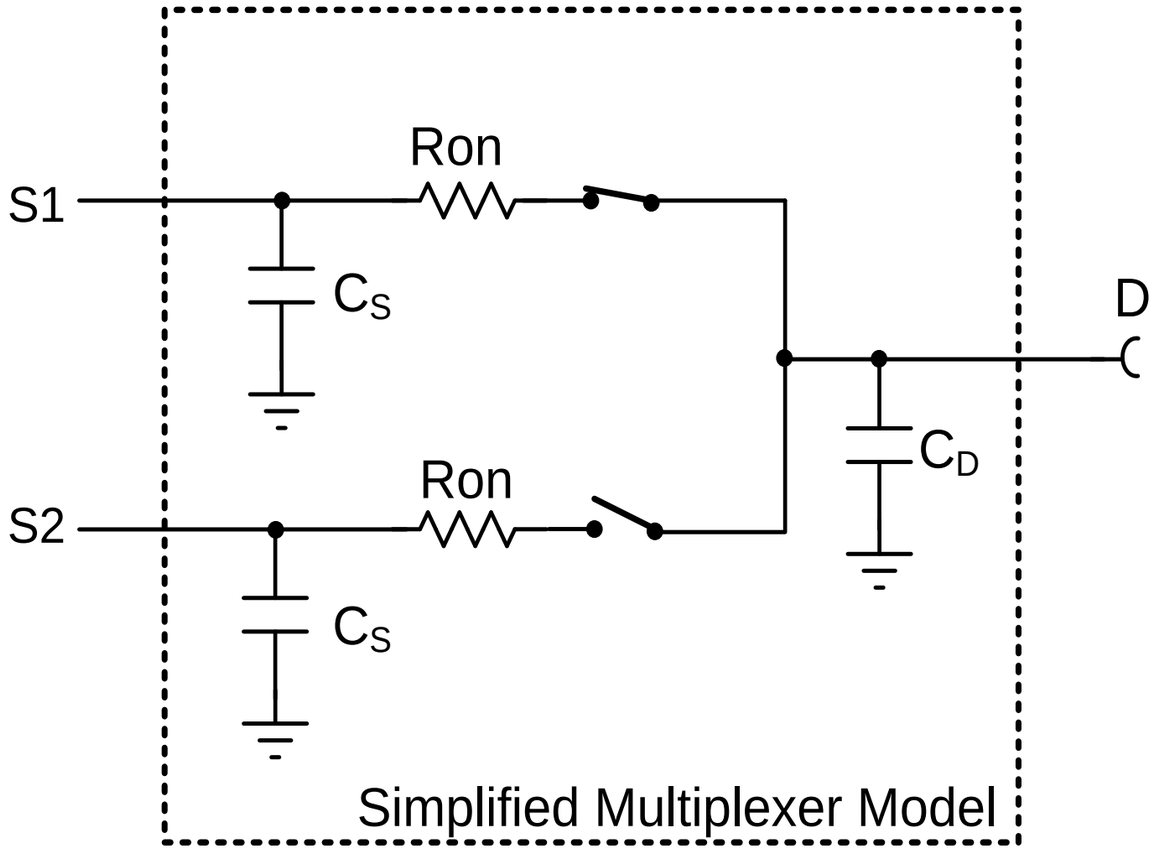
$$AG = -RF/(R1 + R_{ON})$$

MUX ON Resistance (R_{ON})



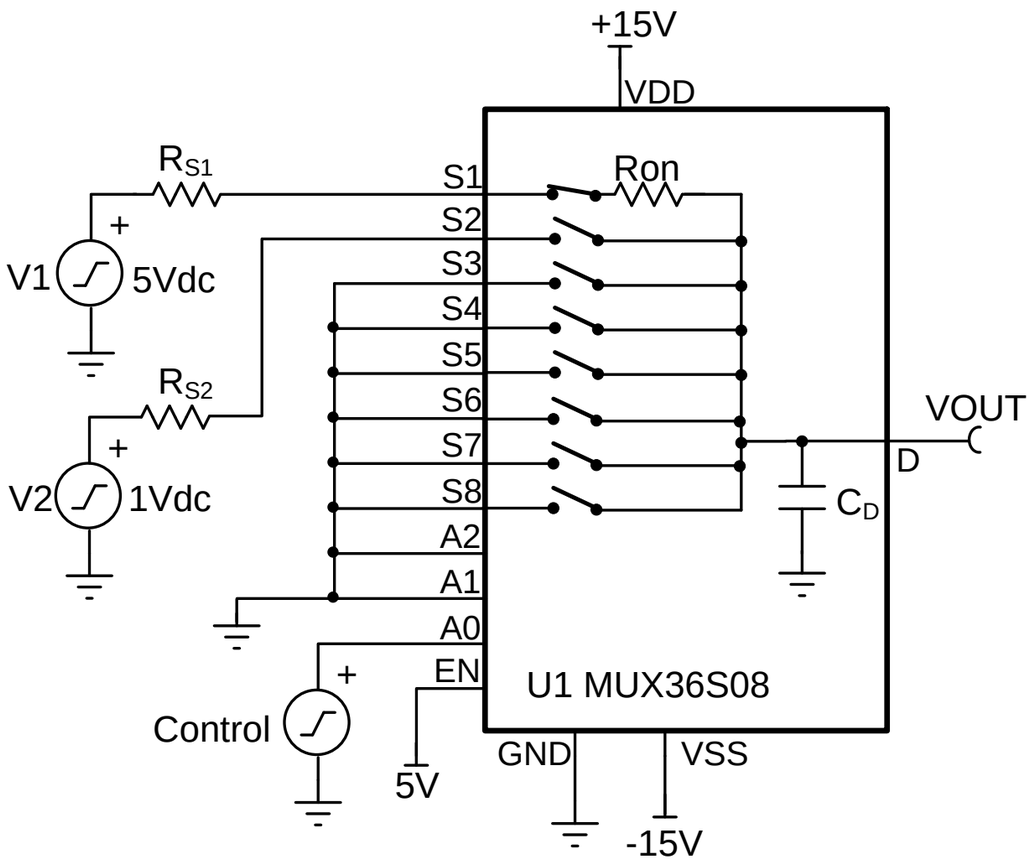
- Recommended to have high impedance stage such as buffer amplifier between MUXOUT and signal conditioning
- High input impedance of buffer addresses errors associated MUX R_{ON} and R_{ON} flatness.

MUX ON Capacitance (C_{ON})



- C_S and C_D represent the switch source and drain capacitance respectively when switch is OFF
- When switch is on, we can approximate MUX on capacitance as $C_{ON} = C_{S\ (ON)} + C_{D\ (ON)}$.
- The drain capacitance C_D is switched from one channel to the next when the MUX switches channels

MUX ON Capacitance (C_{ON}) : Settling Behavior



- Charge on Capacitance C_D when Channel-1 is ON :

$$\boldsymbol{Q_{D1} = V_1 * C_D}$$

- Charge on Capacitance C_D when Channel-2 is ON :

$$\boldsymbol{Q_{D2} = V_2 * C_D}$$

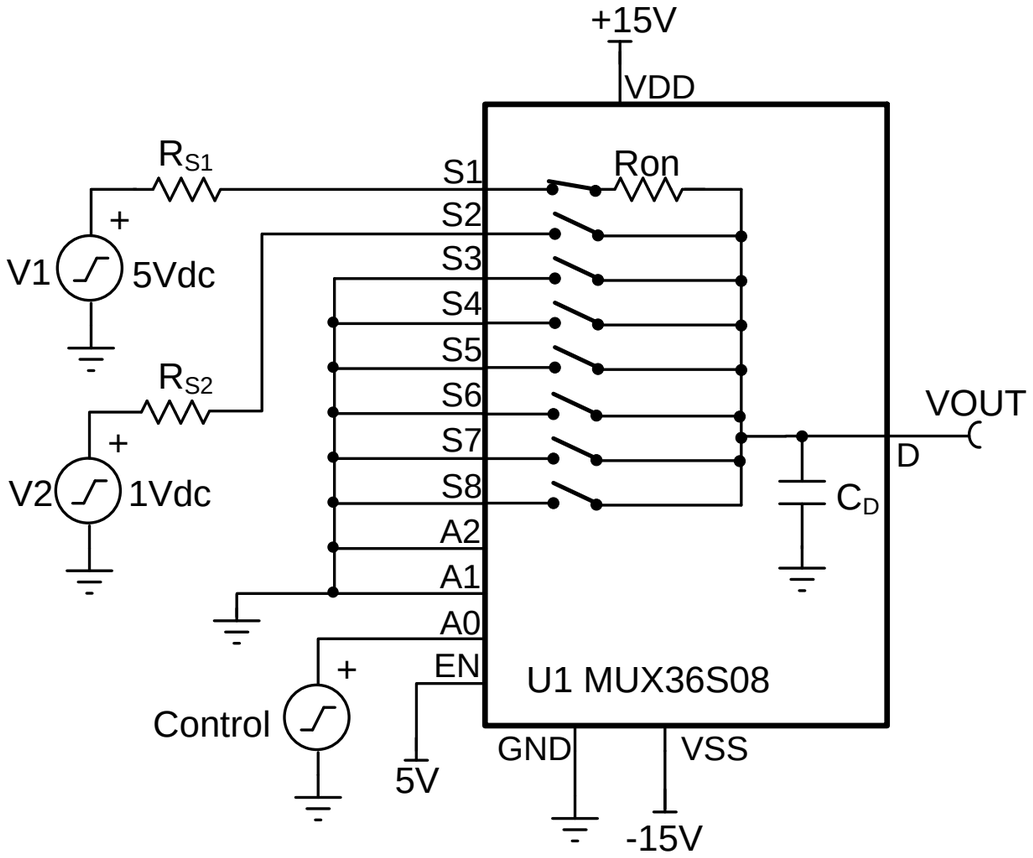
- The difference in charge i.e $\Delta Q = Q_{D1}-Q_{D2}$ should be provided by the input source on channel 2

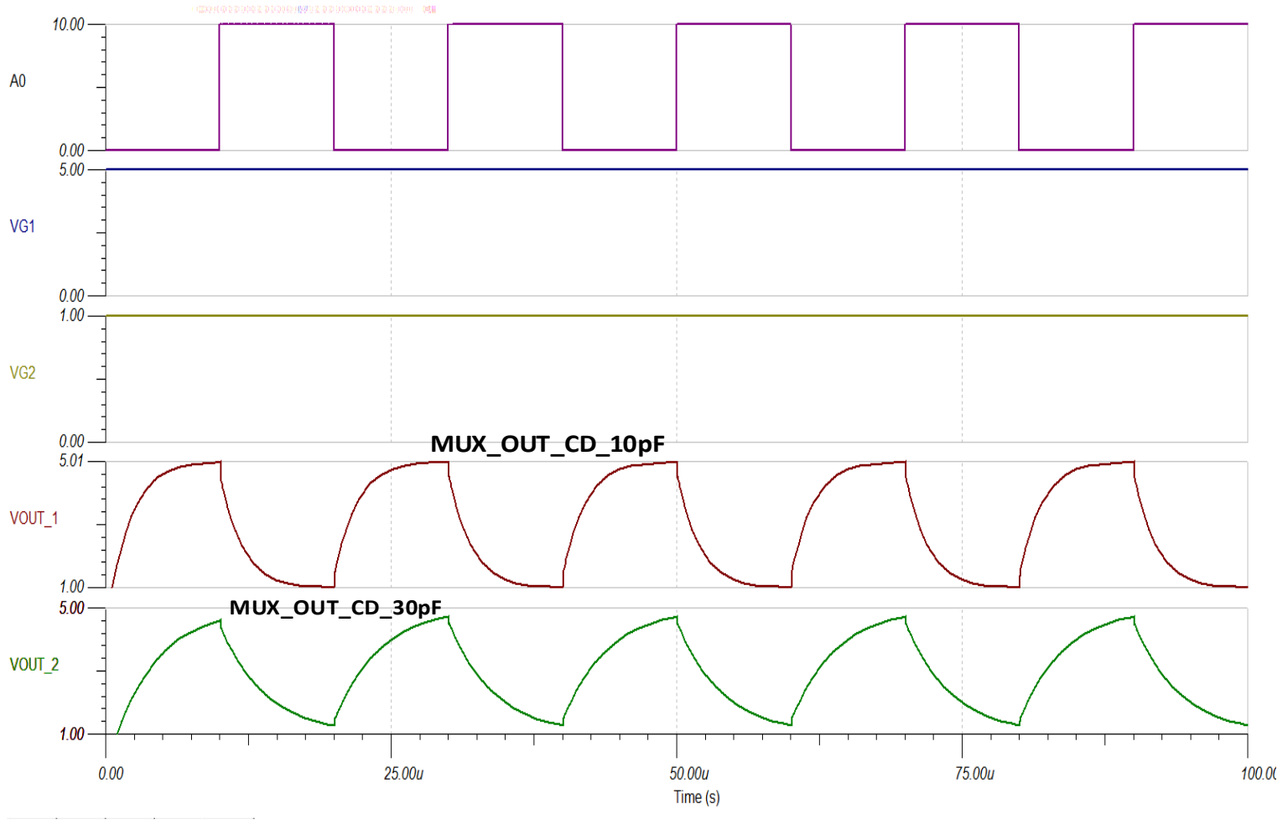
$$\boldsymbol{\Delta Q = (V_1 - V_2) * C_D}$$

- The MUX settling time to N-bit precision is given by:

$$\boldsymbol{T_{MUX-Settle} = K * (R_{ON} + R_{S2}) * (C_D + C_S)}$$
$$\boldsymbol{= K * (R_{ON} + R_{S2}) * (C_{ON})}$$

MUX ON Capacitance (C_{ON}) : Settling Behavior





Thanks for your time!
Please try the quiz.

Basics of Analog Multiplexers – 1

Multiple choice quiz
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Quiz: Basics of Analog Multiplexers – 1

1. A typical CMOS switch is formed by

a. Connecting two NMOS in Series

b. Connecting two PMOS in Series

c. Connecting an NMOS and PMOS in parallel

d. None of the above

2. The ON resistance of a CMOS switch is

a. The resistance between drain and source pin

b. The resistance between Drain and Gate pin

c. Lower than the individual resistance of the NMOS and PMOS transistors that form the switch

d. Both a and c

Quiz: Basics of Analog Multiplexers – 1

3. The ON resistance of a switch can lead to

a. Gain Error

b. Offset voltage error

c. Crosstalk

d. Both a and b

4. To counter gain error introduced due to the ON resistance, it is recommended to

a. Interface the MUX output to a high impedance stage

b. Interface the MUX output to a low impedance stage

c. Interface the MUX output to non-inverting buffer amplifier

d. Both a and c

Quiz: Basics of Analog Multiplexers – 1

5. Higher On capacitance of a multiplexer can lead to
a. Settling issues
b. Gain error
c. Offset error
d. None of the above

6. On capacitance is an important parameter to consider in
a. High input impedance data acquisition systems
b. Fast Switching data acquisition systems
c. Low power circuits
d. Both a and b

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Basics of Analog Multiplexers – 1

Exercises

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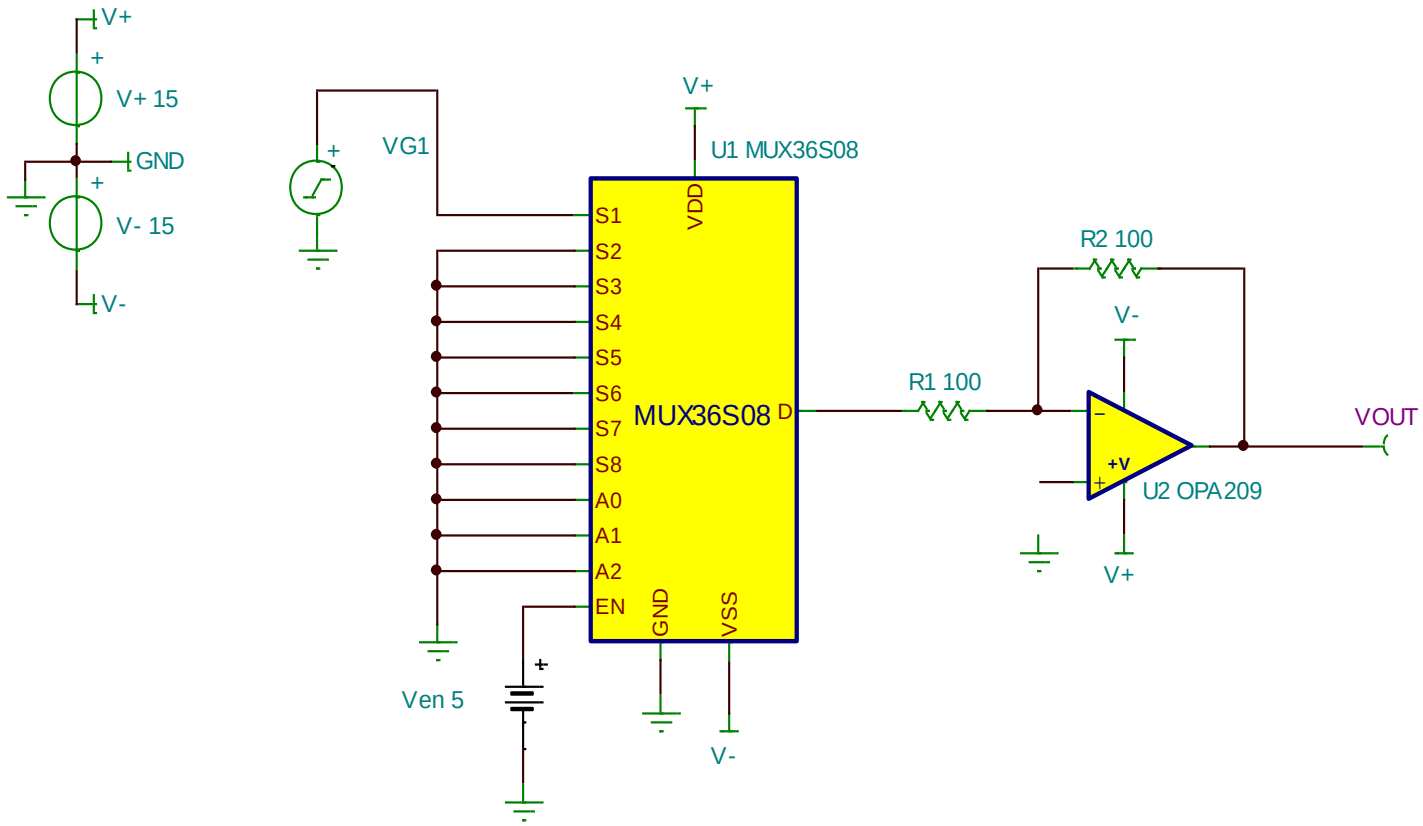
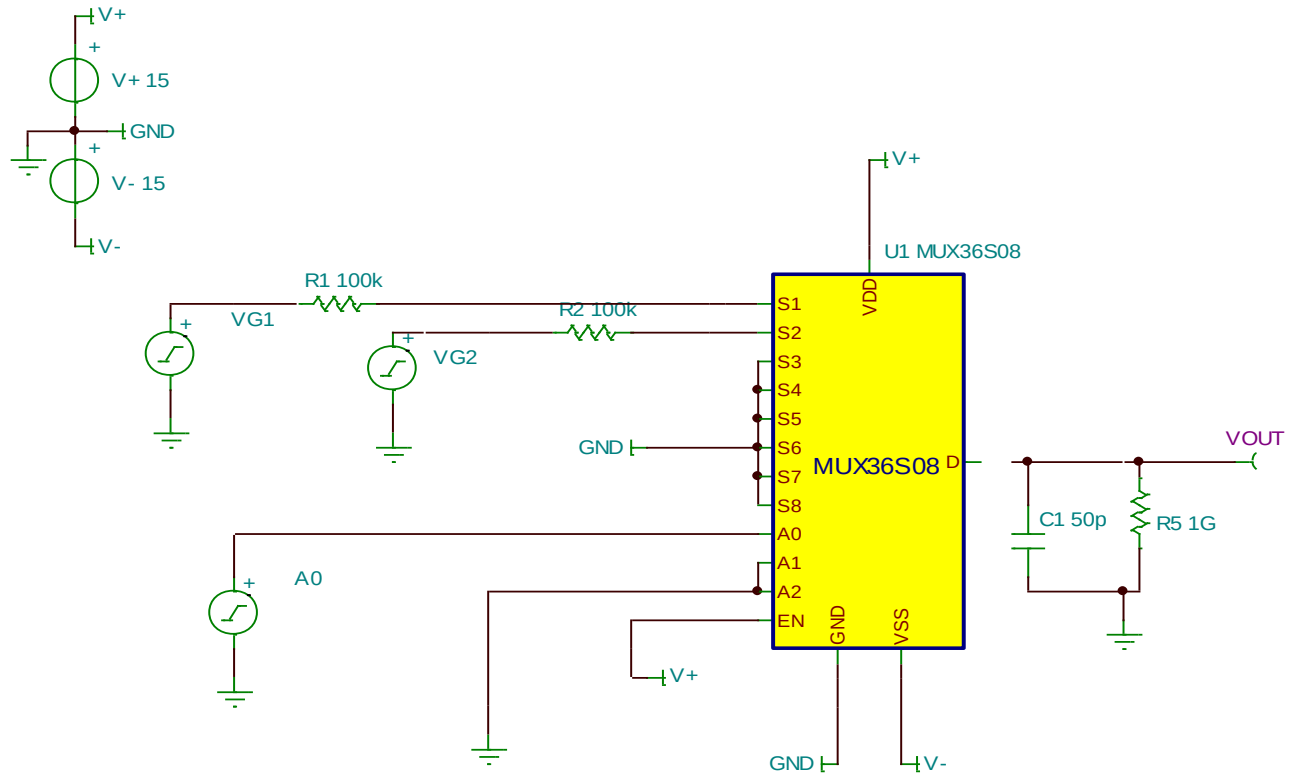
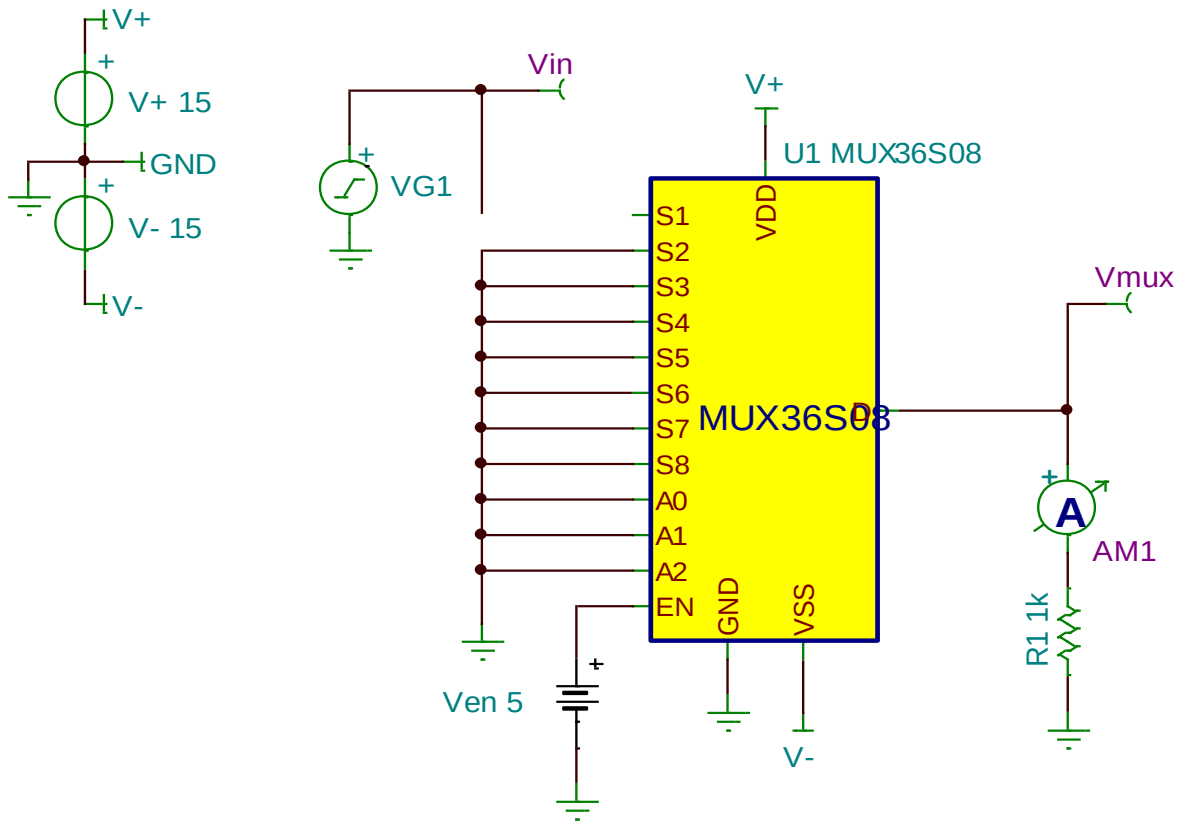
1. In the circuit below, one of the input channels of the MUX36S08 is fed with a $2V_{p-p}$ sinewave signal. The output of the MUX is interfaced with an inverting amplifier with gain of 1. What will be the output of the amplifier? Simulate it using TI-TINA.



2. In the below circuit, the multiplexer input channels are fed with two high-impedance voltage sources. VG1 and VG2 have a DC output of 5V and 1V. The MUX has total on capacitance of 50pF. These channels are switched at 20us. Does the output settle to the input voltage in the given time period? Simulate it using TI-TINA.



3. Using the below circuit, simulate the R_{ON} Flatness. Use a dc transfer characteristic to ramp the input signal from -12V to +12V. Use the Tina Post Processor to calculate R_{ON}.



Basics of Analog Multiplexers – 1

Solution

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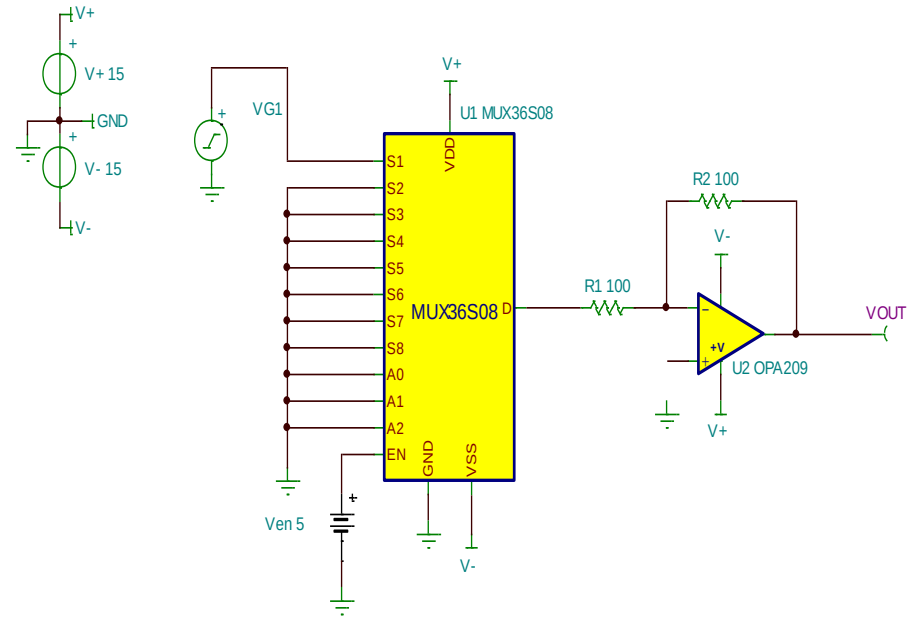
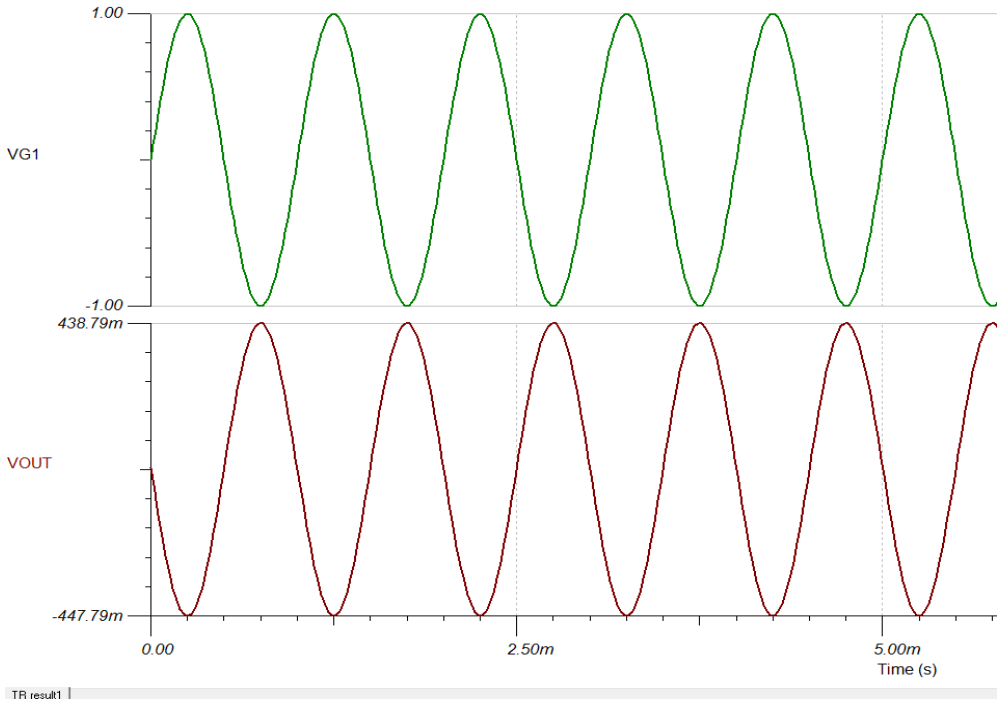
1. In the circuit below, one of the input channels of the MUX36S08 is fed with a $2V_{p-p}$ sinewave signal. The output of the MUX is interfaced with an inverting amplifier with gain of 1. What will be the output of the amplifier? Simulate it using TI-TINA.

Ans: Open TI TINA schematic. Run transient simulation. You will get simulation results as shown here





1. In the circuit below, one of the input channels of the MUX36S08 is fed with a $2V_{p-p}$ sinewave signal. The output of the MUX is interfaced with an inverting amplifier with gain of 1. What will be the output of the amplifier? Simulate it using TI-TINA.

Ans: MUX36S08 has typical on resistance of 125 Ohms. This can be seen in datasheet electrical characteristics

7.5 Electrical Characteristics: Dual Supply

at T_A = 25°C, V_{DD} = 15 V, and V_{SS} = –15 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
ANALOG SWITCH							
	Analog signal range	T_A = –40°C to +125°C		V_{SS}		V_{DD}	V
R_{ON}	On-resistance	V_S = 0 V, I_{CH} = 1 mA			125	170	Ω
		V_S = ±10 V, I_{CH} = 1 mA			145	200	
			T_A = –40°C to +85°C			230	
			T_A = –40°C to +125°C			250	

Effective Gain with MUX R_{ON} is:

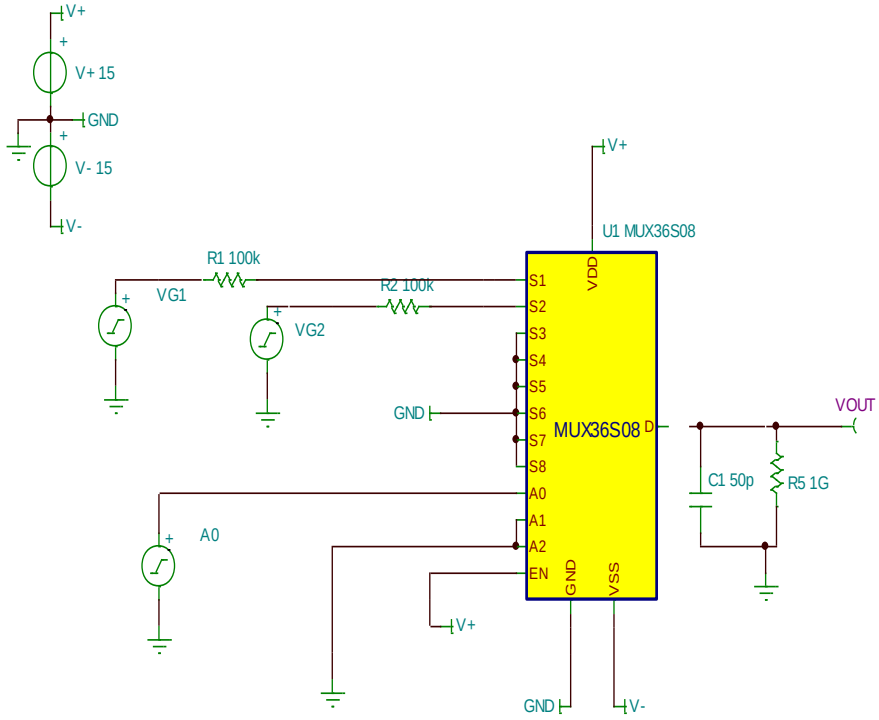
$$AG = -R2/(R1 + R_{ON})$$
$$= 100 / (100+125)$$
$$= 0.444$$

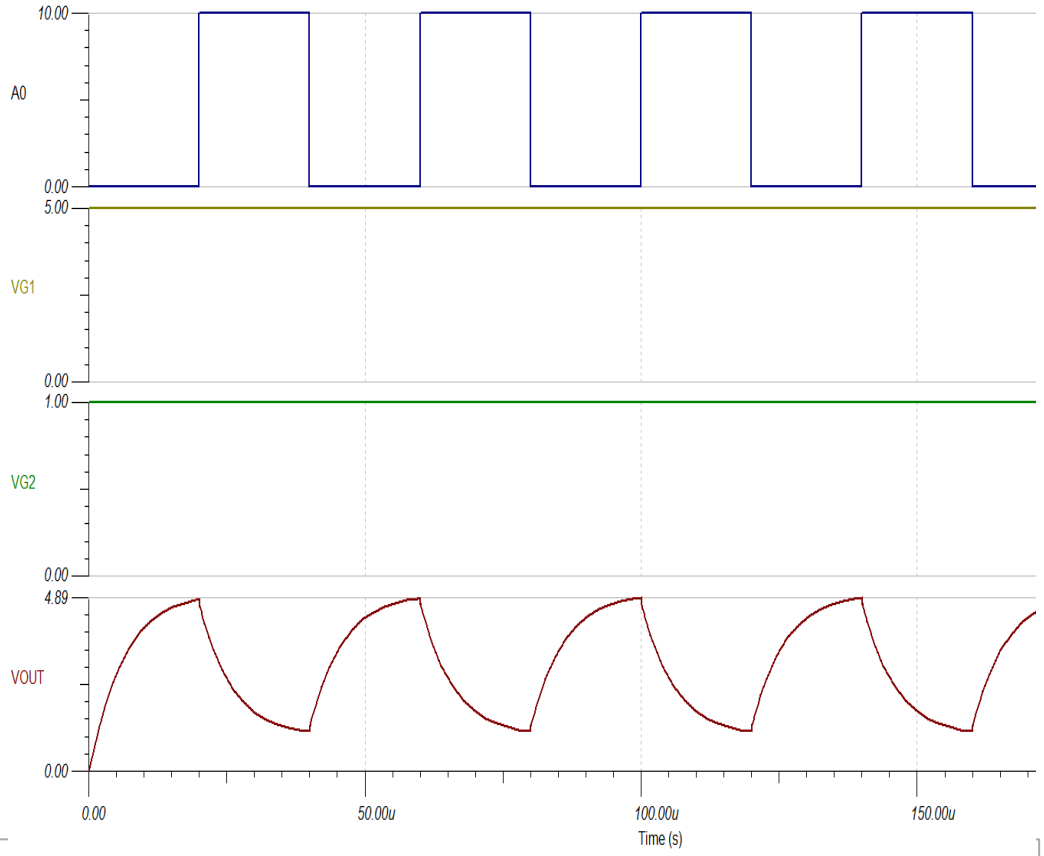
Thus for 2Vpp input signal you will observe voltage around 0.88 at the output of the amplifier.

Ans: To address this gain error, introduce buffer stage between MUX output and inverting amplifier and verify results.

2. In circuit below MUX36S08 input channels are fed with two high impedance voltage sources. VG1 and VG2 have DC output of 5V and 1V. MUX has total on capacitance of 50pF. These channels are switched at 20us time. Does output settle to input voltage in given time period. Simulate it using TI TINA model

Ans: Open TI TINA schematic. Run transient simulation. You will get simulation results as shown here



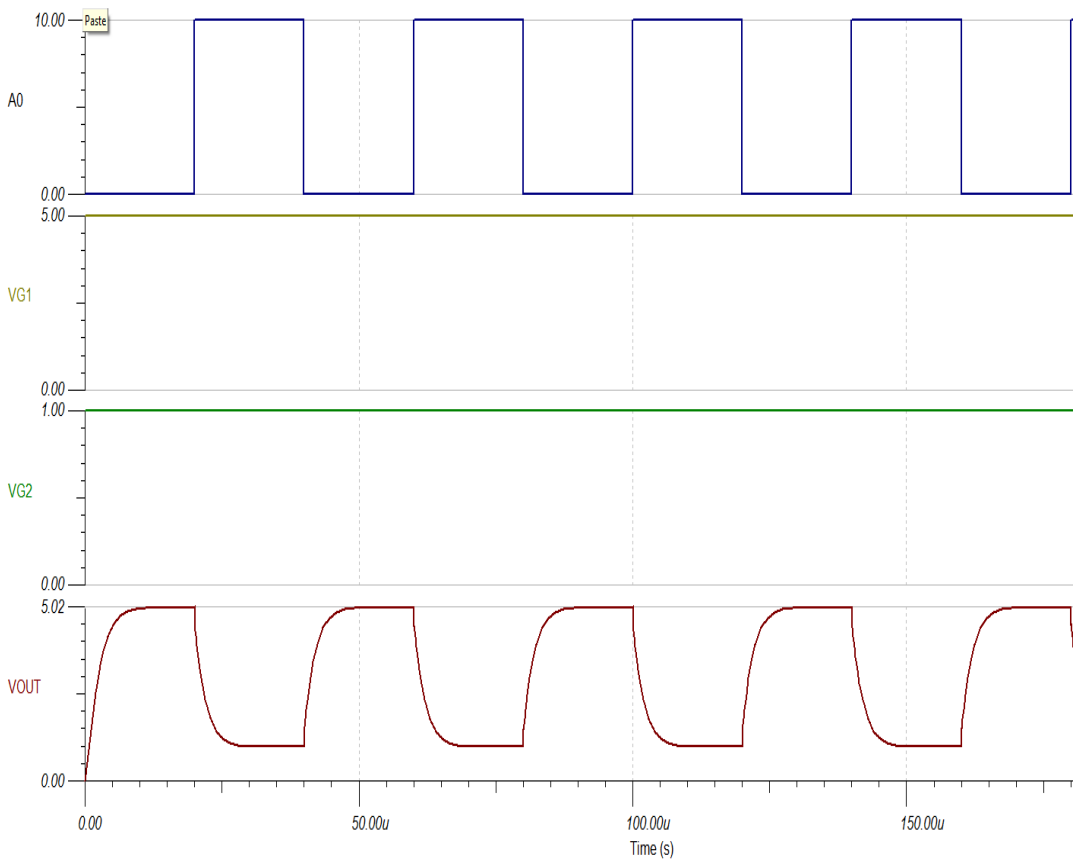


2. In the below circuit, the multiplexer input channels are fed with two high-impedance voltage sources. VG1 and VG2 have a DC output of 5V and 1V. The MUX has total on capacitance of 50pF. These channels are switched at 20us. Does the output settle to the input voltage in the given time period? Simulate it using TI-TINA.

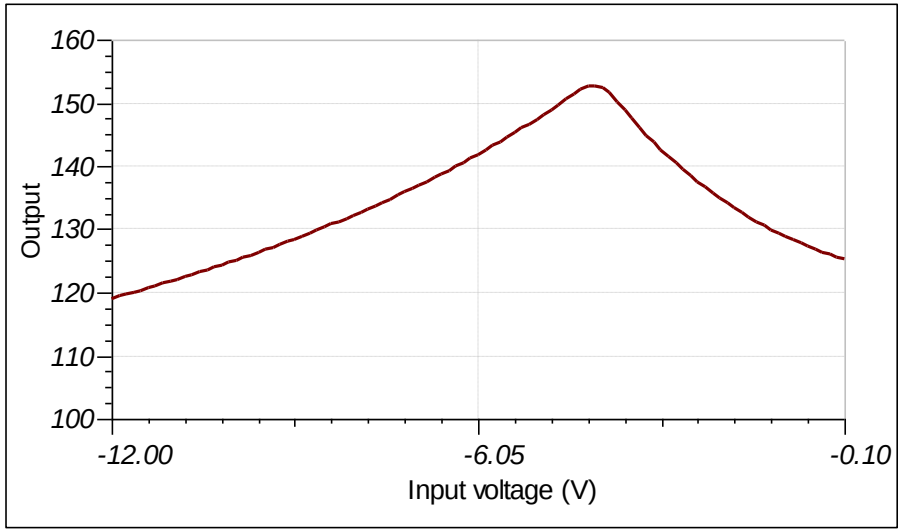
Ans: From simulation results in last slides you can see output of the MUX does not settle to final value of input voltage at respective channel. This is because of long RC time constant formed by MUX on capacitance (50pF) and 100k input impedance of source.

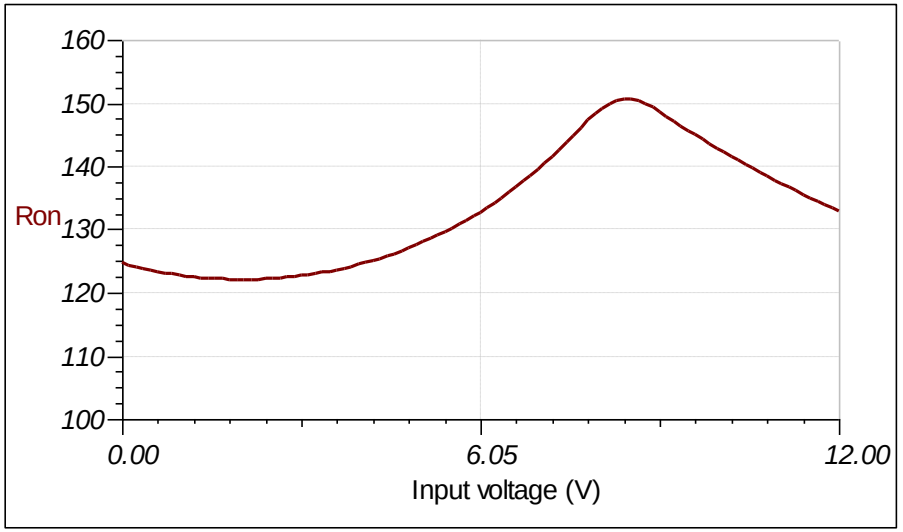
To address this you can simulate same TI TINA schematic with below condition and see output settling

1. **Change capacitor on MUXOUT "D" from 50pF to 10pF**
2. **You will get simulation results as shown here. You can clearly see MUX output settles to input channel value**

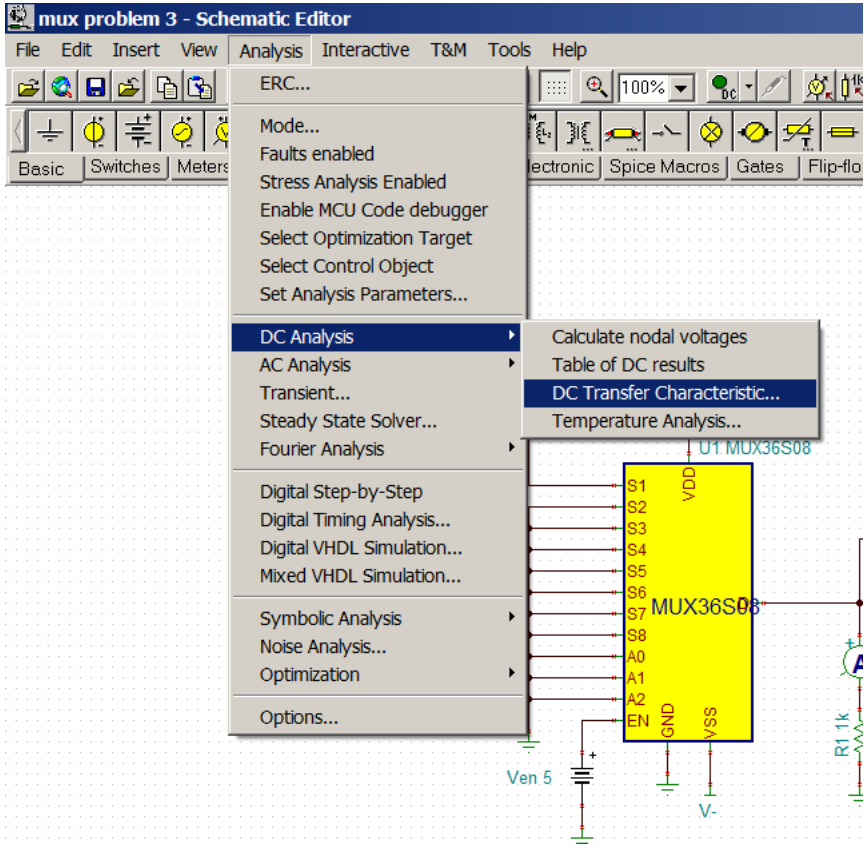


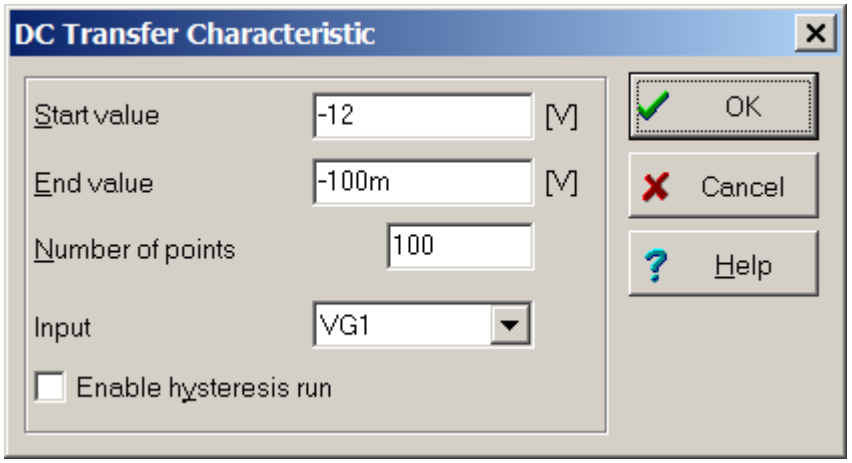
3. The plot below shows the simulation result for Ron. Ron is calculated as Ron=(Vin-Vmux)/AM1. Note that this was done in two different simulation runs to avoid the division by zero (I=0A when Vin=0).



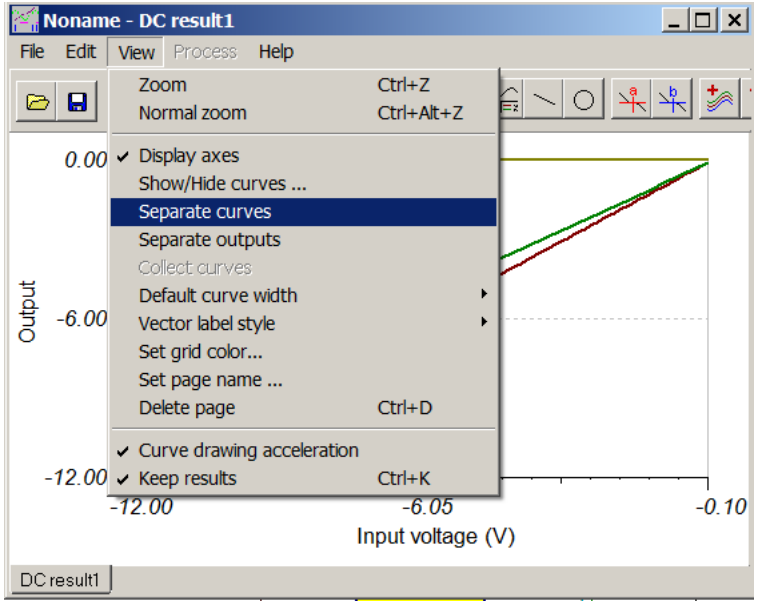


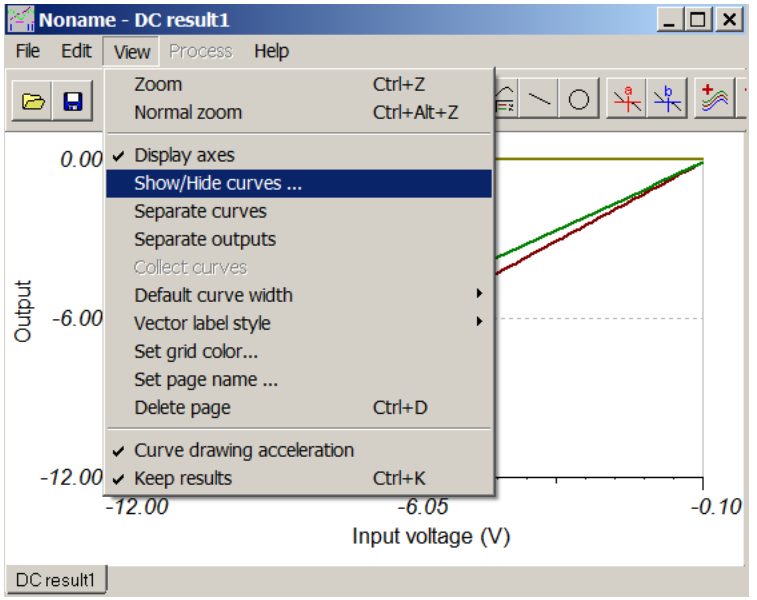
3. (continued). The dc transfer characteristic is done as is shown below.





3. (continued). Below are some TINA features that can be used to format you plots.





3. (continued). The post processor allows you to do math in TINA. In this case we do the calculation Rout = (Vin-Vmux)/AM1

Post processor