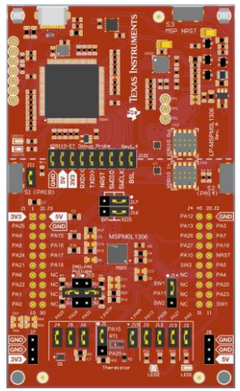
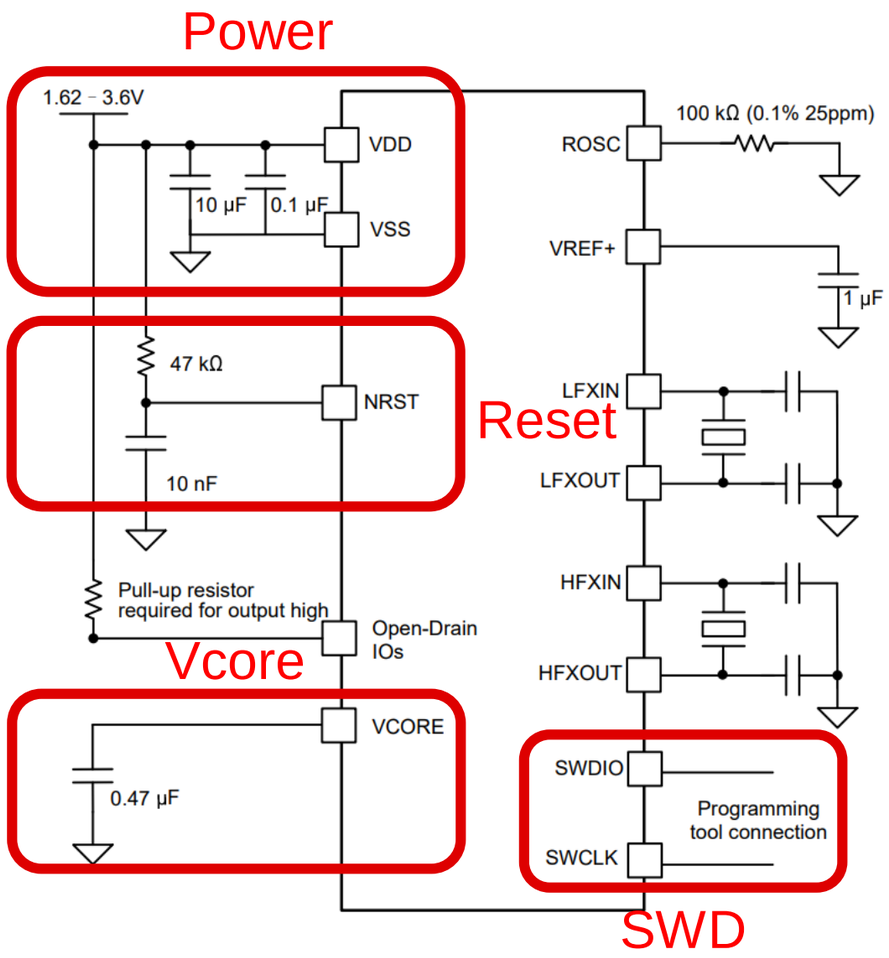
Hardware Development Guide Introduction

—— MSPM0 ecosystem training series

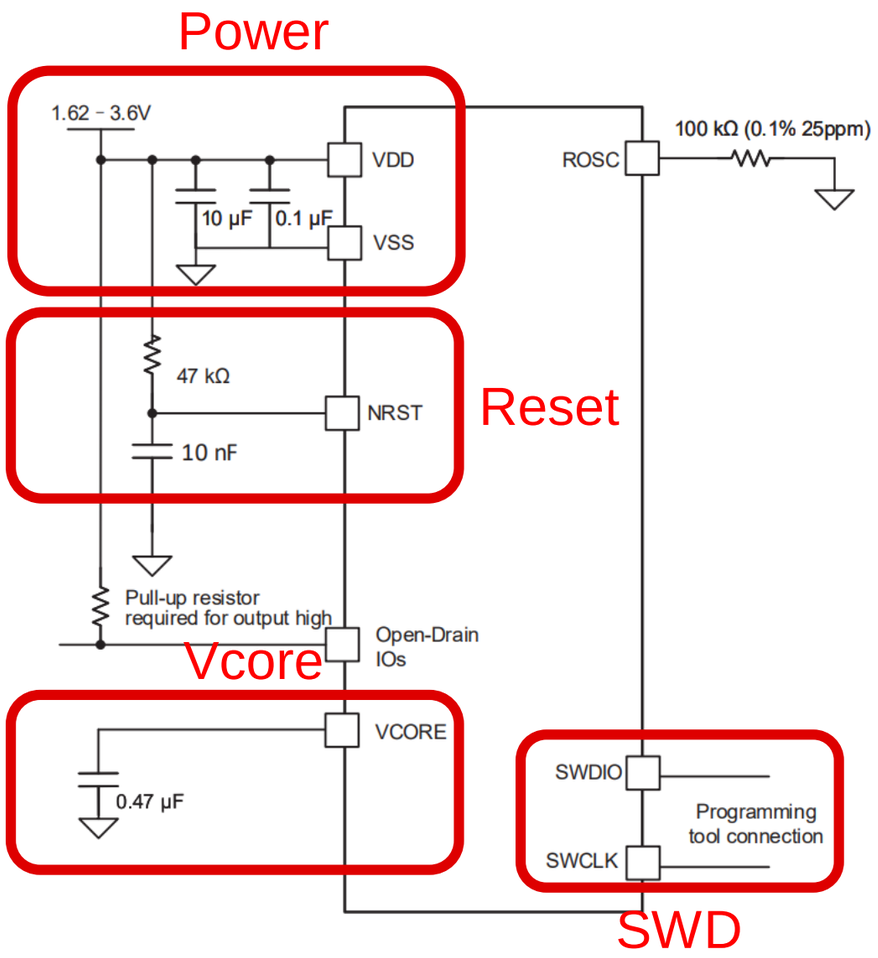
Presented by Johnson He

Hardware Design



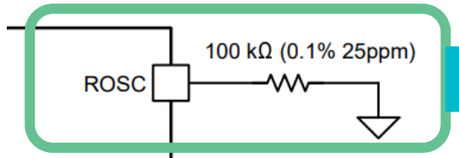


MSPM0G Typical Application Schematic

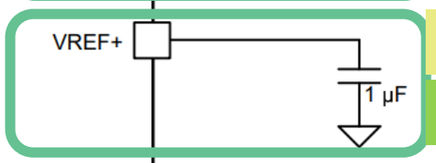


MSPM0L Typical Application Schematic

Hardware Design

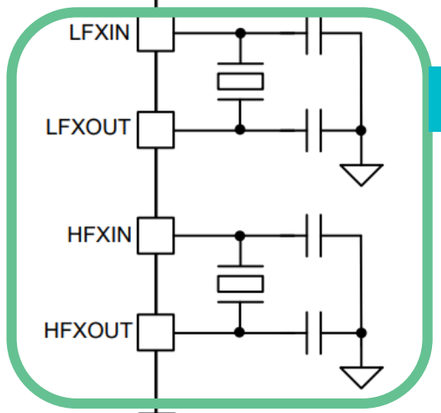


Enable ±1% on-chip HF Oscillator

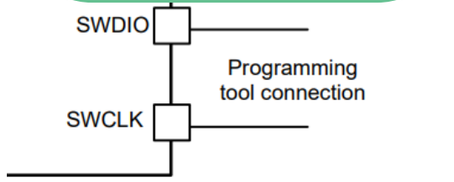


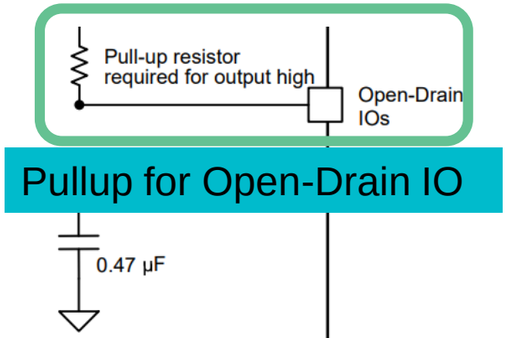
Gx device -> Vref output to pin, need filter capacitor

Lx device -> Need filter capacitor if use external reference



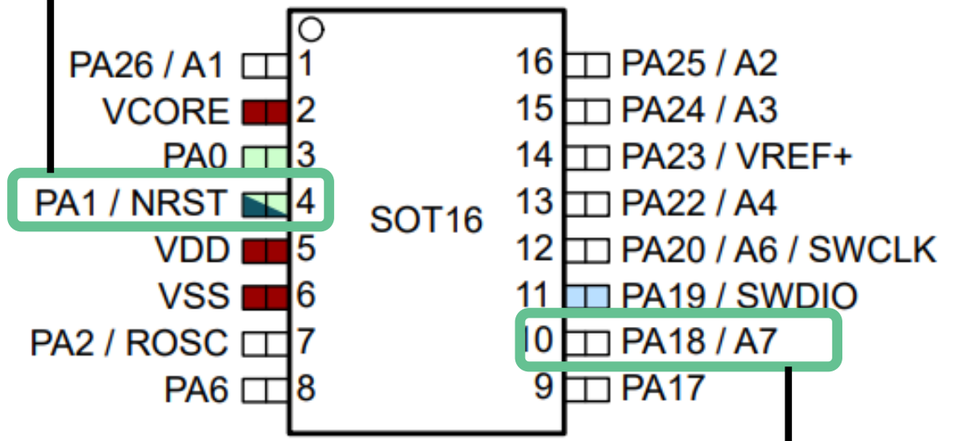
Gx only: External Crystal





Pullup for Open-Drain IO

Pullup to release reset, Reconfiguring NRST as GPIO



PA18: BSL Invoke(Pull-down if don’t need invoke BSL)

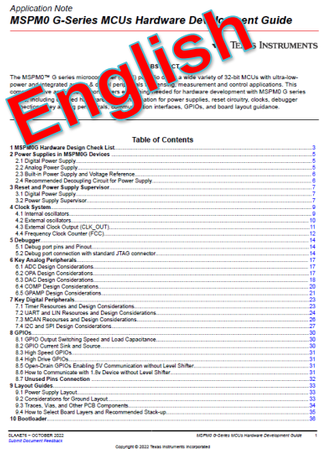
Check List

Pin (1)	Description	Requirements
VDD	Power supply positive pin	Place 10-µF and 100-nF capacitors between VDD and VSS, and keep those part close to VDD and VSS.
VSS	Power supply negative pin	
VCORE	Core voltage (typical: 1.35 V)	Connect a 470-nF capacitor to VSS, do not supply any voltage or apply any external load to the VCORE pin.
NRST	Reset pin	Connect an external 47-kΩ pullup resistor with a 10-nF pulldown capacitor.
ROSC	External reference resistor pin	• Connect an external 100-kΩ ±0.1% 25-ppm resistor to VSS to enable high SYSOSC accuracy if needed. • Keep open is OK if does not have high accuracy requirement for SYSOSC.
VREF+	Voltage reference power supply for external reference input	• When using VREF+ and VREF- to bring in an external voltage reference for analog peripherals such as the ADC, a decoupling capacitor must be placed on VREF+ to VREF-/GND with a capacitance based on the external reference source. • Keep open is OK if external voltage reference is not used.
VREF-	Voltage reference ground supply for external reference input	
SWCLK	Serial wire clock from debug probe	Internal pullup to VDD, does not need any external part.
SWDIO	Bidirectional (shared) serial wire data	Internal pulldown to VSS, does not need any external part.
PA0, PA1	Open-drain I/O	Pull-up resistor required for output high
PA18	Default BSL invoke pin	Keep pulled down to avoid entering BSL mode after reset. The BSL invoke pin can be remapped.
PAx (exclude PA0, PA1)	General-purpose I/O	Set corresponding pin functions to GPIO (PINCMx.PF = 0x1) and configure unused pins to output low or input with internal pullup or pulldown resistor.
OPAx_IN0-(2)	OPAx inverting terminal input 0	This pin is high-impedance, does not need any external part if unused.

MSPM0L134x Only

Reference Resource

MSPM0 Hardware Development Guide


English

Application Note
MSPM0 G-Series MCUs Hardware Development Guide

Texas Instruments

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Application Note
MSPM0 G 系列 MCU 硬件开发指南

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参考資料

Application Note
『MSPM0 G シリーズ MCU ハードウェア開発ガイド』

Texas Instruments

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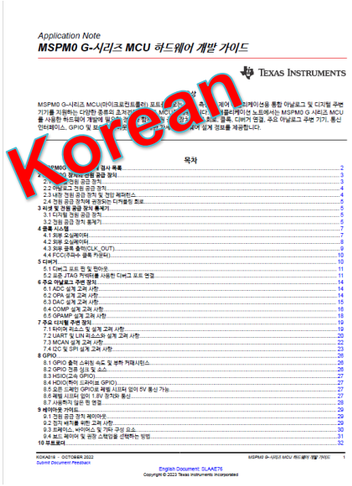

Korean

Application Note
MSPM0 G-시리즈 MCU 하드웨어 개발 가이드

Texas Instruments

목차

Power Supply

Reset & Debugger

Clock System

Bootloader

GPIO

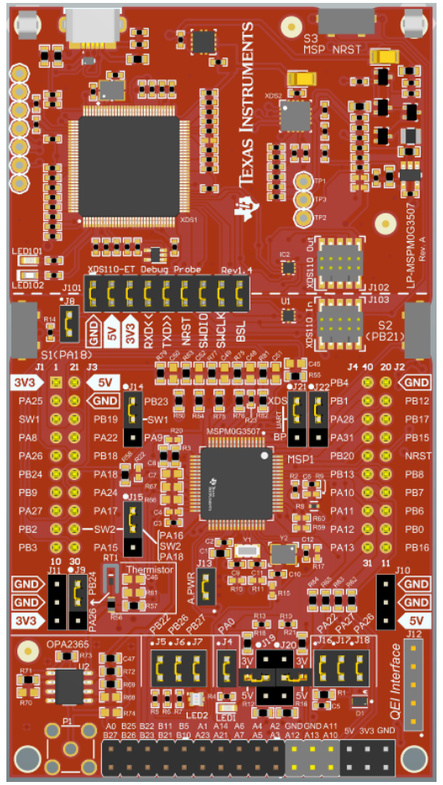
Layout

Digital Peripherals

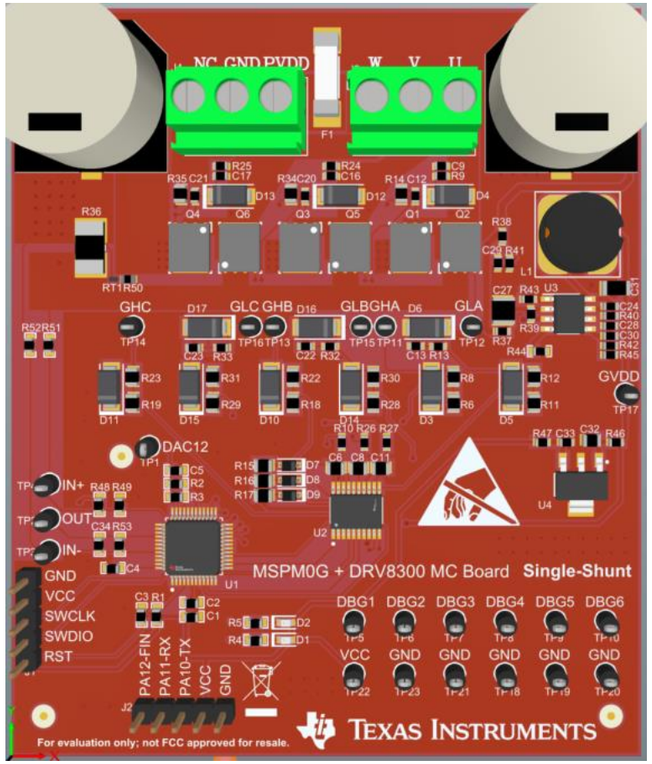
Analog Peripherals

Texas Instruments

Reference Resource

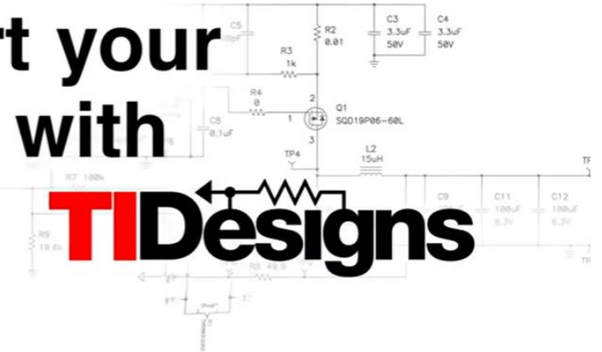


MSPM0 Launchpad



EVM Board

Jumpstart your designs with TIDesigns



TEXAS INSTRUMENTS

TI Design Materials

- Focus on actual application
- Software
- Hardware design files
- Technical documentation and test reports

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