EtherCAT® Master on Sitara™ Processors

EtherCAT® Master on Sitara™ Processors Training Series [Part 3]

Time-Triggered Send (TTS) + Sitara Scalability & Flexibility

Training series agenda

Part 1:

- Overview of Training Series
- Sitara processors family in factory automation
- EtherCAT protocol technology review

Part 2:

- Acontis EtherCAT master software architecture on top of TI-RTOS and RT Linux
- CoDeSys EtherCAT master software architecture on top of RT Linux

Part 3:

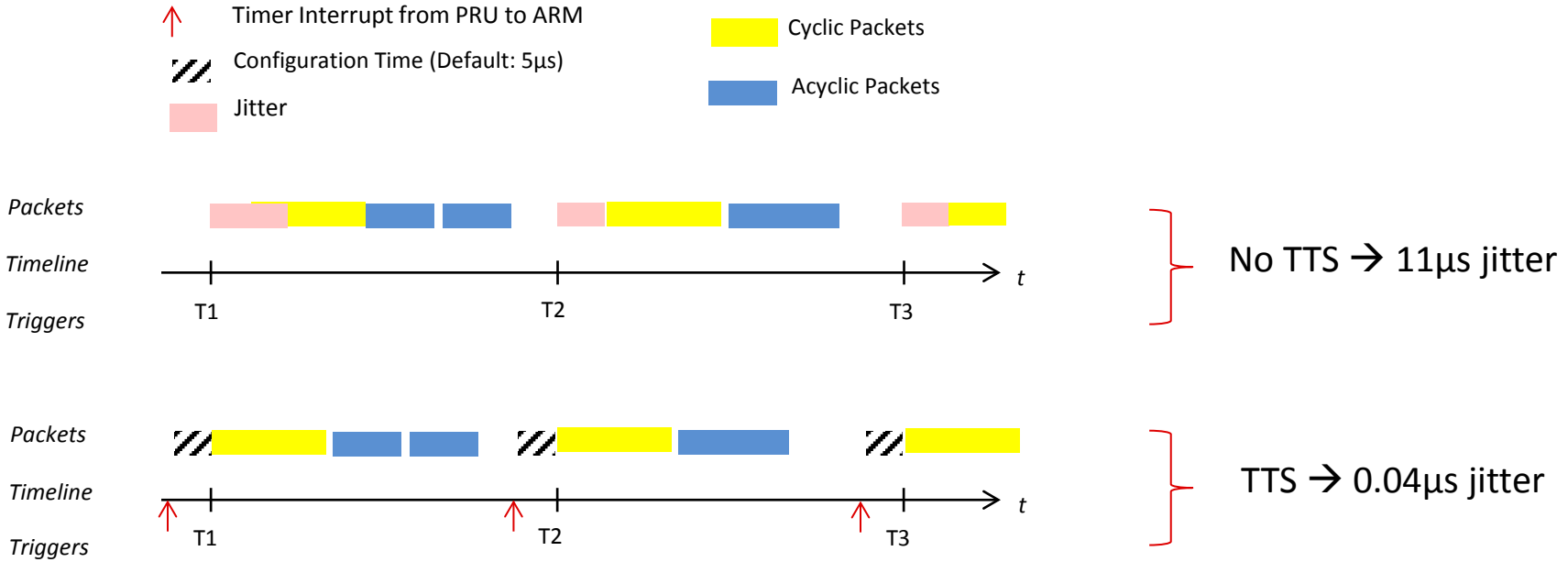
- EtherCAT master + time-triggered send (TTS)
- EtherCAT master on Sitara: A scalable and flexible solution

EtherCAT Master + Time-Triggered Send (TTS)

PRU-ICSS time-triggered send (TTS)

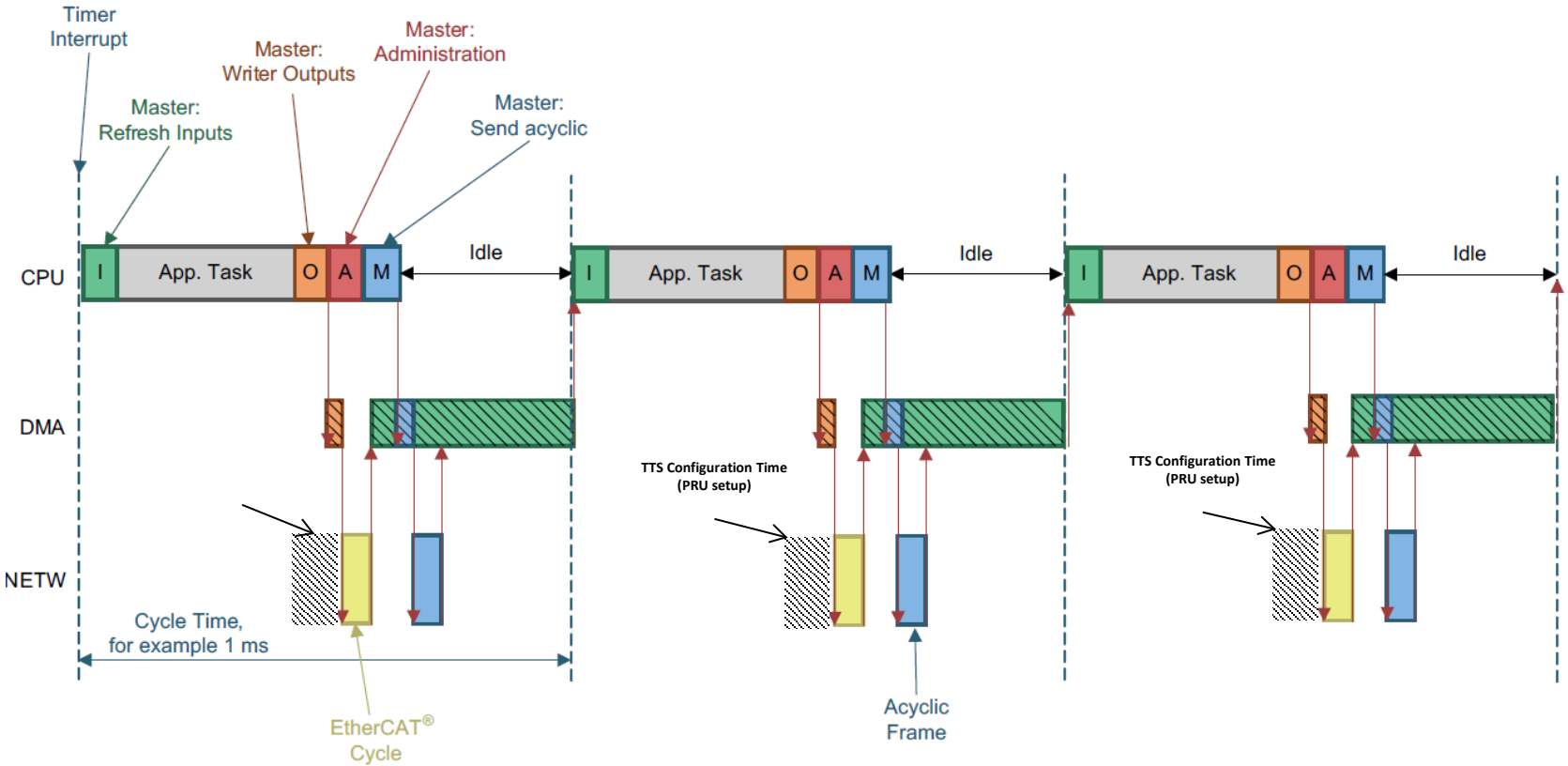
- The EMAC time-triggered send (TTS) is used to expand classical Ethernet to meet deterministic, time-critical, or safety-relevant conditions:
  - Helps to reduce transmission jitter from 10us range to 40ns
  - Can be dynamically enabled and disabled by the host
  - Designed to facilitate transmission of packets at pre-defined cyclic instants/triggers
- How it works:
  - TTS initializes when the application provides the first cyclic trigger and the cycle period.
  - PRU firmware then sets cyclic triggers repeatedly and sends queued cycle packets.

TTS jitter reduction through PRU-ICSS



For more details refer to:
http://processors.wiki.ti.com/index.php/ICSS_EMAC_LLD_developers_guide#Time_Triggered_Send

EtherCAT Master + TTS bus timing diagram



EtherCAT Master on Sitara: A Scalable and Flexible Solution

Sitara processors portfolio for industrial applications

I/O Modules, Slave PLCs, entry-level HMI, RTUs, Merging Units	*Connected Industrial Drives, PLC, mid-range HMI*	*Master PLC, Motion Control, high-end HMI, Protection Relays, Ethernet switches*
		
AM335x	**AM437x**	**AM57x**
• Highly integrated, power-efficient • ARM Cortex-A8 from 300MHz to 1GHz • Low system cost with support for PRU-ICSS for industrial protocols, as well as GbE, CAN, and graphics	• High performance, highly efficient • ARM Cortex-A9 from 300MHz to 1GHz • Expanded peripherals, including upgraded PRU-ICSS for encoder feedback, sigma-delta filtering	• Top-of-the-Line Sitara performance • Single or dual-core ARM Cortex-A15 up to 1.5GHz • Integrated M4 and DSP cores • Upgraded graphics performance, dual PRU-ICSS, PCIe

Key market differentiators

- PRU-ICCS offers TTS to EtherCAT Master.
- EtherCAT Master TI Designs and ready-to-use software available for Acontis EC-Master running on both TI-RTOS and RT-Linux OS.
- TI Design for CoDeSys EtherCAT Master on RT-Linux is in development.
- TI offers the option to use regular Ethernet port (CPSW-GMAC) or PRU-ICSS for running EtherCAT Master.
- Scalability and flexibility; EtherCAT master can be easily ported:
  - From/to AM335x
  - From/to AM437x
  - From/to AM57x

EtherCAT Master Reference Design for AM57x Gb Ethernet & PRU-ICSS

TIDEP-0079

TIDesigns

Features

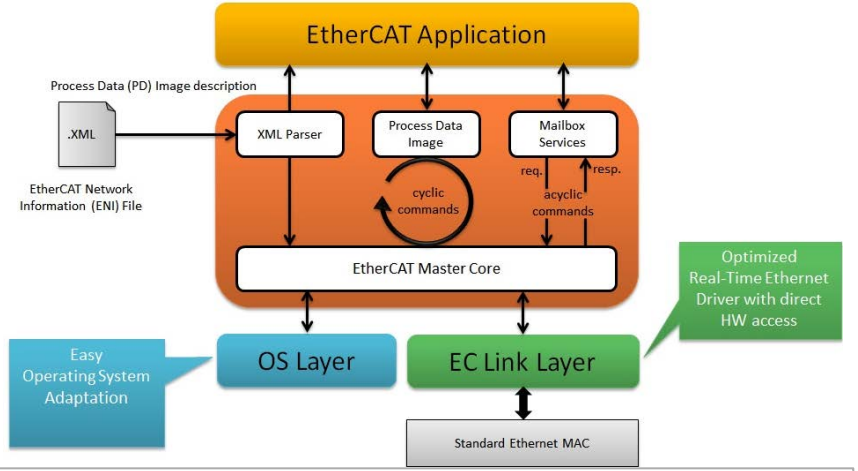
- Demonstrates use of EtherCAT Master on AM572x processor
- Supports use of either Gb switch (CPSW) or PRU-ICSS for EtherCAT master
- Built using the highly-portable industry-accepted Acontis EC-Master stack
- EtherCAT Class A or Class B master stack according to ETG. 1500 specification

Benefits

- Example for implementing EtherCAT master on both the Gb switch (CPSW) and the PRU-ICSS Ethernet ports for design flexibility
- Highly portable Acontis stack combined with high-performance Sitara AM57x CPU provides a flexible EtherCAT master solution
- Cycle CPU consumption: 20us for CPSW and 25us on ICSS-PRU
- This reference design is tested on the TMDXIDK5728 board and includes documentation, software, demo application, and HW design files.

Tools and Resources

- **TIDEP0079**
- **Design Guide**
- **Design files:** Schematics, BOM, Gerbers, software, and more
- **Device datasheets:**
  - AM5728BABCXA
  - TMDXIDK5728



For more information

- Sitara Processors Overview http://www.ti.com/sitara
- EtherCAT Masters TI Designs:
  - Acontis EtherCAT Master Stack Reference Design: http://www.ti.com/tool/tidep0043
  - EtherCAT Master Reference Design on Sitara AM57x Gb Ethernet and PRU-ICSS with TTS: http://www.ti.com/tool/tidep0079
- Online training:
  - Sitara AM57x Processors: https://training.ti.com/am57x-sitara-processors-training-series
  - Sitara AM437x Processors: https://training.ti.com/am437x
- CoDeSys EtherCAT Master: https://www.codesys.com/products/codesys-fieldbus/industrial-ethernet/ethercat.html
- Acontis EtherCAT Master for TI processors: http://www.acontis.com/eng/products/downloads/ethercat-for-ti-processors.html
- Other industrial protocols: http://www.ti.com/tool/PRU-ICSS-INDUSTRIAL-SW
- For questions about this training, refer to the E2E Sitara Processors Forums: https://e2e.ti.com/support/arm/sitara_arm/f/791