Getting Best Performance From Your GSPS and RF Sampling ADC Designs

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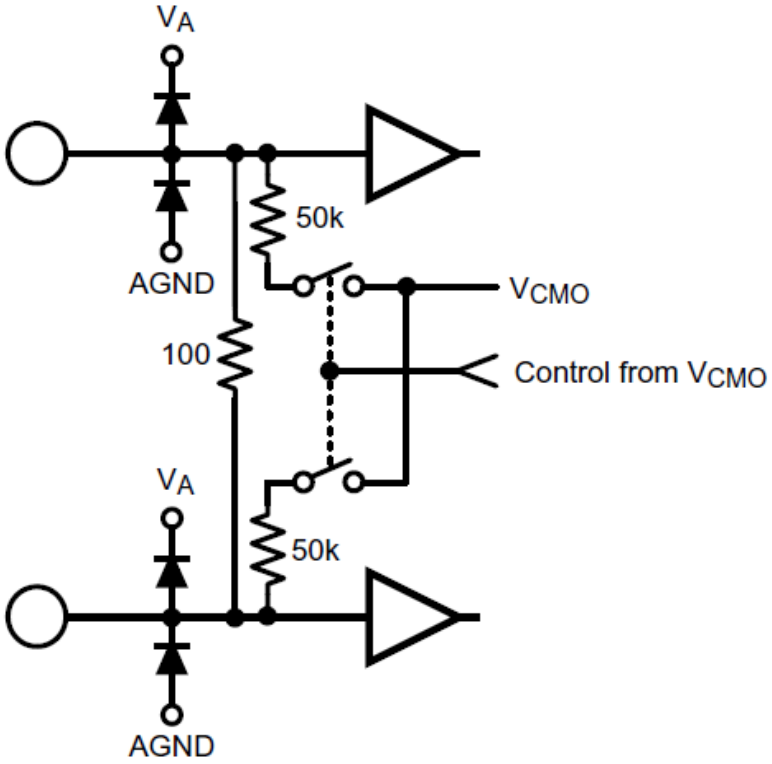
Detailed agenda

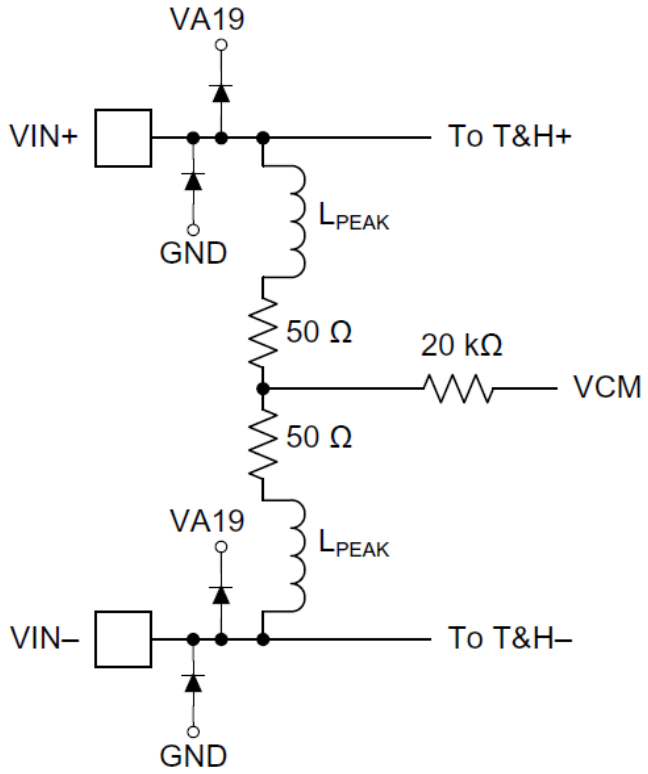
- Matching Networks for GSPS and RF Sampling ADC inputs
  - Characteristics of GSPS and RF Sampling ADC inputs
  - Types of matching networks
  - Methods to determine the appropriate matching network
  - High frequency board design guidelines
  - Verification
- Clocking Requirements for GSPS and RF Sampling ADCs
  - Impacts of phase noise/jitter on ADC performance
  - Sources of phase noise/jitter
  - Basic clock selection criteria
  - Methods to minimize phase noise/jitter

MATCHING NETWORKS FOR GSPS AND RF SAMPLING ADC INPUTS

GSPS ADC inputs – ADC12DXX00RF



GSPS ADC inputs – ADC12J4000



RF Sampling ADC inputs – ADC32RF45

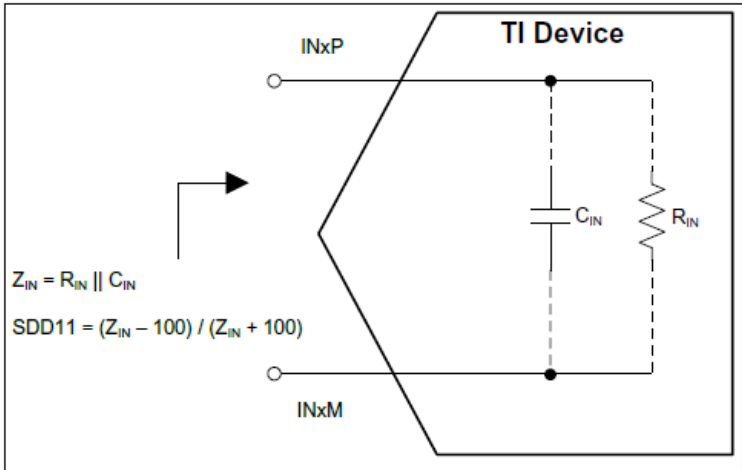


Figure 60. Equivalent Input Impedance

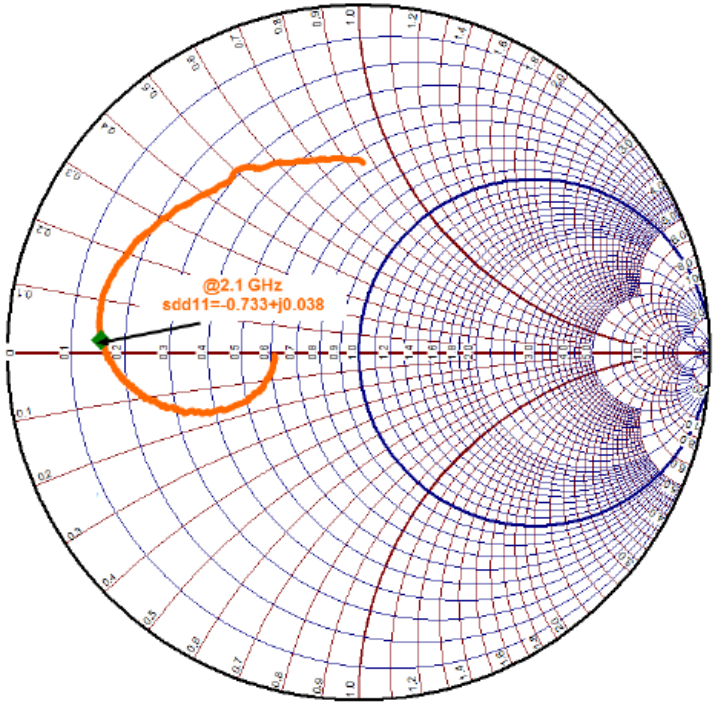
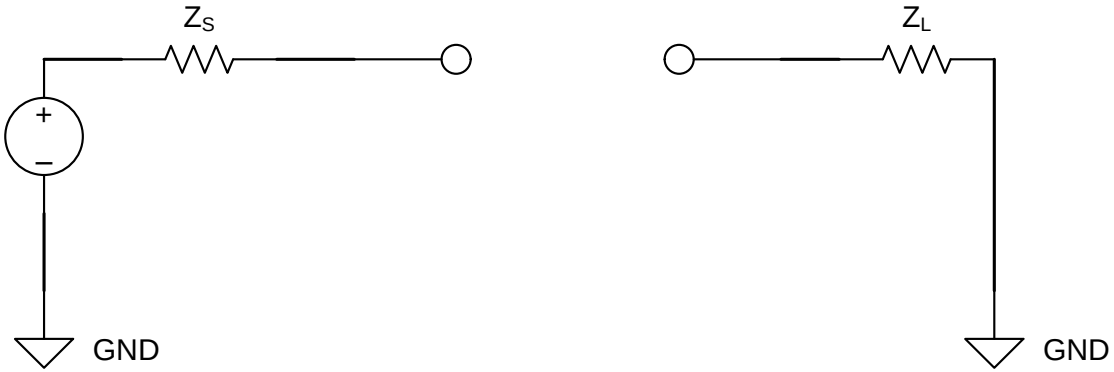


Figure 61. SDD11 Over the Input Frequency Range

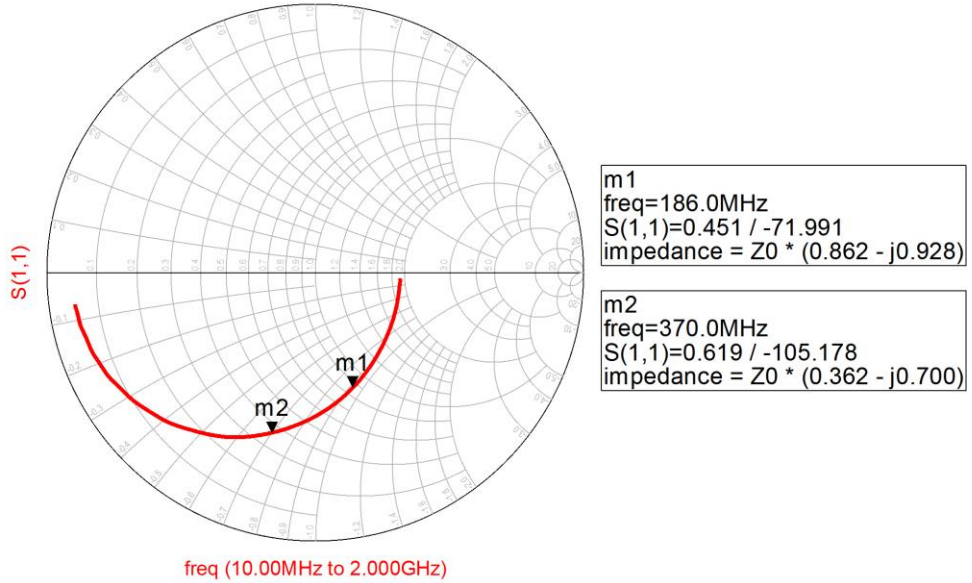
What is impedance matching?

- Signal sources will have a specific output impedance
- Loads or receivers will have a corresponding input impedance
- Systems have matched impedance when source and load impedances are the same



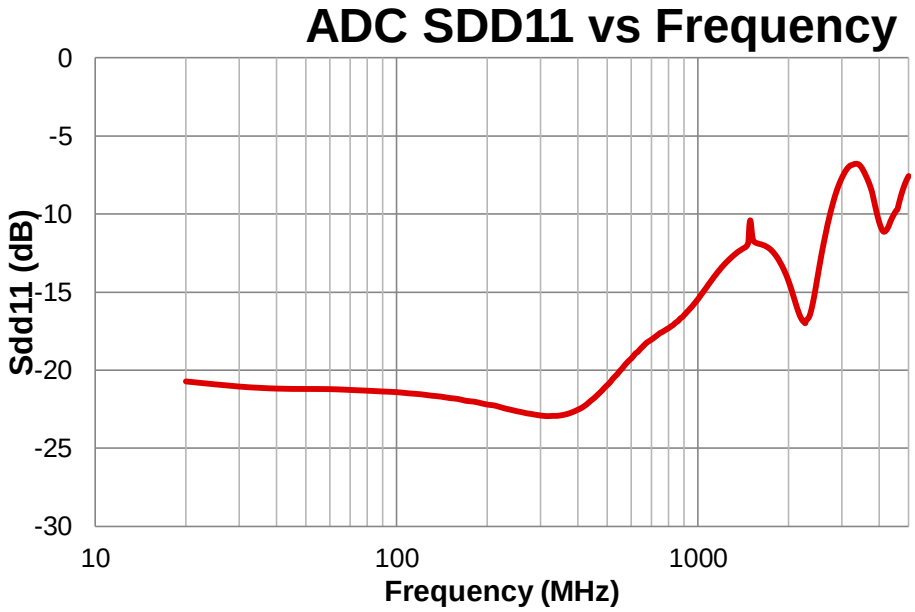
ADC input impedance – Smith Chart

- Smith Chart – Complex Impedance
- Example has significant impedance change at higher frequencies



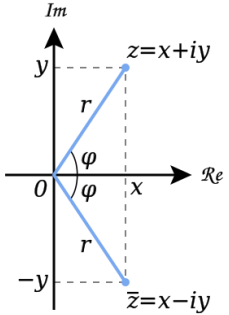
ADC input impedance – S-parameters

- S11 – Input return loss
- This example has better high frequency performance



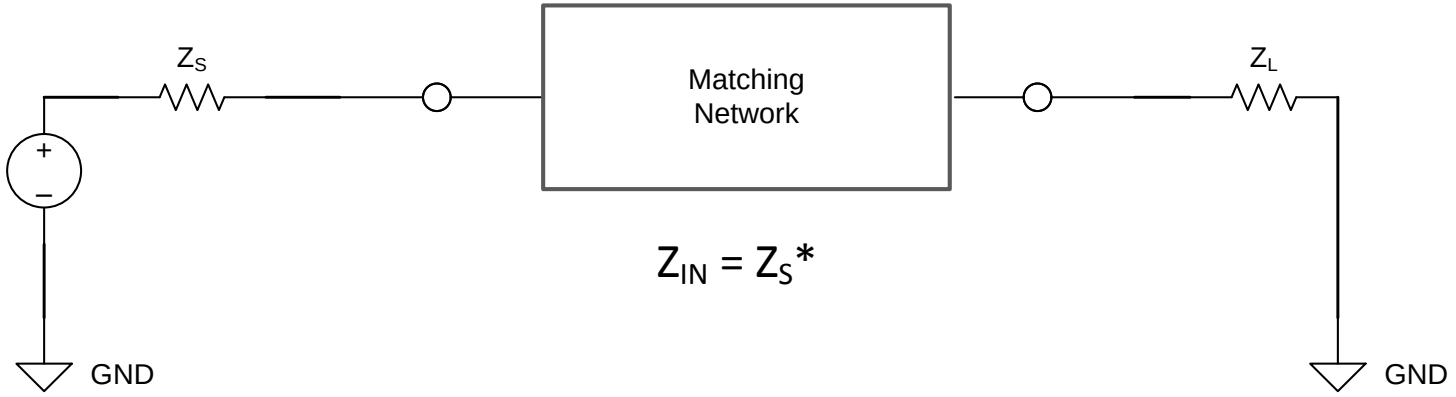
Why is impedance matching important?

- Optimum (most efficient) power transfer occurs when source and load impedances are matched
- For pure resistance this means $R_S = R_L$
- For complex impedance this means the load is the complex conjugate of the source impedance, or: $Z_L = Z_S^*$
- For complex conjugates the real portions are equal, and the complex portions are equal in magnitude and opposite in sign:



Impedance matching

- Source and load devices will have impedances that are fixed by design
- The impedance matching exercise involves designing a network which, in combination with the existing load impedance, provides a matching load to the source



Types of matching networks

1. LC Pi
2. LC Tee
3. TRL ¼ Wave
4. TRL Single/Double Stub
5. LC Bandpass
6. LC Pseudo Lowpass
7. TRL Pseudo Lowpass
8. TRL Stepped Impedance
9. Custom Network

- 1-4 for narrow bandwidths
- 5-8 for wideband matching

Determining the appropriate matching network

- Software modeling
  - Keysight EEsof Genesys
    - http://edadocs.software.keysight.com/display/genesys2009/Match
    - http://www.keysight.com/main/eventDetail.jspx?cc=US&lc=eng&ckey=2589956&nid=-33396.0.00&id=2589956
    - http://www.keysight.com/main/redirector.jspx?ckey=2655545&nid=-33396.0.00&action=ref&lc=eng&cname=AGILENT_EDITORIAL&cc=US
  - Mathworks
    - Antenna https://www.mathworks.com/help/rf/examples/designing-broadband-matching-networks-part-1-antenna.html?s_tid=srchtitle
    - Amplifier https://www.mathworks.com/help/rf/examples/designing-broadband-matching-networks-part-2-amplifier.html?s_tid=srchtitle

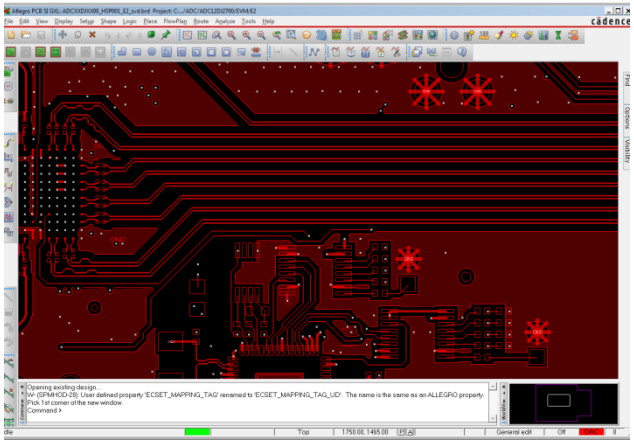
PCB LAYOUT BEST PRACTICES

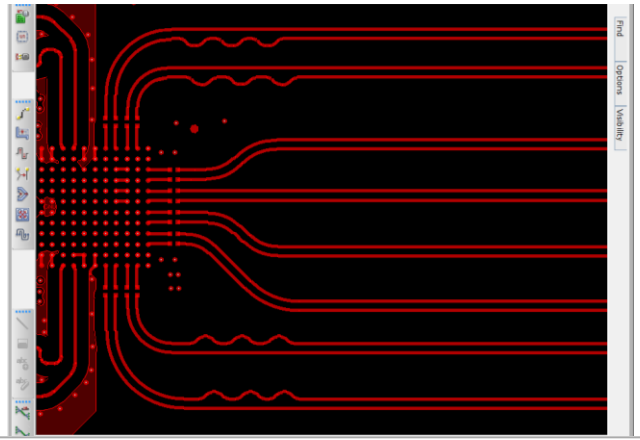
Impedance controlled routing – best practices

- Differential Pairs 100 ohm
- Single Ended 50 ohm
- Minimize discontinuities in differential and SE impedance
- Minimize other signal impairments
- High frequency signal paths (ADC inputs, DAC outputs)
- High speed data links (LVDS, JESD204B, PCIe, etc.)

Differential pairs – stripline coupling

- E1 – Tightly Coupled – Coupling between P and N is key to 100 ohm differential impedance. Serpentines in P or N for length matching alter differential impedance and cause a discontinuity
- A – Loosely Coupled – Reduced coupling between P and N means impedance is more like two 50 ohm traces than a 100 ohm differential pair. Serpentines in one trace for length matching have small effect on diff impedance

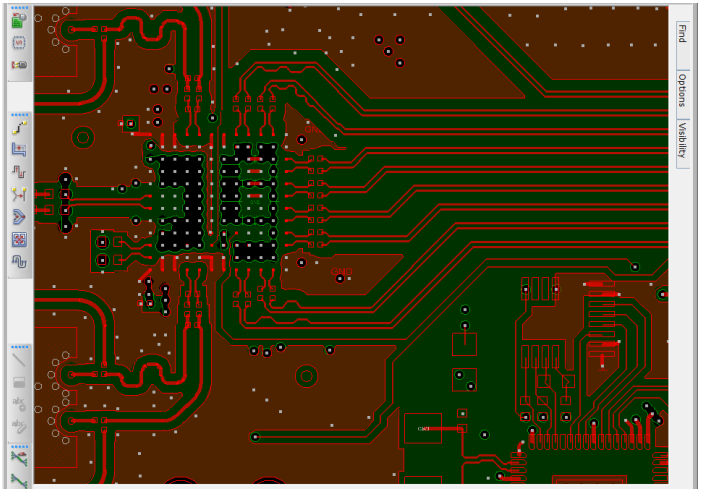


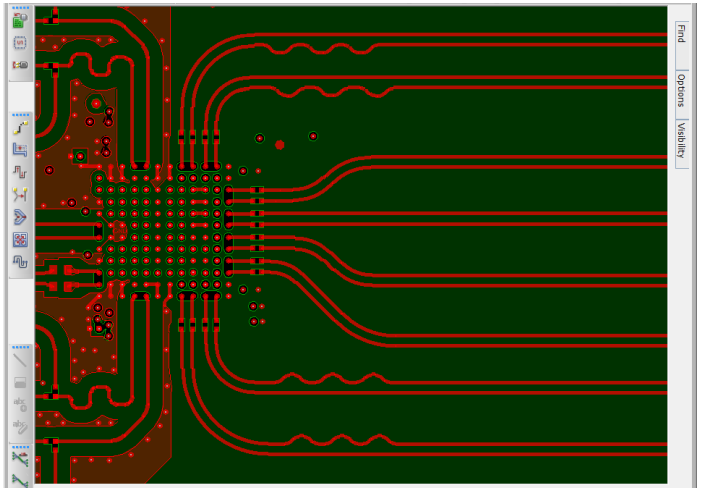


Differential pairs - spacing

- E1 – Tight pair to pair spacing causes increased crosstalk

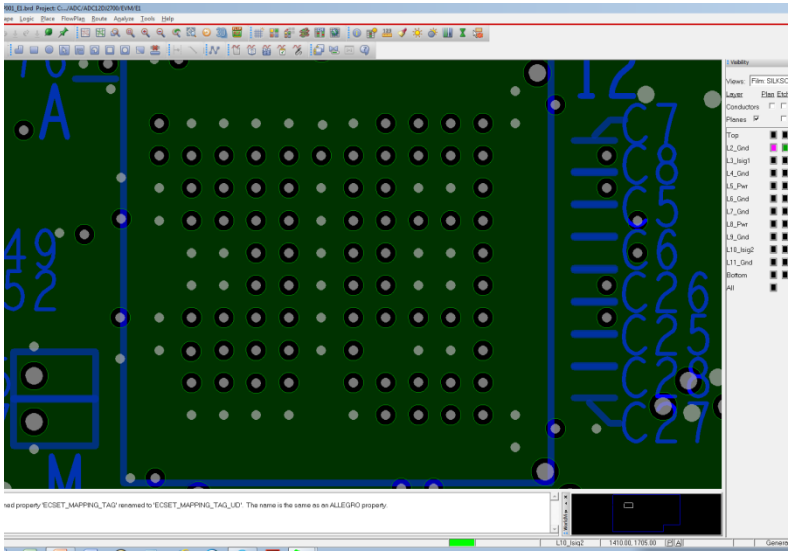
- A – Wide pair to pair spacing minimizes crosstalk

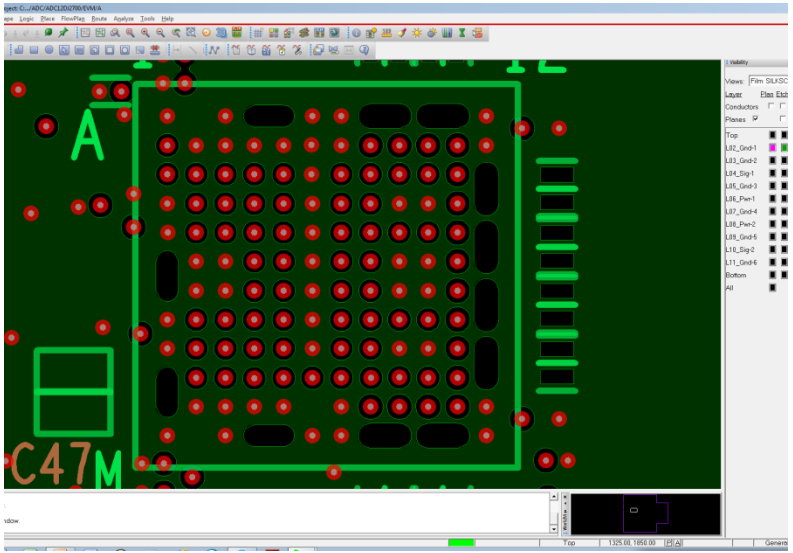




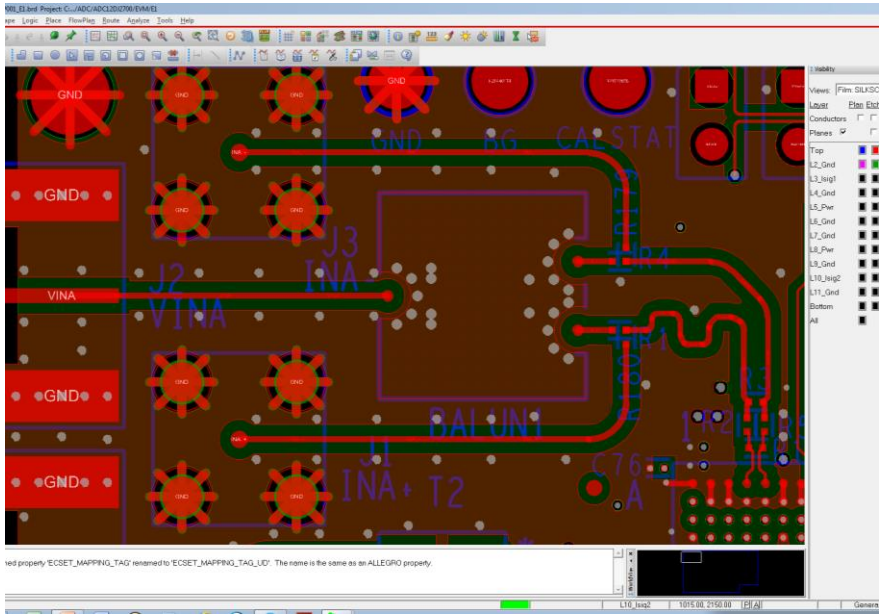
Ground plane details – component pads

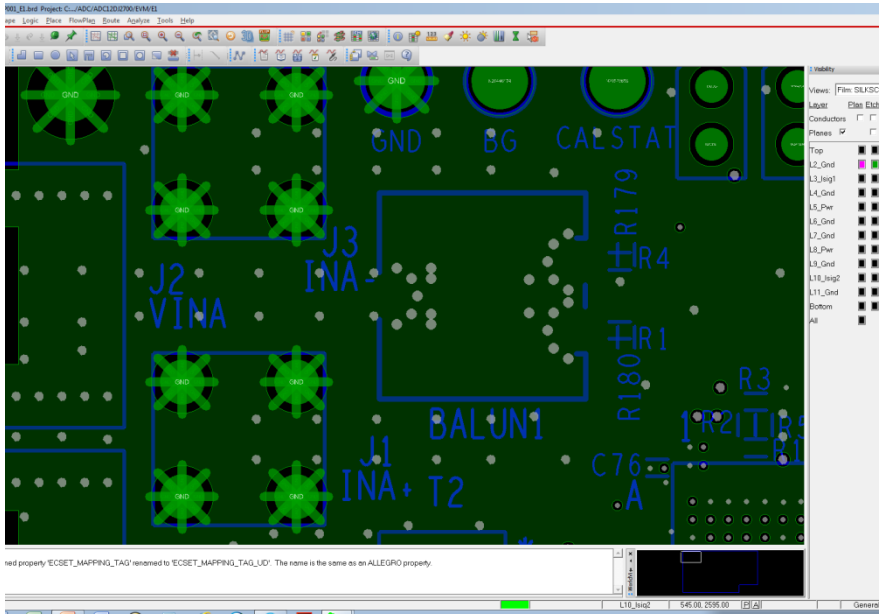
- Add cutouts under component pads to maintain 50 ohm SE impedance at those locations
  - IC pads
  - Connector pads (SMA, etc.)



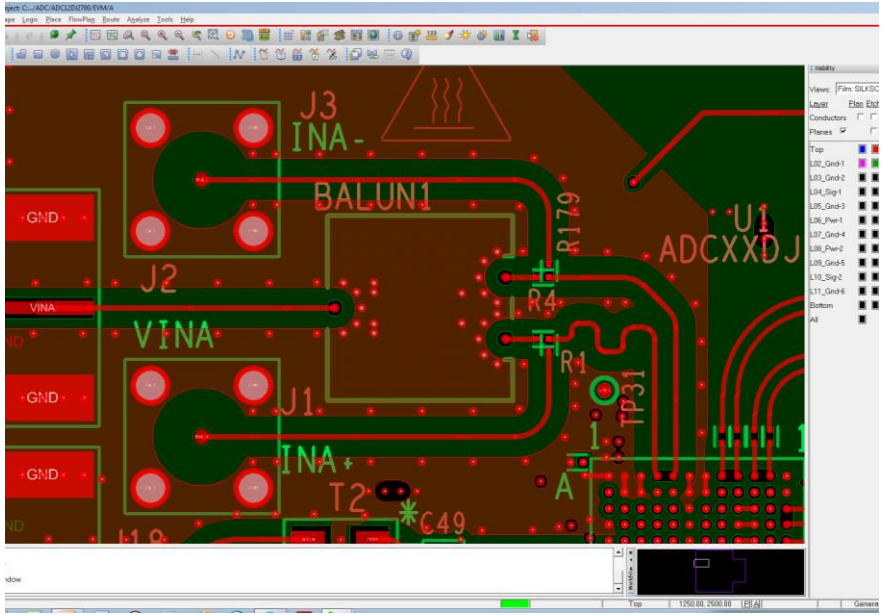


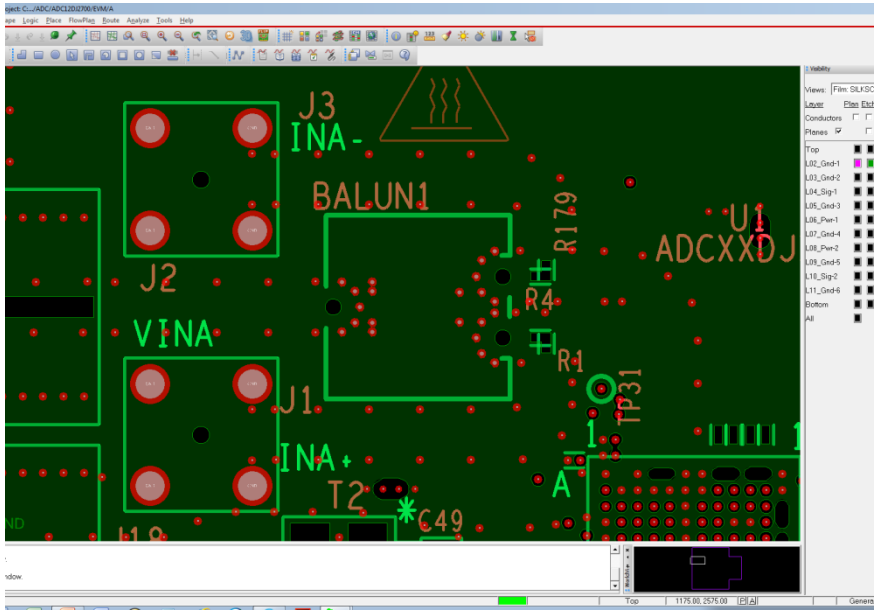
Component Pads – No ground voids





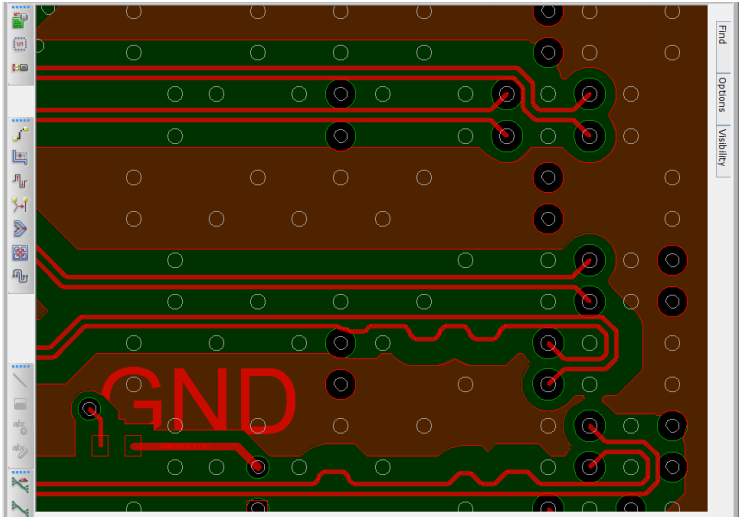
Component Pads – With ground voids

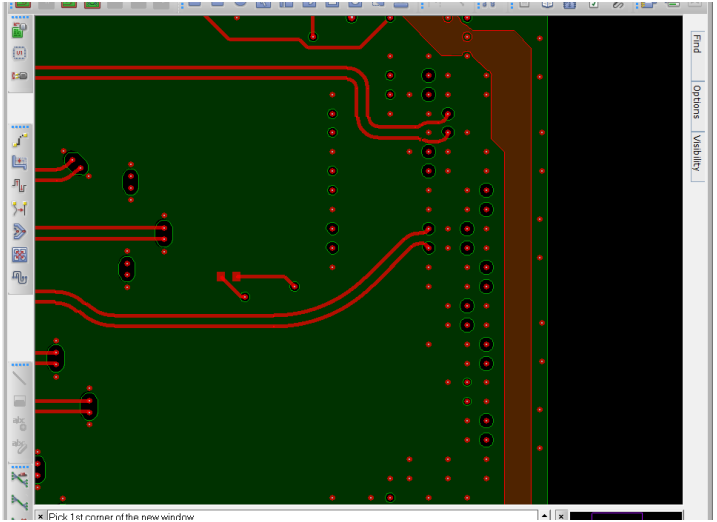




Ground plane details – ground voids

- Ensure good continuous ground plane under high speed traces
- Move or eliminate signal or ground vias near high speed traces to keep related ground voids away



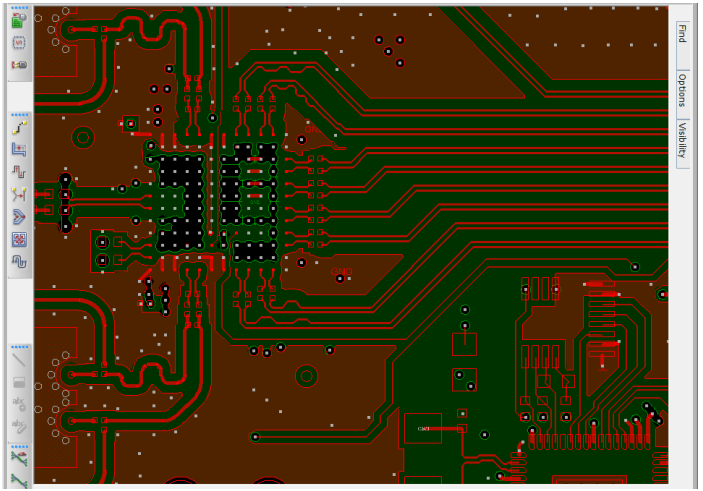


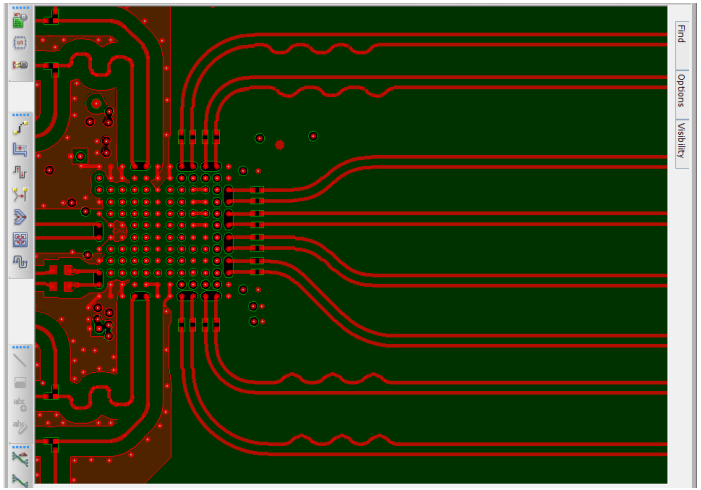
Minimizing impedance discontinuities

- Corners
  - Use 45 or smooth curves for high frequency signals
- Layer changes – vias
  - Minimize stubs
  - Provide adjacent GND tie vias
  - Adequate GND pullback from signal vias

Corners

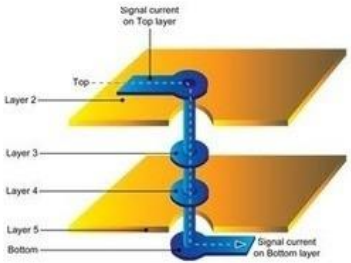
- For high frequency signals avoid 90 degree corners
- Use 45 degree (up to a 1-2 GHz) or radiused curves (above 2 GHz)



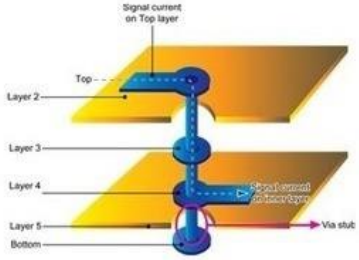


Layer change vias – avoid stubs

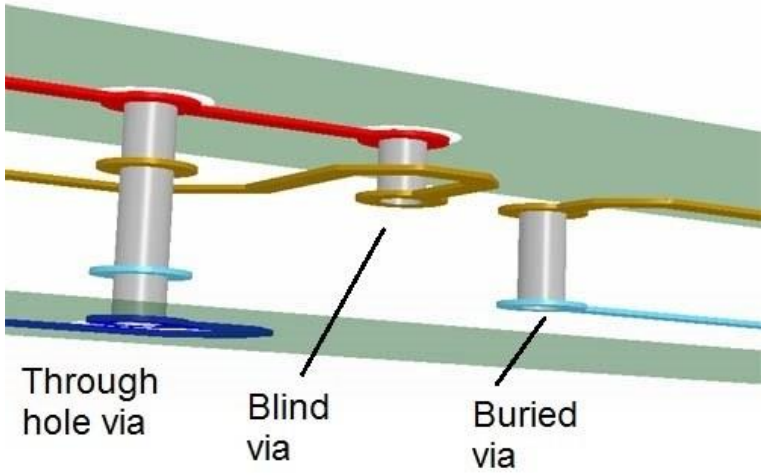
- Good - Via top (L1) to bottom (L12) has no stubs
- Bad - Via from top to L3 has large via extending to bottom of multi-layer board
  - Avoid this, or if absolutely necessary then back drilling, blind or buried vias can be used



No stub when a trace jumps from top layer to bottom layer

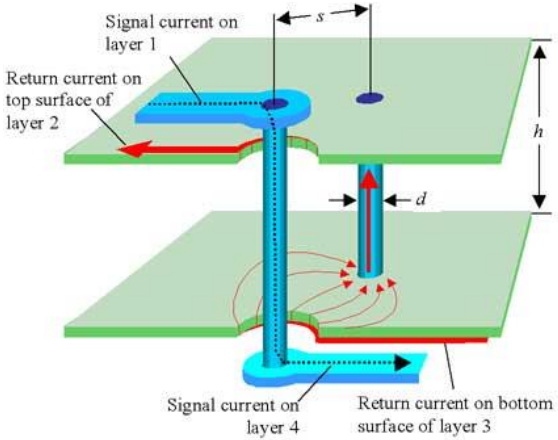


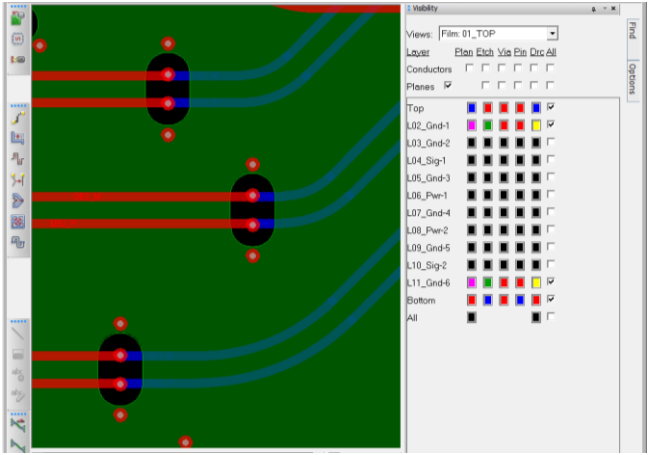
small stub gets created when a trace goes from top layer to an inner layer



Layer change vias – ground-tie reference vias

- Signal transitions from L1 to L12
- L1 signal is referenced to GND on L2, L12 signal is referenced to L11
- Image current in reference planes needs a low impedance path
- L2 and L11 ground planes must be tied together near where the signal via is located





PCB stackup – dielectrics and weaves

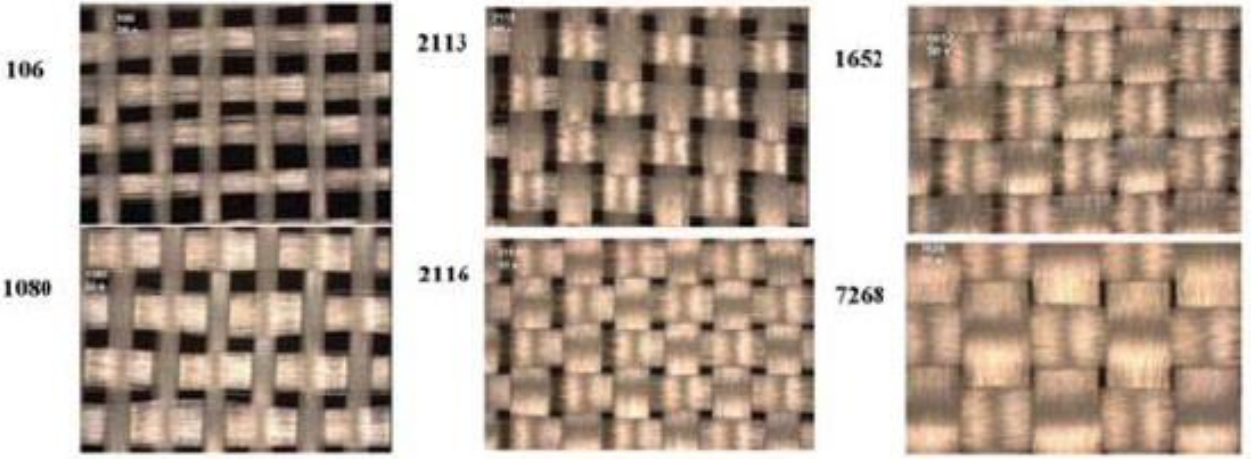
- Select low loss high frequency substrates for high frequency trace needs
  - Rogers 4350B
  - Panasonic Megtron 6
  - Use high frequency materials only on needed layers to reduce cost

Material Group	Vendor Specific	FR4 Relative Cost Factor
170 Tg FR4 (Baseline)	Nelco 4000-6	1
High Tg / Reliability-Filled	Isola 370HR	1.1
High Speed / Low Loss	Isola FR408	1.8
High Speed / Low Loss	Nelco 4000-13 EP	2.1
High Speed / Very Low Loss	Nelco 4000-13 EP SI	3.2
High Frequency	Arlon 85N	4
High Frequency	IS680-3.45	4.2
High Frequency	Megtron 6	5
High Frequency	Rogers 4350B	5.6

PCB stackup – dielectrics and weaves

- Use high frequency materials only on needed layers to reduce cost
- User tighter or flattened glass fiber weave for critical traces/layers
- Dielectric constant is more uniform

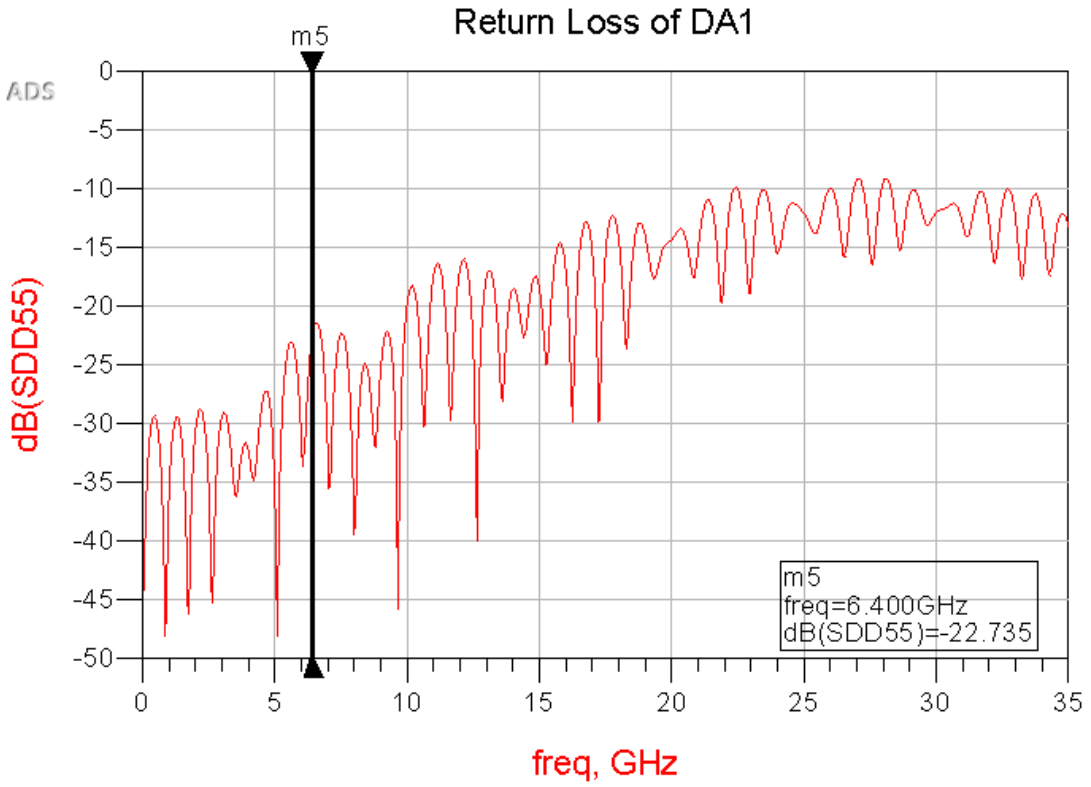
Figure 3. Different Styles of Fiberglass Weaves



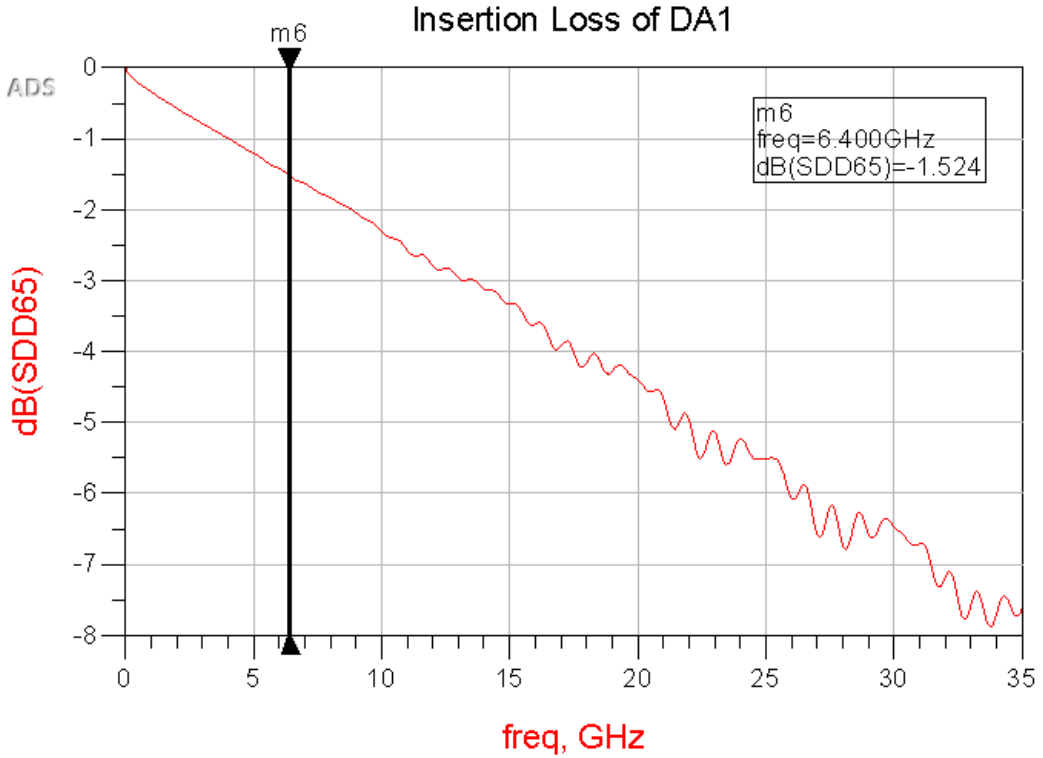
Post-layout simulation

- Modeling of TX, circuit board channel and RX
- Common tools are ADS, HFSS
- Modeled parameters
  - Return loss – reflection of transmitted signal as a function of frequency
  - Insertion loss – attenuation of transmitted signal as a function of frequency
  - TDR – reflection of transmitted pulse, gives indication of impedance discontinuities along the channel

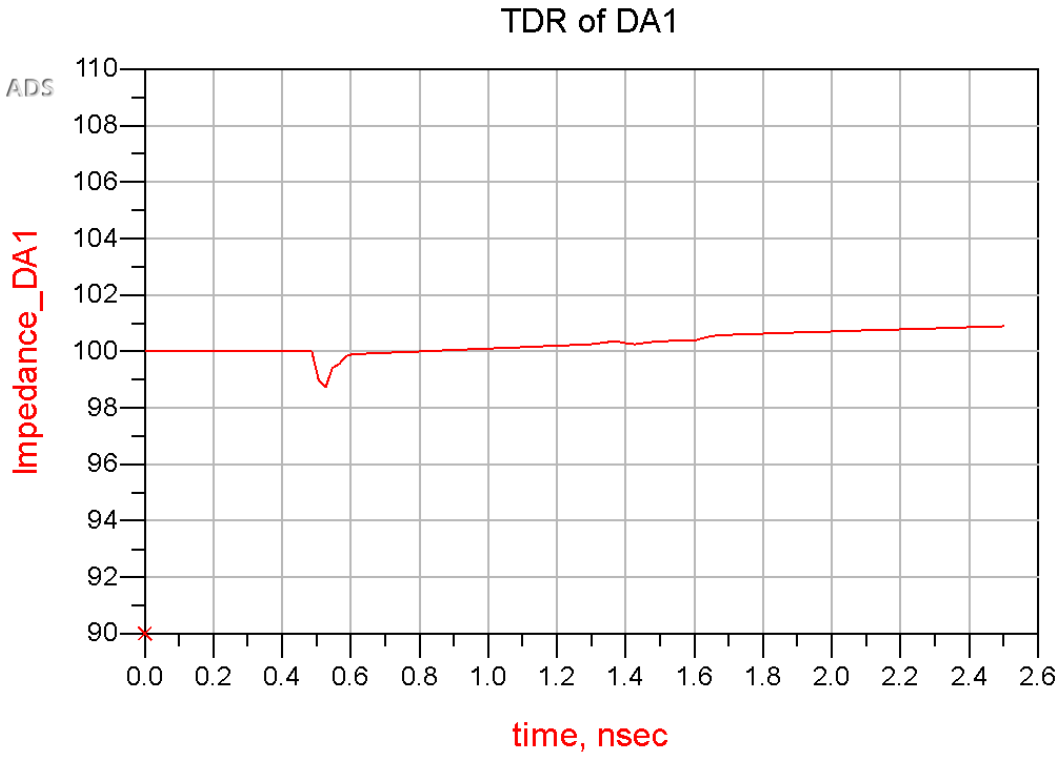
Return loss


Return Loss of DA1
m5
ADS
0
-5
-10
-15
-20
-25
-30
-35
-40
-45
-50
dB(SDD55)
0
5
10
15
20
25
30
35
freq, GHz
m5
freq=6.400GHz
dB(SDD55)=-22.735

Insertion loss

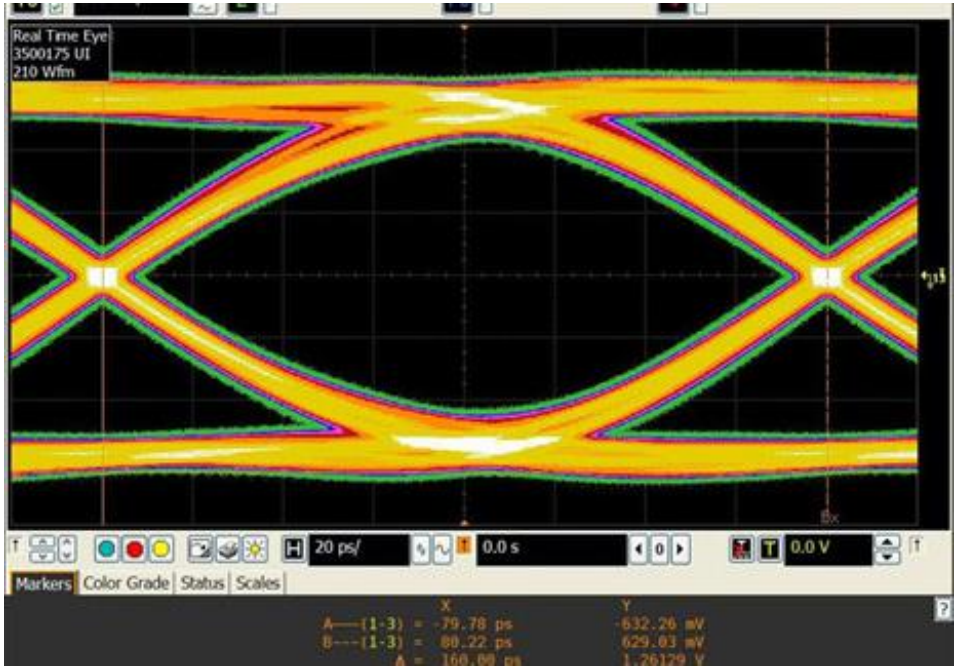


TDR


TDR of DA1
ADS
Impedance_DA1
110
108
106
104
102
100
98
96
94
92
90
0.0
0.2
0.4
0.6
0.8
1.0
1.2
1.4
1.6
1.8
2.0
2.2
2.4
2.6
time, nsec

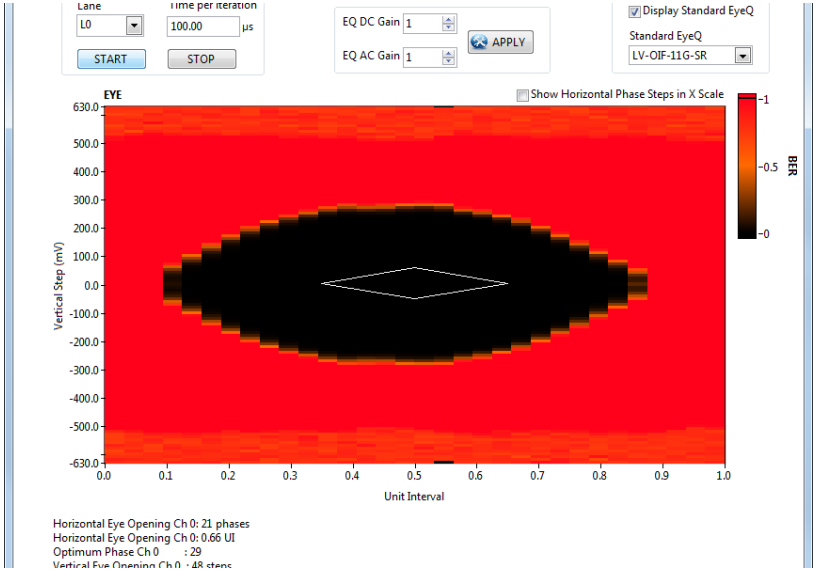
Verification - measurements

- Use test equipment to measure eye quality
  - Need good connector or probe access to signals



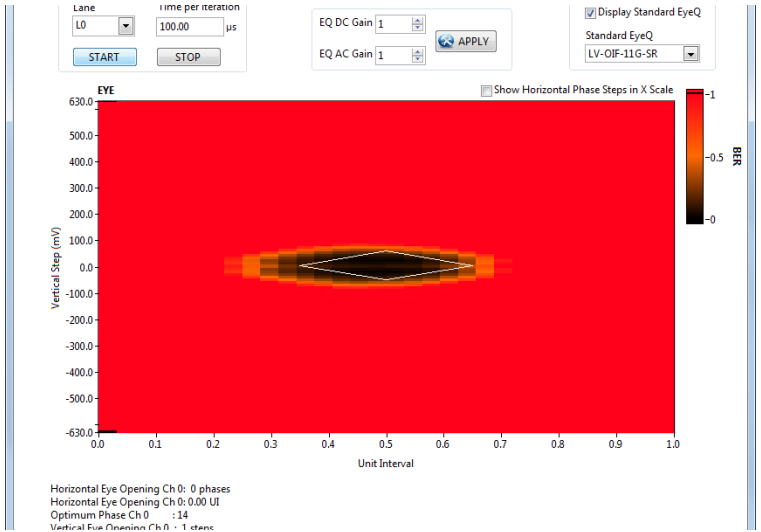
Verification - measurements

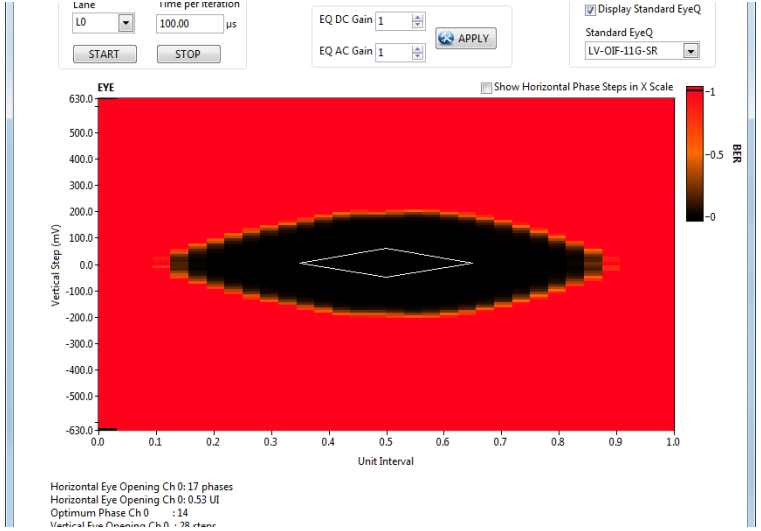
- Eye diagram analysis
  - Send adequately random data on link (PRBSxx)
  - Use eye-scan feature of data receiver to reconstruct RX eye



Verification – optimize, update measurements

- Optional – Compensate for channel impairments
  - Use TX de-emphasis or pre-emphasis
  - Use RX equalization
  - Second plot below shows results with increased TX pre-emphasis





CLOCKING REQUIREMENTS FOR GSPS AND RF SAMPLING ADCS

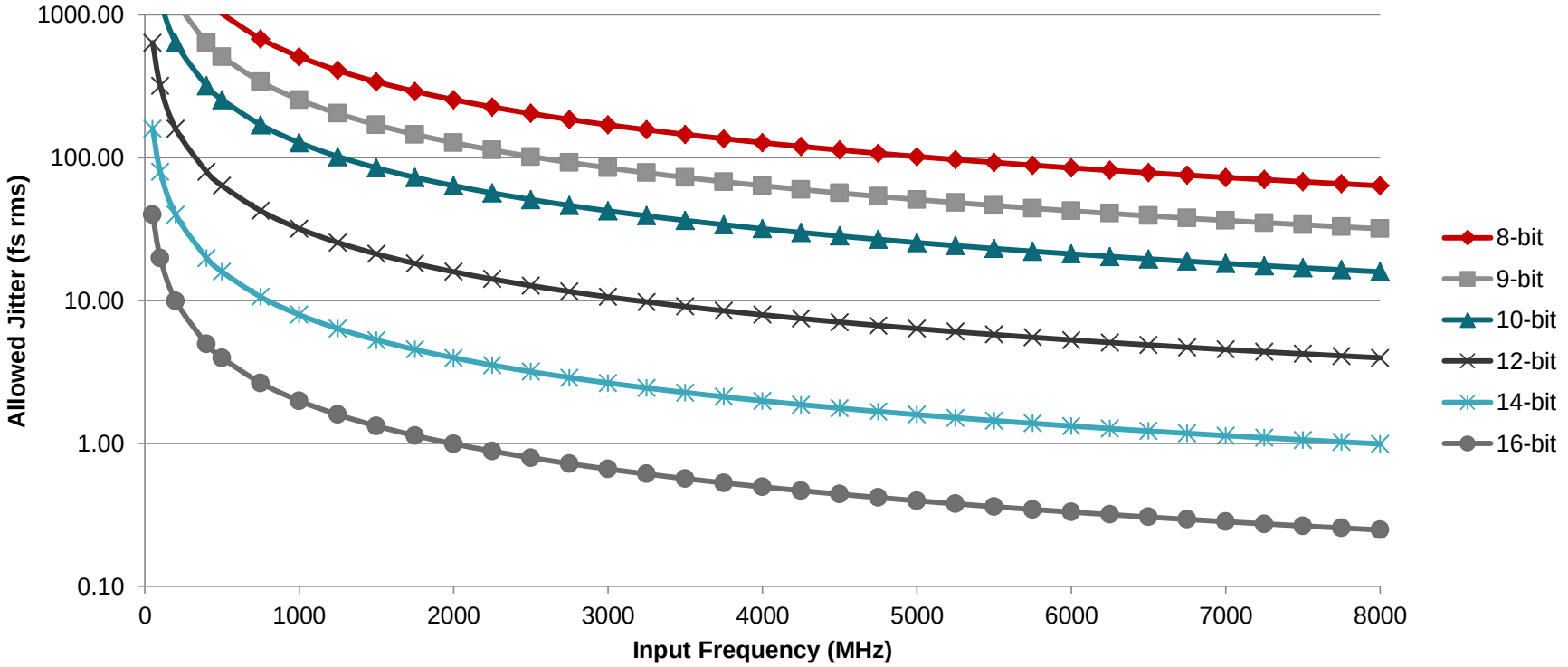
ADC general clocking requirements

- Amplitude Requirements for CLK+/-
  - 0.4 to 2.0 Vpeak-to-peak differential (equivalent to 0.2V to 1.0V V_{ID})
- Jitter Requirements
  - Jitter must be low enough to not limit SNR performance of ADC *at desired input frequency*
  - See standard relationship between jitter and ENOB in AN-1791

$$T_{j(rms)} = (V_{IN(p-p)} / V_{INFSR}) * (1/(2^{(N+1)} * \pi * f_{in}))$$

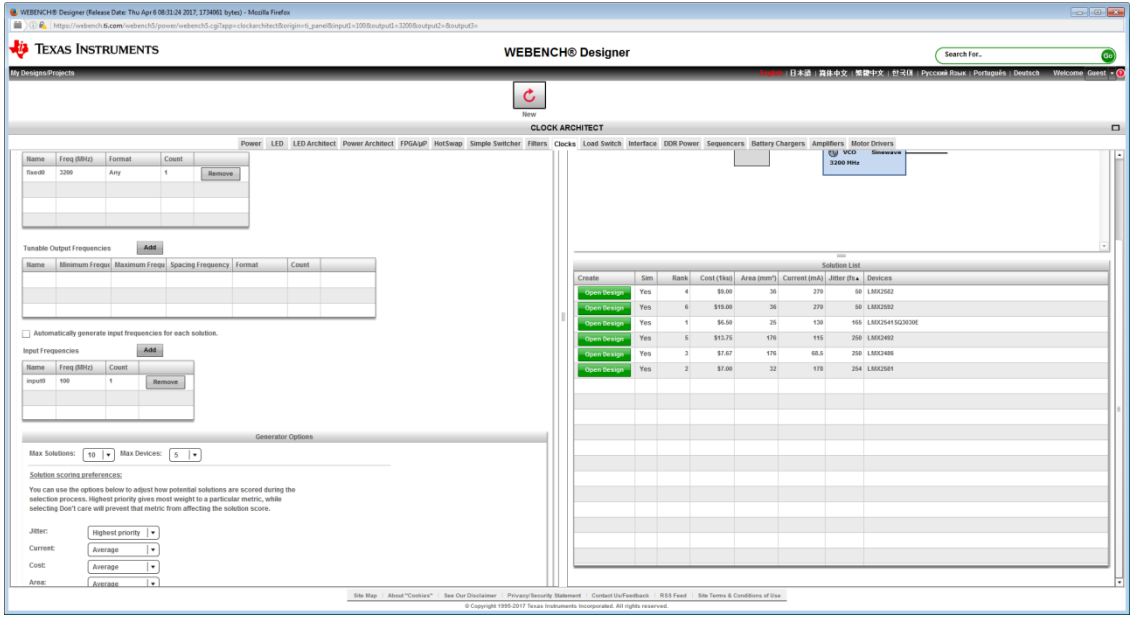
- Total jitter is RMS sum of ADC inherent aperture jitter and clock jitter
- Clean PLL/VCO based sources recommended
  - LMX2582, LMX2594, LMK048xx, etc.
- Lab sources, issues and mitigation
  - Good quality RF generators are low jitter but relatively high in harmonics
  - Harmonics should be attenuated with a bandpass or lowpass filter

Impacts of jitter on ADC performance



Clock source selection

- Minimize jitter (phase noise) at clock source
  - Choose appropriate clock source
  - Use https://webench.ti.com, optimize for best jitter



Methods to minimize jitter

- Ensure board routing does not add jitter to clock path
  - Keep clock signals away from other dynamic/noisy signals
  - Avoid parallel routing with digital, other clocks, signals, etc.
  - Use multi-layer board designs to maximize isolation
- Trace Routing
  - 50 single ended, 100 Ohm differential
- Minimize distortion on clock routing
  - Avoid impedance discontinuities
  - Avoid sharp angles, use 45 degree or smooth curves

Clock delivery

- Clock source output mode and termination
  - Need adequate signal amplitude and slew rate
  - Need to properly terminate to signal path
- ADC and DAC clock input termination
  - Many ADCs have 100 Ohm on-chip termination
- AC Coupling
  - ADC differential clock inputs must be AC coupled
- Single Ended to Differential Conversion
  - Some clock sources are SE and must be converted to differential
  - BALUN transformer is most common way to do this
  - Active clock distribution devices can also perform this function