High VOLT Interactive

Where power supply design meets collaboration

[High side bias challenges and solutions in half bridge gate drivers]

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What will I get out of this session?

- Purpose:

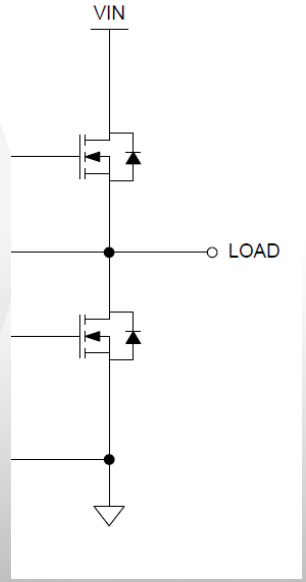
Understand various challenges associated with high side bias design in half bridge gate driver circuits. The presentation will also propose solutions to those challenges.

- Part numbers mentioned:
  - UCC27282, UCC27201/11/12
  - LM510x
- Reference designs mentioned:
  - TIDM-AUTO-DC-LED-LIGHTING
- Relevant End Equipment's:
  - Telecom power supplies
  - Automotive Headlights
  - Drones, Motor Drives, etc.…

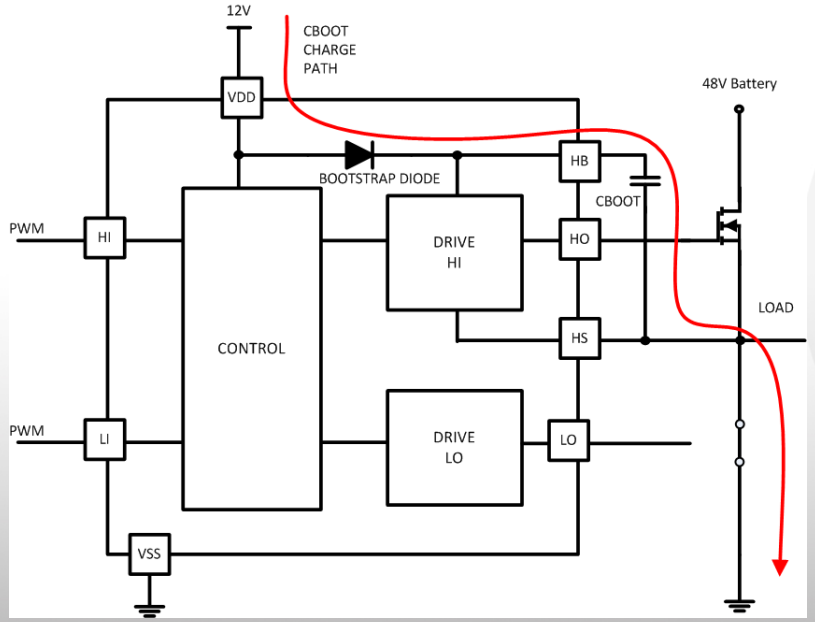
Ways to generate high side bias for half-bridge circuit?

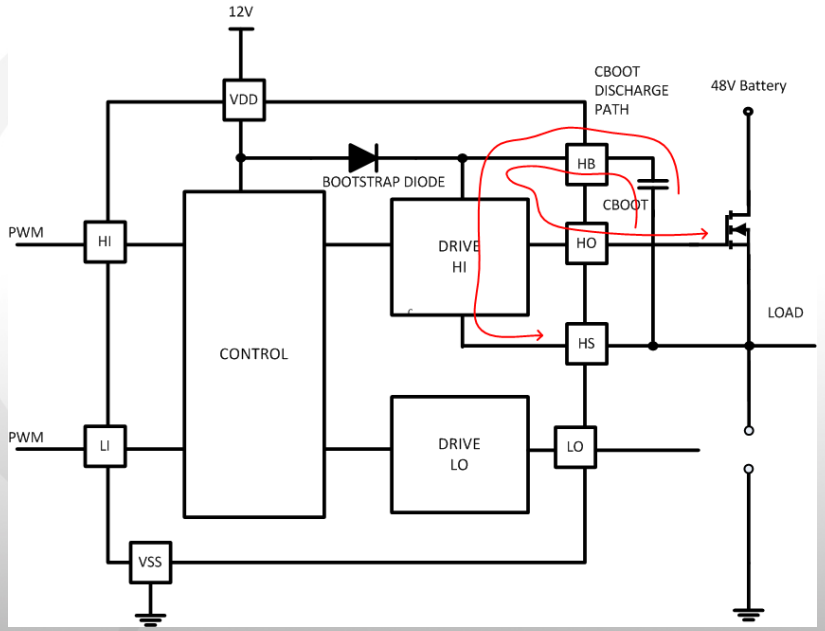
- **A) Bootstrap**
- B) Gate Driver Transformer
- C) Windings off of the flyback
- D) Buck conversion from the input/output

How to generate bias to drive this gate to source



Bootstrap supply charging/discharging operation





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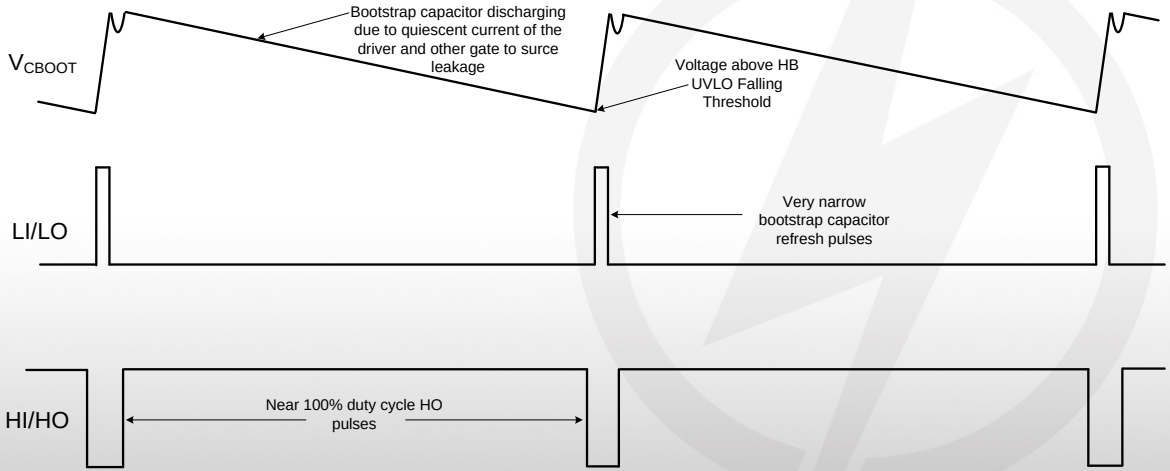


Key parts/components of bootstrap supply/bias?

- A) Bootstrap Diode
- B) Bootstrap Capacitor
- C) Charging/Discharging Element
- D) Supply Capacitor

Key influencers in bootstrap supply design

- Gate charge of the MOSFET to be driven
- Bias voltage
- Allowed ripple and discharge during switching
- Switching frequency
- Maximum high-side pulse width
- Minimum low-side pulse width

Basic bootstrap capacitor design equations

$$\Delta V_{HB} = V_{DD} - V_{DH} - V_{HBL}$$

where

- V_{DD} = Supply voltage of the gate drive IC
- V_{DH} = Bootstrap diode forward voltage drop
- $V_{HBL} = V_{HBRmax} - V_{HBH}$, HB falling threshold

$$Q_{Total} = Q_G + I_{HBS} \times \frac{D_{Max}}{f_{SW}} + \frac{I_{HB}}{f_{SW}}$$

where

- Q_G = Total MOSFET gate charge
- I_{HBS} = HB to VSS Leakage current
- D_{Max} = Converter maximum duty cycle
- I_{HB} = HB Quiescent current

Absolute Minimum Value of Bootstrap Capacitor

$$C_{Boot} = \frac{Q_{Total}}{\Delta V_{HB}}$$

Effect of value of bootstrap capacitor

- Ripple voltage
- Diode peak current
- Operating voltage range
- Value of gate to source resistance
- Operating range of duty cycle
- Switching frequency
- Low side minimum pulse width

No high frequency filter capacitor on HB

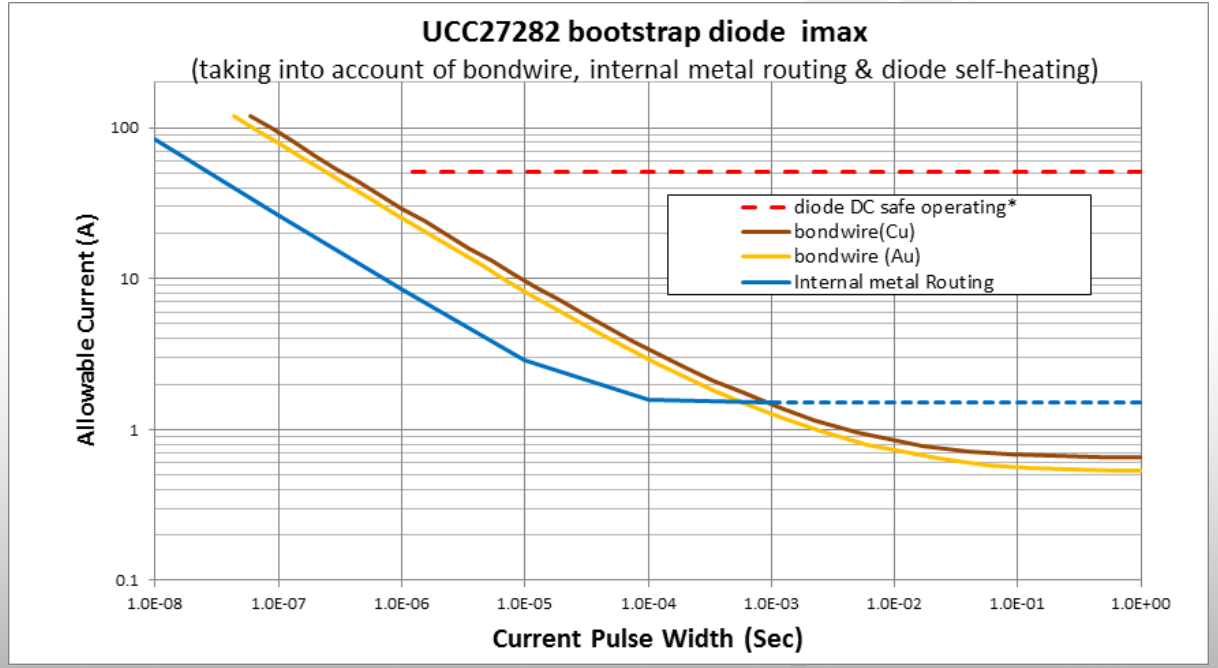
Factors affecting boot diode peak forward current capability

- Diode dynamic impedance
- Value of bootstrap capacitor
- Voltage needed to be charged
- Charging pulse width
- Rds(on) of the charging MOSFET
- Any other series impedance
- Not a datasheet parameter
- Can be modeled and simulated

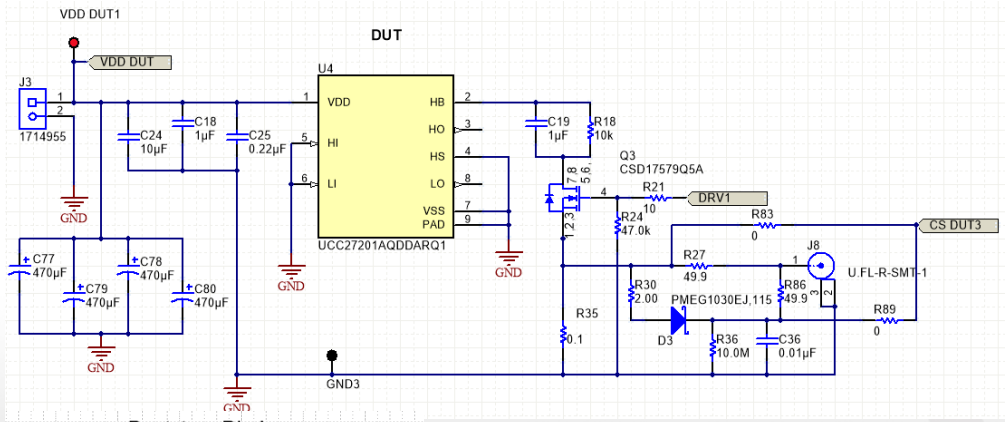
$$Ipk = C\frac{dV}{dt}$$

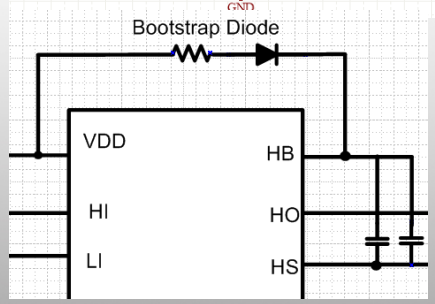
$$Ipk = \frac{dV}{Rdynamic}$$

Simulation of Boot diode peak forward current capability

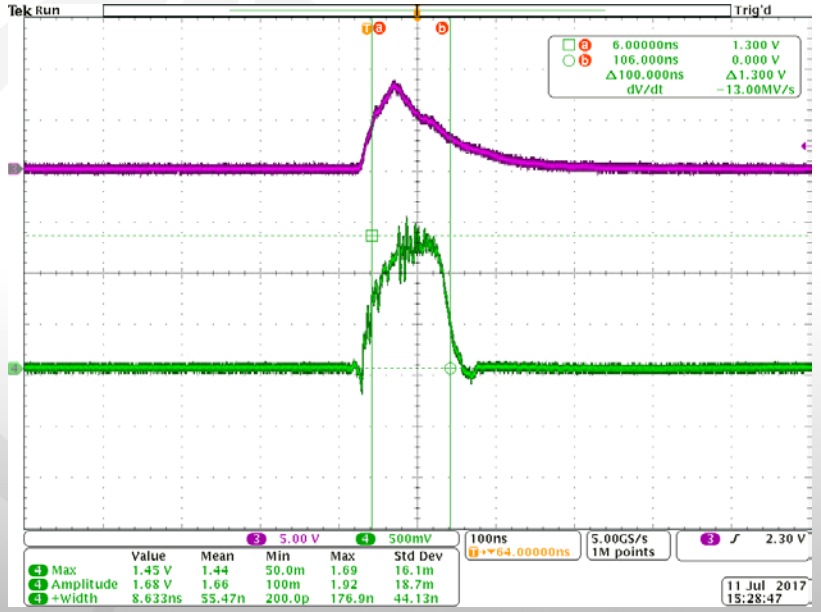


Bench testing of boot diode peak forward current capability





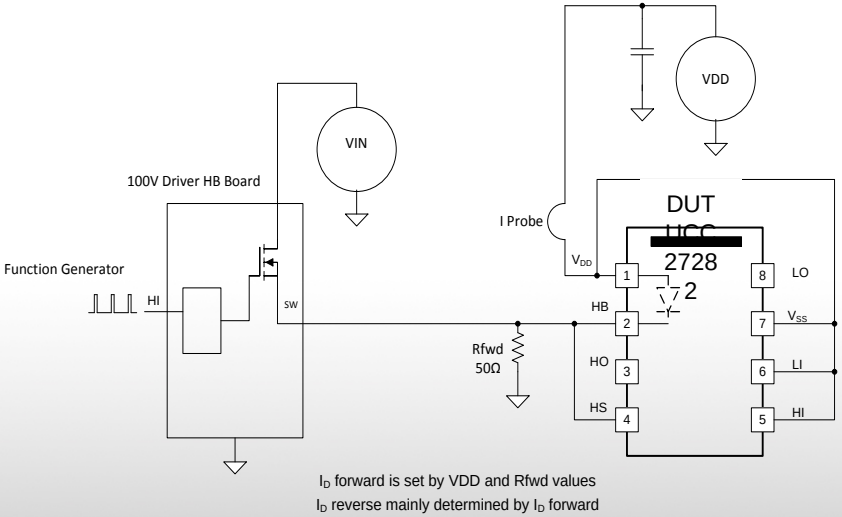
Driver IC without built-in bootstrap diode

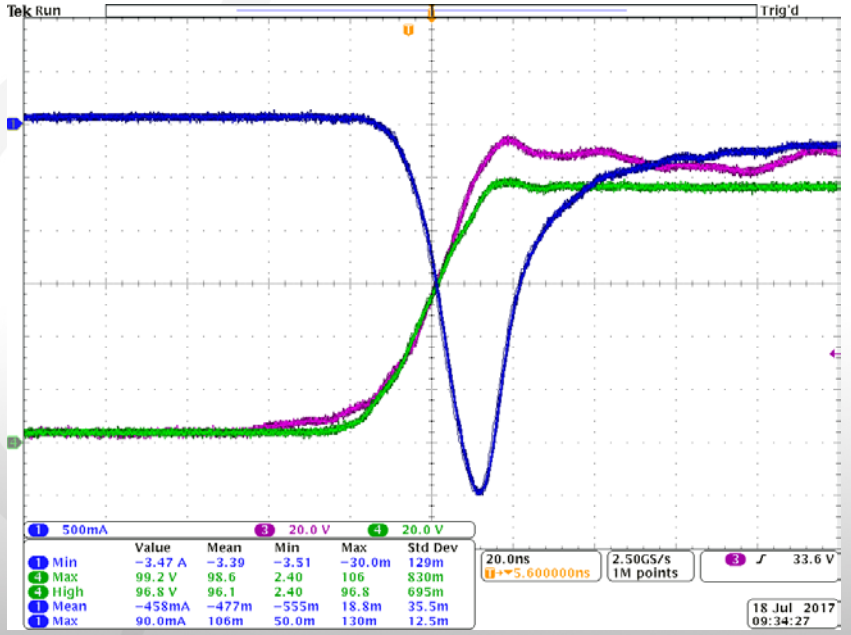


Factors affecting boot diode peak reverse current capability

- Diode forward current
- Diode reverse bias voltage
- Bootstrap capacitor value
- Not a datasheet parameter
- Not easy to simulate at IC level

Bench testing of Boot diode peak reverse current capability



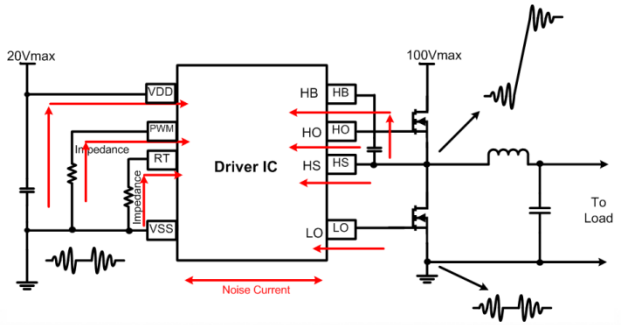


Solution: Clamp LO minimum pulse width or place external Schottkey diode

Effect of frequency, pulse width, UVLO delay, & temperature

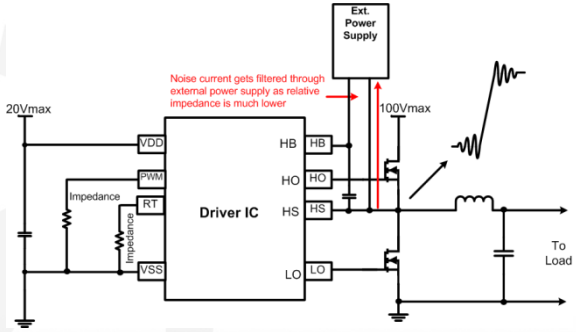
- High switching frequency -> Low value bootstrap capacitor
- Low switching frequency -> High value bootstrap capacitor
- Very High switching frequency -> External Schottkey bootstrap diode option
- High switching frequency -> Additional low profile, low value, high frequency bypass bootstrap capacitor
- Temperature
- UVLO Delay
- Gate to source resistor and other external leakage path from HS to VSS

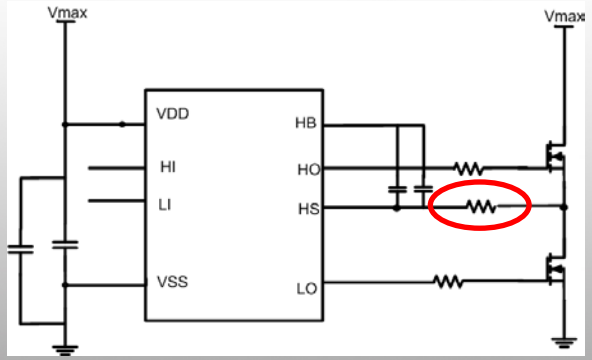
Effect of switch Node slew rate and noise



How noise affects driver IC

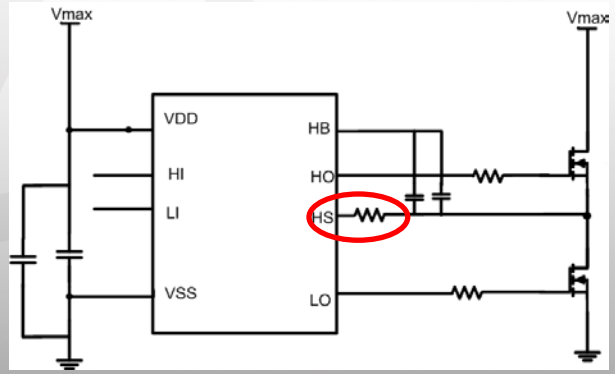
How to diagnose if boot supply is causing issues



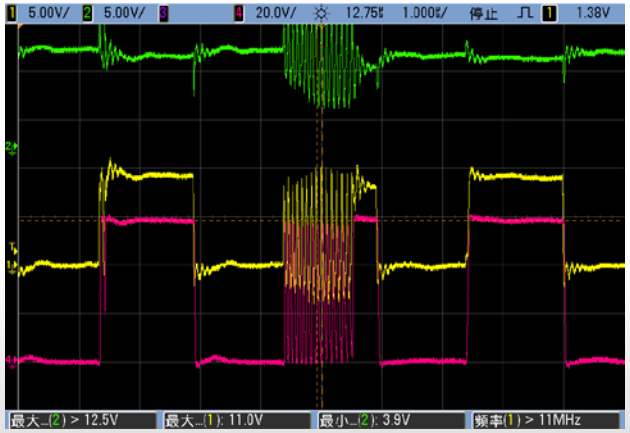


Resistor in both charging and discharging path

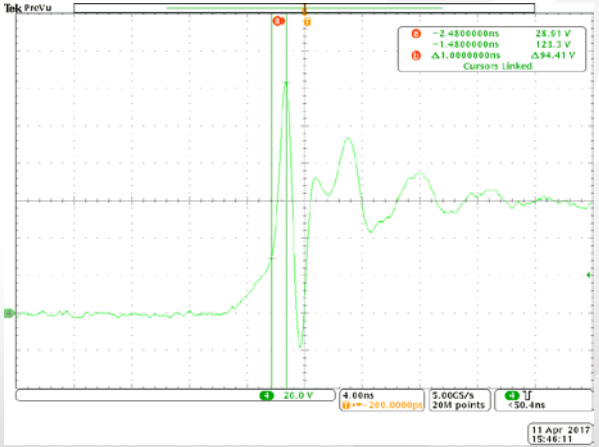
Resistor in discharging path affecting fall time



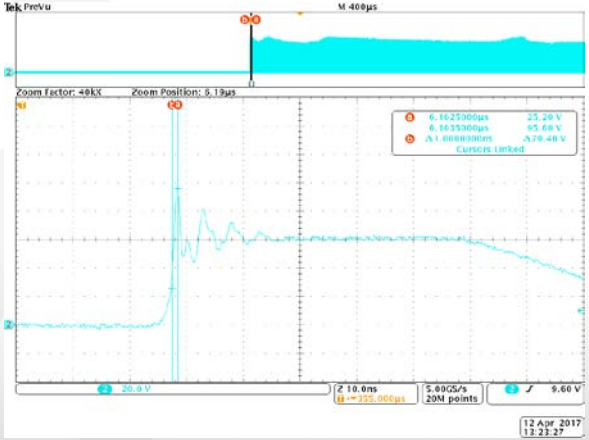
Effect of switch node slew rate and solution



CH1=HO-HS, CH2=HB-HS, CH4=HS



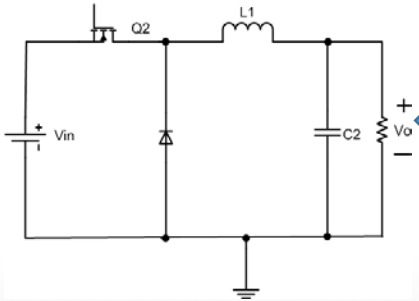
High dV/dt on HS pin, 90V/ns, Cb=0.1uF



High dV/dt on HS pin, 90V/ns, Cb=22nF

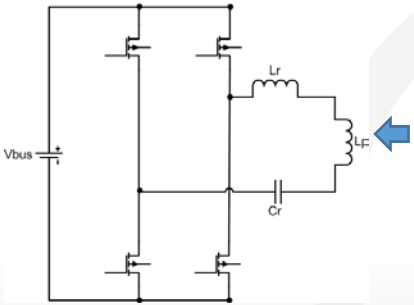
Bridge driver and boot supply challenges with topologies

Diode Rectified Buck



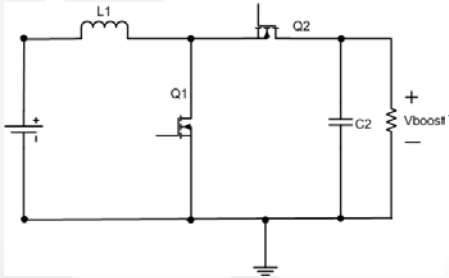
Charging of Bootstrap capacitor?

Full Bridge LLC

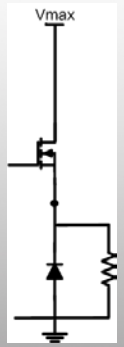


Oscillations on one of the HS node based on switching sequencing

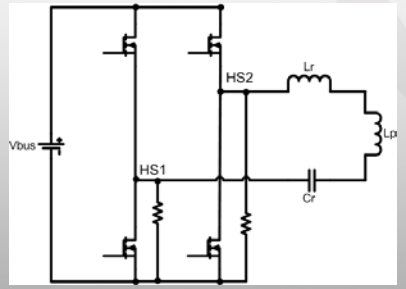
Synchronous Boost



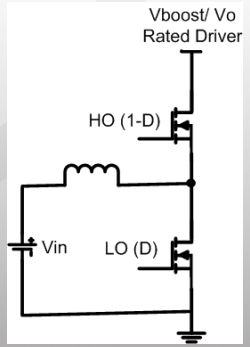
What is driver bus voltage and which FET is high side/low-side



High impedance resistor for Charging of Bootstrap capacitor?



Turn-on both low side FETs at the same time or place resistor from HS to ground

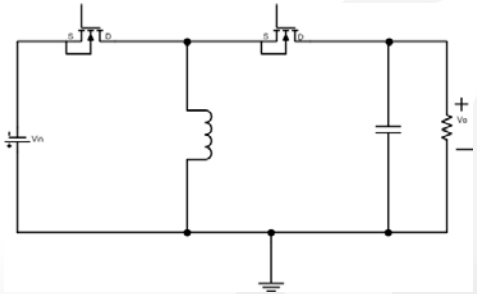


Low side FET determines duty cycle

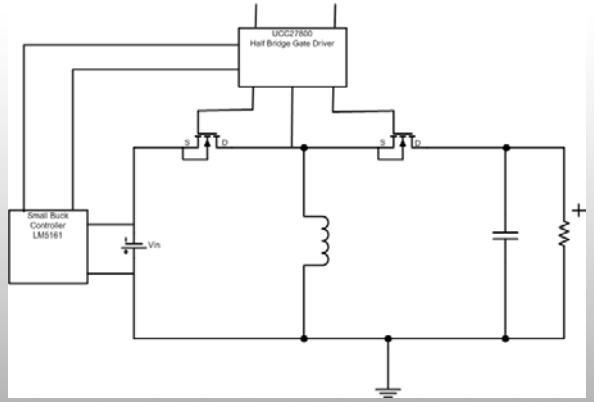
Vo=Vbus

Bridge driver and boot supply challenges with topologies

Synchronous Buck-Boost

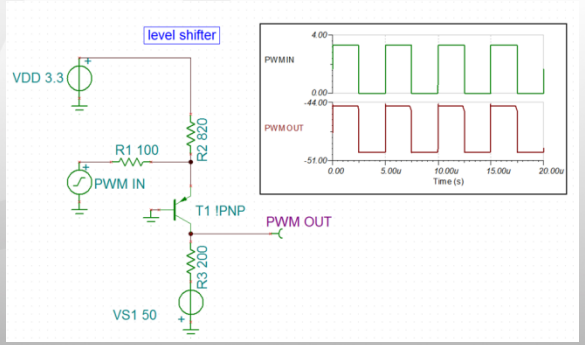


Can half-bridge driver be used?
How it is biased?
How about input signals?



Half-bridge driver biased from Vin

Inputs are level shifted up to negative rail



Summary

- There are multiple variables as well as multiple operating conditions that need to be considered while designing a bootstrap supply around half-bridge gate driver.
- Bootstrap diode characteristics such as peak forward and reverse current, play an important role in reliable operation of the bootstrap diode and also HB driver.
- Optimum bootstrap capacitor need to be selected based on overall system operation.
- Switching frequency and pulse width has impact on bootstrap bias design
- Topology and switching pattern also need to be considered while selecting half bridge driver as well as designing bootstrap bias supply

Thank you

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