FPD-LINK Product Overview

Nov 2017

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Texas Instruments

Agenda

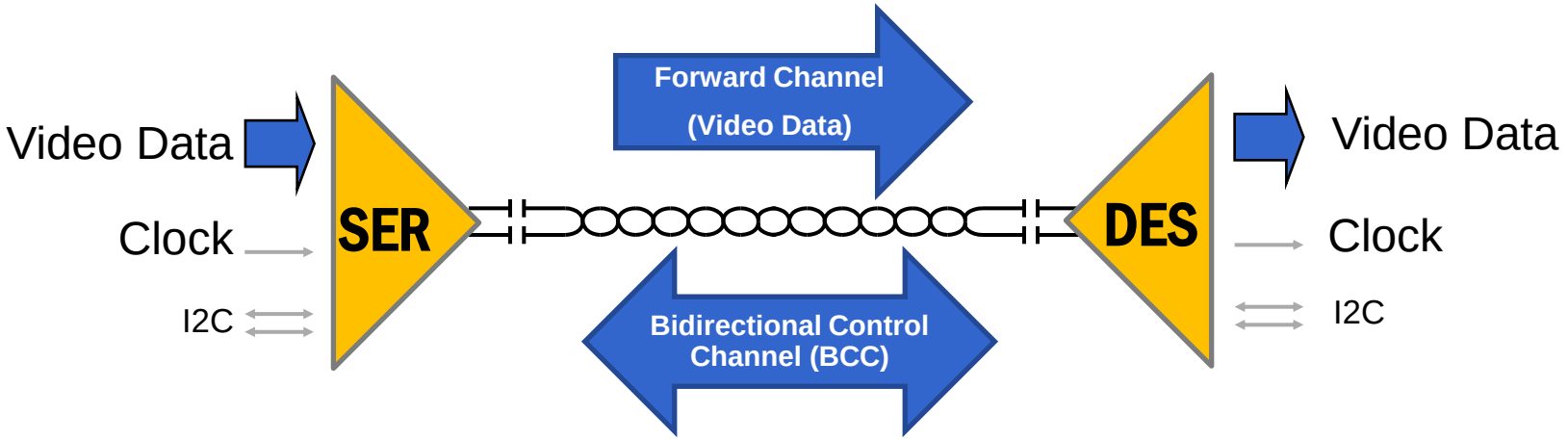
- FPD-Link Overview
  - General Features
  - In-vehicle Infotainment(IVI)
  - Advanced Driver Assistance Systems (ADAS)
- FPD-Link Features
  - Payload, Line Rate, Unit Interval explanation
  - Adaptive EQ
  - I2C Communication and Alias
  - Link Diagnostic
  - Power-over-coax (PoC)
  - Cable Requirement
  - CMLOUT Monitoring
  - Built-in-self Test (BIST) Mode
- Resources and Collateral
- Fault Analysis

FPD-Link III

Serializer / Deserializer

- **Benefits:**
  - **Reduce cable harness cost and weight**
  - **Low EMI with differential LVDS**
  - **Diagnostics features**

Replaces multiple interfaces (wires) with one pair

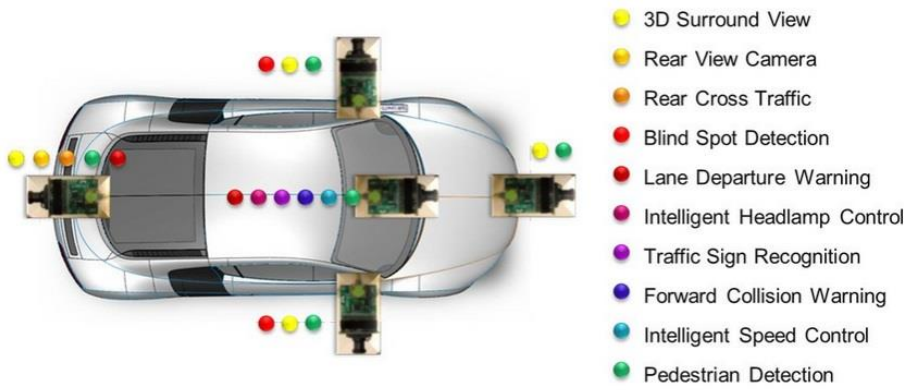


FPD-Link Application

IVI: In-Vehicle Infotainment

Infotainment Displays

ADAS: Advanced Driver Assistance Systems



ADAS Surround View Cameras

FPD-Link

Automotive Cable

Point-to-Point

FPD-Link

FPD-Link

Automotive Cable

Point-to-Point

FPD-Link

Head-Unit

High-Speed - 6Gbps+

High-Resolution – 2K

Low-Latency - nano sec

Connections

FPD-Link Highlights

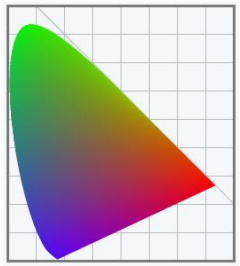
General

- Video, Bidirectional Control (I^2C), GPIO and Power
  - Over single twisted pair or coaxial cable assemblies
- Adaptive equalization compensates for cable type, length, age and condition
- Multiple interface options: RGB, YUV, OpenLDI (LVDS), MIPI CSI-2, HDMI

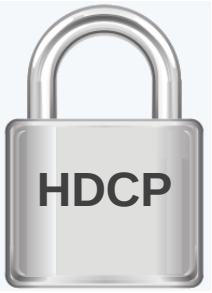
Infotainment

1080p Full HD

- Support for 720p and 1080p
- Easy-to-use HDCP content protection
- Dithering, White Balance, and Test Patterns



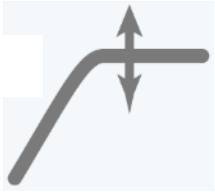
White balance
FRC Dithering



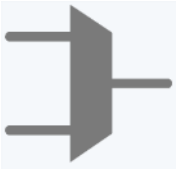
High-bandwidth
Digital Content Protection

Driver assist

- Support for 1 and 2 Megapixel image sensors
- Very low latency
- Internal Pattern Generator
- Temperature, PoC voltage Diagnostics

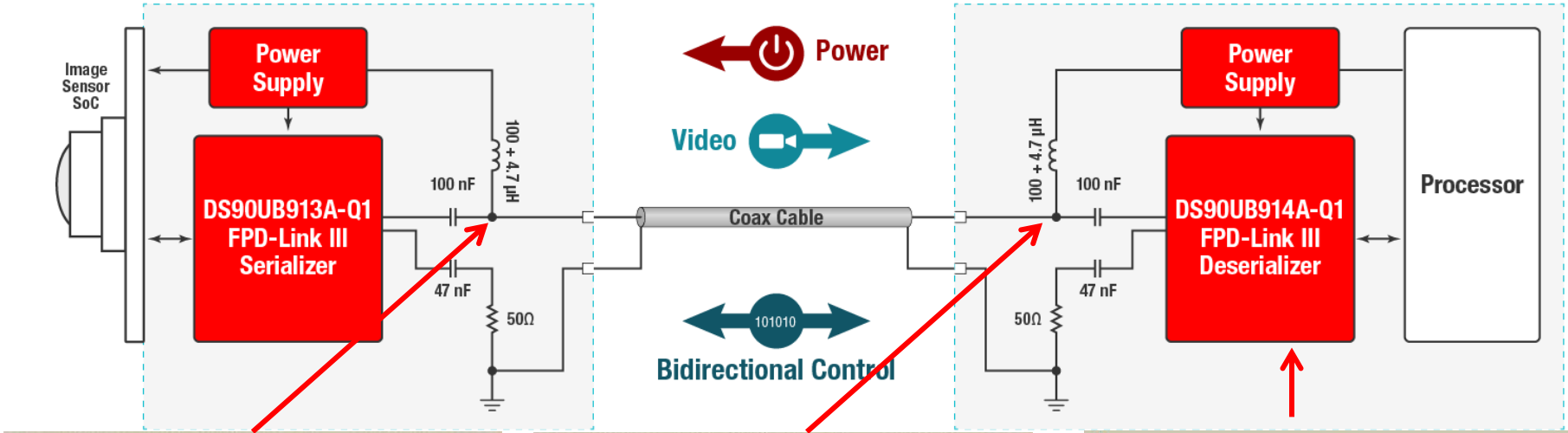


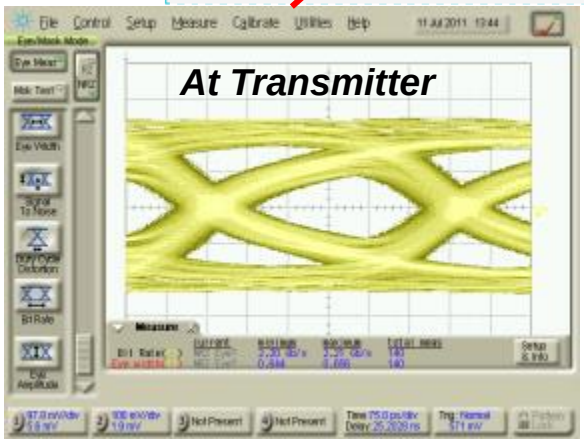
Adaptive Equalization

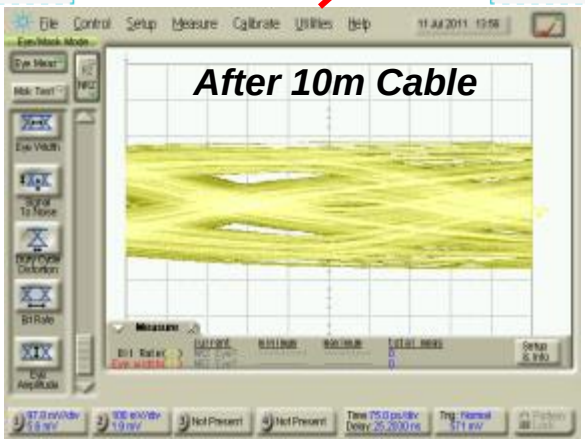


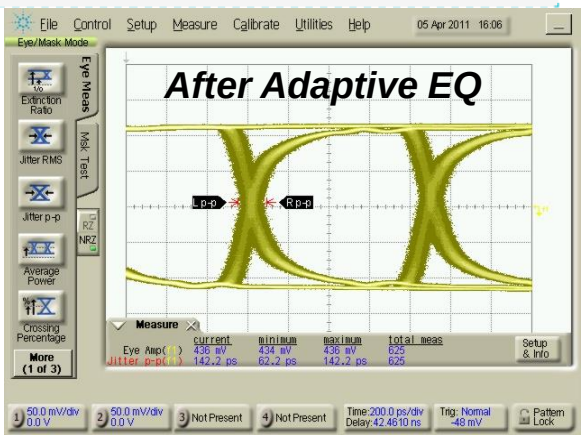
2:1 camera mux

Adaptive Equalization







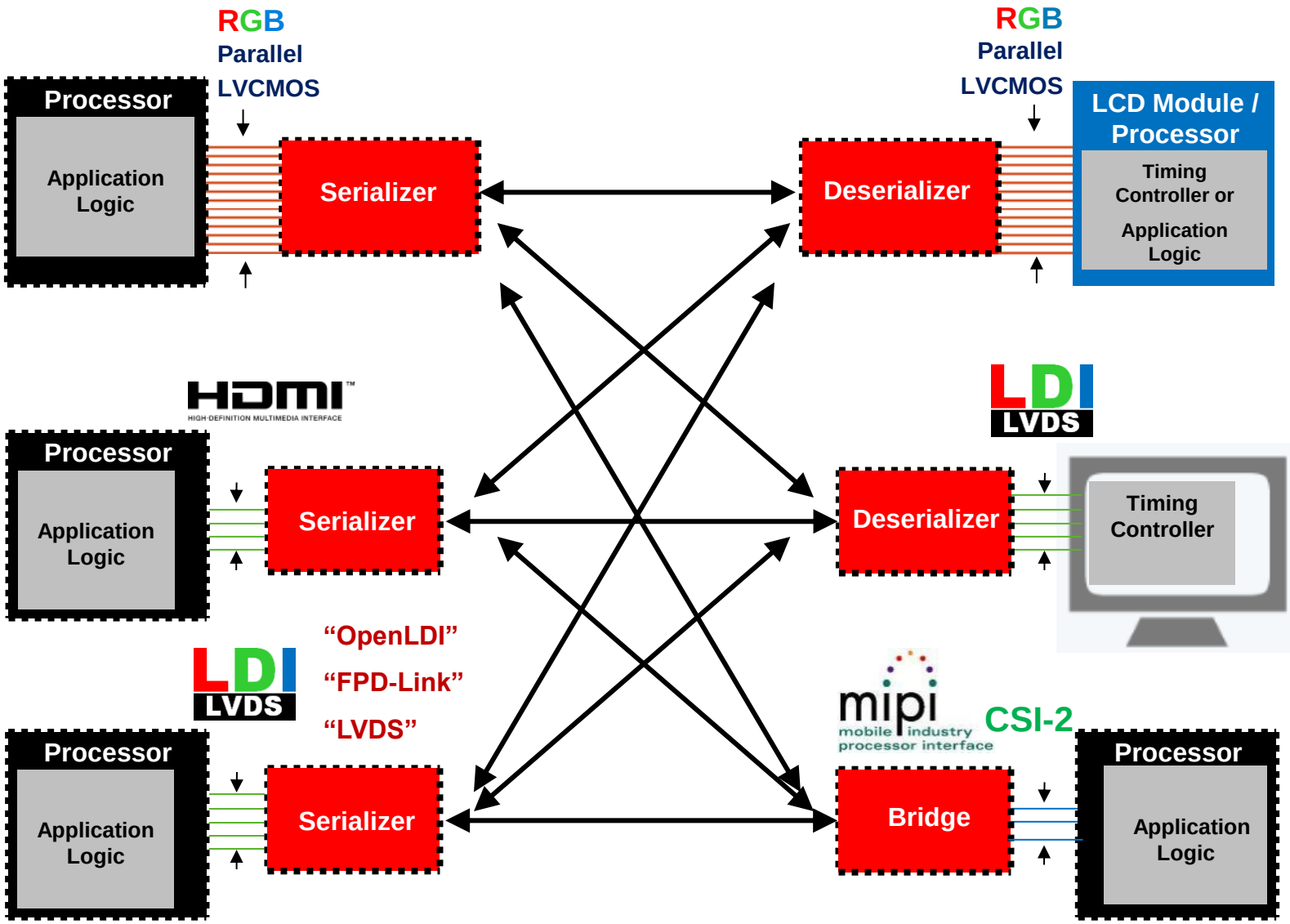


Automatic adaptation (no need to program EQ)

No EMI impact (because it is at the receiver

Diagnostic function (can read EQ registers)

Multiple System Interface Options

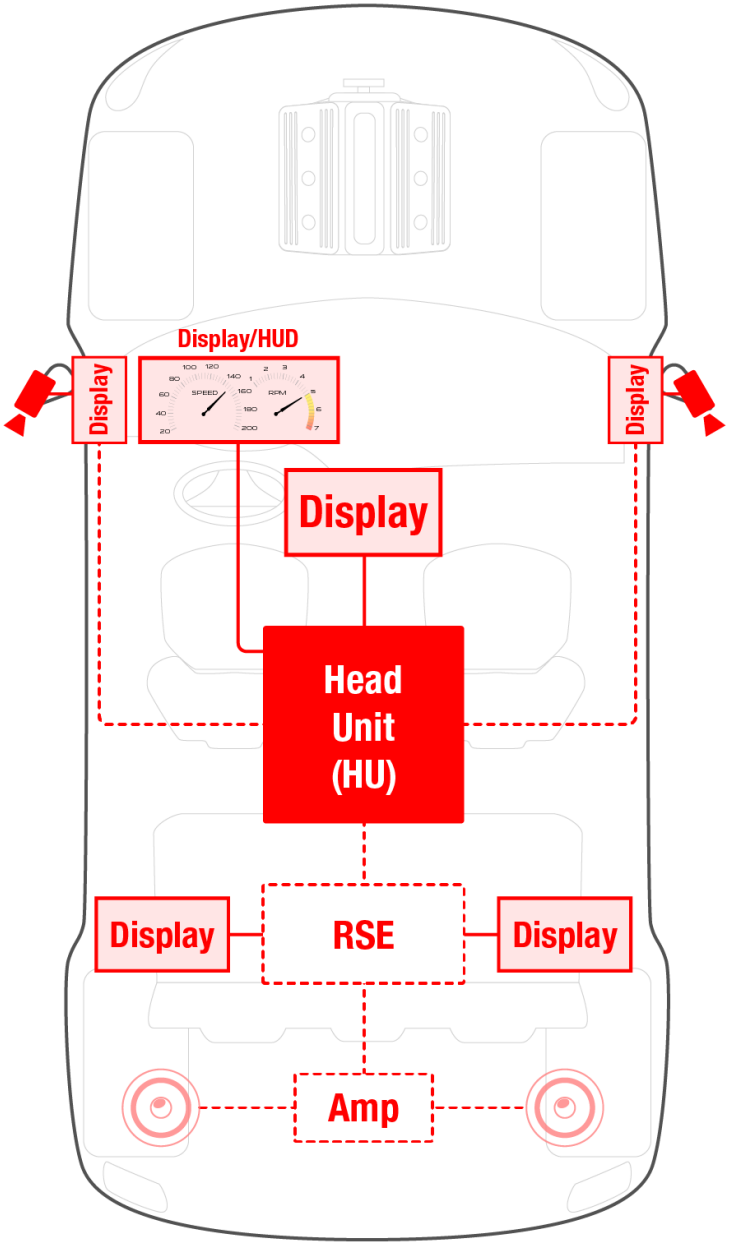


Industry Standard I/Os

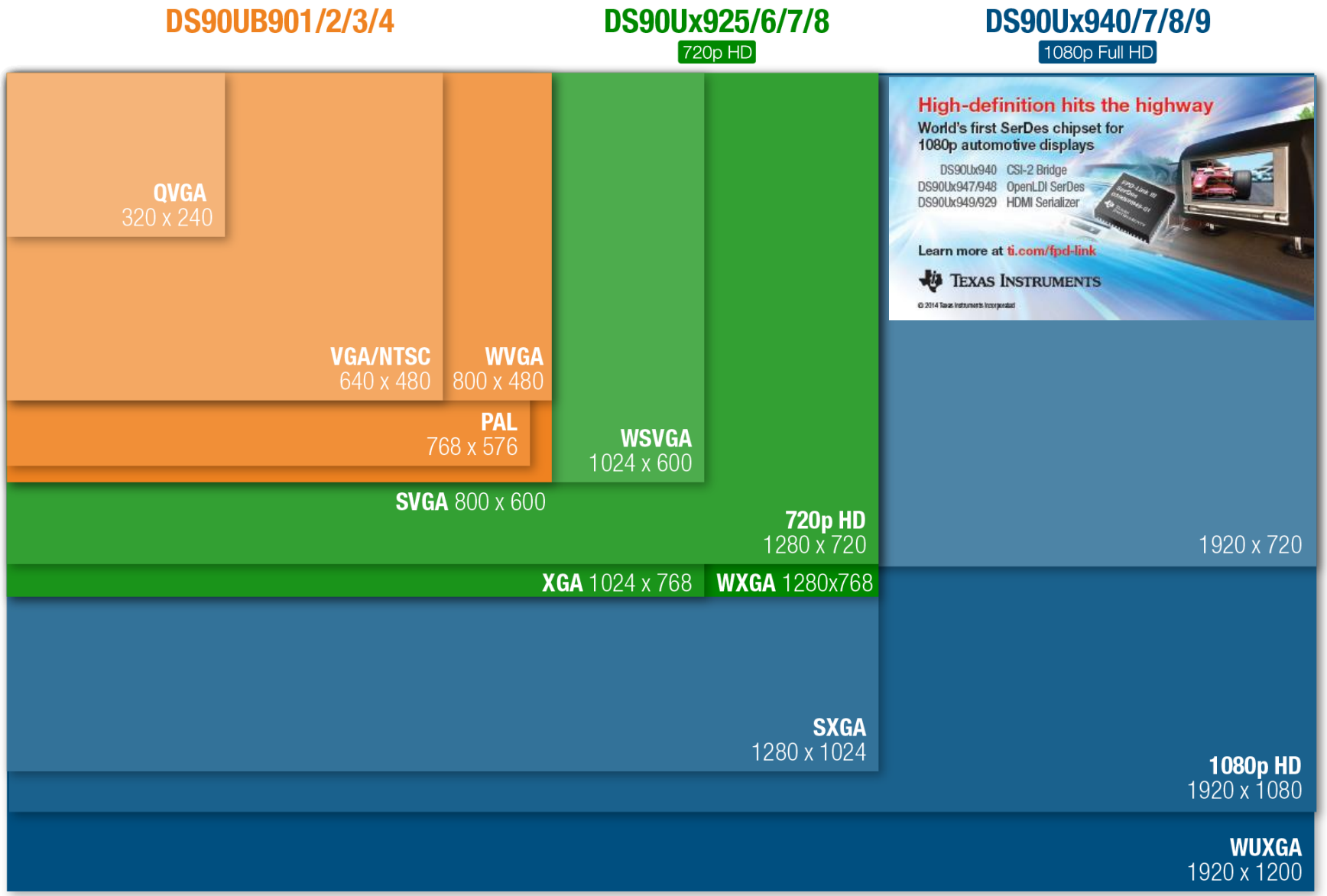
FPD-Link Infotainment Applications

Connecting Head Units to Displays

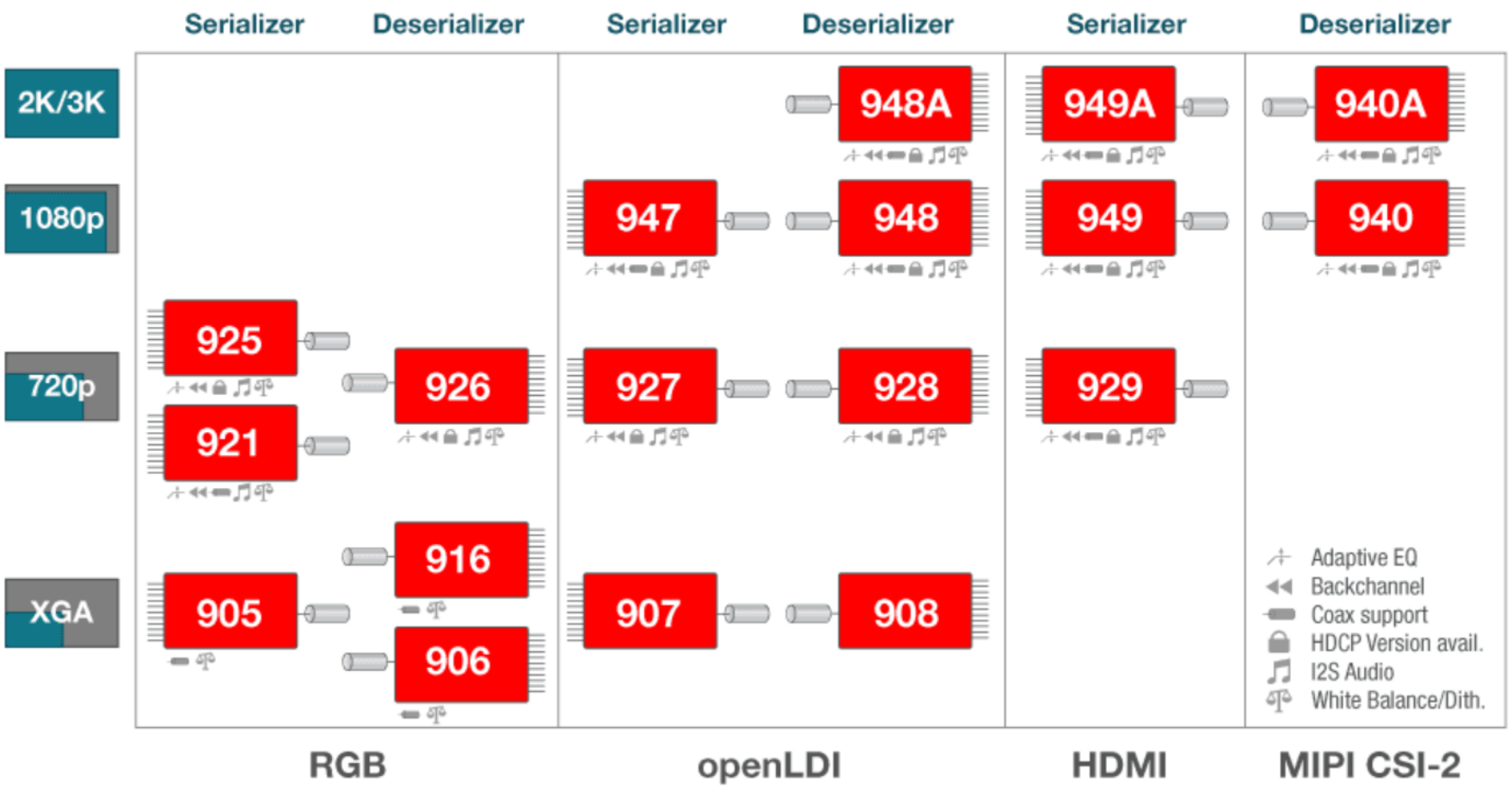
IVI: In-Vehicle Infotainment



FPD-Link Portfolio by Display Resolution



FPD-Link products for infotainment displays



FPD-Link IVI Features

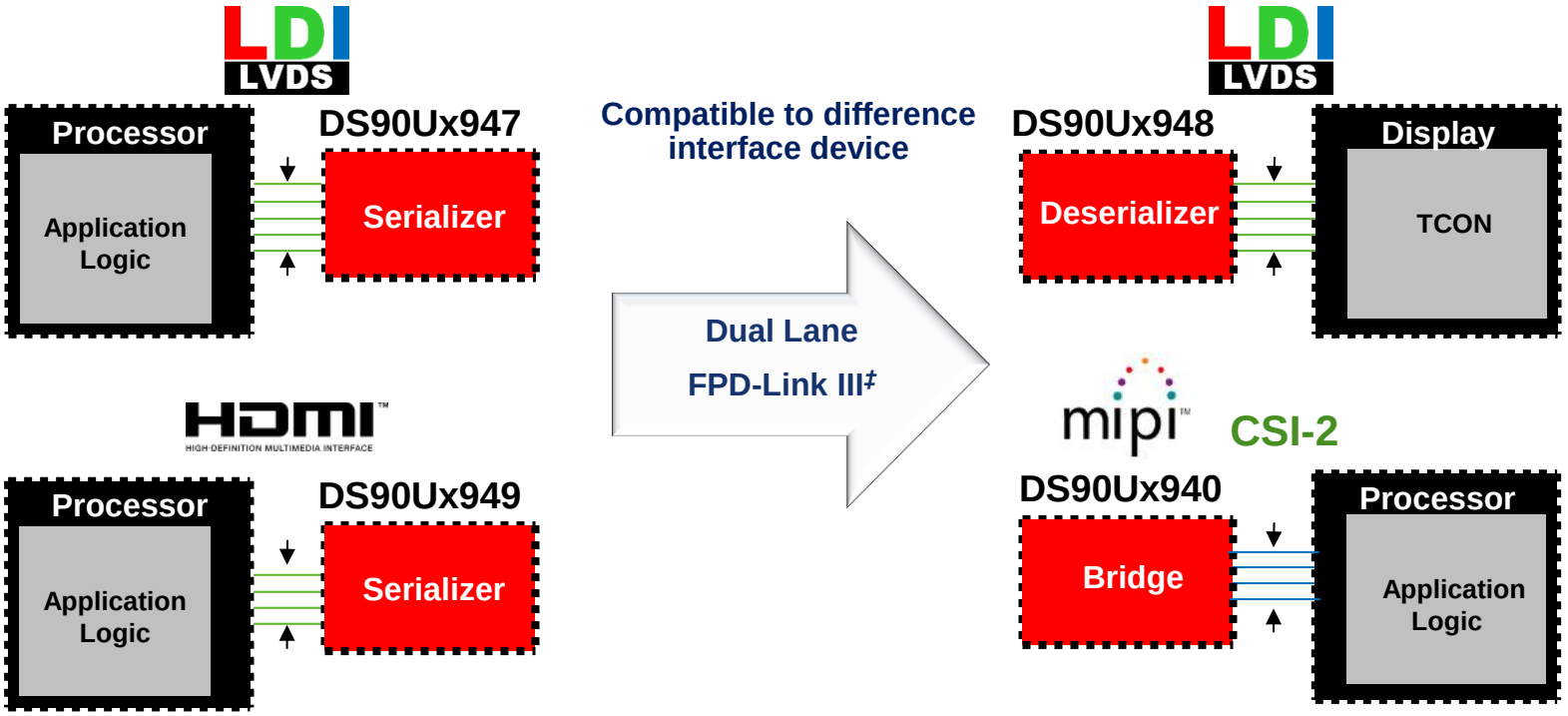
System Interface	PCLK (MHz)	Display Resolution	Adaptive EQ	Back-channel	Spread Spectrum	White Balance/Dithering	I2S Audio	HDCP Version	Coax	Serializer	Deserializer
Open LDI	25-170	1920 x 1080	✓	✓	✓	✓	✓	✓	✓	DS90UB947 DS90UH947	DS90UB948 DS90UH948
	25-210	2880 x 1080	✓	✓	✓	✓	✓	✓	✓		DS90UH948A
	5 - 85	1280 x 720	✓	✓	✓	✓	✓	✓		DS90UB927 DS90UH927	DS90UB928 DS90UH928
	5 - 65	1024 x 768			✓					DS90UR907	DS90UR908
Parallel RGB	5 - 96	1920 x 1080	✓	✓	✓	✓	✓		✓	DS90UB921	DS90UB922
	5 - 85	1280 x 720	✓	✓	✓	✓	✓	✓		DS90UB925 DS90UH925	DS90UB926 DS90UH926
	5 - 65	1024 x 768			✓	✓			✓	DS90UR905	DS90UR906 DS90UR916
HDMI™	25-170	1920 x 1080	✓	✓	✓	✓	✓	✓	✓	DS90UB949 DS90UH949 DS90UB929	
	25-210	2880 x 1080	✓	✓	✓	✓	✓	✓	✓	DS90UH949A	
MIPI® CSI-2	25-170	1920 x 1080	✓	✓	✓	✓	✓	✓	✓		DS90UB940 DS90UH940
	25-210	2880 x 1080	✓	✓	✓	✓	✓	✓	✓		DS90UH940A

UB, support back channel, FPDLINK3

UH, HDCP, FPDLINK3
UR, FPDLINK2

FPD-Link III 1080p60 Infotainment Family

System Interfaces

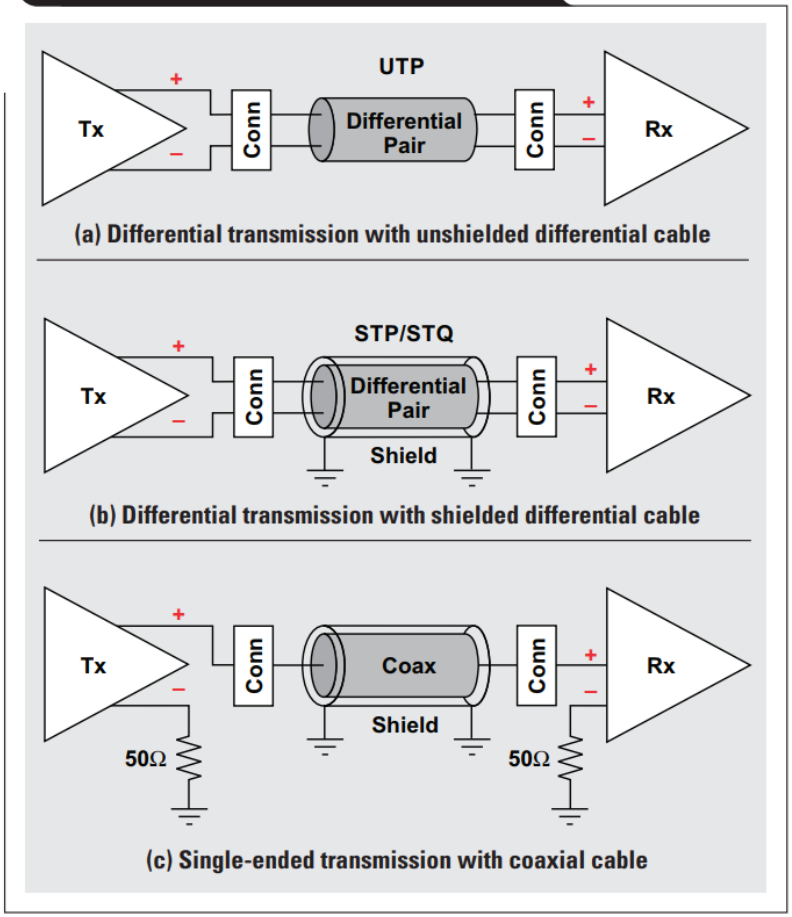


‡ : Conventional Single Lane FPD-Link III in backward compatible mode (to and from DS90Ux92x devices)

What you need to know about high-speed cables for FPD-Link III SerDes

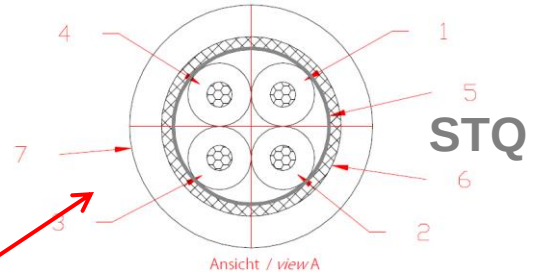
By T. K. Chin
Systems Manager, Ethernet and FPD-Link Product Line

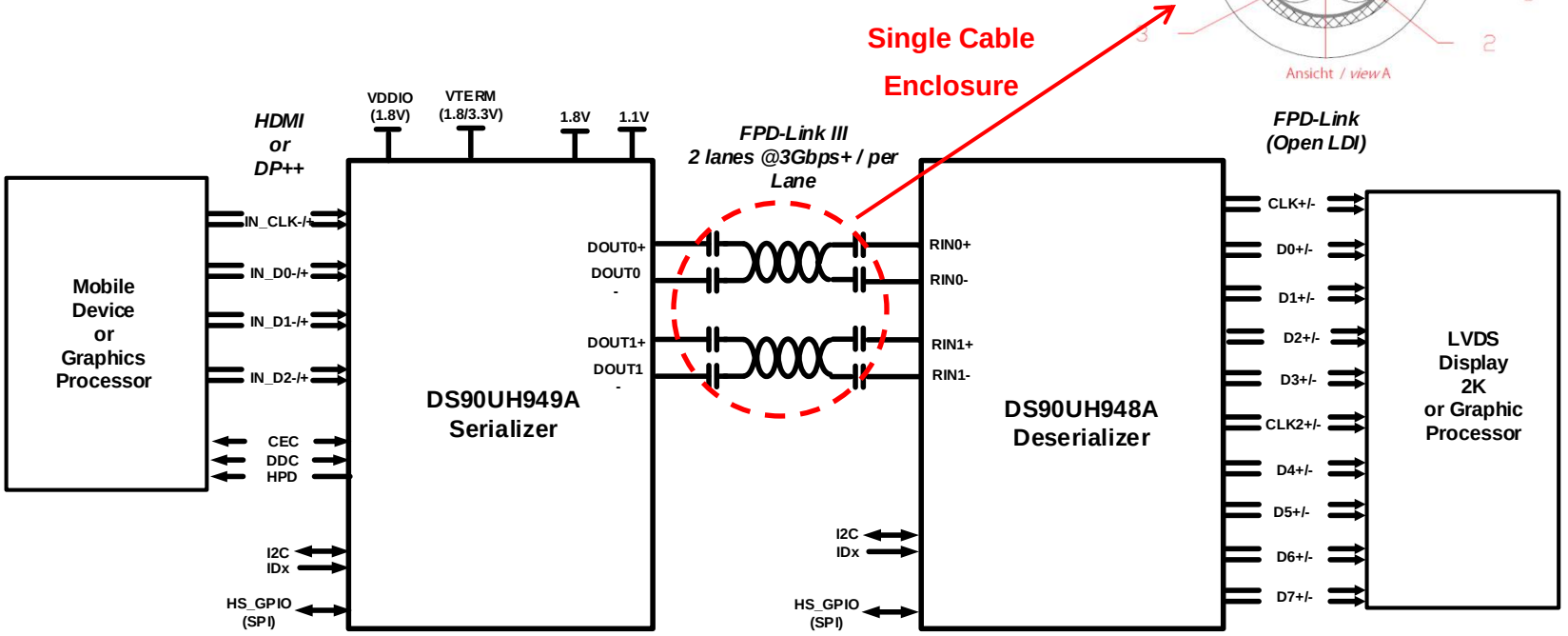
Figure 1. Single-end and differential signaling topologies



http://www.ti.com/lit/an/slyt726/slyt726.pdf

DS90UB947/8A 2K Application

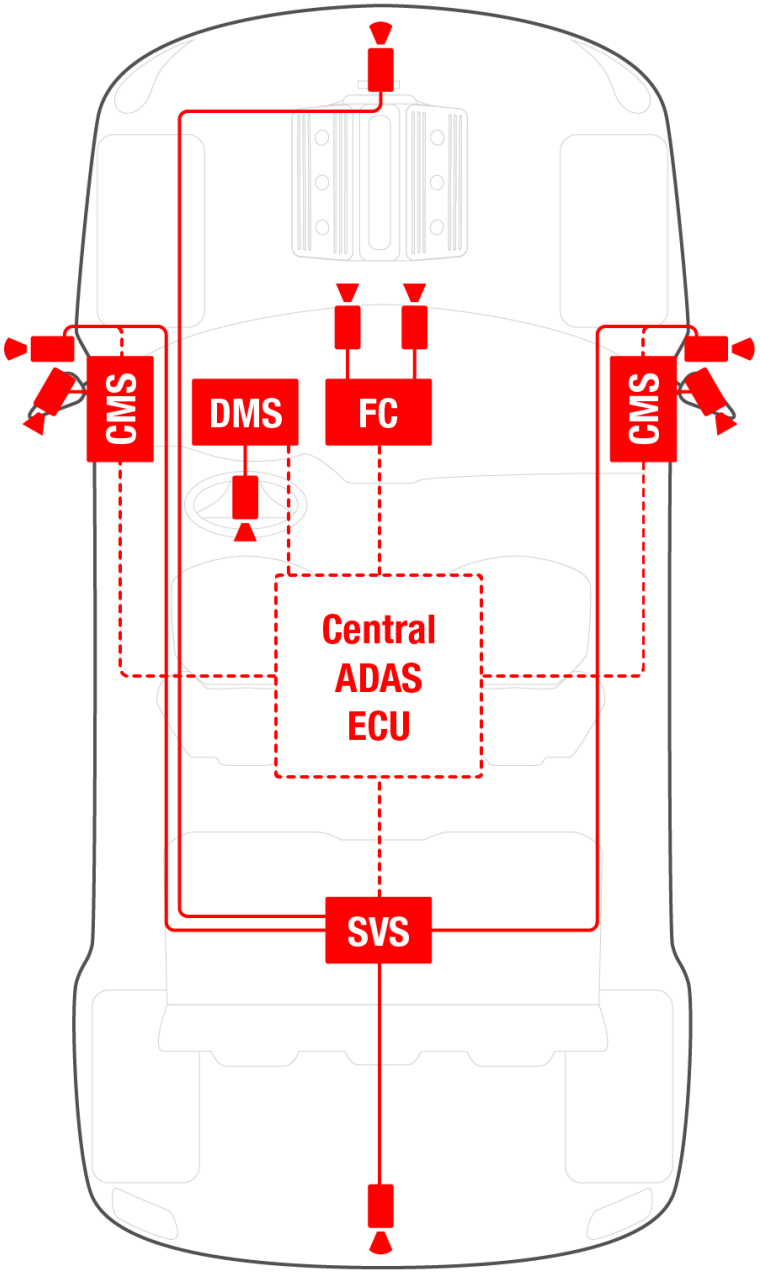




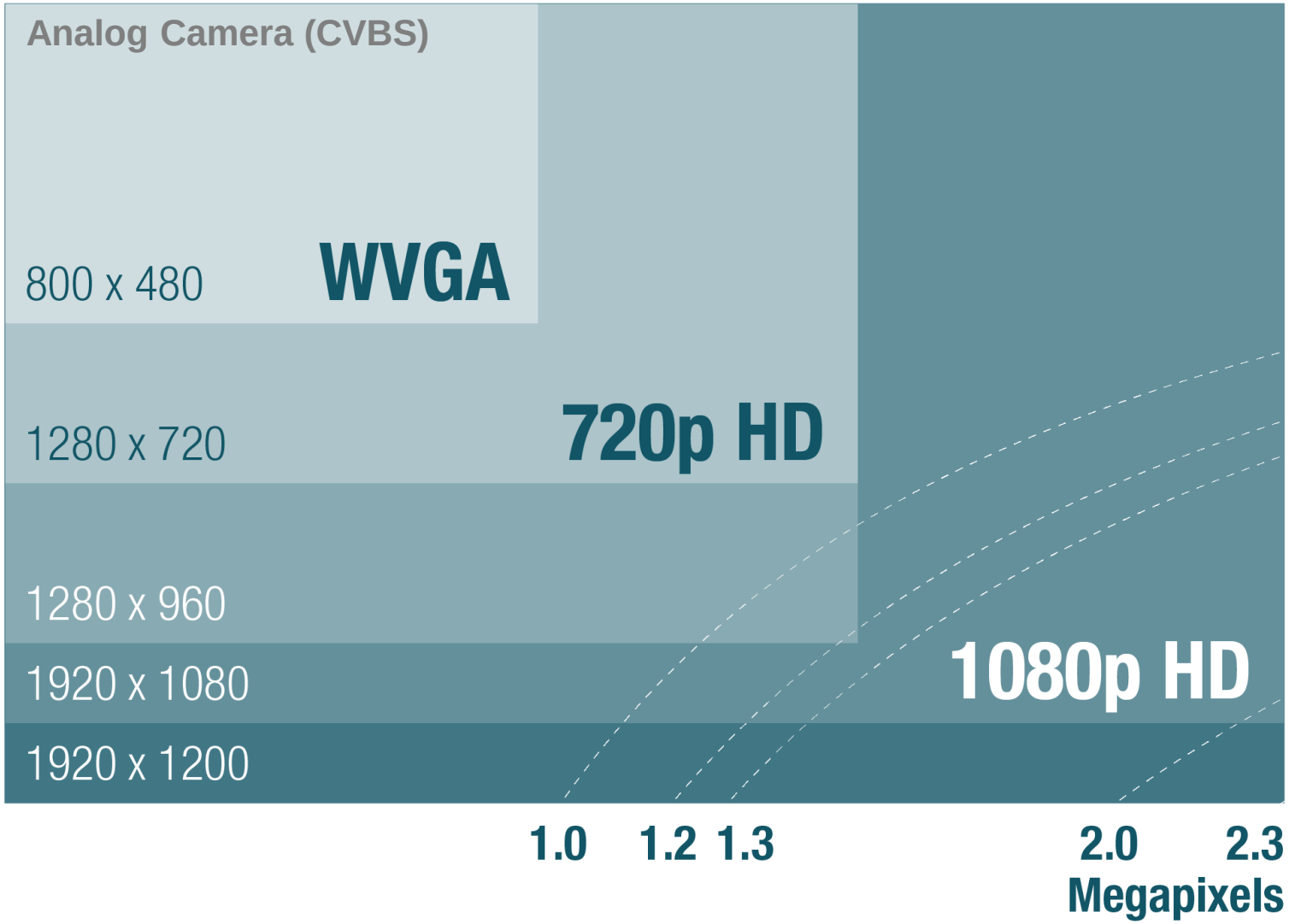
- ❑ Supports Pixel Clock up to 200 MHz for 2K
- ❑ 2880 x 1080p60
- ❑ Dual lane FPD-Link III
- ❑ Backward compatible to 720p generation (DS90Ux92x)
- ❑ High Speed Bidirectional GPIOs up to 2.5MHz in the back channel, OR
- ❑ SPI control interface up to 3.3Mbps in the backchannel
- ❑ I²C Control Interface up to 1MHz

FPD-Link ADAS Applications

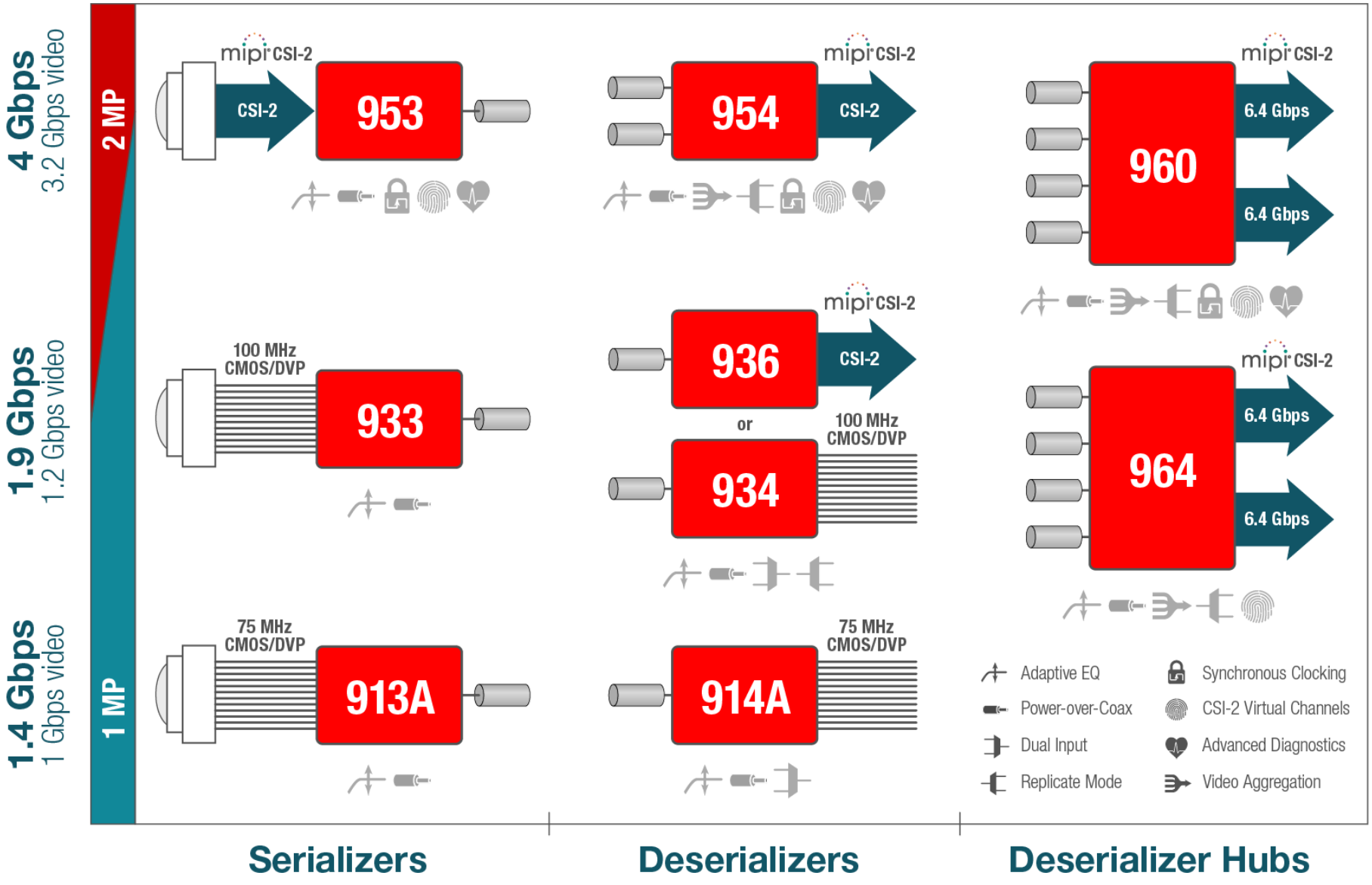
Connecting High Resolution Cameras



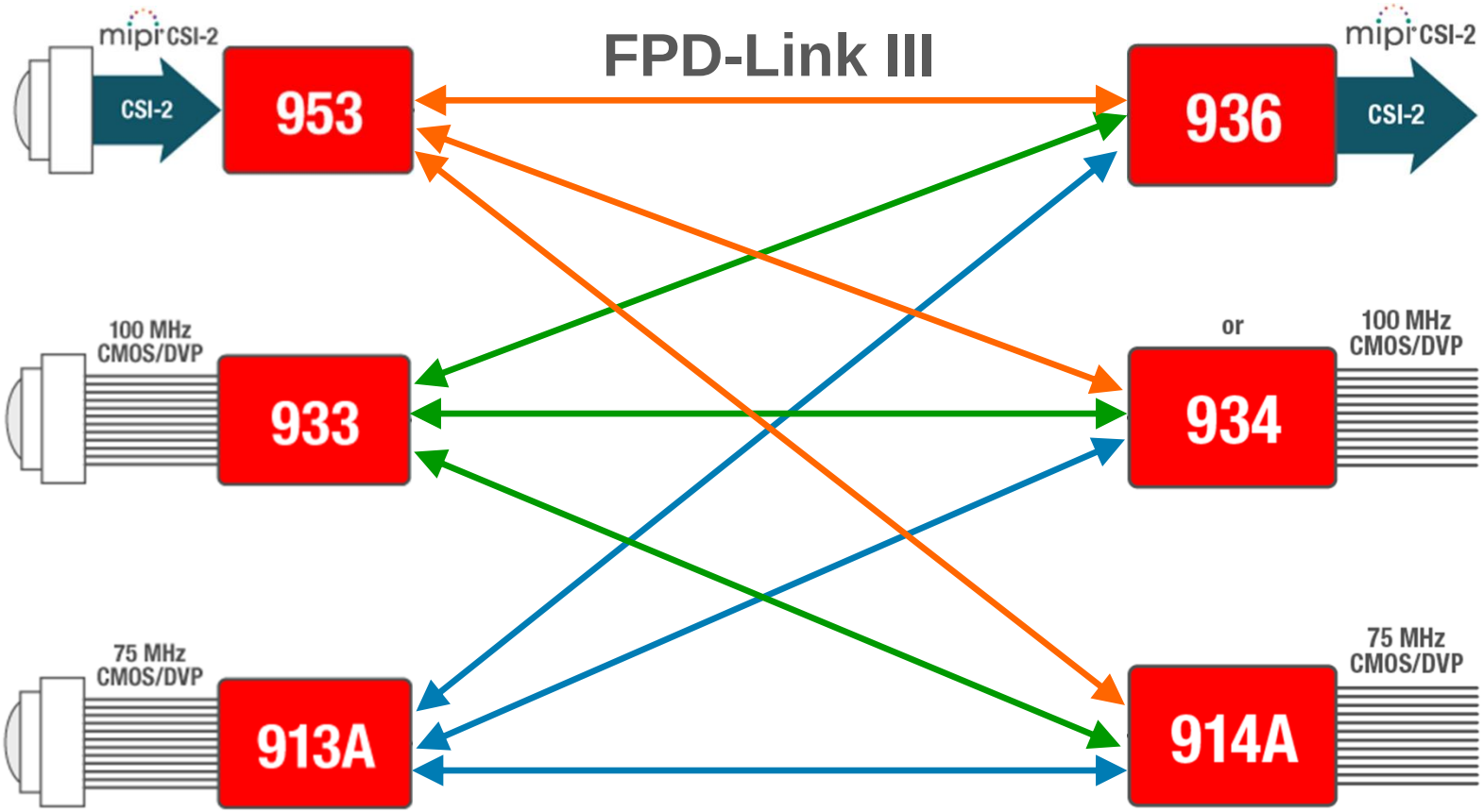
Common Imager Resolutions



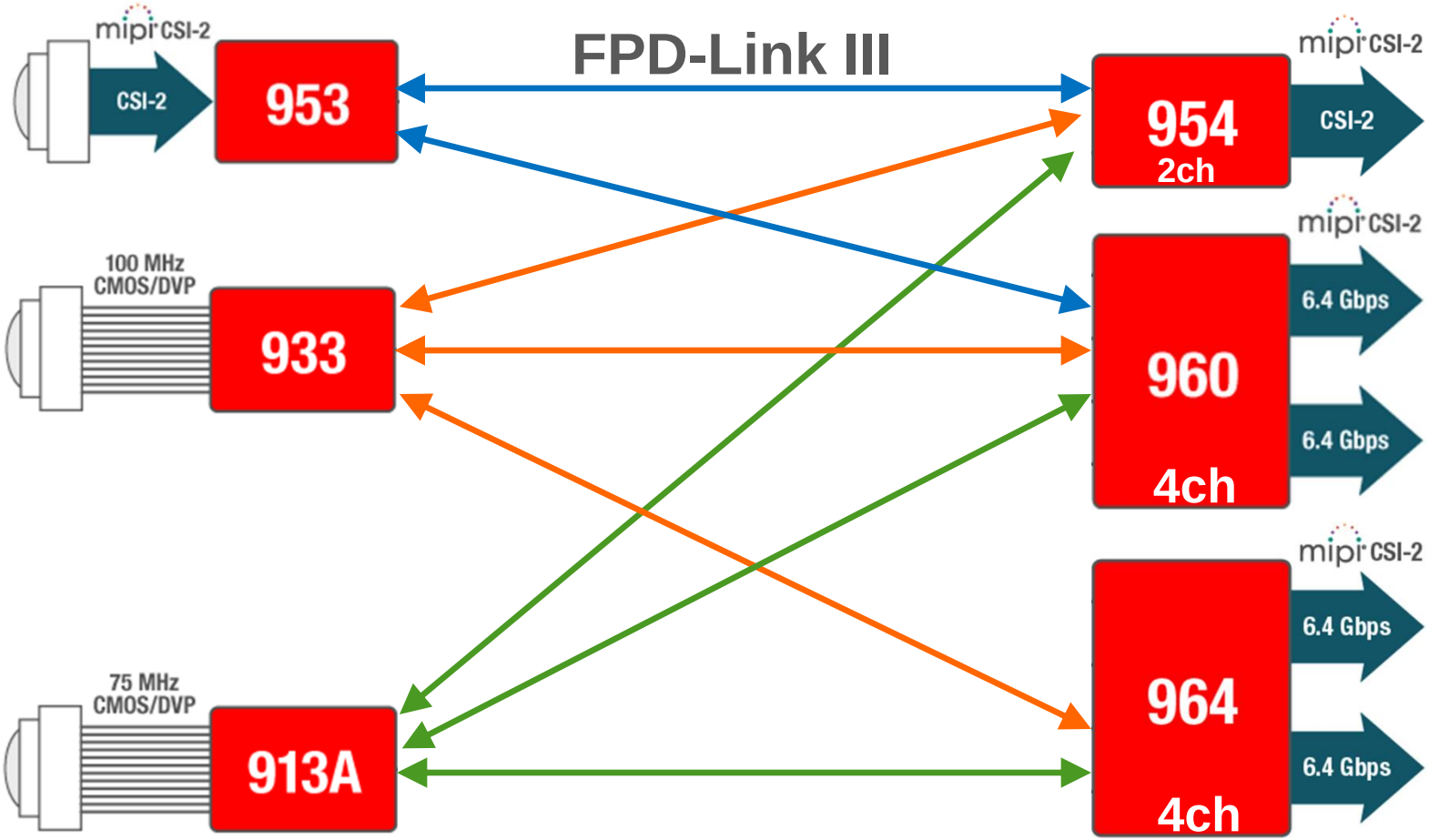
FPD-Link ADAS Portfolio



SER/DES Companion Options for ADAS



SER/DES HUB Solutions for ADAS



DS90UB933/934

TIDesigns

Features

- Serializes 12 bits up to 100 MHz
- Ultra-low <25 us control channel latency
- On-chip internal oscillator for quick camera start-up
- Adaptive receiver equalization
- **1MP/60fps or 2MP/30fps**

Benefits

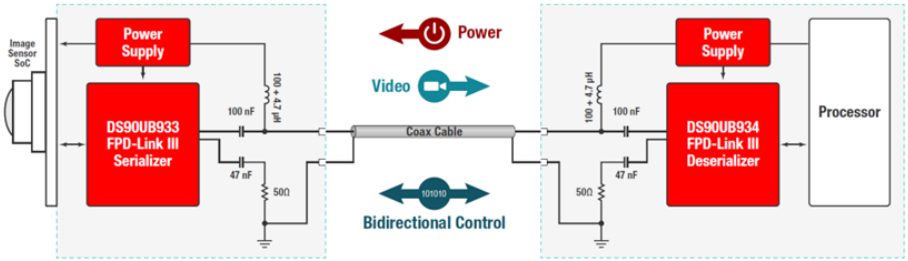
- Supports higher resolution camera imagers
- Allows ISP function to be moved out of the camera to the ECU side, enabling smaller cameras and lowering thermal imager noise
- Cameras are ready quickly after starting car
- Compensates for cable degradation effects due to ageing and bending

Applications

- Automotive camera applications
- Satellite RADAR
- Industrial/medical imaging & security & surveillance

Tools & Resources

- **Cable Characteristics & PoC App Notes**
- **EVM & Design Files**
- **ALP EVM Software GUI**
- **Device Datasheets:**
  - DS90UB933-Q1
  - DS90UB934-Q1



DS90UB964

TIDesigns

Features

- Aggregates up to 4 cameras up to 12 bits@100 MHz
- Dual MIPI CSI-2 output ports
- Virtual channel support tags cameras and exposures
- Ultra-low latency
- Adaptive receiver equalization compensates for cable ageing

Applications

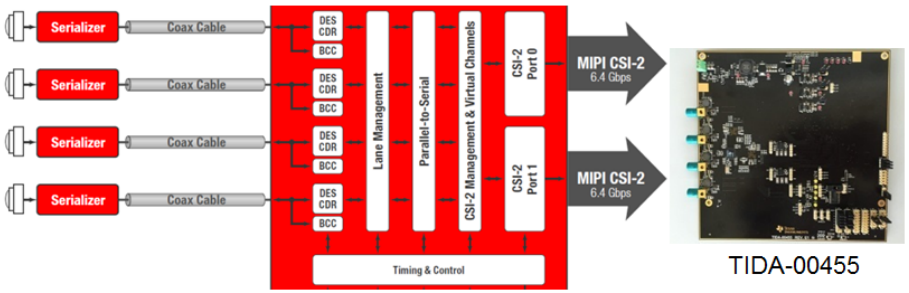
- Automotive camera applications
- Satellite RADAR
- Industrial/medical imaging & security & surveillance

Tools & Resources

- **TIDA-00455 Surround View Ref Design**
- **EVM & Design Files**
- **ALP EVM Software GUI**
- **Device Datasheets:**
  - DS90UB964-Q1

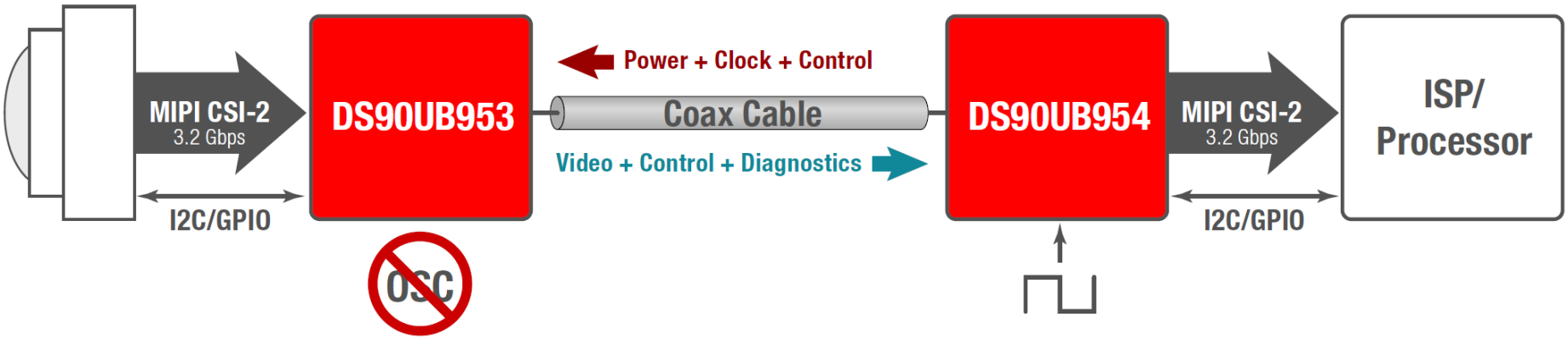
Benefits

- Delivers video from 4 cameras to a single SoC video port
- Easily creates 2nd copy of video data for use in other video paths such as viewing (display) and data logging
- Separates multiple camera and exposure information so the SoC can easily distinguish this data
- Allows ISP function to be moved out of the camera to the ECU side, enabling smaller cameras and lowering thermal imager noise
- Cameras are ready quickly after starting car
- Compensates for cable degradation effects due to ageing and bending



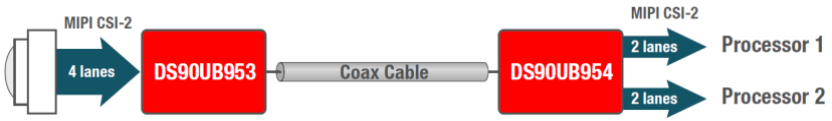
TIDA-00455

DS90UB953/954
2MP MIPI CSI-2 Ser/Des



- Supports 2MP image sensors with MIPI CSI-2 interfaces
  - Up to 4 data lanes and clock lane
  - YUV, RAW and RGB data types
  - High Speed, Low Power and Ultra Low Power modes

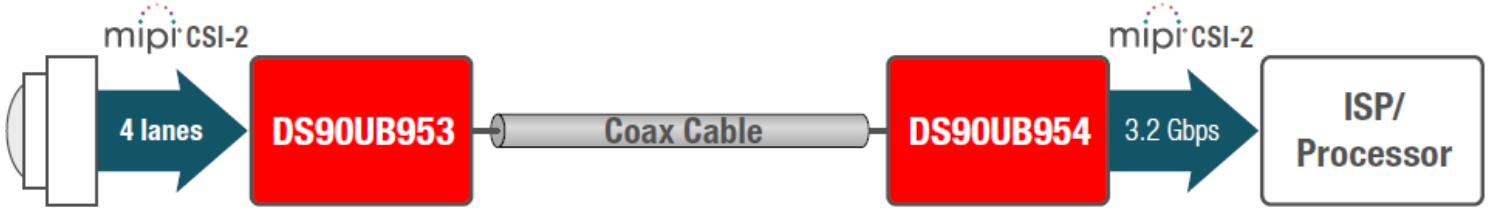
Replicate mode



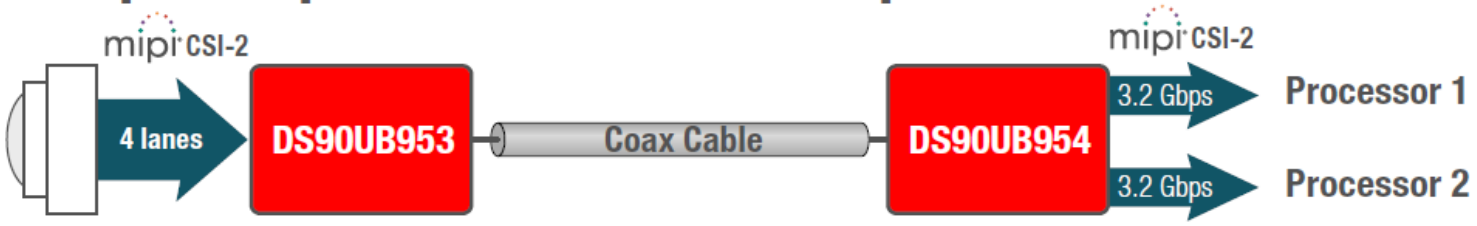
- Receiver-side clocking ensures all cameras are synchronous
- No 953 register writes if control channel errors present
- Reads Power-over-Coax (PoC) input voltage & internal temp
- Easier PoC support, smaller inductors
- Forward and back channel CRC
- 954 has 2 independent camera “hub” inputs and output replicate mode
- Small footprint (36 QFN) enables compact camera module design

DS90UB953/954 – Flexible Interfaces

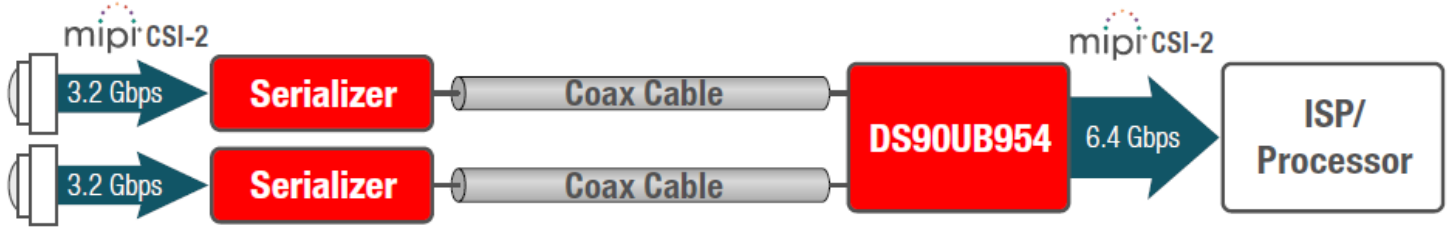
Single 2MP camera example



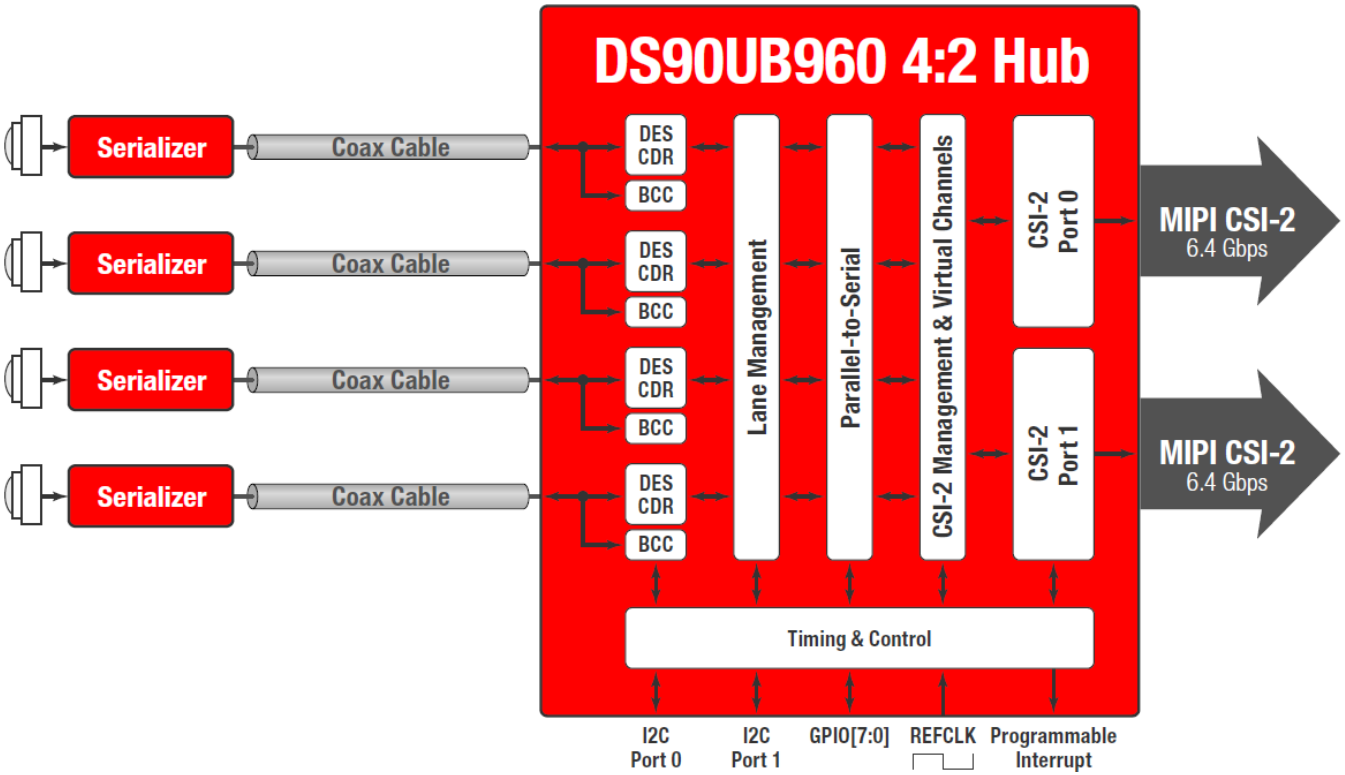
Output replicate mode example



Dual camera example



DS90UB960/964
4:2 Camera Deserializer Hub



- Aggregates up to four 2MP cameras
  - Full 2MP HD & 60fps support
  - Coaxial or single differential pair
- 2x 6.4 Gbps MIPI CSI-2 output ports
  - Flexible mapping of cameras to port(s)
  - Aggregate & replicate modes
- CSI-2 virtual channel support
- (960) had Synchronous clocking mode with 953
- Programmable frame sync generator
- Adaptive Receiver Equalization
- 2x I2C ports up to 1MHz
  - Program 2 cameras using both I2C buses or multiple cameras using I2C broadcast
- 8 GPIOs
- Compatible with 953, 933, & 913A serializers
  - 964 version supports 933/913A only

Clock Source Selection

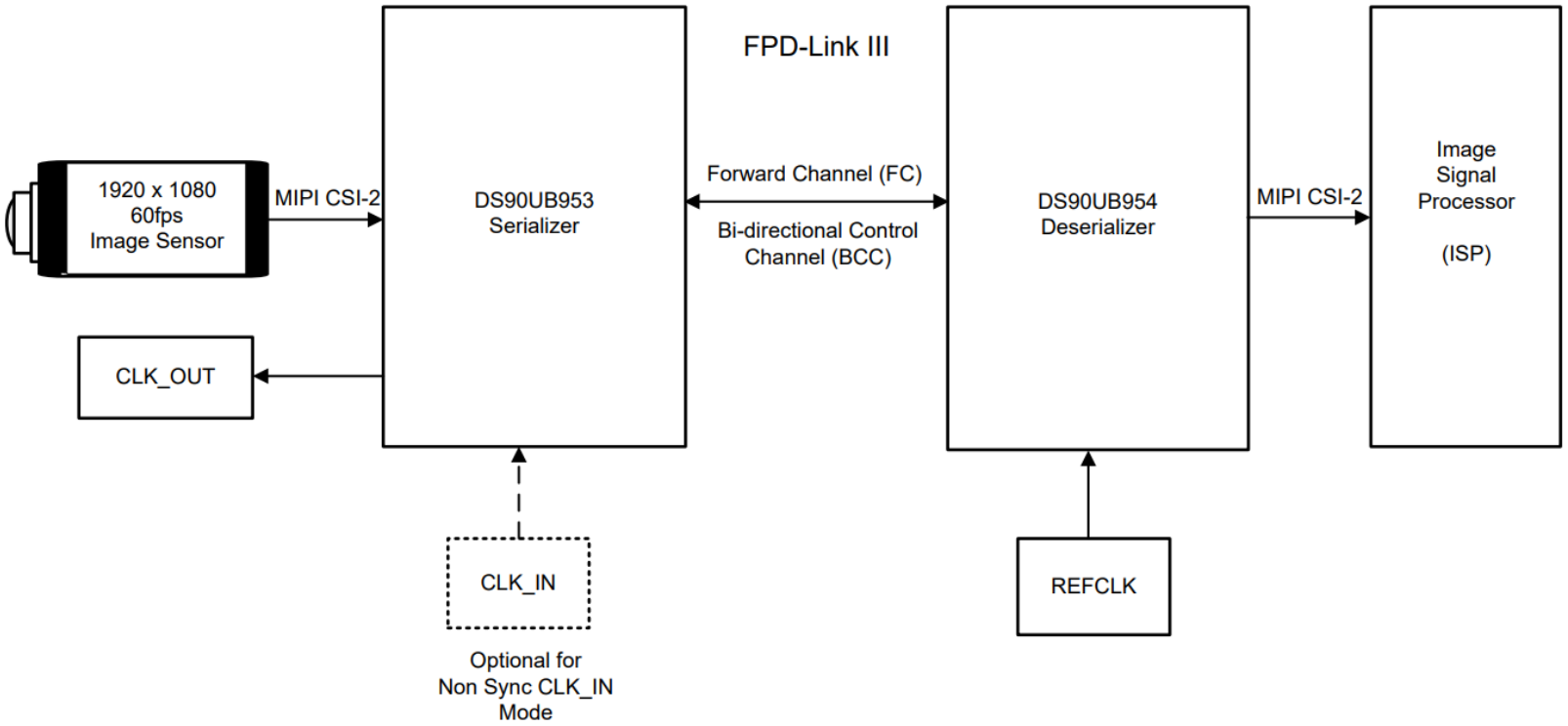


Figure 9. Clocking System Diagram

Frame Synchronization

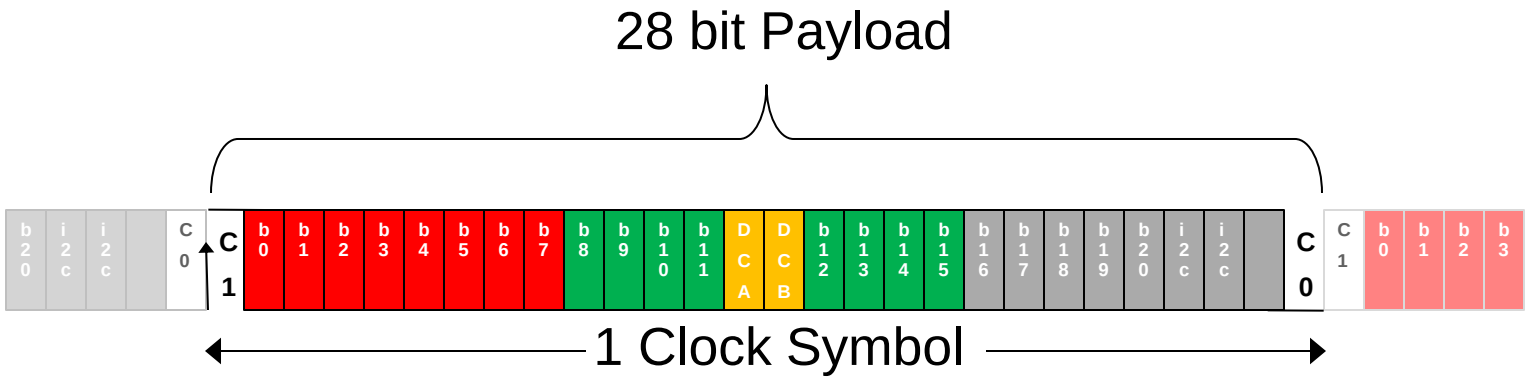
1. Synchronous: Back Channel Synchronous Clock extracts a clock reference from the bidirectional communications link back channel, and internal PLLs generate the required clocks. This modes locks multiple sensors frequencies to a central clock domain.
   - The DS90UB953-Q1 generates a programmable reference clock for the image sensor.
   - The back channel clock rate is determined by the reference clock that is being provided to the deserializer.
2. Non Sync CSI_Clk: CSI Clocking uses the CLK signal at the CSI interface as the clock reference for the FPD output stream.
   - External onboard reference clock to the camera is required
   - 953 uses the CSI-CLK as the clock source for the FPD link data
   - 953 FPD rate is proportional to the CSI clock rate
   - Back channel speed must be below 10-Mbps (Manchester) rate
   - AC Cap of 0.1 µF is required
3. Non Sync CLK_IN: External Clock Reference uses an external oscillator as a reference and generates the required clock for the FPD forward channel for that reference.
   - External onboard reference clock is required to provide reference clock to the 953 CLK-IN pin
   - FPD rate is running at constant rate proportional to the external reference clock
   - The CSI rate is independent of the FPD rate
   - Back channel speed must be below 10-Mbps (Manchester) rate
   - AC Cap of 0.1 µF is required

DRAFT
TI Confidential - NDA

FPDLINK

- Fundamental (payload, line rate, UI, jitter)
- Adaptive EQ
- I2C and Alias
- Link Diagnostics
- Power-over-coax
- Cable Requirement
- CMLOUT Eye Diagram Monitor
- Build-in-self Test (BIST)

ADAS FPD-Link III Payload
91x/93x/95x



C1 = Clock bit HIGH

C0 = Clock bit LOW

DCA & DCB = Link Overhead

DIN[n:1] -> DS90UB903/4: 24 Data Bits (18-bit RGB+3 + I2C)

Note: Payload bits are *Randomized, Balanced & Scrambled*

FPD-Link III Math: DS90UB903/904 - 43 MHz Example

- 43 MHz Input Clock (pixel clock, PCLK)
  - 23.26 ns period
- 1 UI (Unit Interval) serial data bit is 1/28th of clock period:
  - 23.26 ns / 28
  - **1 UI = 830 ps**
- Serial line rate:
  - 43 MHz x 28 bits = 1.20Gbps

Jitter needs to be less than 398.4ps.

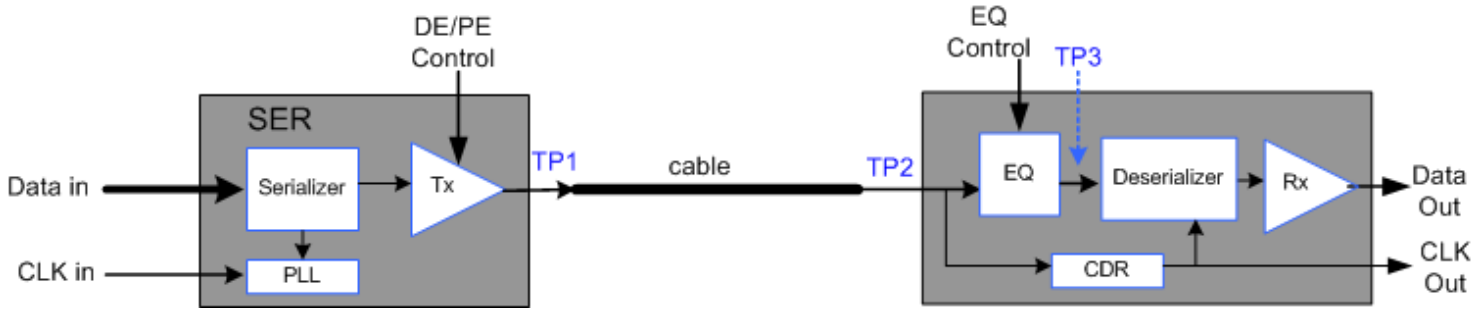
Oscilloscope Requirements:

- **50-ohm terminated**
- **> 2 x Line Rate**

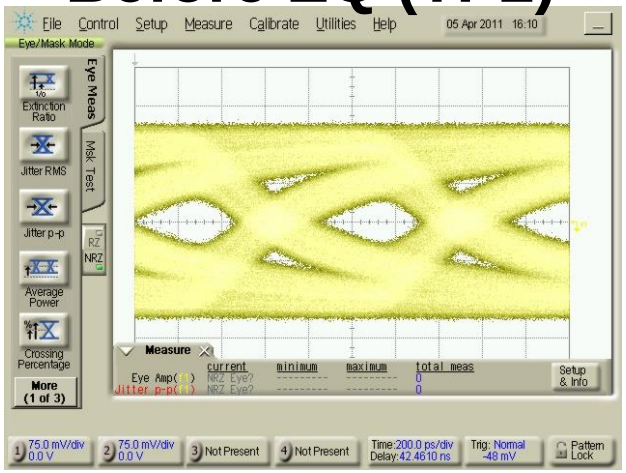
Symbol	Parameter	Conditions	Pin/Freq.	Min	Typ	Max	Units
t_{DD}	Deserializer Delay	Default Registers Register 0x03h b[0] (RRFB = 1) (Figure 17)	10 MHz–43 MHz	4.571T + 8	4.571T + 12	4.571T + 16	ns
t_{DDLT}	Deserializer Data Lock Time	(Figure 15)(2)	10 MHz–43 MHz			10	ms
t_{RJIT}	Receiver Input Jitter Tolerance	(Figure 19, Figure 21)(3)(4)	43 MHz		0.53		UI

FPDLINK Adaptive Equalization (EQ)

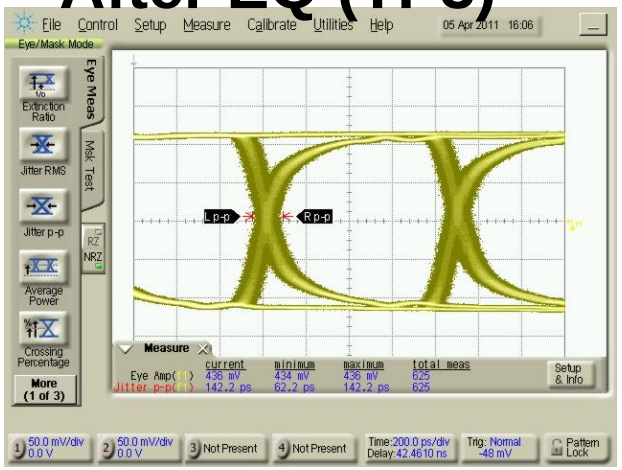
- Gain curve in Deserializer compensates for cable loss
- Programmable gain setting
- Enhanced ADAPTIVE EQ – automatically selects gain to compensate for cable loss (no programming)



Before EQ (TP2)



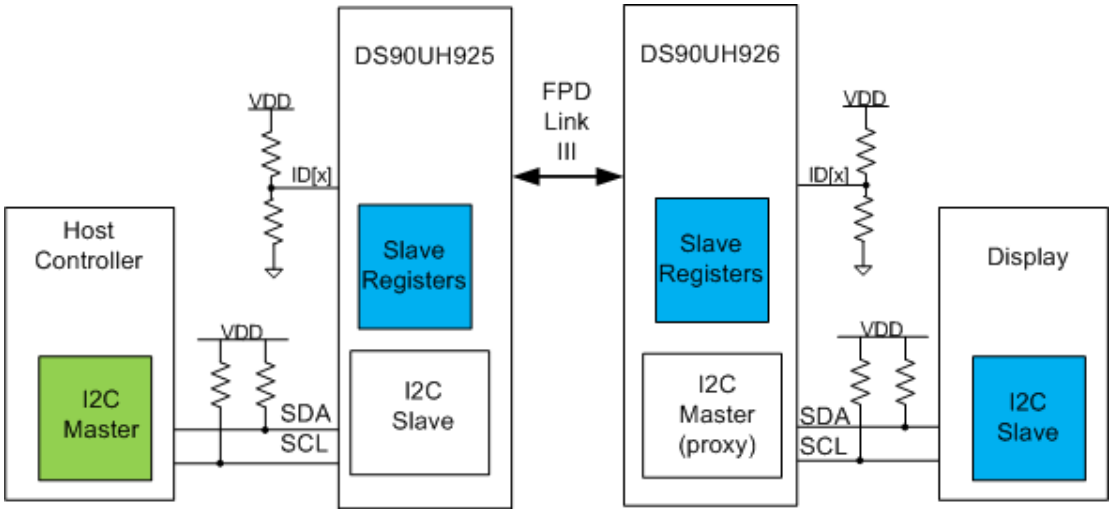
After EQ (TP3)



Texas Instruments

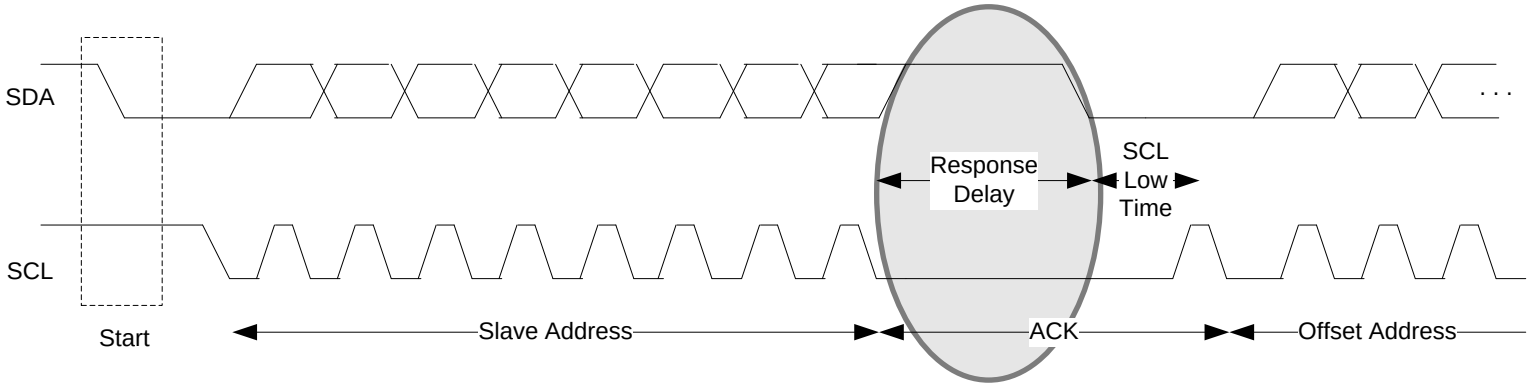
I2C Control Interface Communication

- I2C compatible interface bridged over link – up to 400kHz
  - Multi-master arbitration supported
  - Clock stretching required
- Local and remote I2C access
- Up to 16 unique addresses – configurable via ID[x]



I2C Clock Stretch

SCL Stretching by local Ser/Deser provides necessary time delay for remote device acknowledge across link



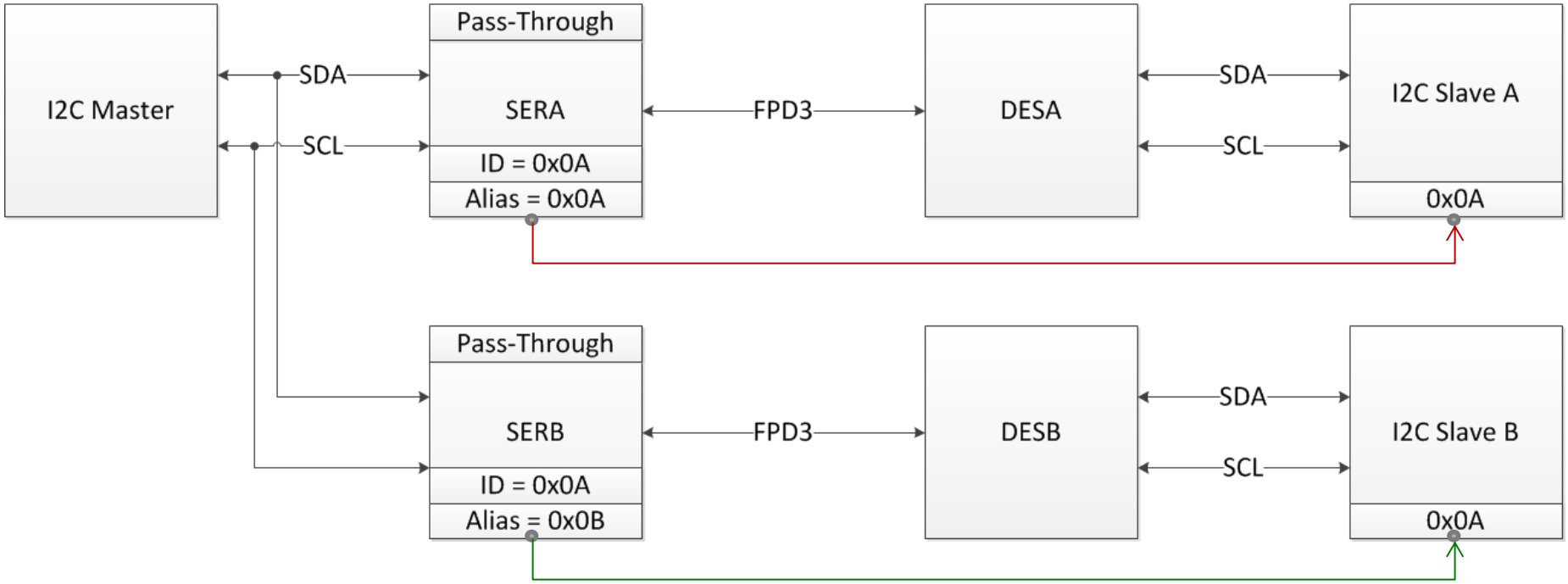
- **For remote accesses, the "Response Delay" shown is on the order 10 – 15 us for DS90UB901/2/3/4Q and DS90UB913/914Q**
- **The "Response Delay" includes the latency time of the control channel packing and serialization protocol across the differential link to the remote peripheral**

I2C R/W Remote Slave

1. If SER is connected and system is powered up, DES 0x06 register will auto load SER address.
2. Set I2C Pass-through (SER 0x03[1]→1'b
3. Set SlaveID0 (SER 0x07→0x0A)
4. Set SlaveAlias (SER 0x08→0x0A)
5. Read/Write to Slave using address 0x0A

I2C Access Multiple Remote Slaves

- Why SlaveAlias register? → Eliminates remote slave ambiguity
- Set I2C Pass-through (SERA, SERB 0x03[1]→1'b)
- Set SERA Slave ID (SERA 0x07→0x0A)
- Set SERA Slave Alias (SERA 0x08→0x0A)
- Set SERB Slave ID (SERB 0x07→0x0A)
- Set SERB SlaveAlias (SERB 0x08→0x0B)
- Read/Write to Slave A with address 0x0A, Slave B with address 0x0B



I2C over DS90UB913/4 FPD-Link III with Bidirectional Control Channel

http://www.ti.com/lit/an/snla222/snla222.pdf

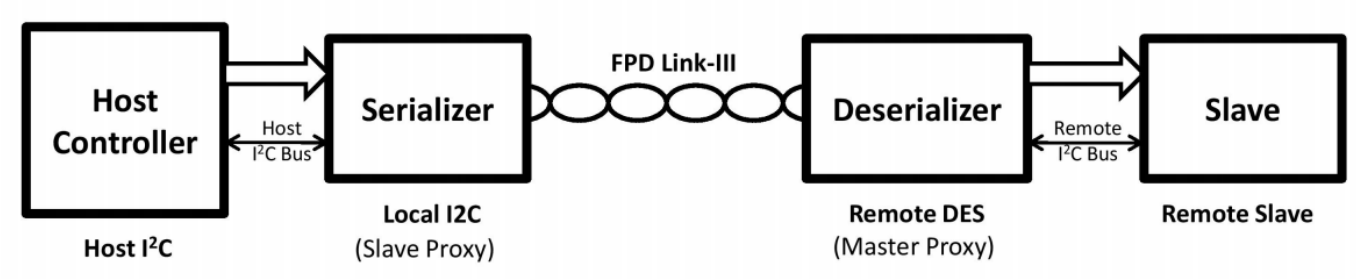
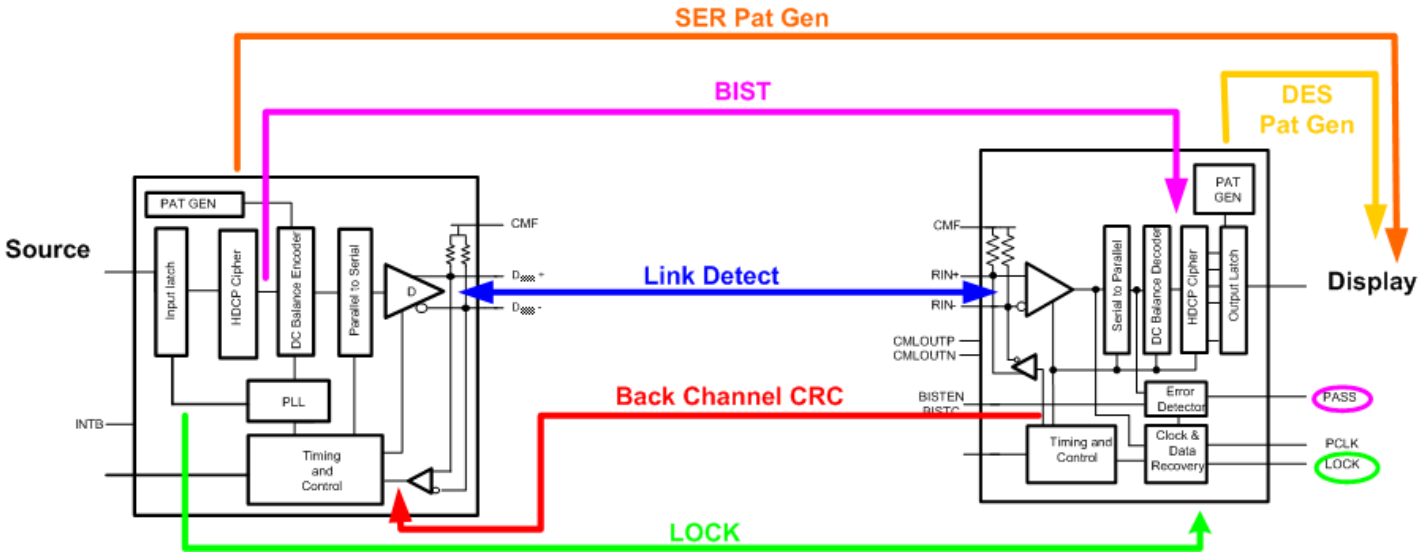


Figure 7. I²C Master attached to Serializer

Table 6. Typical I²C bit rates

Host I²C Rate	Remote I²C Rate	Master Proxy register settings		Net Bit Rate
		"SCL High Time" register	"SCL Low Time" register	
100 kbit/s	77 kbit/s (Default)	0x82 (Default)	0x82 (Default)	41 kbit/s
100 kbit/s	100 kbit/s	0x64	0x64	47 kbit/s
400 kbit/s	100 kbit/s	0x64	0x64	72 kbit/s
400 kbit/s	400 kbit/s	0x32	0x32	155 kbit/s

Link Diagnostics



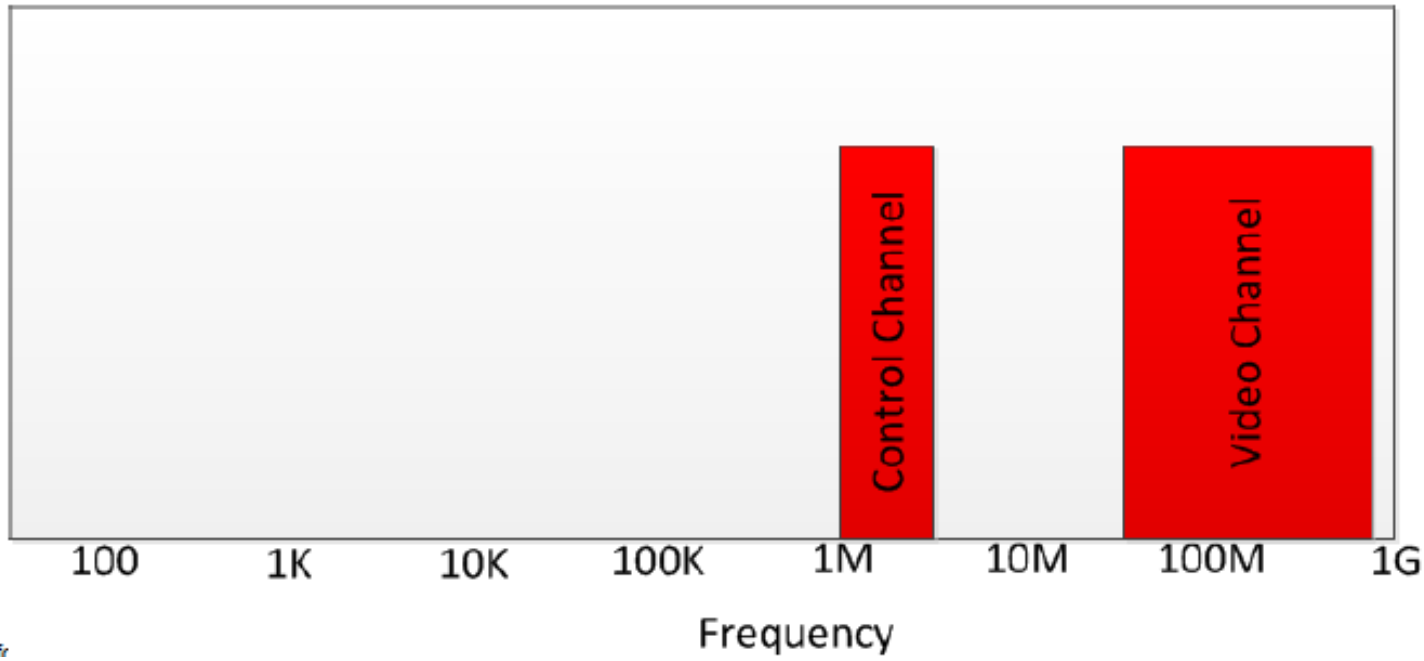
1. **LOCK: Verifies link established between SER and DES – CDR has "locked" to incoming serial data stream. Monitor LOCK pin.**
2. **BIST (Built-in Self Test): Verifies data integrity of link between SER and DES. Monitor PASS pin.**
3. **CRC: Integrity of backchannel link. Error reporting via register.**
4. **PAT GEN: Visually validate data path without video source. Test pattern generated by SER or DES.**
5. **LINK DETECT: Remote verification of link between SER and DES. Monitor register in SER.**

FPD-Link III for Driver Assist Power-over-Coax

- PoC Overview
- Inductor Selection Criteria
- Cable requirement
- PoC FPDLINK Performance Test

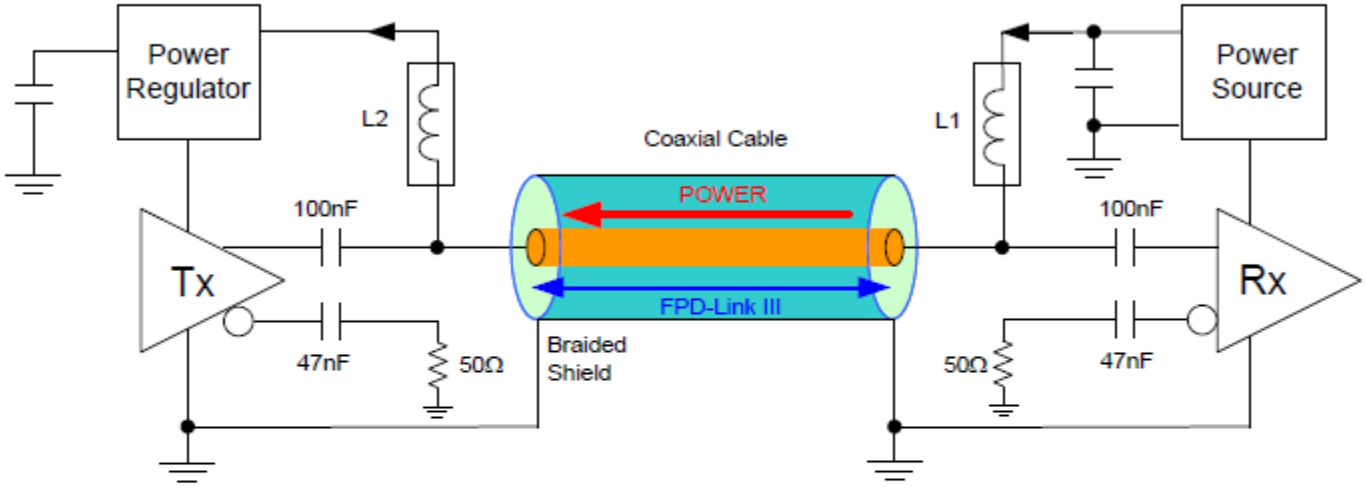
Overview of FPD-III

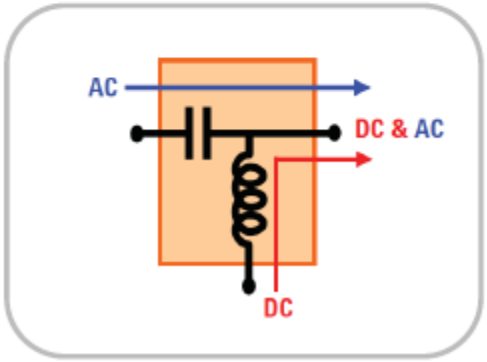
- FPD-III has a high speed forward channel, and a lower speed bidirectional backchannel, which is all sent over either a piece of coax cable, or a single pair in a shielded twisted pair cable.
- The forward and back channels are separated in the frequency domain



TI Infr

Power Over Coaxial Cable Concept

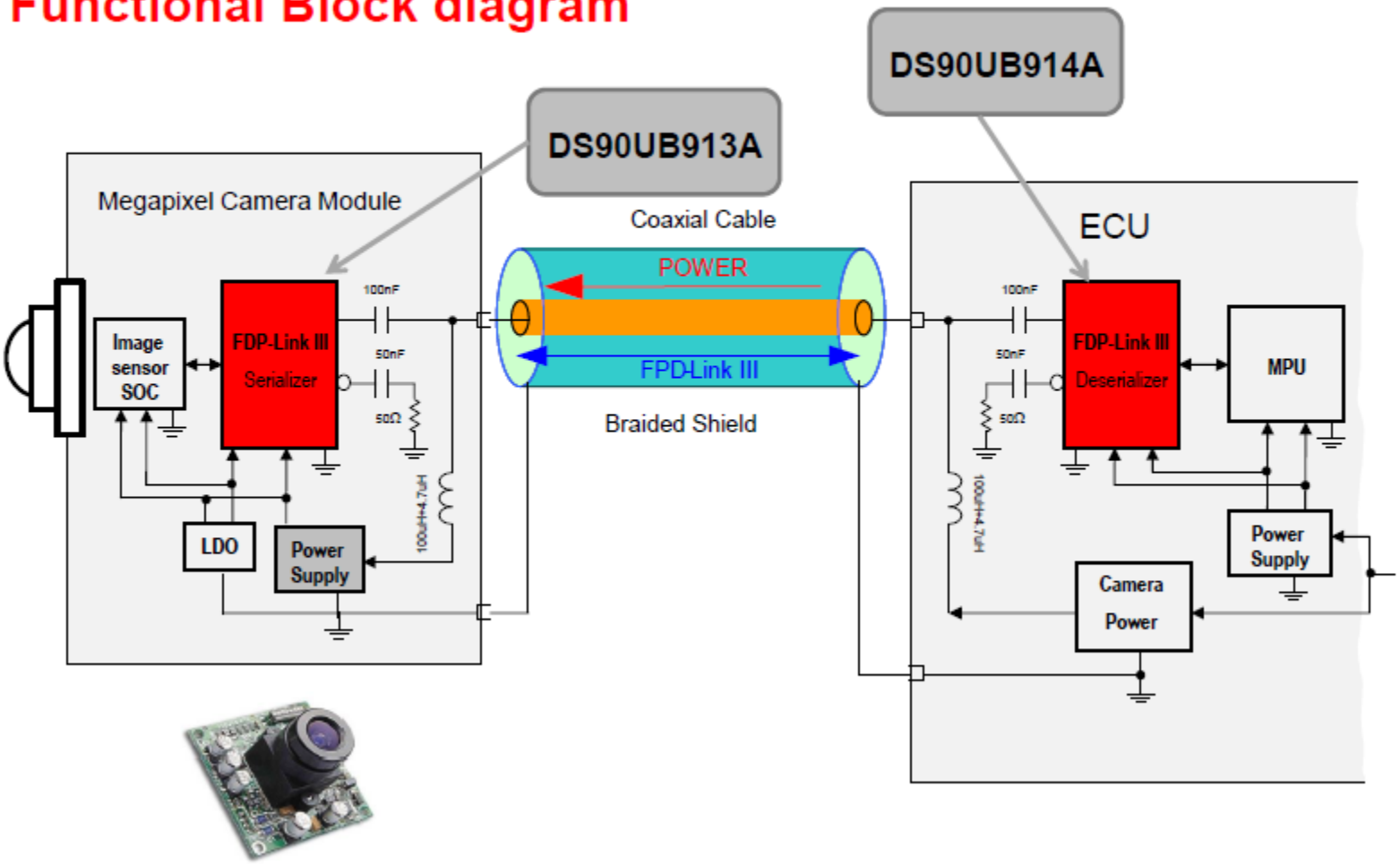




- Same implementation for many years on antenna connections

FPD-link III and Power over Coax

Functional Block diagram



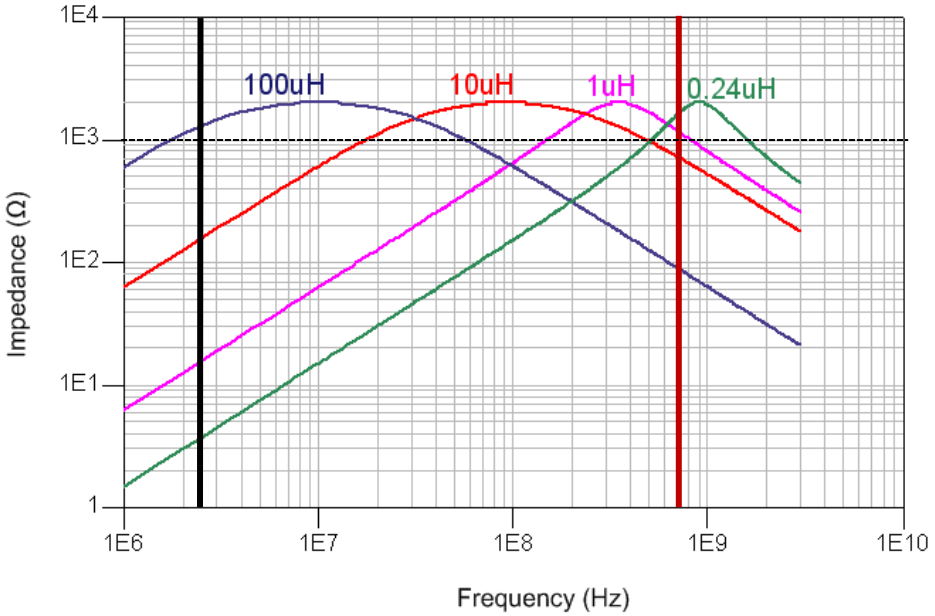
Power Over Coaxial Cable Overview

- Power injected on coax cable at Deserializer; drawn from other end of cable
- Power over Coax or Differential Pairs provides power distribution for remote sensors, i.e., cameras
- Typical current range 0.2A to 0.5A, voltage of 5-8V, <4 Watts
- Cable braid used as ground return
- Inductor selected to provide required AC impedance over operating frequency range of the differential signals- Forward & Back-channel
- Ensure inductor saturation and **RMS** current requirements are met

Coupling Inductor Selection Criteria

- Impedance vs. Frequency ➔ Inductance Value
  - Select component to have high impedance (~1kOhm) at operating frequency of serial communication channel
    - SRF and Q parameters impact this characteristic curve
  - DS90UB913A/914A
    - High Speed Forward channel: 700MHz max
    - Low Speed Backchannel: 2.5MHz, target 1MHz (provides margin)
- Saturation/RMS Current
  - Max current @ minimum voltage delivered at camera
  - Higher Isat & IRMS requires larger footprint
  - I_{RMS} important to limit camera heat!
- Size
  - Optimize selection to meet criteria listed above to achieve smallest footprint

Power over Coaxial: inductor selection



Impedance Versus Frequency Plot for a Single Inductor

FPD-Link III	*Max PCLK (MHz)*	*Forward Channel Line Rate (Gbps)*	*Embedded Bidirectional Control Channel*	*Target Power Feed Inductance*
DS90UB913A/914A	100	1.400	Yes	100uH + 4.7uH

- **Forward channel is 700MHz.**
- **Back channel is 2.5MHz with 30% frequency variation.**

PoC Cable S-parameter Requirements

- **Insertion Loss**
- **Return Loss**

What you need to know about high-speed cables for FPD-Link III SerDes (3Q 2017)

http://www.ti.com/lit/an/slyt726/slyt726.pdf

S-parameter

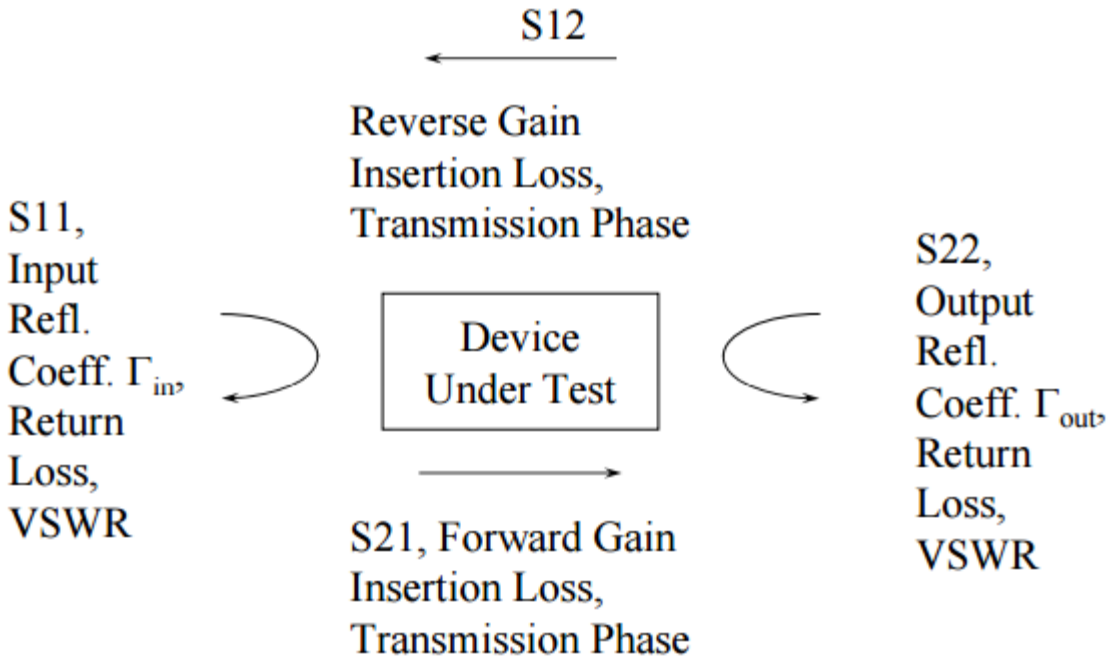
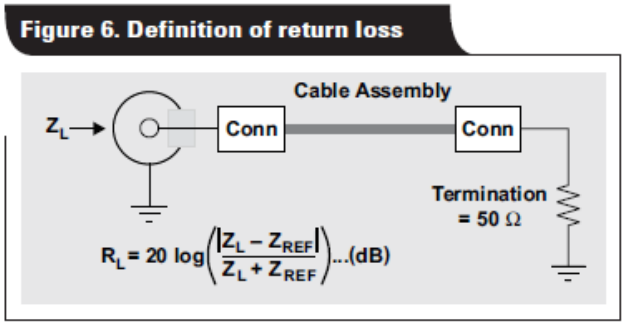


Figure 6. Definition of return loss



FPD-LINK Connection

Figure 2. FPD-Link III infotainment subsystem using HSD connectors with a STQ differential cable

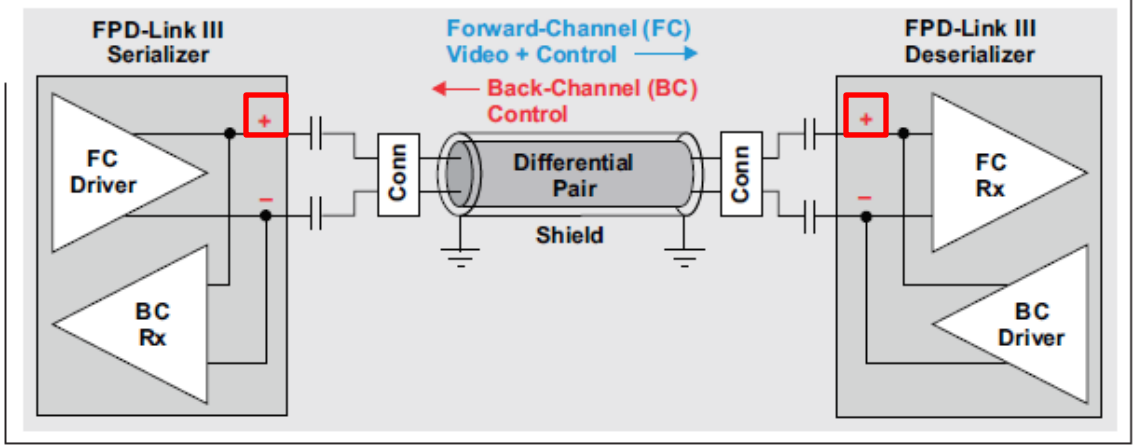
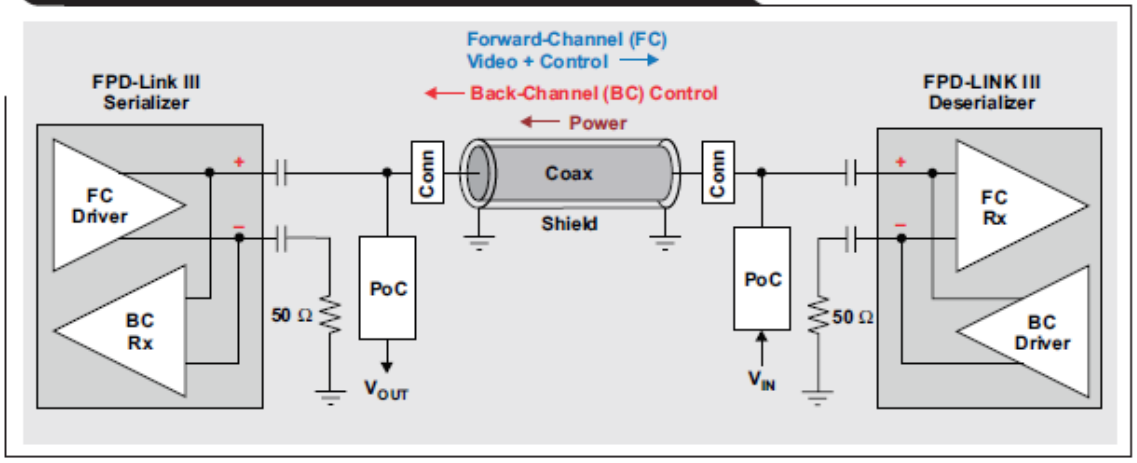


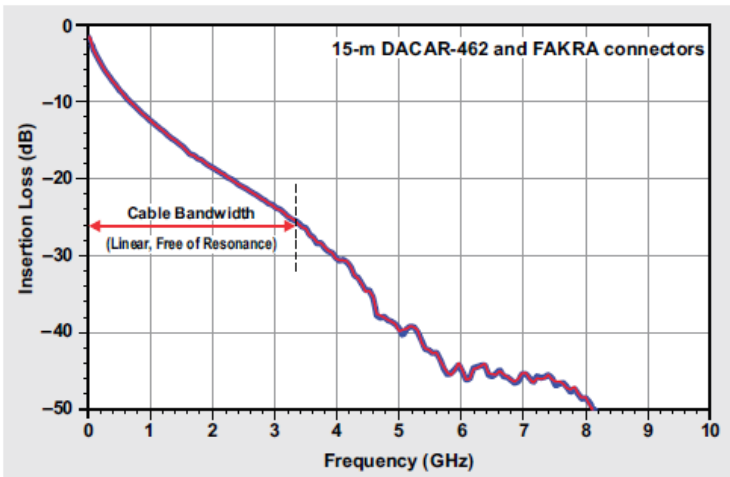
Figure 3. FPD-Link III driver-assistance subsystem using FAKRA connectors with a coaxial cable

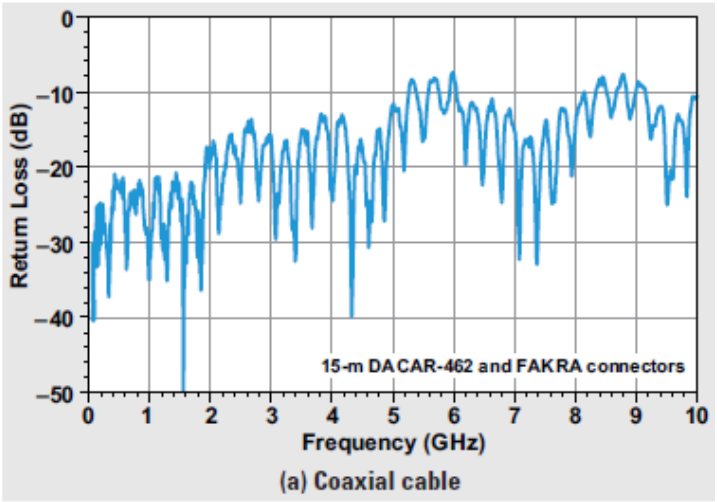


Insertion Loss and Return Loss

Coax

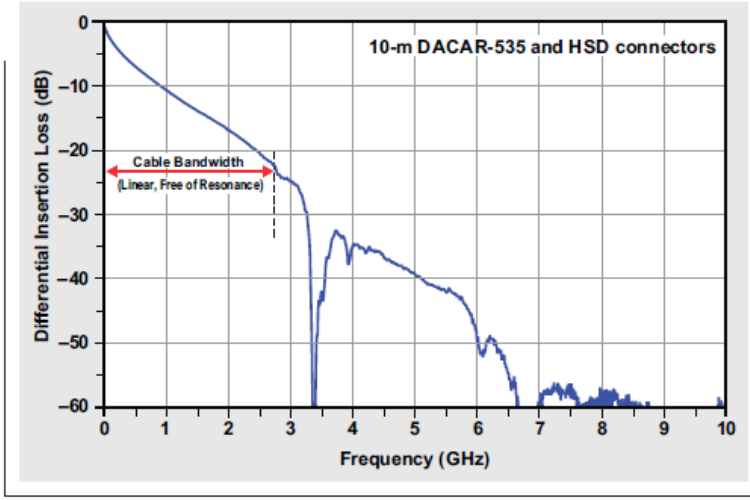
Figure 8. Insertion loss of a 15-m coaxial cable

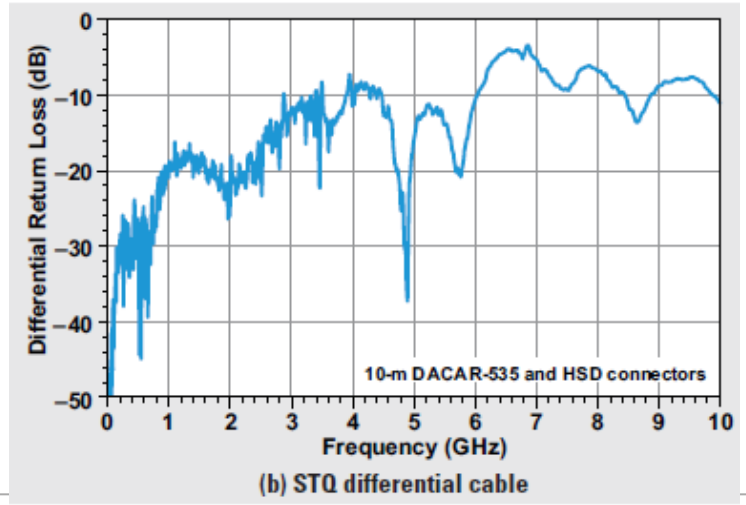




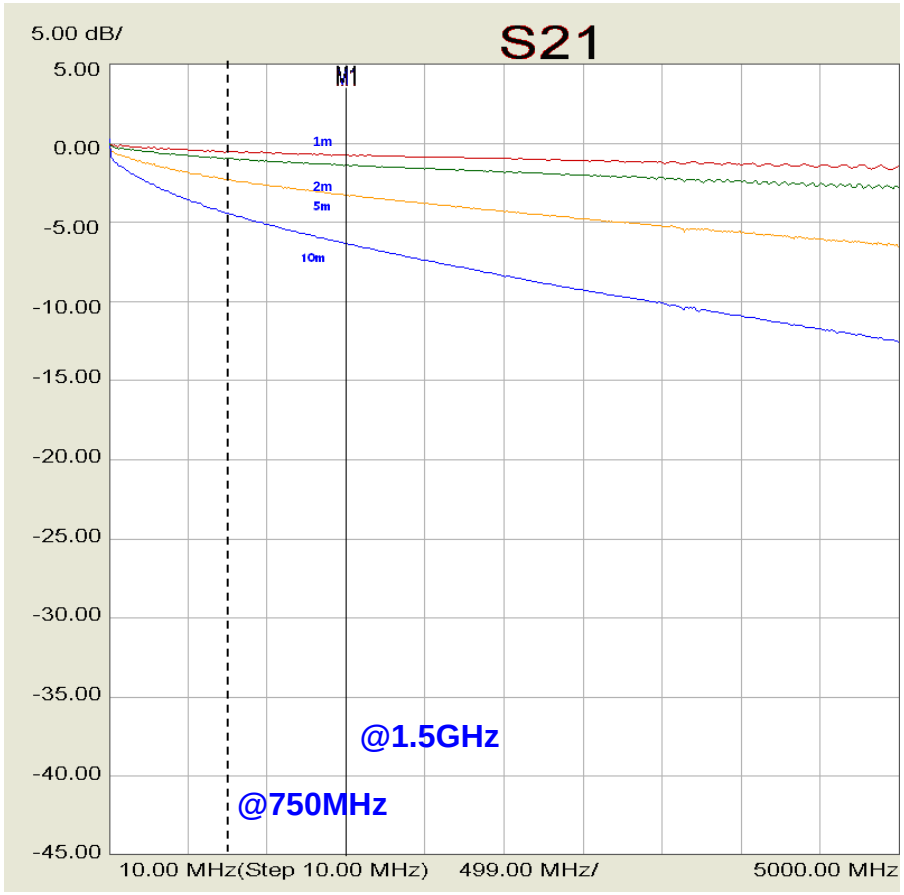
STQ

Figure 9. Insertion loss of a 10-m STQ differential cable





50 Ω Single-ended Coaxial (FAKRA/RTK 031)



Across cable lengths:

1m

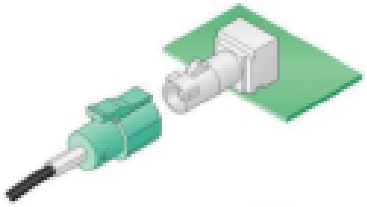
2m

5m

10m

FAKRA

Coaxial Cable/Connector



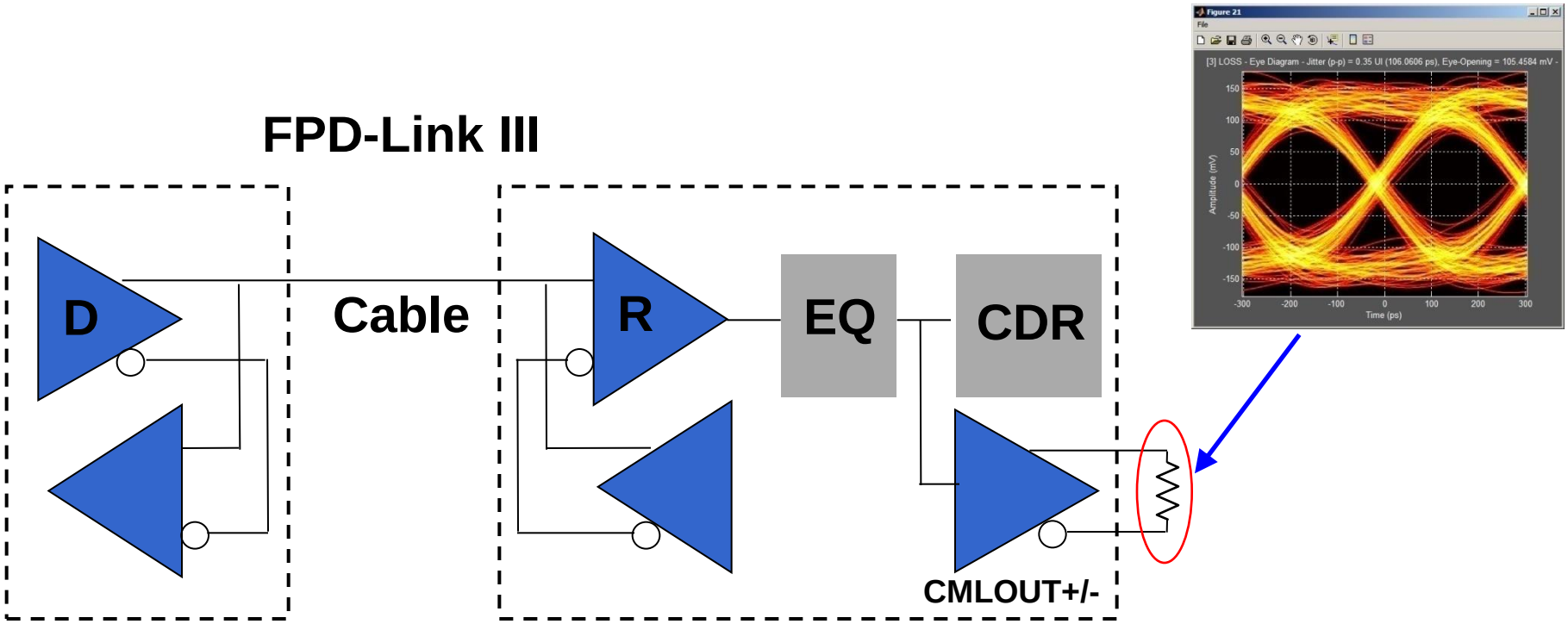
- **Multiple suppliers:**

- **Rosenberger/Leoni, AMP, TE Connectivity (Tyco), Molex, Delphi, Pasternack, Flontec, Shikoku**

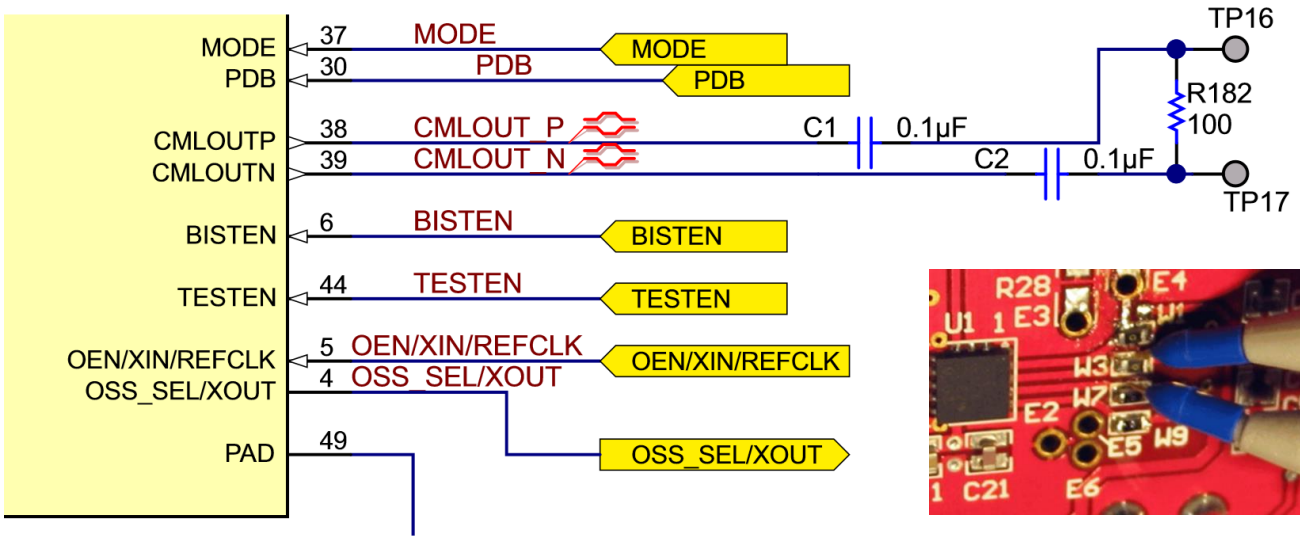
FPD-Link Performance Measurement

- CML Output Eye Diagram
- Build-in-self Test (BIST)

Monitor Output of Equalized Signal



Measure CMLOUT to See Signal Quality



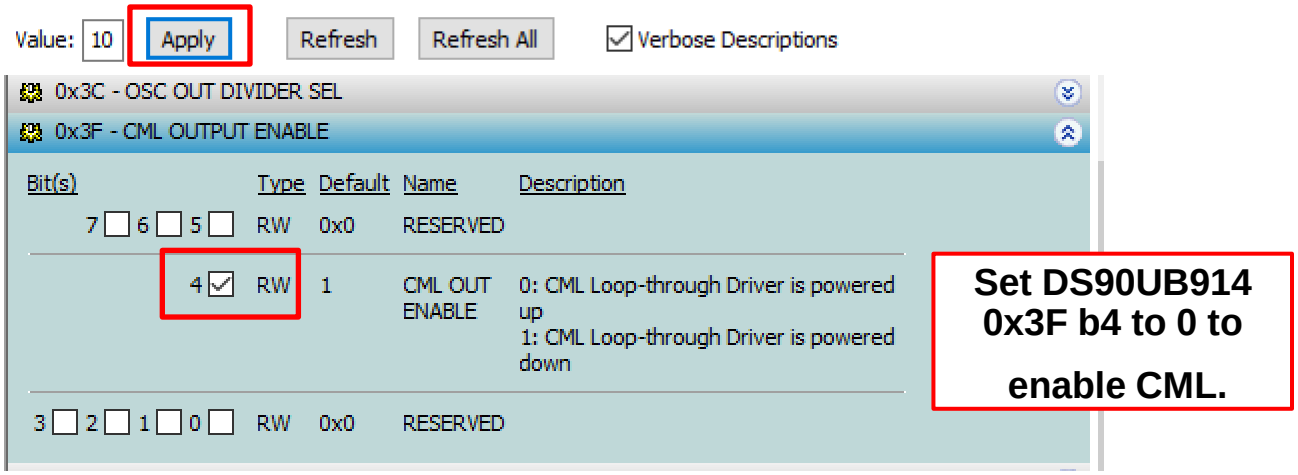
PIN		I/O TYPE	DESCRIPTION
NAME	NO.		
DIAGNOSTIC PINS			
CMLOUTP	38	O	Channel monitor loop-through (CML) driver differential output. Typically routed to test points and not connected. For monitoring terminate CMLOUT with a 100-Ω differential load.
CMLOUTN	39		

DS90UB914A-Q1 CML OUTPUT Enable 0x3F b4 Set 1

Hardware pin

0x3F	CML Output Enable	7:5	RSVD			Reserved.
		4	CML OUT Enable	RW	1	CML Output Driver Enable is Active-Low. 0: CML Loop-through Driver is powered up. 1: CML Loop-through Driver is powered down.
		3:0	RSVD			Reserved.

Analog Launchpad GUI

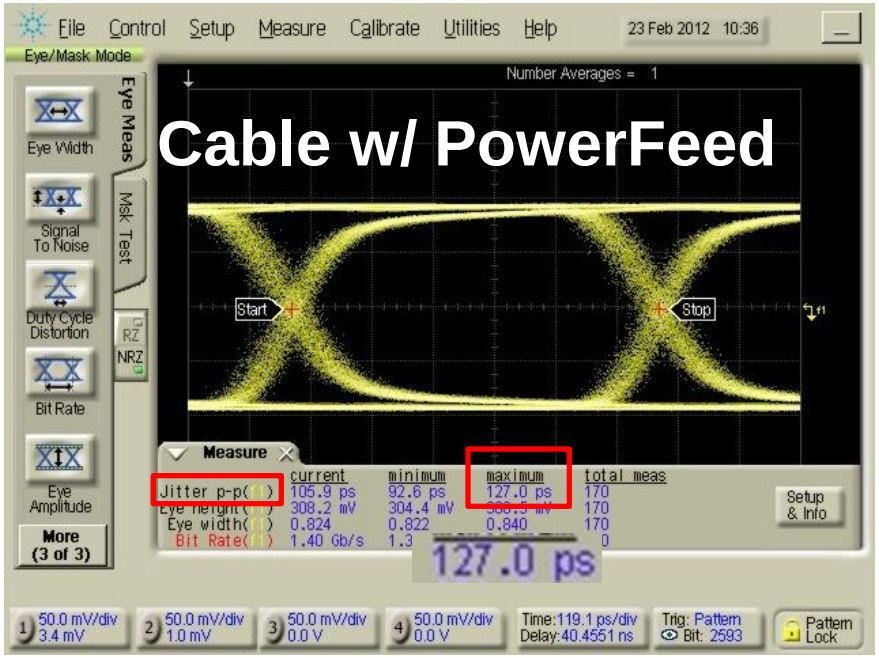


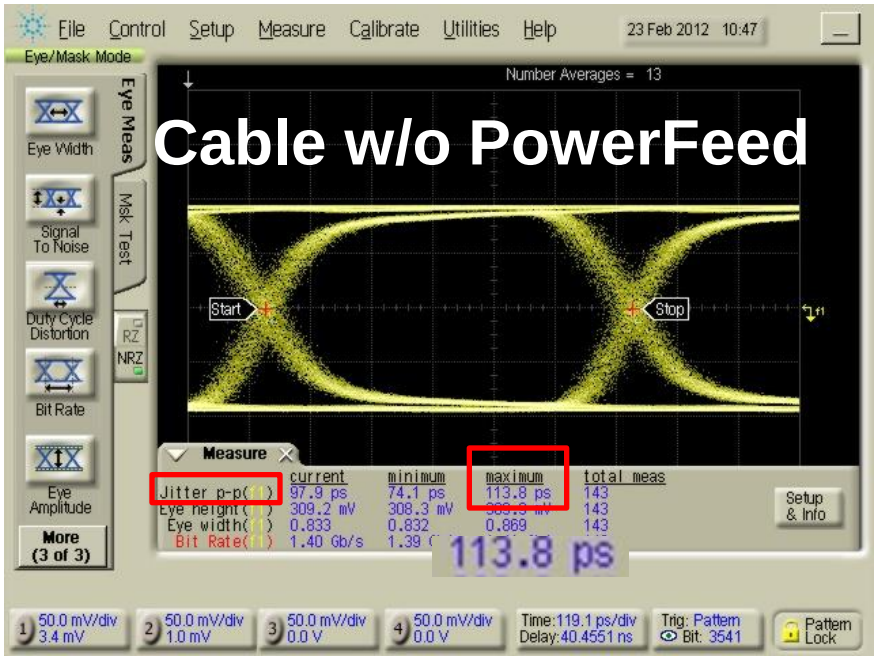
Set DS90UB914 0x3F b4 to 0 to enable CML.

Change port if needed.

SEL	46	Input LVCMOS w/ pulldown	MUX Select Line SEL = L, RIN0+/- input. This selects input A as the active channel on the Deserializer. SEL = H, RIN1+/- input. This selects input B as the active channel on the Deserializer.

CMLOUT Eye Diagrams
with and without Power Feed (PoC)





Recovered Data Eye Diagram after 10m Coaxial Cable

DS90UB914A-Q1 CML Output Eye Diagram Calculation

CML MONITOR OUTPUT DRIVER SPECIFICATIONS (CMLOUTP, CMLOUTN)				
E_w	Differential output eye opening	R_L = 100 Ω Jitter frequency > f / 40 (see Figure 20)	0.45	UI
E_H	Differential output eye height		200	mV

Assume use 12-bit low frequency mode:

Line rate = PCLK x 28-bit

Line rate = 1.4Gbps

PCLK = Line rate / 28 = 1.4G / 28 = 50MHz

Ew = 0.45UI

Ejitter = 1 – Ew = 0.55UI

Line rate = 1.4Gbps = 700MHz

1UI = 1/ (PCLK x 28-bit) = 714ps

Jitter tolerance = 714ps * 0.55 = 392.7ps #

CML output with PoC Jitter: 127ps

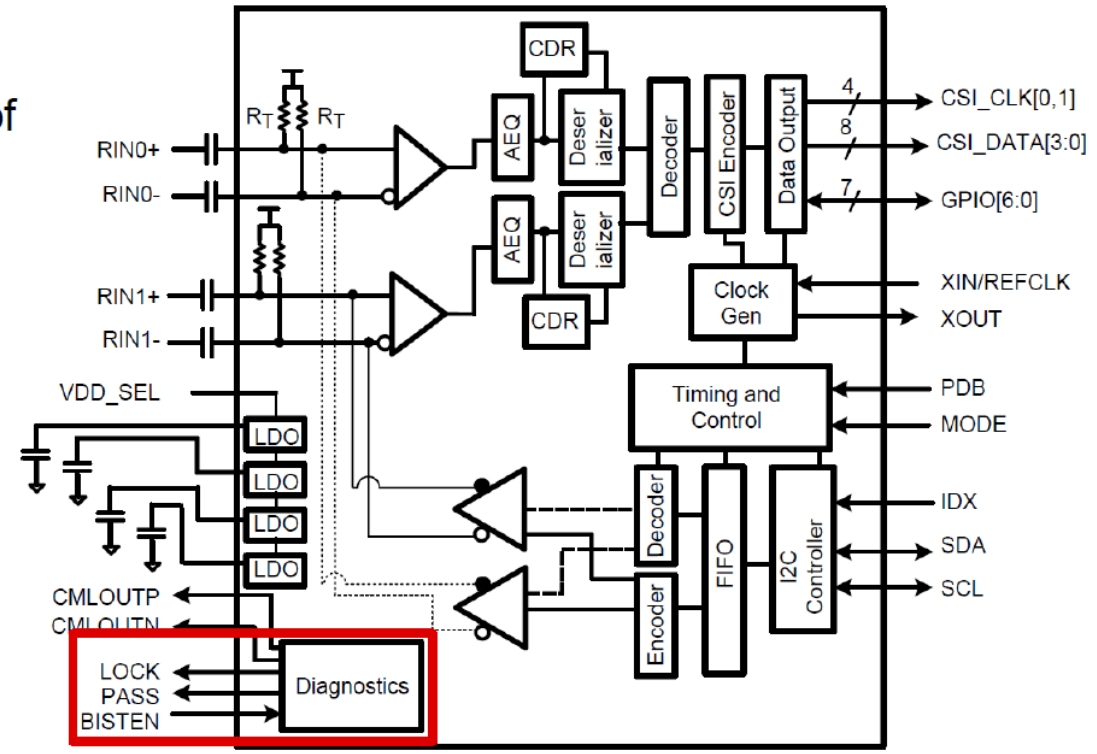
CML output w/o PoC Jitter: 113.8ps

Conclusion: Chipsets with PoC jitter is 127ps which is less than 392.7ps jitter tolerance.

DES is able to lock data.

Built In Self Test (BIST): Definition

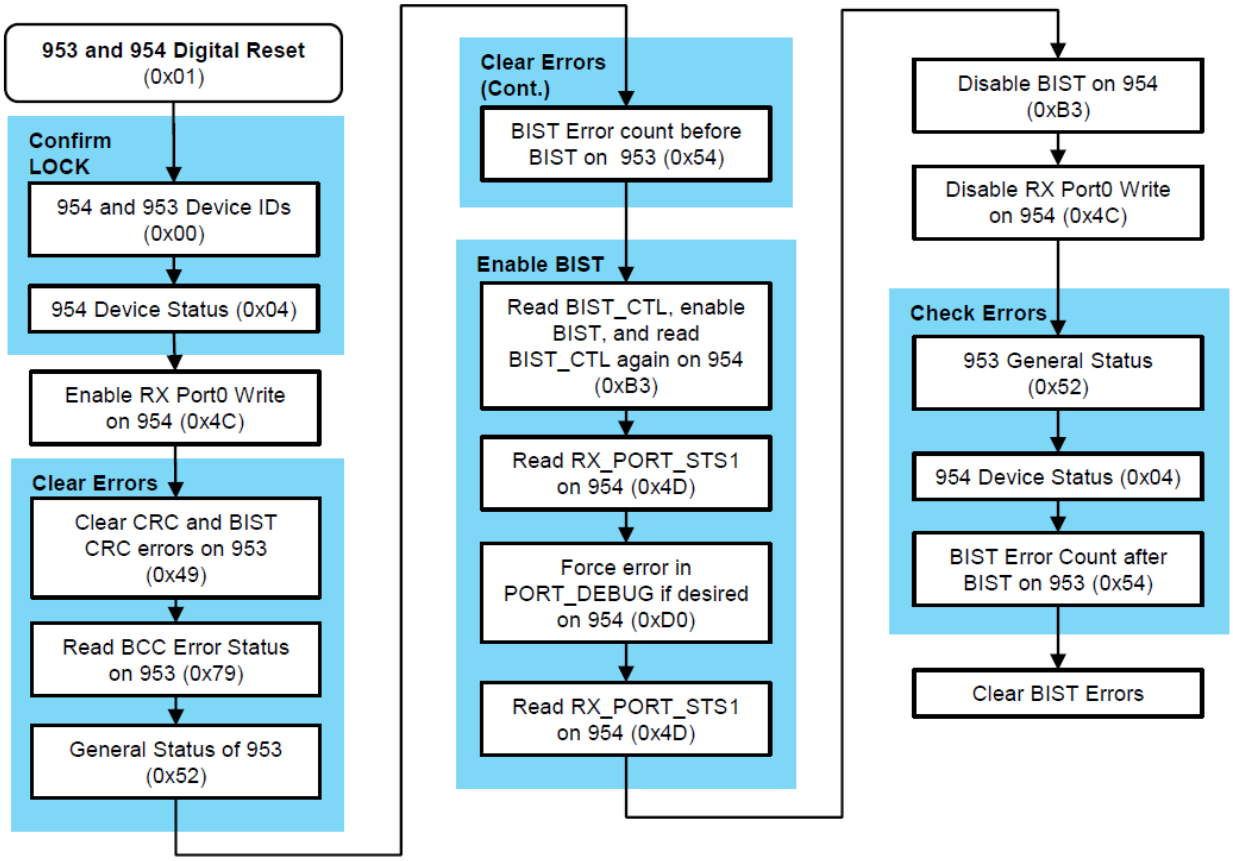
- Definition of BIST:
  - SER outputs continuous stream of a pseudo-random sequence and overrides the BCC.
  - The DES detects the test pattern and monitors it for errors
  - Tests link independently of CSI data
  - BIST checks FC and BC
    - Parity errors = FC errors
    - CRC errors = BC errors



Texas Instruments

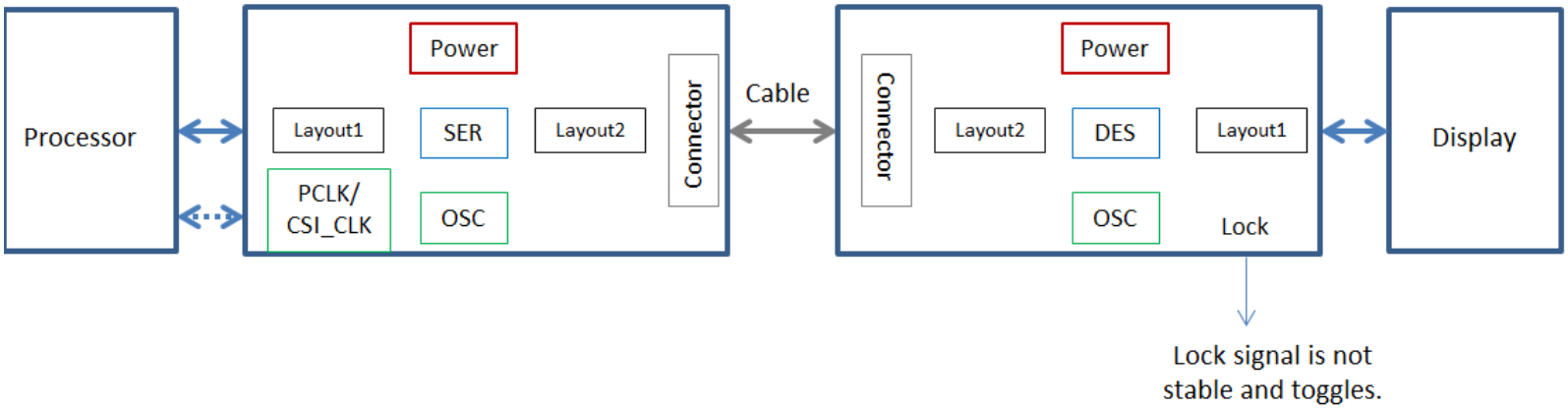
Built In Self Test (BIST): Steps

- Steps for BIST:
  - Digitally reset 953 and 954
  - Confirm Lock between devices
  - Clear any previous errors
  - Enable BIST
    - Force errors if necessary
  - Check for errors
    - Refer to flowchart



Texas Instruments

FPD-LINK Fault Analysis



Possible root causes for lock not stable problem:

1. No length matching at Layout 1
2. Power ripple at DES
3. Oscillator exceeding jitter
4. Connector impedance insufficient causing return loss too high
5. Cable return loss and insertion loss
6. PoC inductor impedance insufficient causing return loss too high(ADAS product)
7. AC coupling capacitor for line rate
8. Termination resistor
9. Power ripple at SER
10. Pixel clock/ CSI clock jitter

FPD-LINK Fault Analysis

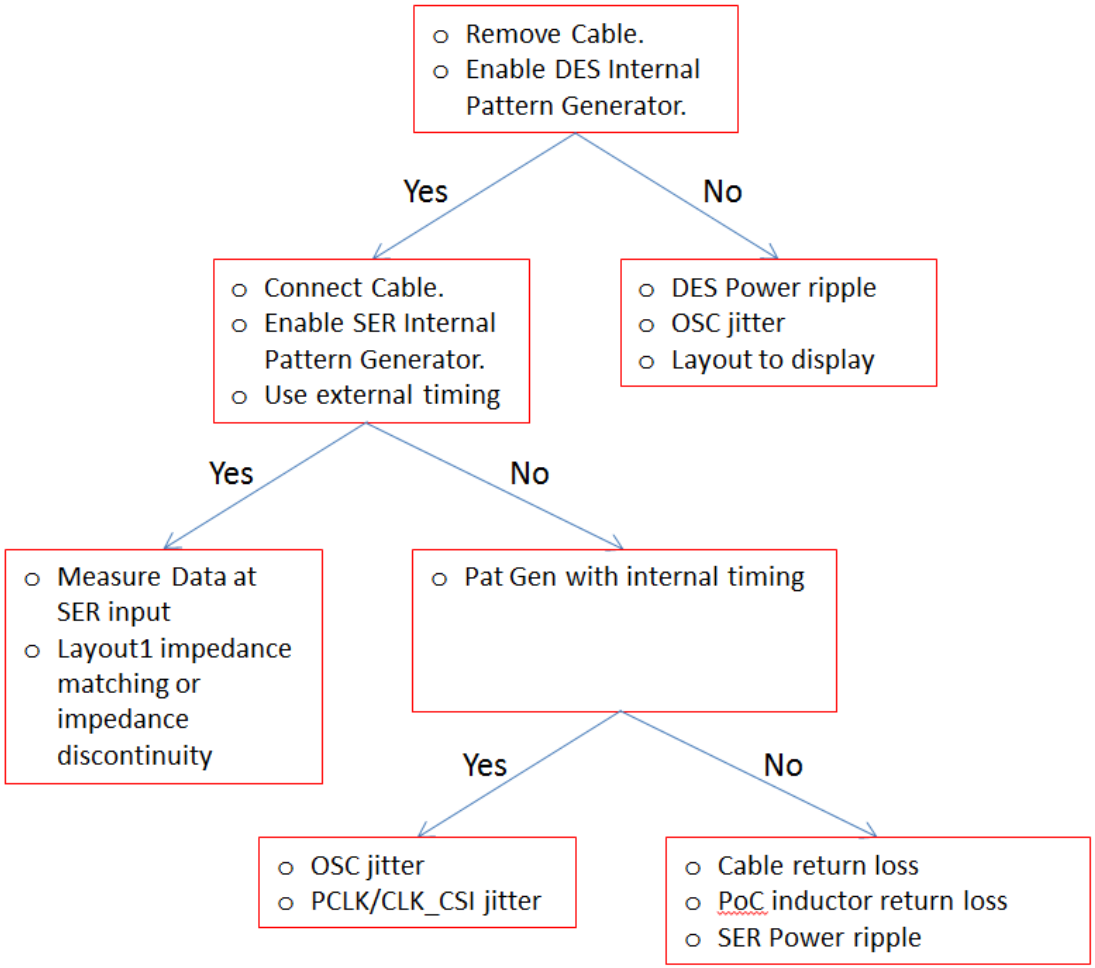


Image Lock: Yes
Image no lock: No

DS90UB953-Q1 and DS90UB954-Q1 TI Training

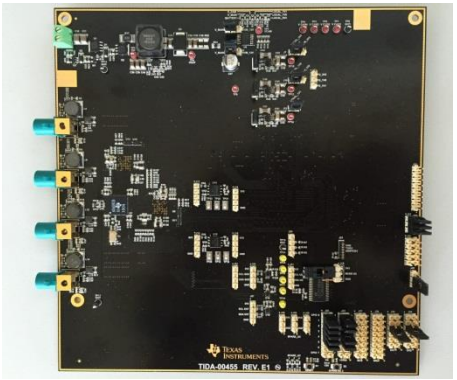
https://training.ti.com/ds90ub953954-system-design-operation

1. DS90UB953/954 System Design & Operation: Overview
2. DS90UB953/954 System Design & Operation: Typical Customer Issues
3. DS90UB953/954 System Design & Operation: Basic Design Rules
4. DS90UB953/954 System Design & Operation: 953-954 Link Design
5. DS90UB953/954 System Design & Operation: Sensor-953 Link Design
6. DS90UB953/954 System Design & Operation: 954-ISP/SoC Link Design
7. DS90UB953/954 System Design & Operation: Hardware Design

ADAS FPD-Link Reference Designs

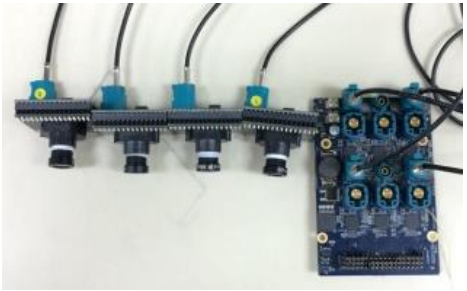
TDA Ruggedized Video Processor (RVP)

- Performs CMS, SVS, stereo cam, mono cam+ RADAR fusion, & other applications
- TDA3x or TDA2x +DS90UB960
- Supports Aptina, OVT, & Sony sensors
- Samples NOW



TIDA-00455 SVS Reference Design

- OV10640+DS90UB964+ OV490
- TDA2xx processor
- Call TI for info

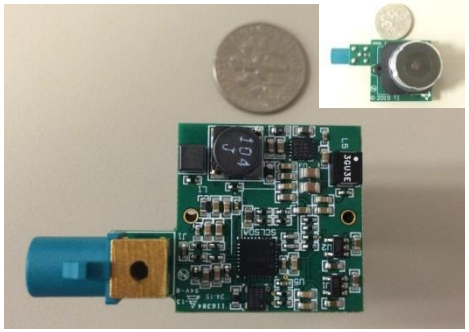


TIDA-00162 Multi-Camera System

- Supports up to 6 cameras
- OV10635+DS90UB913A/914A
- FMC connector plugs into FPGA or MCU board for video processing

TIDA-00421 1.3MP Camera

- OV10640 +DS90UB913A
- TLV702 300 mA LDO
- TPS62170 Buck in 2x2 QFN
- Small 20x20 mm PCB

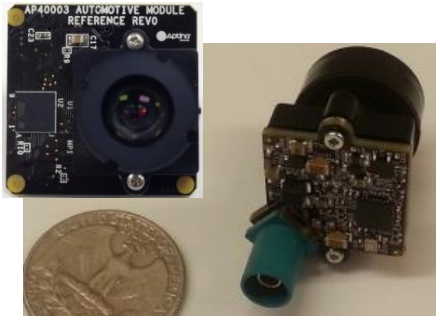


PMP10653 Camera Module

- OV10640+DS90UB913A
- Wide-Vin LM53603Q1 DC/DC
- High PSRR LDO LP5907

PMP9351 Camera Module

- OV10635+DS90UB913Q
- LP3990 linear Vreg



TIDA-00262 1MP Camera

- AR0140AT+DS90UB913A
- TPS3836E18-Q1 220nA Supervisor
- TPS62170-Q1 DC/DC

TIDA-00098 1MP Camera

- AP0101AT+DS90UB913A
- LM34919C, TPS62231 buck regulators

Thank you.

Q&A

Back Up

FPD-LINK Collateral

- What you need to know about high-speed cables for FPD-Link III SerDes (3Q 2017)

http://www.ti.com/lit/an/slyt726/slyt726.pdf

- Cable Requirements for the DS90UB913A & DS90UB914A

http://www.ti.com/lit/an/snla229/snla229.pdf

- How to design remotely-powered cameras for automotive applications(1Q 2017)

http://www.ti.com/lit/an/slyt702/slyt702.pdf

- Sending Power Over Coax in DS90UB913A Designs

http://www.ti.com/lit/an/snla224/snla224.pdf

- Ten tips for successfully designing with automotive EMC/EMI requirements(3Q 2015)

http://www.ti.com/lit/an/slyt636/slyt636.pdf

- I2C over DS90UB913/4 FPD-Link III with Bidirectional Control Channel

http://www.ti.com/lit/an/snla222/snla222.pdf