LLC Converter Operating Principles and Optimization for Transient Response

High Voltage Power

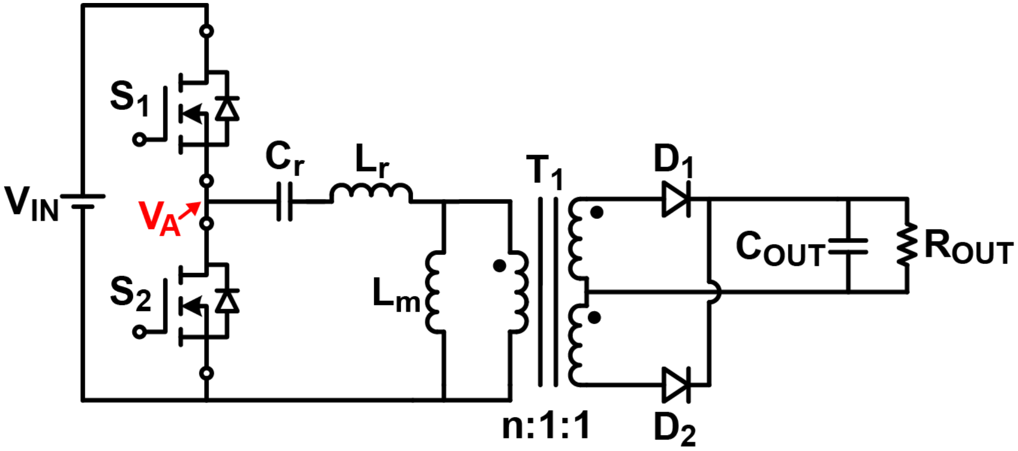
High Voltage Controllers

Agenda

- LLC Converters: Topology Benefits and Example Applications
- Basic Operating Principle
- LLC Power Stage Design Example
- Direct Frequency Control vs Hybrid Hysteretic Control
- Transient Response Considerations
- Test Results

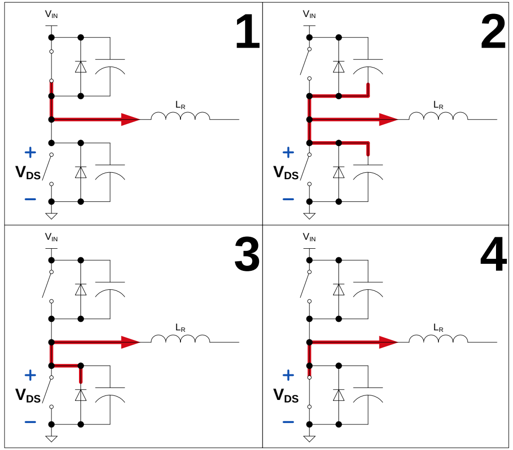
LLC Topology Benefits

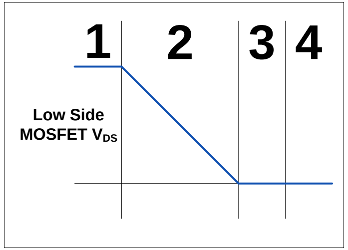
- Soft switching over entire load range
- Reduced EMI signature (sinusoidal primary current)
- Efficiency of ~93% to 96% realizable
- Easy Magnetics integration



ZVS Switching

- Zero volt switching achievable when there is enough circulating current in the LLC power stage
- At gate turn-off, circulating current discharges the switch node capacitance
- Switch node must fully discharge during the dead time before the next gate turn-on
- ZVS greatly reduces switching losses and minimizes EMI





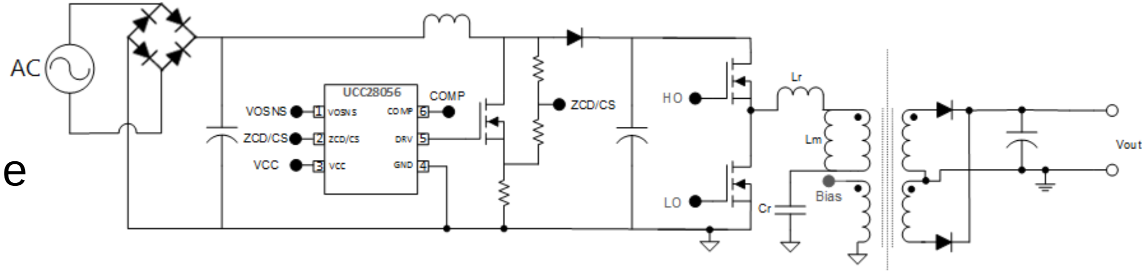
LLC Common Applications

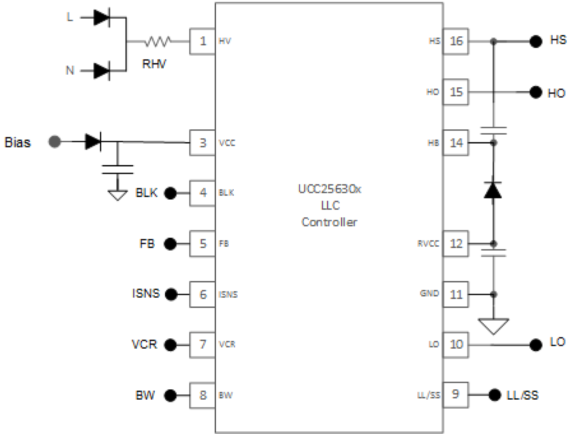
- Common Design Characteristics
  - Narrow, High voltage input
    - PFC input (~400V)
    - Low line input (85V to 120V)
    - High line input (190V to 265V)
  - Output Power
    - 100W to 1kW
    - High Efficiency Desired (~93% to 96%)
- Common Applications
  - OLED/LED TV
  - All-In-One (AIO) Power
  - AC Adapter
  - Projector

~100W – 1000W

Example Application

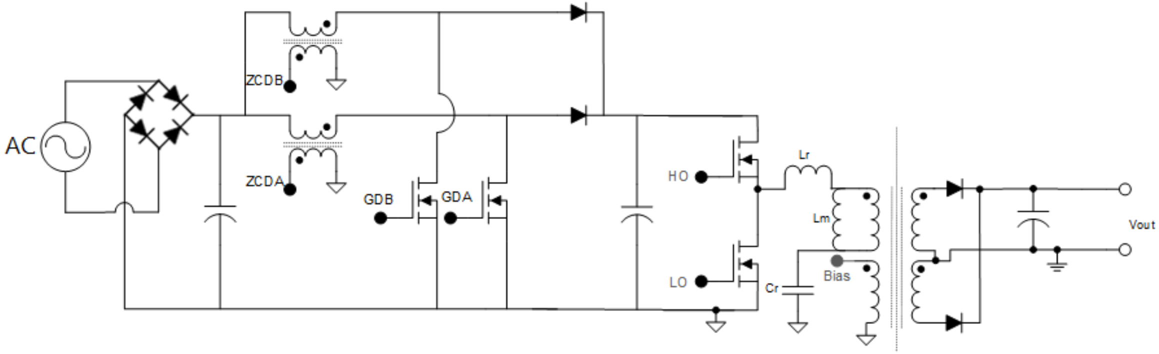
- UCC28056 + UCC25630x
- Single Phase Transition Mode PFC + LLC
- Up to 300W
- System architecture minimizes number of high voltage dividers
  - maximizes efficiency across entire load range

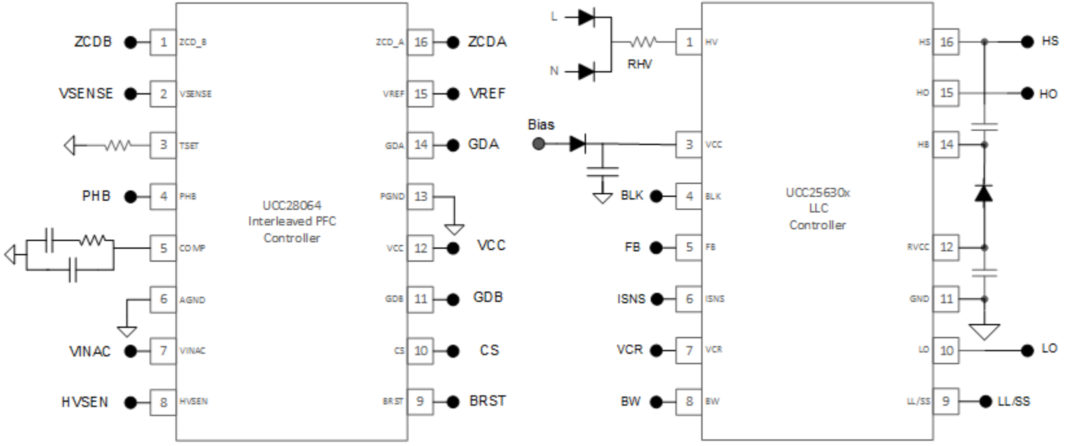




Example Application

- UCC28064 + UCC25630x
- Interleaved Transition Mode PFC + LLC
- Greater than 300W
- Low profile designs
- High light load efficiency via phase shedding





PFC + LLC System Level Considerations

UCC28056

- 75W to 300W
- Very low standby power
- enables systems to meet energy standards while keeping PFC on during standby
  - Greatly simplifies power architecture
- No AUX winding required for zero cross detection

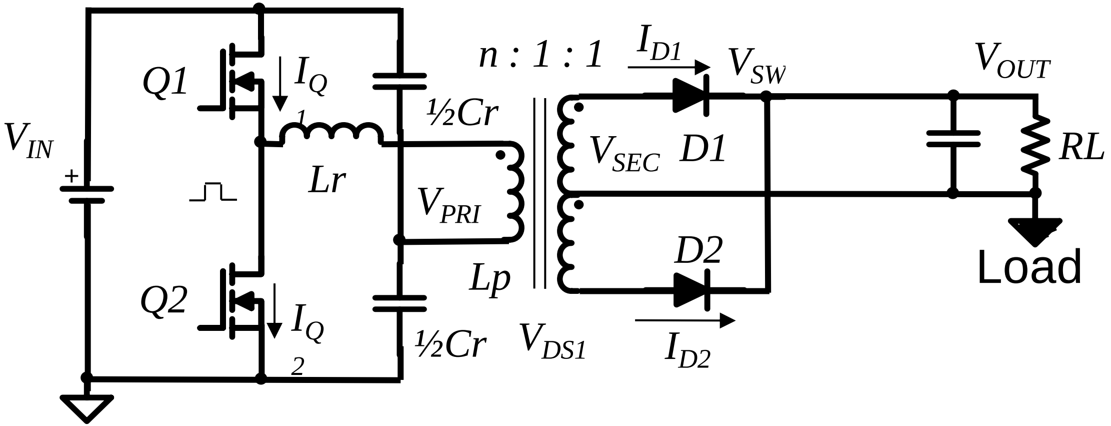
UCC28064

- 300W to 700W
- Reduced current ripple – higher system reliability
- User adjustable phase management and burst mode threshold to achieve low standby power
- Soft burst-on and burst-off avoids audible noise

LLC Operating Principle

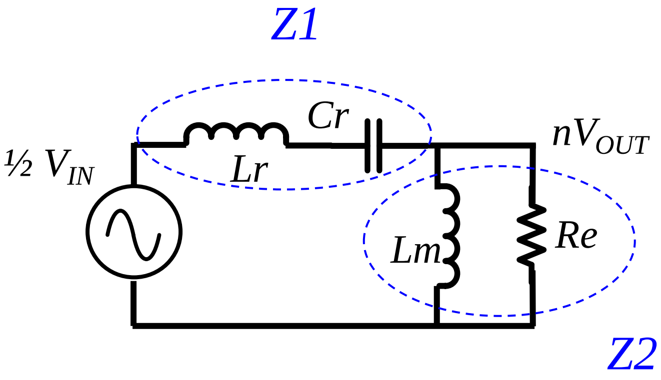
LLC Operating Principle

- Lr, Cr, Lp and reflected RL forms an impedance divider
- Complex Gain Equation
- Gain varies by varying frequency.
- LLC operates at a fixed 50% duty cycle



LLC Operating Principle

- Lr, Cr, Lp and reflected RL forms an impedance divider
- Gain varies by varying frequency
- Q1 and Q2 always operating at 50% duty cycle
- Regulation achieved by modulating switching frequency

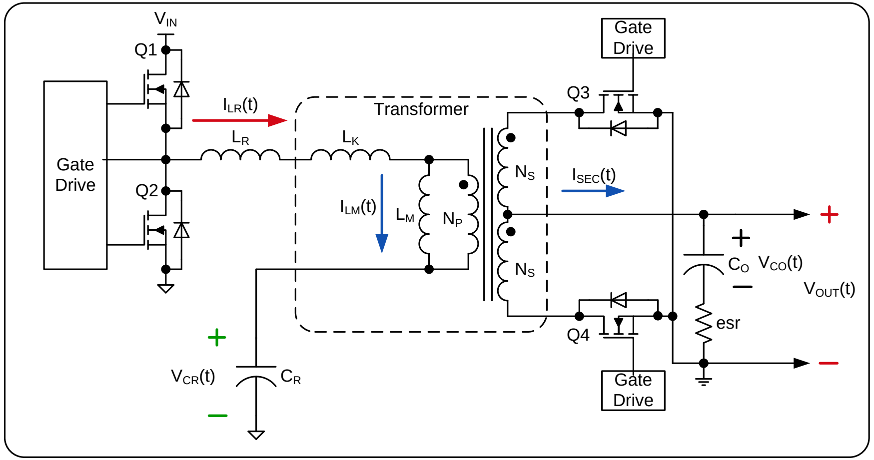


$$Z_1 = 2\pi F \times L_r + \frac{1}{2\pi F \times C_r}$$

$$Z_2 = \frac{2\pi F \times L_m \times R_e}{2\pi F \times L_r + R_e}$$

$$V_{OUT} = \frac{Z_2}{Z_1 + Z_2} = \frac{V_{IN}}{2n}$$

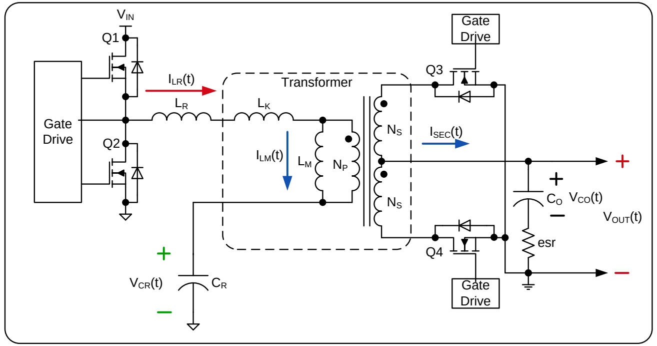
LLC Operating Principle



State	Q1	Q2	Q3	Q4
1	ON	OFF	OFF	ON
2	ON	OFF	ON	OFF
3	ON	OFF	OFF	OFF
4	OFF	ON	OFF	ON
5	OFF	ON	ON	OFF
6	OFF	ON	OFF	OFF

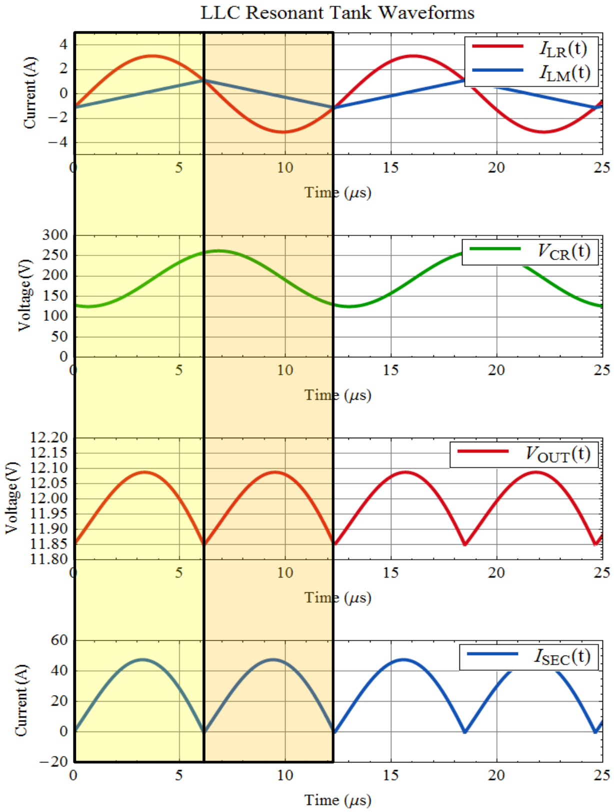
LLC Operating Principle: At Resonance

- When switching frequency is equal to resonant frequency of LLC tank:
  - Two possible states
  - Power stage gain equal to 1



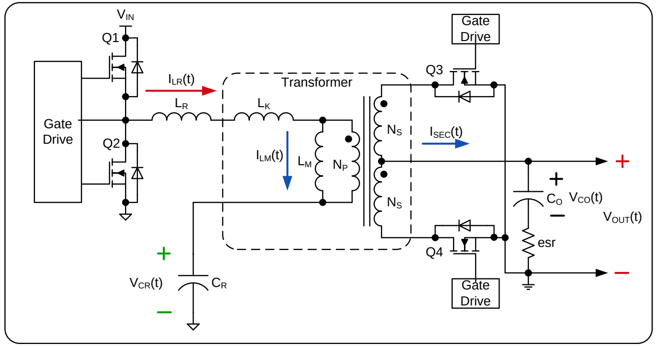
Mode State Sequence: 1→5

State	Q1	Q2	Q3	Q4
1	ON	OFF	OFF	ON
2	ON	OFF	ON	OFF
3	ON	OFF	OFF	OFF
4	OFF	ON	OFF	ON
5	OFF	ON	ON	OFF
6	OFF	ON	OFF	OFF



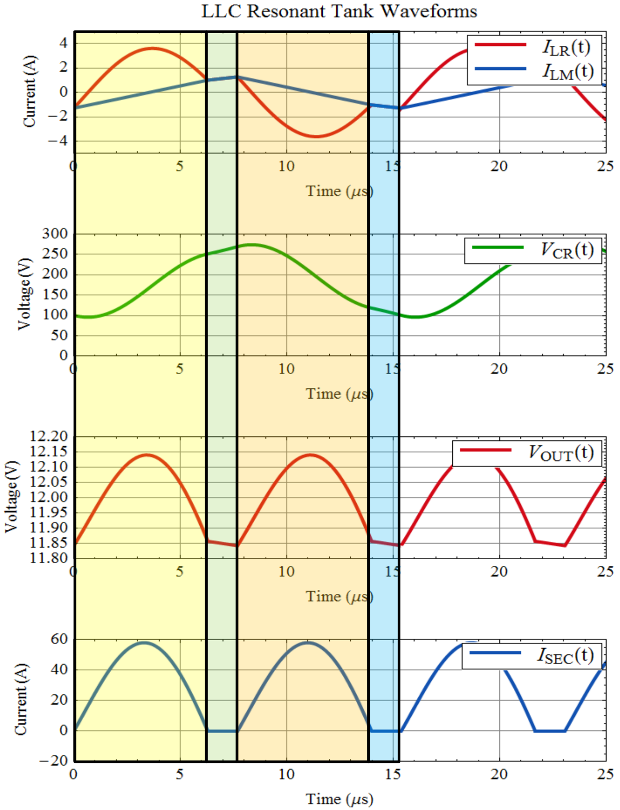
LLC Operating Principle: Below Resonance

- When switching frequency is less than resonant frequency of LLC tank:
  - Four possible states
  - Power stage gain > 1



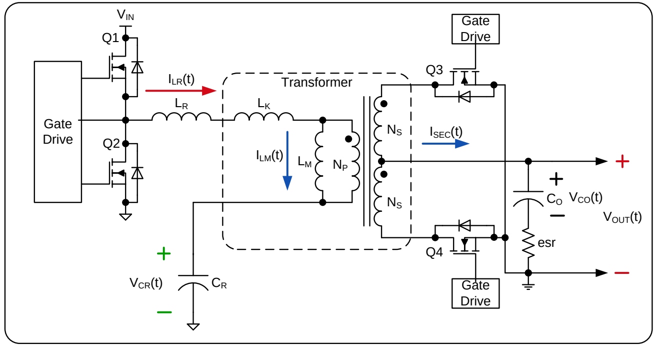
Mode State Sequence: 1→3→5→6

State	Q1	Q2	Q3	Q4
1	ON	OFF	OFF	ON
2	ON	OFF	ON	OFF
3	ON	OFF	OFF	OFF
4	OFF	ON	OFF	ON
5	OFF	ON	ON	OFF
6	OFF	ON	OFF	OFF



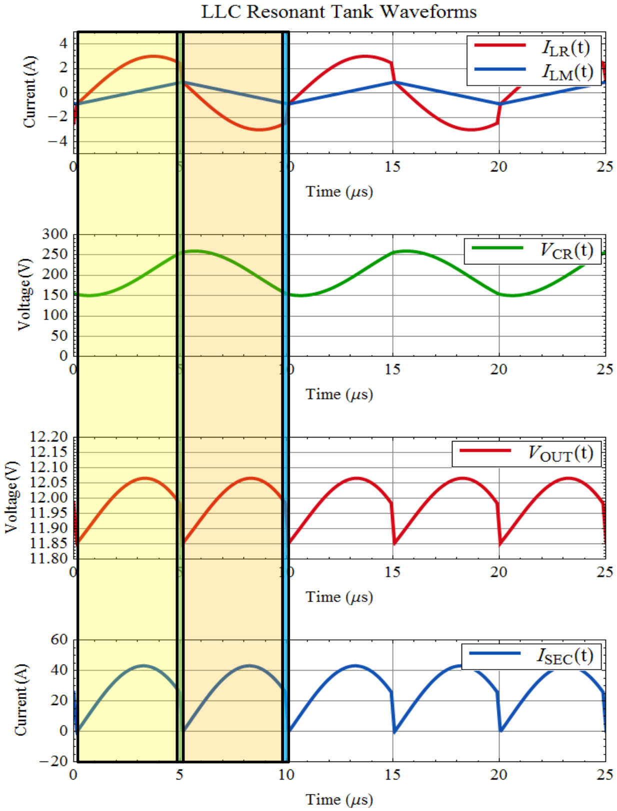
LLC Operating Principle: Above Resonance

- When switching frequency is greater than resonant frequency of LLC tank:
  - Four possible states
  - Power stage gain < 1



Mode State Sequence: 1→4→5→2

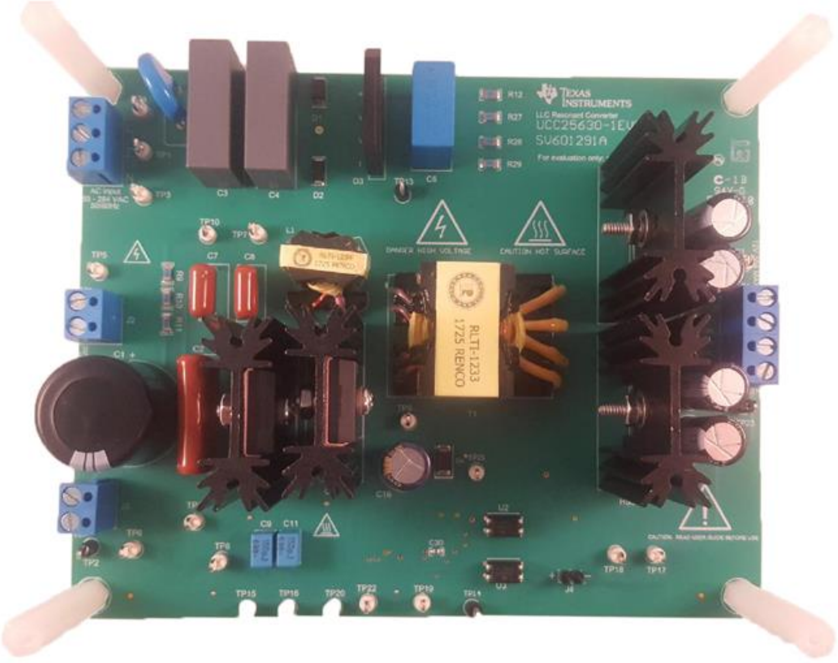
State	Q1	Q2	Q3	Q4
1	ON	OFF	OFF	ON
2	ON	OFF	ON	OFF
3	ON	OFF	OFF	OFF
4	OFF	ON	OFF	ON
5	OFF	ON	ON	OFF
6	OFF	ON	OFF	OFF



LLC Design Example

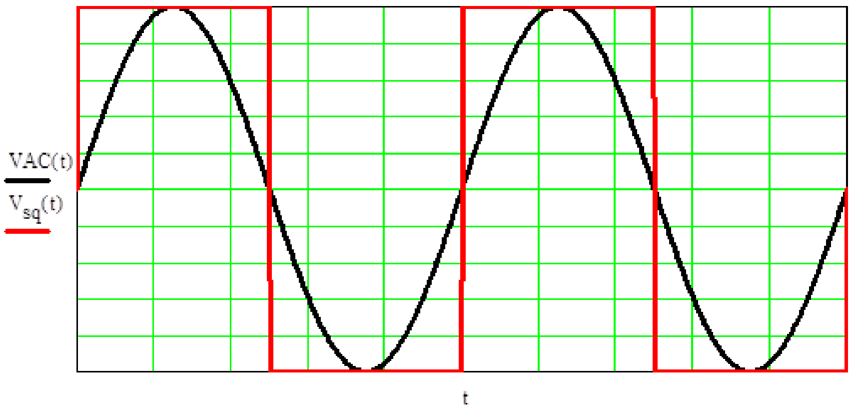
LLC Power Stage Design Example

- Input Voltage Range: 340V to 410V
- Output Voltage: 12V
- Total Output Power: 120W
- Switching Frequency
  - Total Range: 50kHz to 160kHz
  - Resonant Frequency: 100kHz
- Diode Rectification



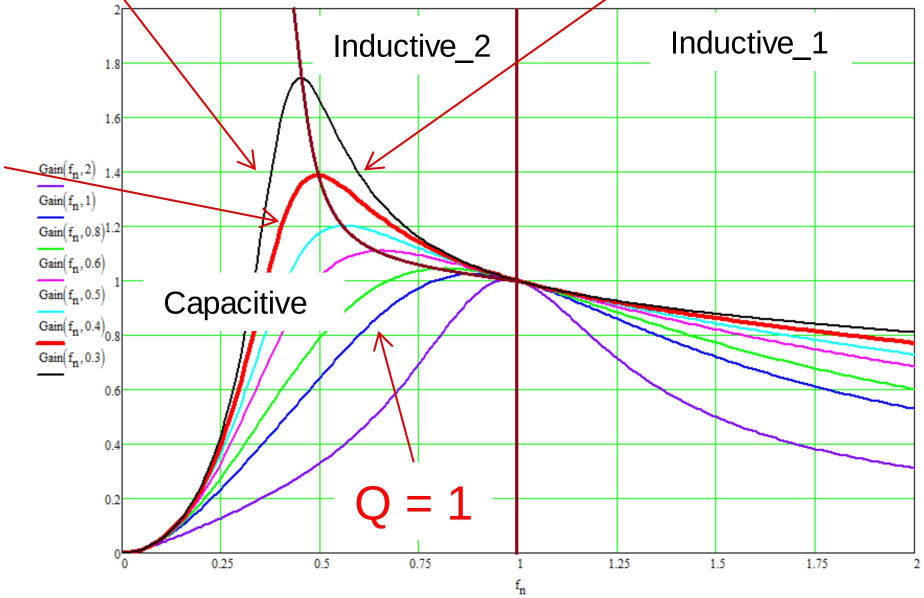
LLC Power Stage: First Harmonic Approximation

- LLC power stage analysis is difficult
  - No easy analytical solution
- First harmonic approximation is common design approach
  - Assumes only the first harmonic of the switching waveform is significant
  - Reasonably accurate close to resonant frequency
  - Increasingly inaccurate as operating point moves away from resonant frequency



LLC Stage: Gain Characteristic

- $Q = (\sqrt{(L_R/C_R)})/R_E$
- Resonant Tank peak gain increases as Q decreases – ie. as load decreases
- ΔG/ ΔF slope changes as switching frequency crosses from Inductive to Capacitive region – AVOID this
  - – Loss of ZVS and control law reversal!
- ZVS is possible in Inductive regions
  - Possible ≠ Guaranteed
- Operate in Inductive regions



ΔG/ ΔF is positive

ΔG/ ΔF is negative

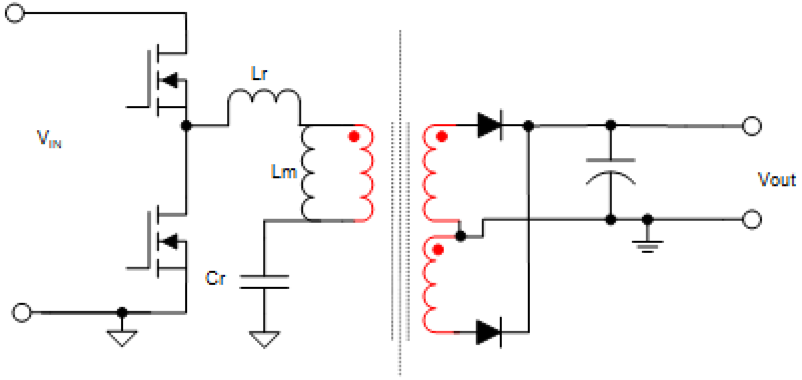
Q = 0.4

Q = 1

LLC stage gain vs normalised resonant frequency with Q as a parameter

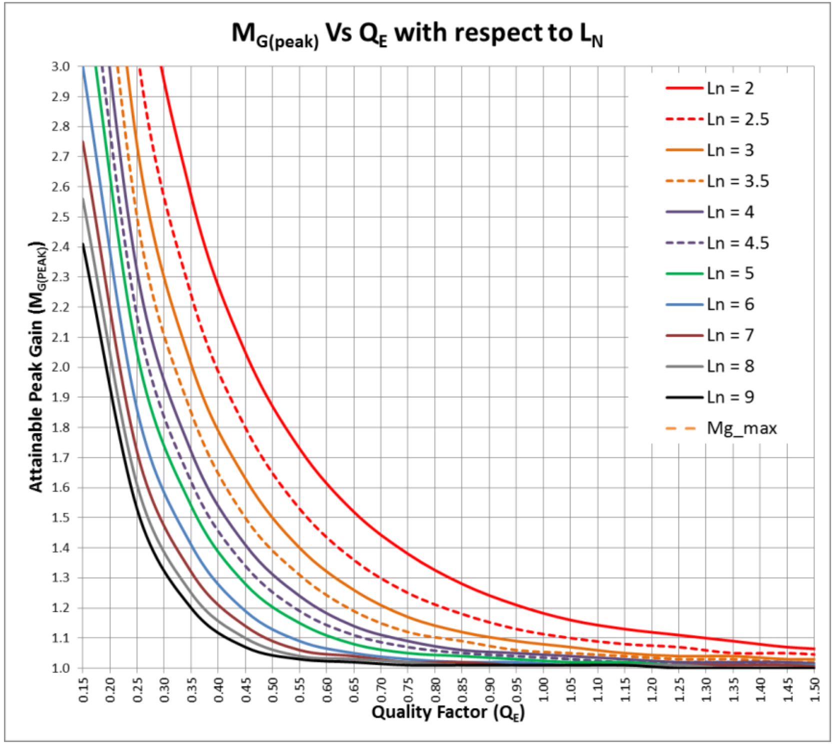
LLC Power Stage Design Example: Transformer Turns Ratio and LLC Gain

- Determine Transformer Primary:Secondary Turns Ratio
  - $n = \frac{V_{IN\_nominal}/2}{Vout} = \frac{390/2}{12} = 16.25$
  - Turns ratio selected as 16
- Determine LLC power stage gain range
  - $M_{g\_min} = n\frac{V_{out}+V_{f\_diode}}{V_{IN\_max}/2} = 16\frac{12+0.5}{410/2} = 0.976$
  - $M_{g\_max} = n\frac{V_{out}+V_{f\_diode}+V_{loss}}{V_{IN\_min}/2} = 16\frac{12+0.5+0.5}{340/2} = 1.224$



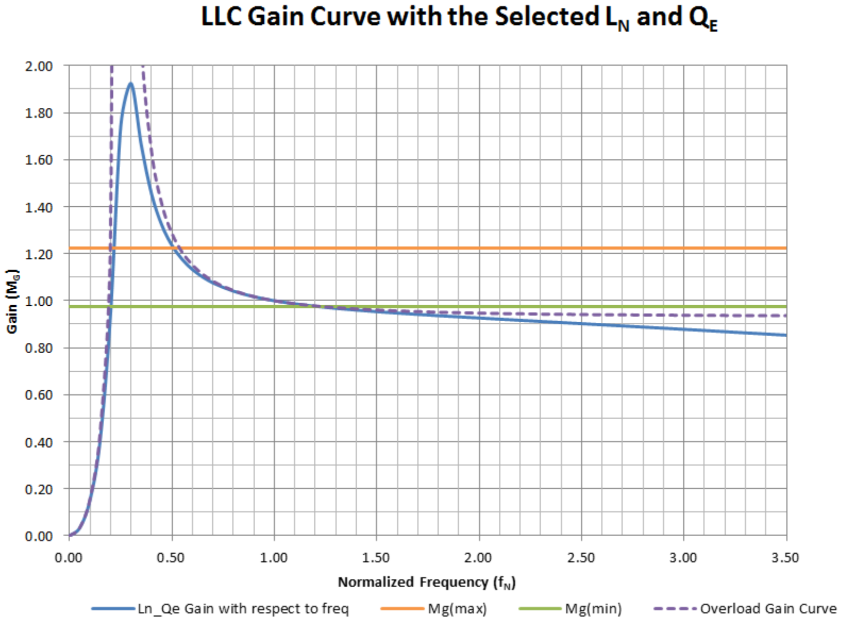
LLC Power Stage Design Example: LLC Tank Parameters

- Calculate equivalent load resistance Re
  - $R_e = \frac{8\times n^2}{\pi^2}\times\frac{V_{out}}{I_{out}} = \frac{8\times 16^2}{\pi^2}\times\frac{12}{10} = 249\Omega$
- Select ratio of magnetizing Inductance to resonant inductance: Ln
  - $L_n = \frac{L_m}{L_r}$
- Select Quality Factor: Qe
  - $Q_e = \frac{\sqrt{L_r/C_r}}{R_e}$
- Goal is to select Ln and Qe from graph so that attainable gain is > Mg_max
  - Ln of 13.5 and Qe of 0.15 selected
- Graph can be obtained from UCC25630x Calculator:
  - http://www.ti.com/product/UCC256302/toolssoftware



LLC Power Stage Design Example: LLC Tank Parameters

- Select resonant capacitance: Cr
  - $C_r = \frac{1}{2\pi \times Q_e \times F_{res} \times R_e} = \frac{1}{2\pi \times 0.15 \times 100kHz \times 249\Omega} = 42.6nF$
  - Use Cr = 44nF
- Select resonant inductance: Lr
  - $L_r = \frac{1}{(2\pi \times F_{res})^2 C_r} = \frac{1}{(2\pi \times 100kHz)^2 44nF} = 57.58\mu H$
  - Use Lr = 61.5µH
- Select magnetizing inductnace: Lm
  - $L_m = L_n \times L_r = 13.5 \times 61.5\mu H = 830.25\mu H$
  - Use 830µH
- Double check actual component values satisfy Mg_peak > Mg_max
  - Having some margin of Mg_peak > Mg_max is needed

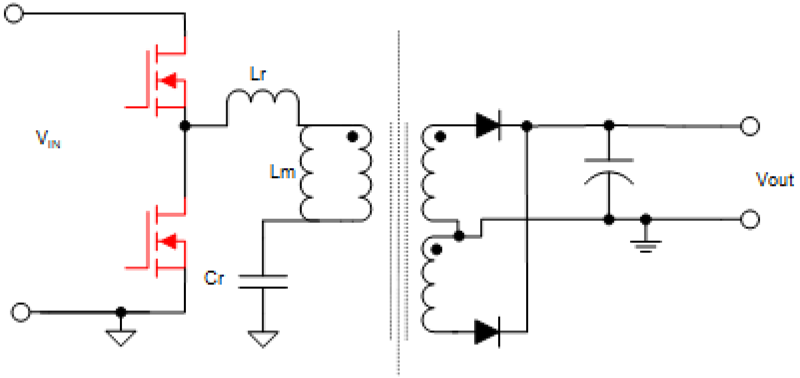

LLC Gain Curve with the Selected L_N and Q_E

FHA Calculation →

$$\mathrm{Gain}(f_n, Q) := \left| \frac{L_n \cdot f_n^2}{L_n \cdot f_n^2 + (f_n^2 - 1) \cdot (1 + j\, f_n \cdot L_n \cdot Q)} \right|$$

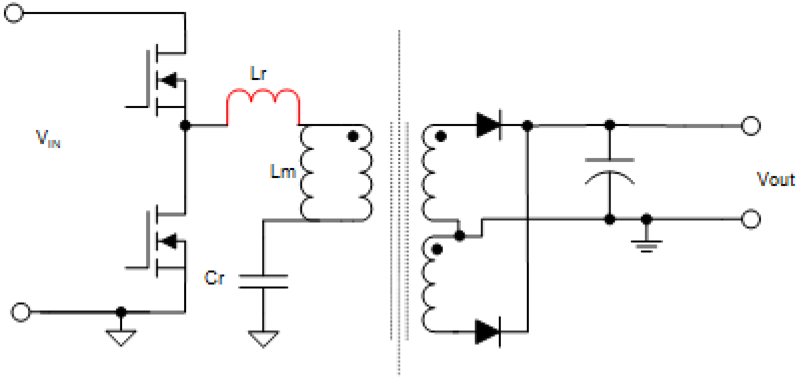
LLC Power Stage Design Example: Primary side MOSFETs

- Select Primary Side MOSFET' based on primary side resonant current and voltage stress
  - Primary RMS current: $I_{oe} = \frac{\pi}{2\sqrt{2}} \times \frac{I_{out}}{n} = \frac{\pi}{2\sqrt{2}} \times \frac{1.1\times 10A}{16} = 0.764\ A$
  - RMS magnetizing current: : $I_m = \frac{2\sqrt{2}}{\pi} \times \frac{n\times V_{out}}{2\pi F_{min\times Lm}} = \frac{2\sqrt{2}}{\pi} \times \frac{16\times 12}{2\pi 50kHz\ \times 830\mu H} = 0.659\ A$
  - Total resonant Current: $I_r = \sqrt{{I_{oe}}^2 + {I_m}^2} = \sqrt{(0.764\ A)^2+(0.659\ A)^2} = 1.01\ A$
  - Choose MOSFET with current rating 1.1 times the total resonant current
  - Max voltage stress each MOSFET sees is equal to the input voltage
    - Choose MOSFET rated to 1.5 times the max input voltage



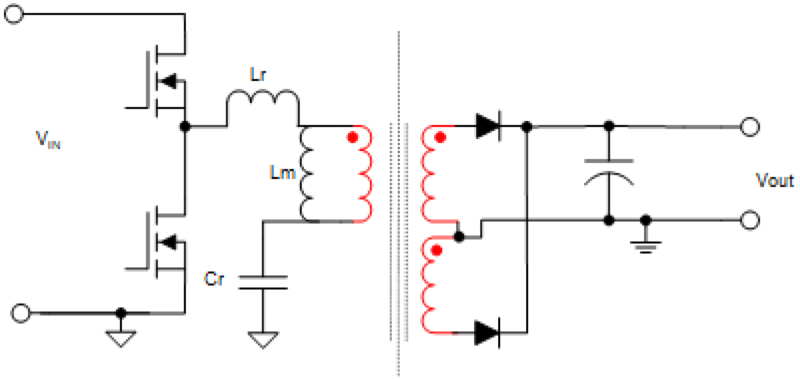
LLC Power Stage Design Example: Resonant Inductor

- Resonant inductor spec
  - Resonant inductance can either be implemented as discrete, external inductor or as the leakage inductance of the transformer (saves space)
  - For external resonant inductor, the maximum AC voltage across inductor is $V_{LR} = 2\pi F_{min} L_R I_R = 19.6V$
  - Complete Spec:
    - Inductance: 61.5µH
    - Rated Current: 1.1A
    - Terminal AC Voltage Rating: 20V
    - Frequency Range: 50kHz to 111kHz



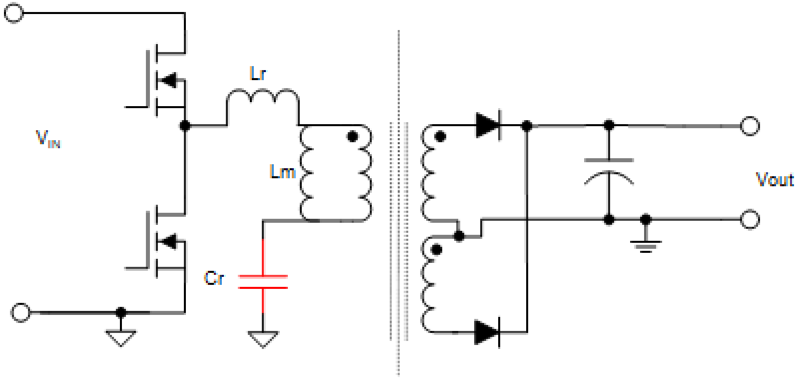
LLC Power Stage Design Example: Transformer

- Calculate secondary side currents
  - $I_{oes} = n \times I_{oe} = 16 \times 0.764\ A = 12.218\ A$
  - Current in each secondary winding:
    - $I_{ws} = \frac{\sqrt{2} \times I_{oes}}{2} = \frac{\sqrt{2} \times 12.218}{2} = 8.639\ A$
- Total Transformer Spec
  - Turns Ratio Primary : Secondary = 32 : 2
  - Primary Magnetizing Inductance: 830µH
  - Primary Winding Current: 1.1 A
  - Secondary Winding Current: 8.639 A
  - Switching Frequency Range: 50kHz to 111kHz



LLC Power Stage Design Example: Resonant Capacitor

- Calculate AC voltage on resonant capacitor
  - $V_{CR\_AC} = \frac{I_r}{2\pi F_{min} C_r} = \frac{1.1\ A}{2\pi \times 50kHz \times 44nH} = 72.5V$
- Calculate peak resonant capacitor voltage
  - $V_{CR\_peak} = \frac{V_{in\_max}}{2} + \sqrt{2} V_{CR\_AC} = \frac{410V}{2} + \sqrt{2} \times 72.5V = 307.5V$

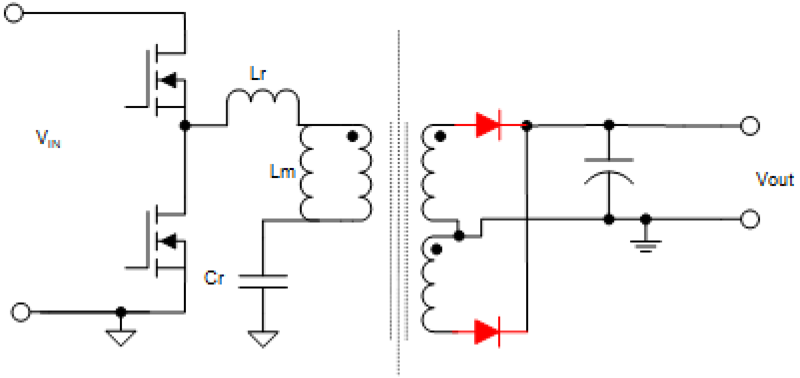


- Total resonant capacitor spec
  - Peak Voltage: 308V
  - Rated Current: 1.1A
  - Low dissipation factor preferred to limit temperature rise in the resonant capacitor

LLC Power Stage Design Example: Rectifier Diodes

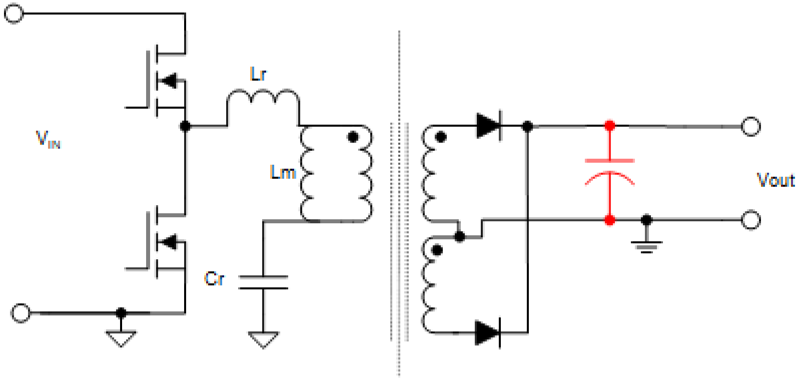
- Calculate half-wave average current
  - $I_{ws} = \frac{\sqrt{2} \times I_{oes}}{\pi} = \frac{\sqrt{2} \times 12.218}{\pi} = 5.503\ A$

- Calculate required voltage stress rating for each diode
  - $V_{DB} = 1.2 \times \frac{V_{IN\_max}}{n} = 1.2 \times \frac{410}{16} = 30.75V$



LLC Power Stage Design Example: Output Capacitance

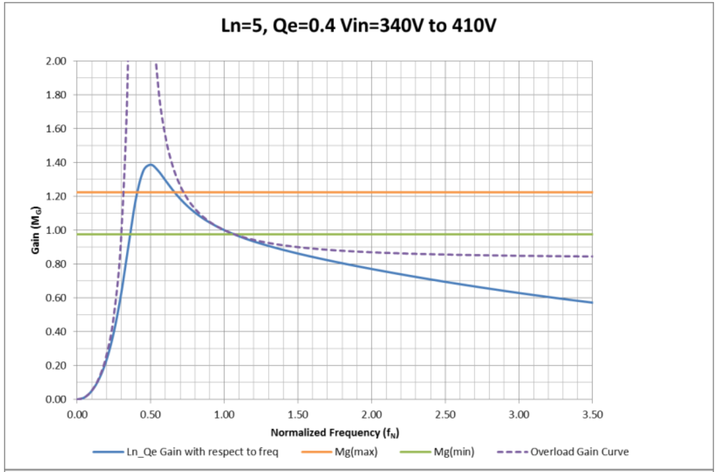
- Required Capacitor RMS Current Rating
  - $I_{Cout} = \sqrt{(\frac{\pi}{2\sqrt{2}} Iout)^2 - Iout^2} = \sqrt{(\frac{\pi}{2\sqrt{2}} 10)^2 - 10^2} = 4.84\ A$
- Max ESR
  - Determined by maximum allowable ripple voltage at steady state
  - $ESR_{max} = \frac{V_{out(pk-pk)}}{\frac{\pi}{2} Iout} = \frac{0.3V}{\frac{\pi}{2} \times 10} = 19m\Omega$
- Larger ESR results in more heat, reduced capacitor lifetime and larger output ripple

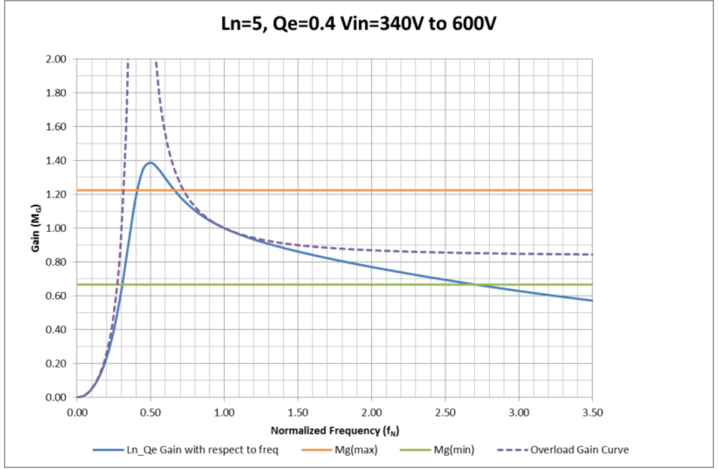


LLC Design Considerations

Why is Narrow Input Voltage Preferred?

- Min and Max input voltage determines necessary gain range
- Larger input voltage range results in larger required power stage gain range
- Operating point move further away from resonant frequency
  - Poor efficiency!
- FHA becomes less reliable
- Greater possibility for converter to operate in capacitive region and zero current switching
  - Avoid this

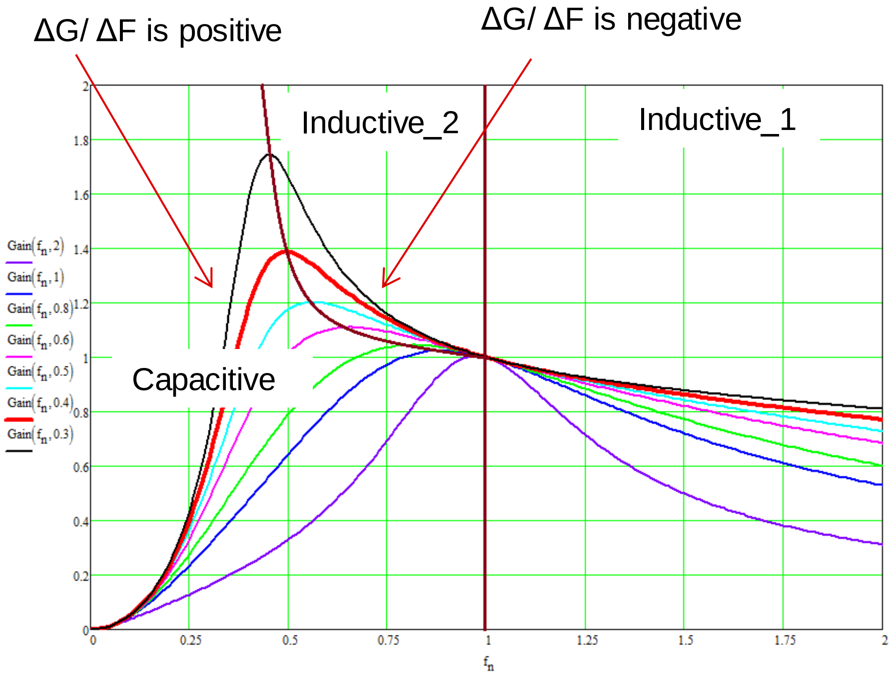

Ln=5, Qe=0.4 Vin=340V to 410V


Ln=5, Qe=0.4 Vin=340V to 600V

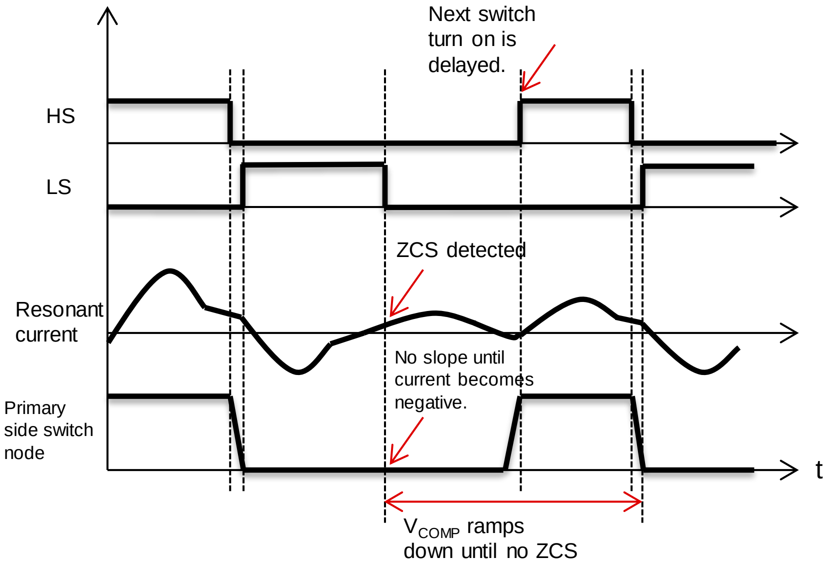
ZCS Avoidance

- ZCS leads to conduction of body diode in primary side MOSFETs
  - Large dI/dt spike
  - Greater stress on primary side MOSFETs and probability of damage greatly increases

- Gain-Frequency relationship becomes inversed



ZCS Avoidance

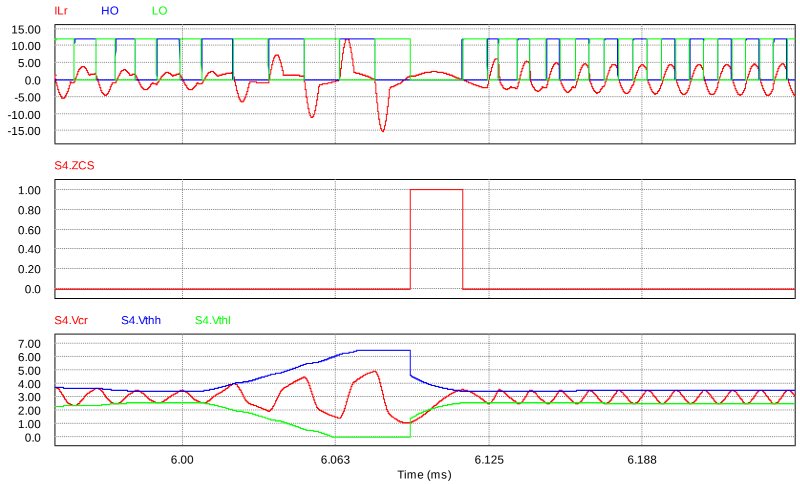


Next switch turn on is delayed.

ZCS detected

No slope until current becomes negative.

V_{COMP} ramps down until no ZCS



- UCC25630x algorithm incorporates ZCS avoidance
- Polarity of the inductor current is sensed at gate turn off edge
- ZCS is detected if at HS or LS turn off edge, the direction of the resonant current (Ipolarity) is not correct
- HS or LS switch will not be turned on until the next slew is detected on primary side switch node.
- Vcomp will be rapidly ramped down until there a complete switching cycle without a near ZCS event is detected.

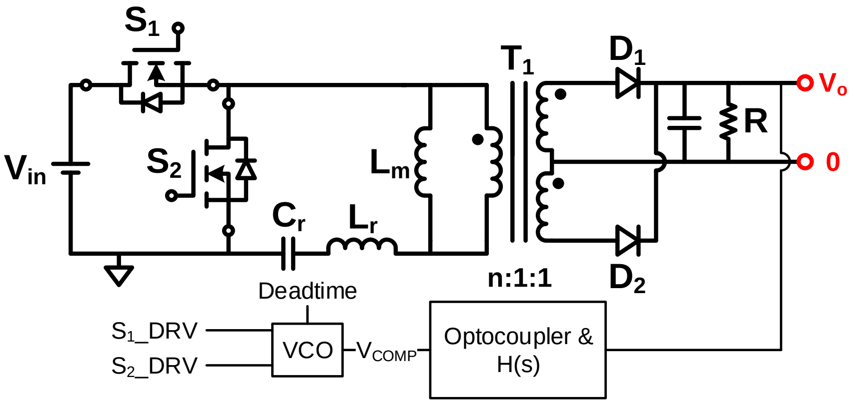
Direct Frequency Control vs Hybrid Hysteretic Control

Direct Frequency Control (DFC)

- Analogous to voltage mode control

- Limited bandwidth and slow transient response

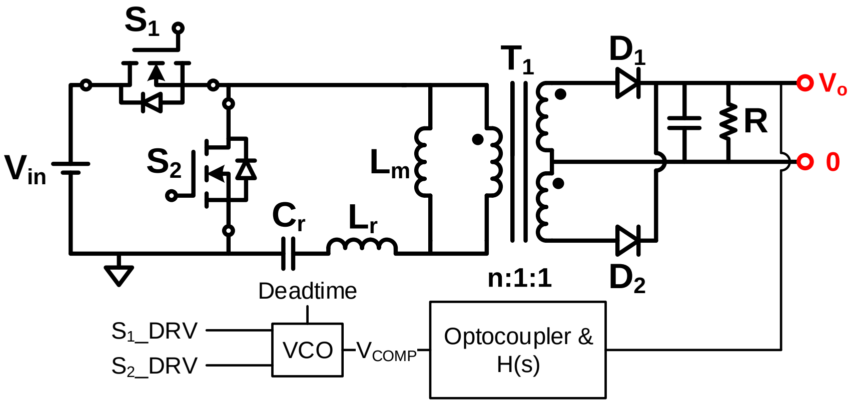
- Complex power stage transfer function



Direct Frequency Control (DFC)

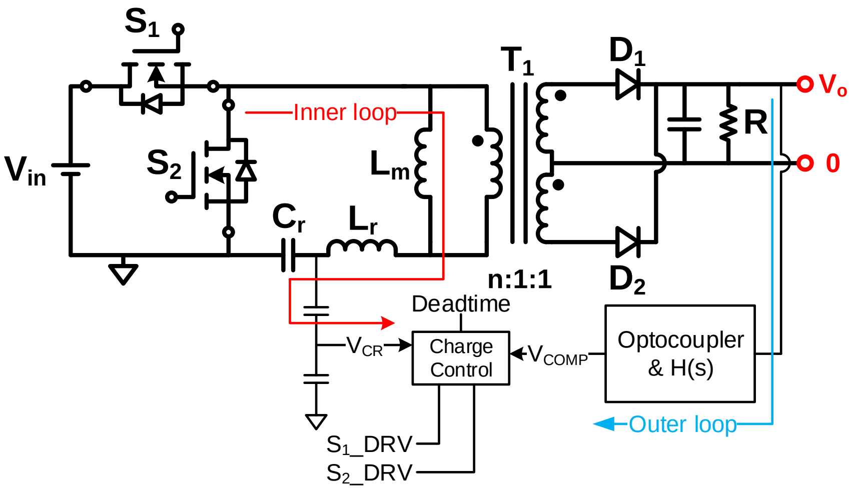
- Power stage transfer function difficult to express analytically

- Compensation strategy is typically begin with integrator and increase bandwidth if enough phase margin is available



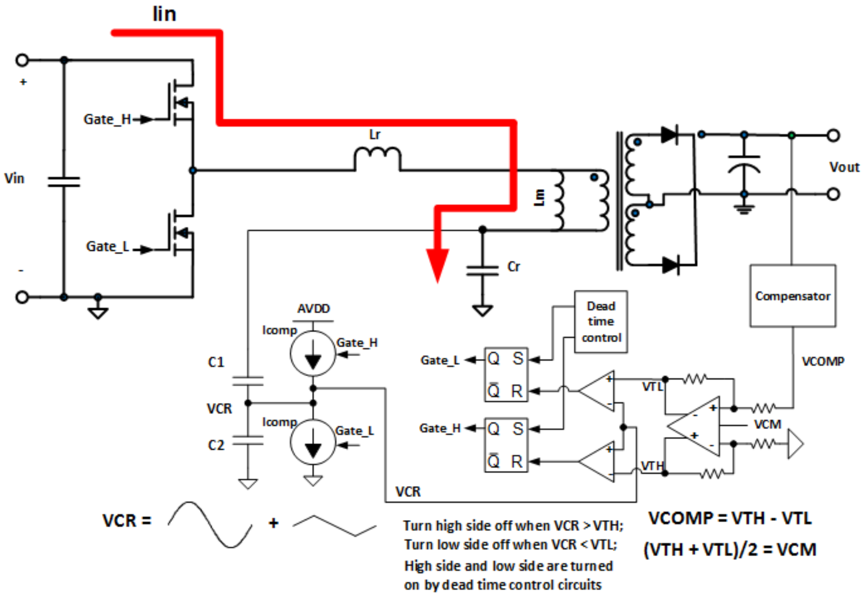
Hybrid Hysteretic Control (HHC)

- Charge control with added frequency compensation ramp
- Analogous to current mode control with added slope compensation
- 1st order power stage transfer function
- Higher bandwidth and fast transient response



Hybrid Hysteretic Control (HHC)

- HHC operating principle
- Gate turn off thresholds (VTH and VTL) are derived from feedback
- Gate turn off determined by comparing VCR to VTH and VTL
- Gate turn on determined by adaptive dead time circuit



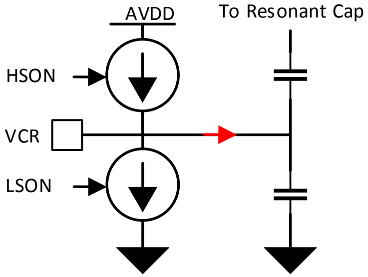
Turn high side off when VCR > VTH;
Turn low side off when VCR < VTL;
High side and low side are turned on by dead time control circuits

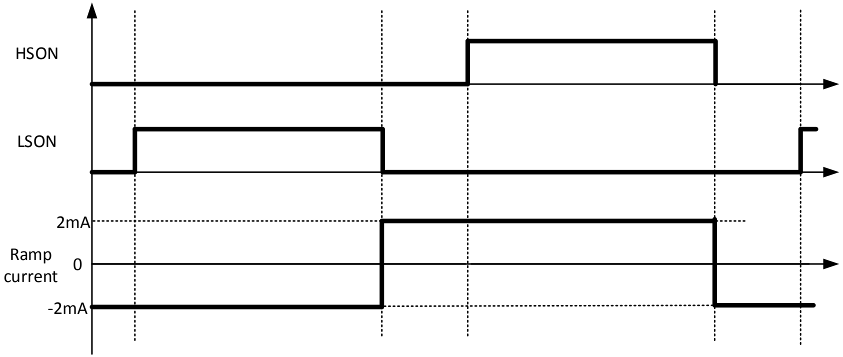
VCOMP = VTH - VTL

(VTH + VTL)/2 = VCM

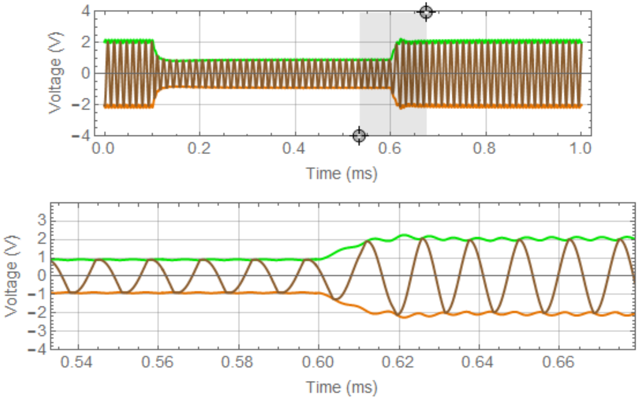
Hybrid Hysteretic Control (HHC)

- Current sources on/off control synchronous to gate signal turn off edge
- Inherent negative feedback for low side and high side gate signal balance
- Automatically maintain the bias voltage at 3V – **<u>no need for extra resistor dividers</u>**
- Current sources are turned off during burst off period – **<u>reduce standby power consumption</u>**

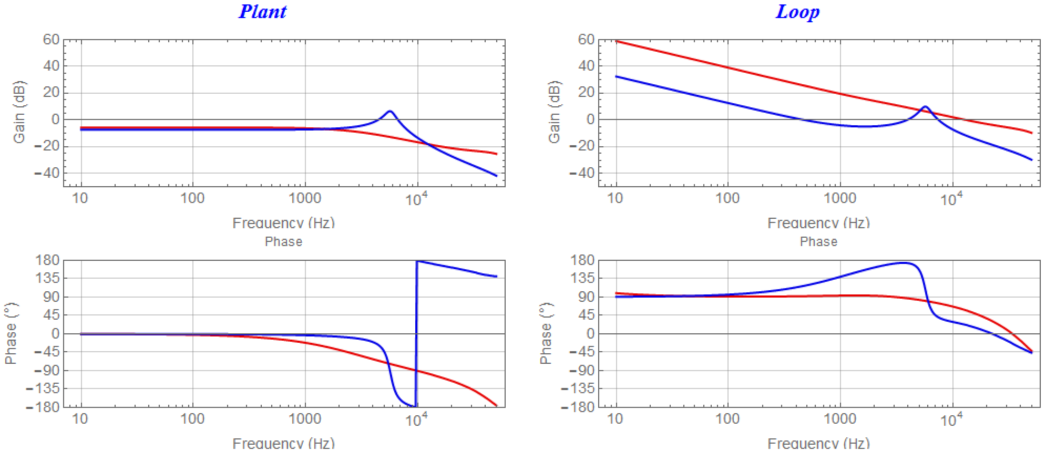




Hybrid Hysteretic Control (HHC)



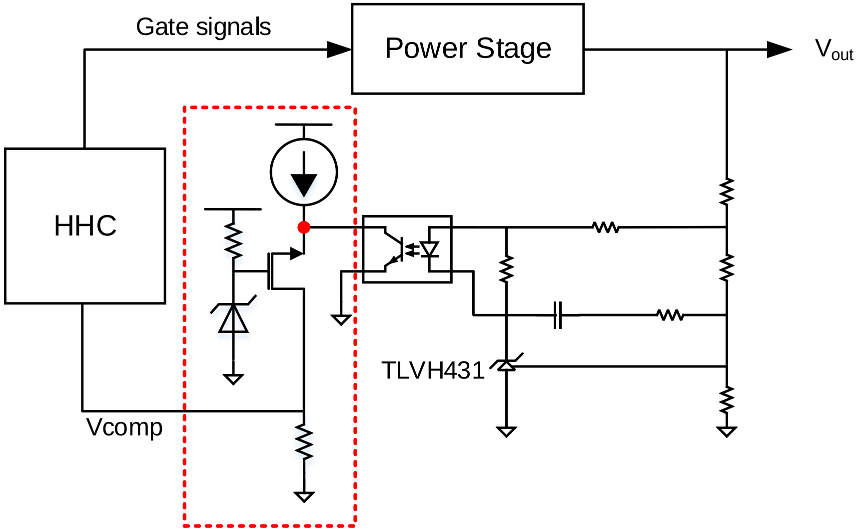
- ~1st order system
- Able to achieve higher bandwidth



— Frequency control — HHC

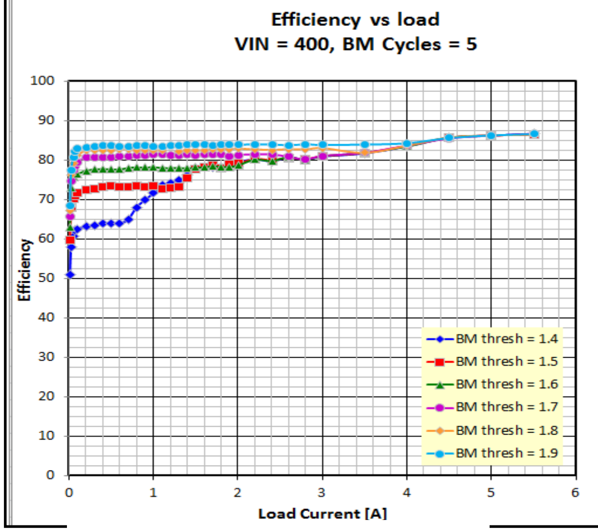
Hybrid Hysteretic Control (HHC)

- Optocoupler collector voltage regulated at a constant voltage
- No extra pole introduced due to the optocoupler parasitic capacitor
  - **<u>Higher loop bandwidth and fast transient</u>**
- Small bias current (82uA) is used to limit the optocoupler current at light load
  - **<u>Low standby power consumption</u>**

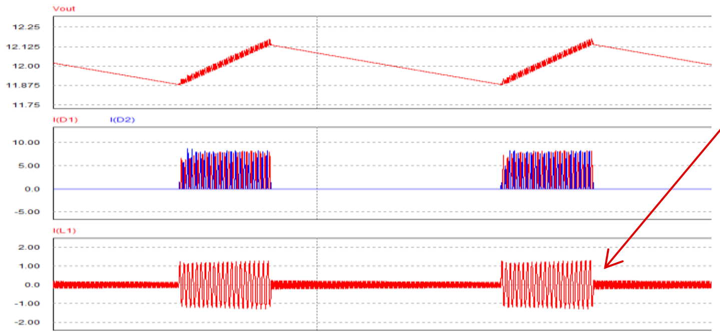


HHC: Burst Mode Control

- Advanced burst mode
  - Converter operates at the operating point with the highest efficiency during the burst period
  - Burst mode threshold tunable through external resistors

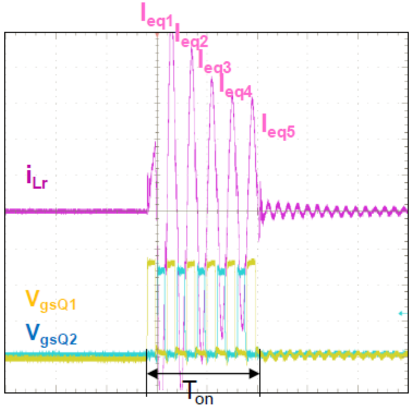


Efficiency vs. load for different V_{IN} with different BM threshold setting

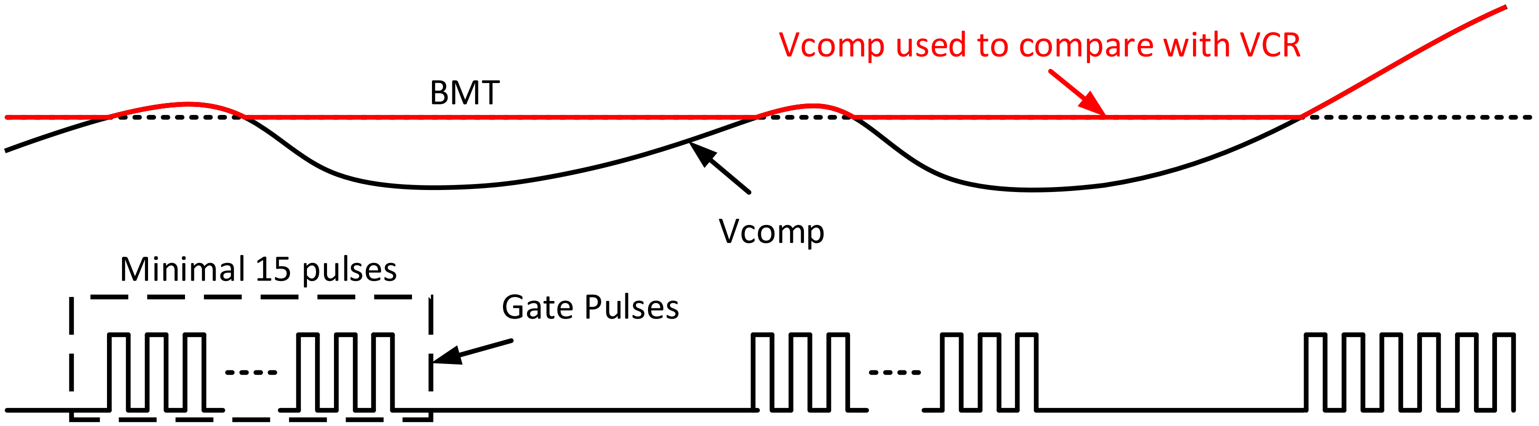


UCC25630x: I_{res} stays at optimal efficiency operation condition in every switching cycle

Conventional solution: I_{res} is not optimized



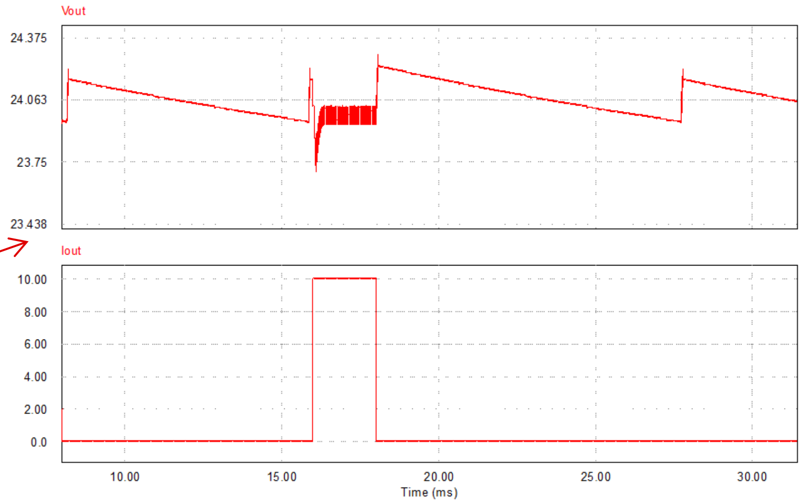
HHC: Burst Mode Control



- Burst mode allows system to turn on for a minimal of 15 switching pulses and turn off for a longer time to improve the light load efficiency – **Low standby power consumption**
- The higher value of Vcomp and burst mode threshold (BMT) is used to compare with VCR for pulse generating guarantee a fast transient from light load/no load to full load – **Fast transient**

HHC: Burst Mode Control

- Fast exit from burst mode without large V_{OUT} dip
  - No need for secondary side wake up circuit



Load step between 0.5% load and full load. V_{OUT} dip is ~100 mV

HHC Benefits

Fast Transient Response

- HHC simply plant to ~1st order system, allowing for a higher system bandwidth
- Innovated feedback chain removes extra pole introduced by the optocoupler parasitic capacitor
- Burst mode implementation allow the system to get out of burst mode fast, to guarantee for a fast transient from light load to heavy load

Low Standby Power Consumption

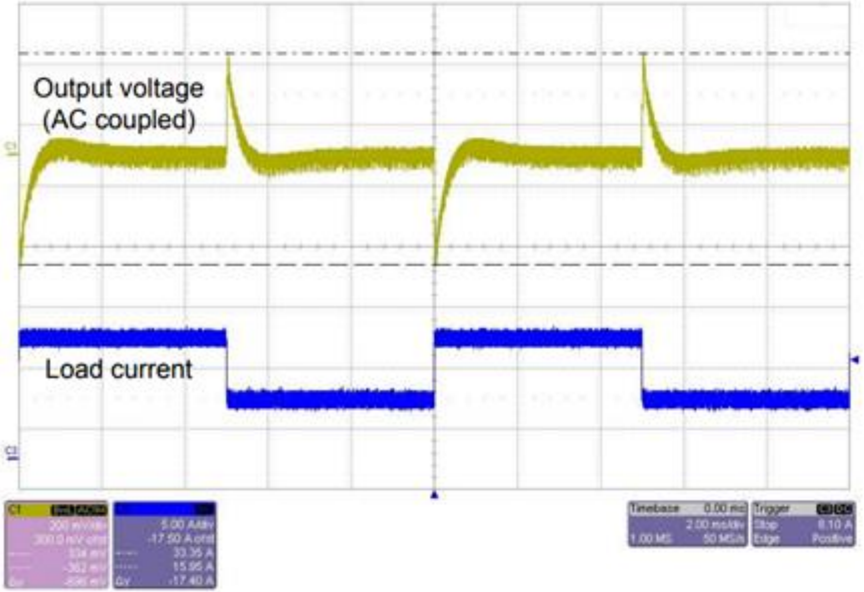
- Slope compensation remove the need for extra resistors to maintain the dc bias voltage on VCR
- Low optocoupler bias current helps to achieve a low standby power consumption on feedback loop
- Burst mode improve the light load efficiency by turning off the switching for certain period

LLC Transient Response

Load Transient Response

- Performance metric describing the power supply’s response to sudden change in load current

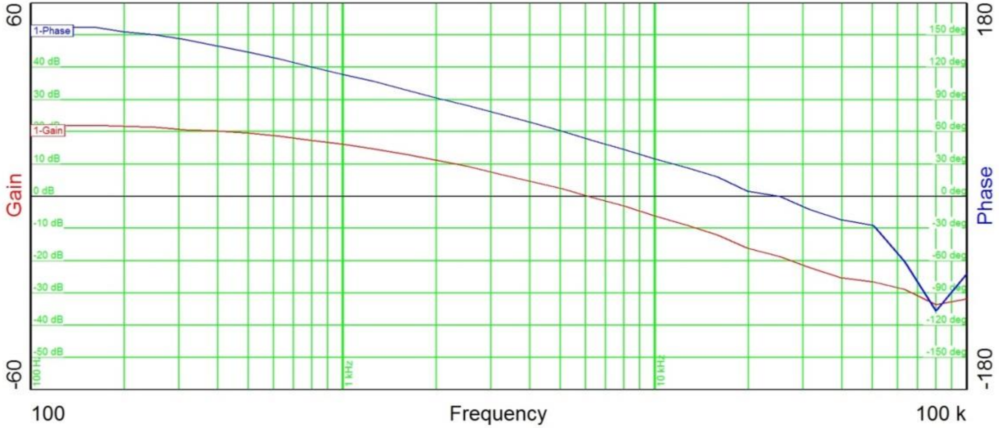
- Factors to consider
  - Max output voltage deviation
  - Time needed for output voltage to return to regulation set point
  - Settling time behavior



Load Transient Response

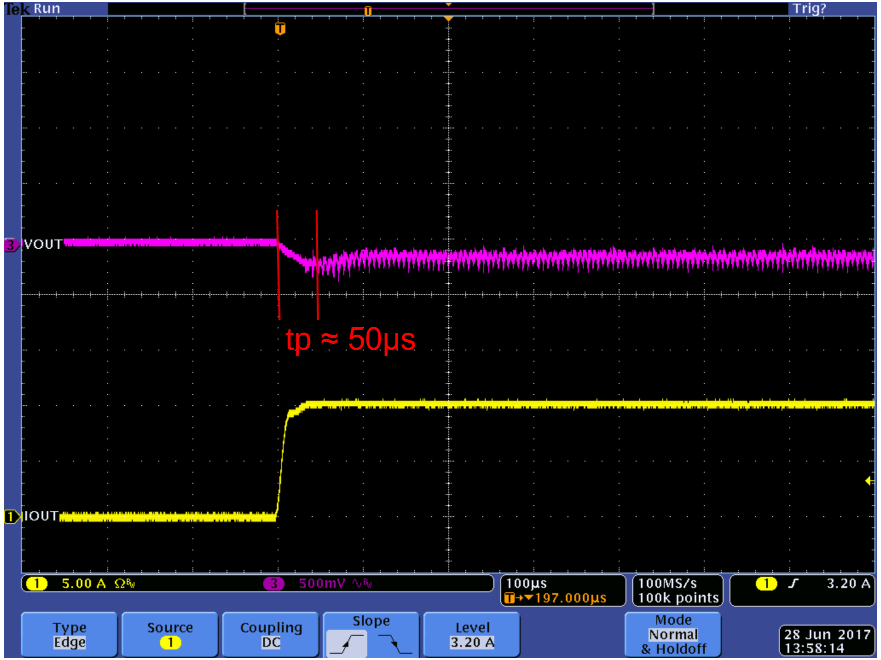
- Transient response dependent on converter bandwidth and phase margin

- Approximation of delay between transient event and converter response from bode plot
    - $t_p = \frac{1}{4\times f_c}$
    - Fc is crossover frequency
    - Tp is time from start of transient event to valley of output voltage dip
    - Approximation does not include slew rate or ESR considerations



Load Transient Response

- UCC25630-1EVM crossover frequency: 6kHz
- Approximation of delay between transient event and converter response:
  - $t_p = \frac{1}{4 \times f_c} = \frac{1}{4 \times 6kHz} = 50\mu s$



tp ≈ 50µs

Type Edge
Source 1
Coupling DC
Level 3.20 A
Mode Normal & Holdoff
28 Jun 2017 13:58:14

Load Transient Response

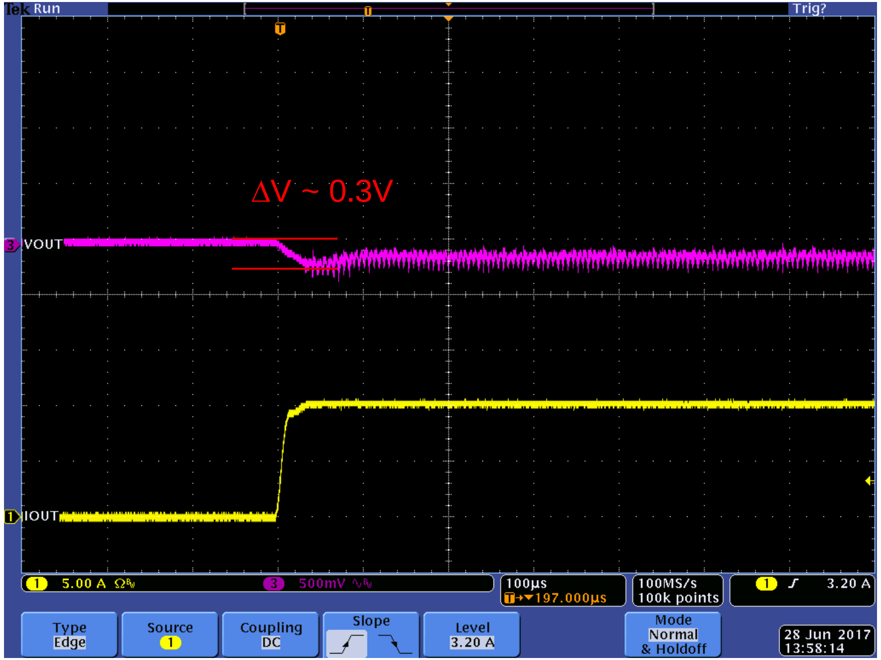
- Converter is unable to instantaneously react to transient event

- After the transient event but before converter responds, charge is transferred from output capacitance to the load, resulting in output voltage droop

- Maximum droop in output voltage dependent on closed loop output impedance, load step and slew rate

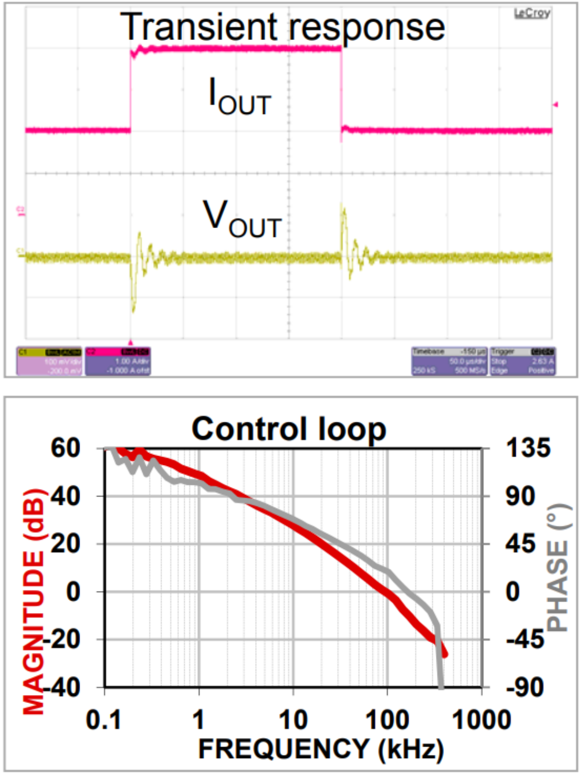
Load Transient Response

- Maximum voltage droop can be approximated from total output capacitance and ESR
  - $\Delta V_{out} = \frac{\Delta I_{LoadStep} \times \Delta t_p}{C_{out}} + \Delta I_{LoadStep} \times R_{ESR}$
  - $\Delta V_{out} = \frac{10\ \text{A} \times 50\,\mu s}{1968\ \mu F} + 10\ A \times 1.75 m\Omega = 272\text{mV}$

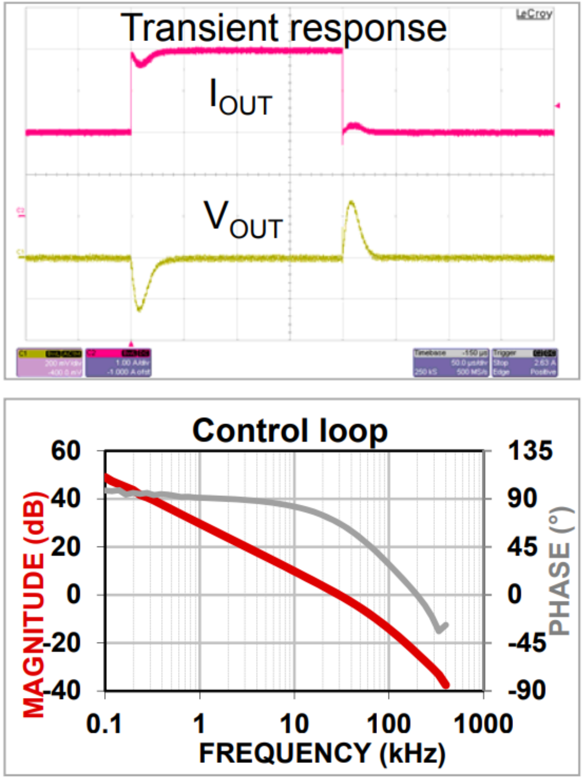

ΔV ~ 0.3V

Load Transient Response

- Phase margin describes stability of the power converter
- determines the output voltage settling time and settling behavior
- Insufficient phase margin results in underdamped response and oscillation in output voltage
- >45° phase margin a must, >60° phase margin preferred



Phase Margin=20°



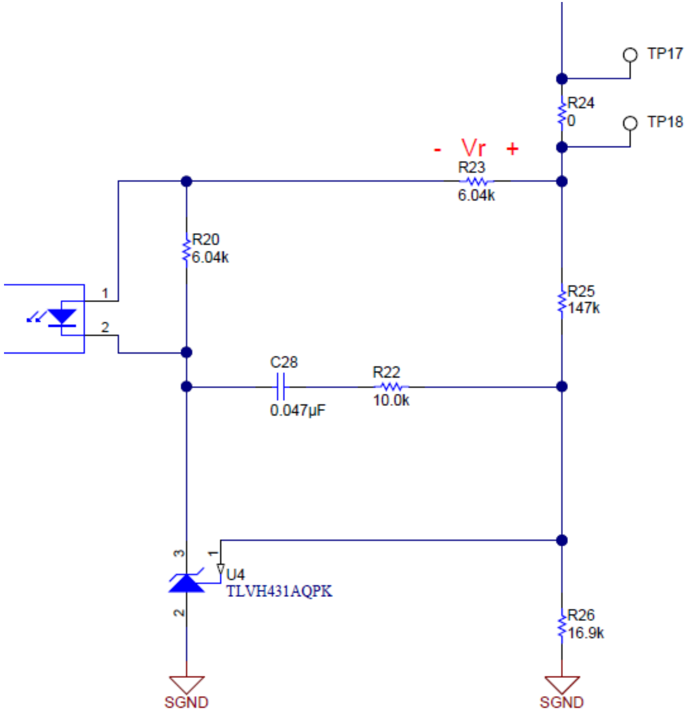
Phase Margin=67°

Compensation Goals

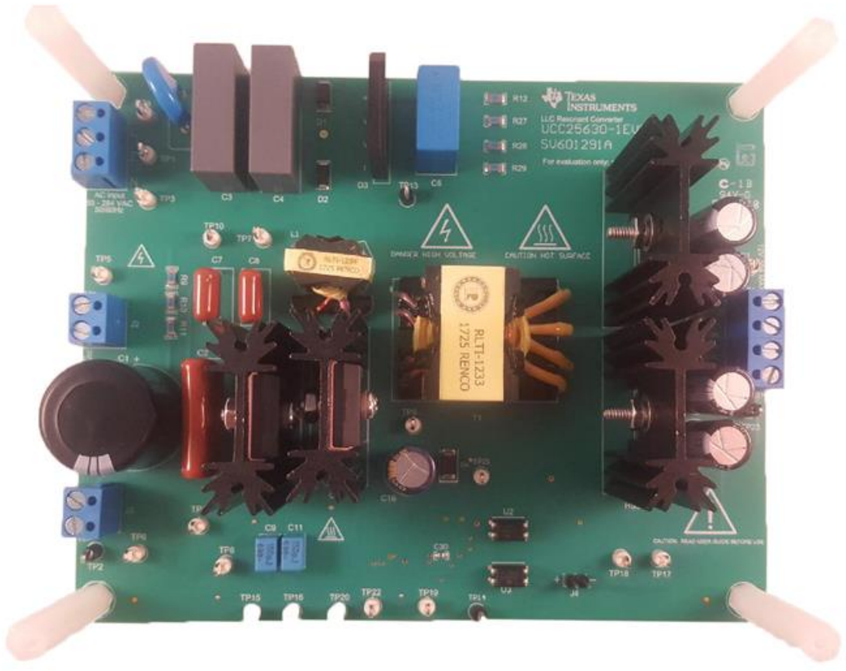
- Target higher bandwidth for faster transient response
- Maintain at least >45° phase margin at crossover frequency
- >10dB gain margin

Isolated Compensation

- Type II
  - $F_z = \frac{1}{2\pi C_{28}(R_{22}+R_{25})}$
  - $\frac{V_r(s)}{V_o(s)} = \frac{1+sC_{28}(R_{25}+R_{22})}{sC_{28}R_{25}}$
- R22 used to adjust mid-band gain of the feedback network



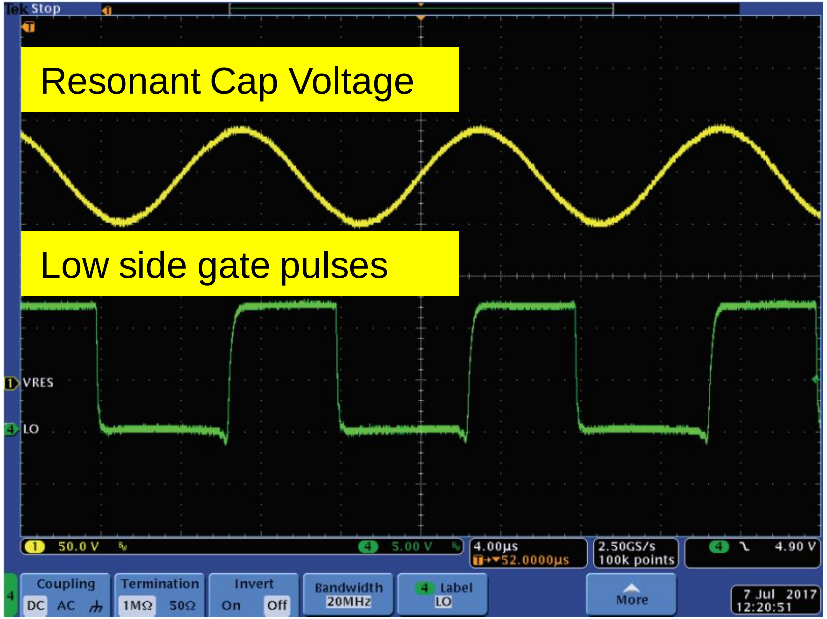
Test Results: UCC25630x EVM



- Input voltage: 340 Vdc – 410 Vdc
- Output voltage: 12 Vdc
- Output current (rated): 10A
- Resonant frequency: 96kHz

Test Results: Typical Waveforms

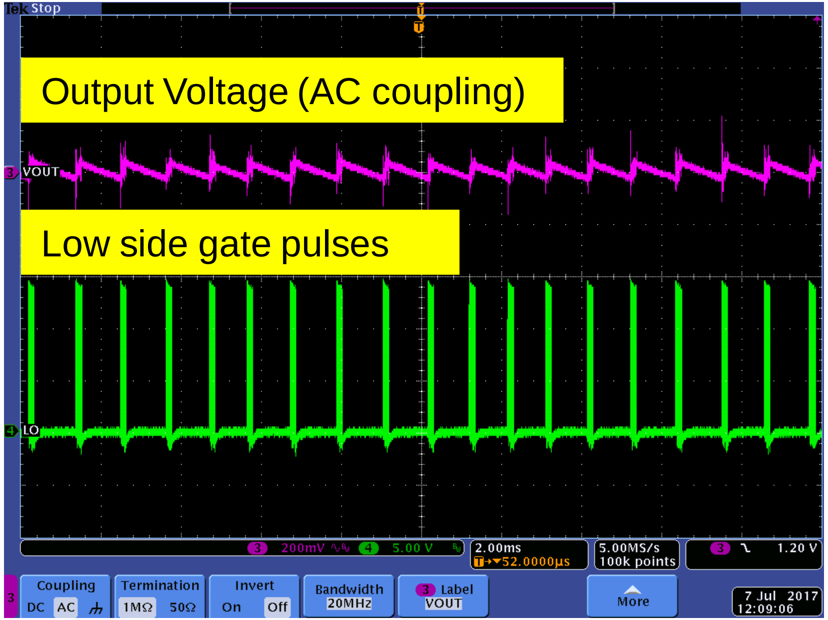
Full Load (10A)



Resonant Cap Voltage

Low side gate pulses

Light Load (0.1A)

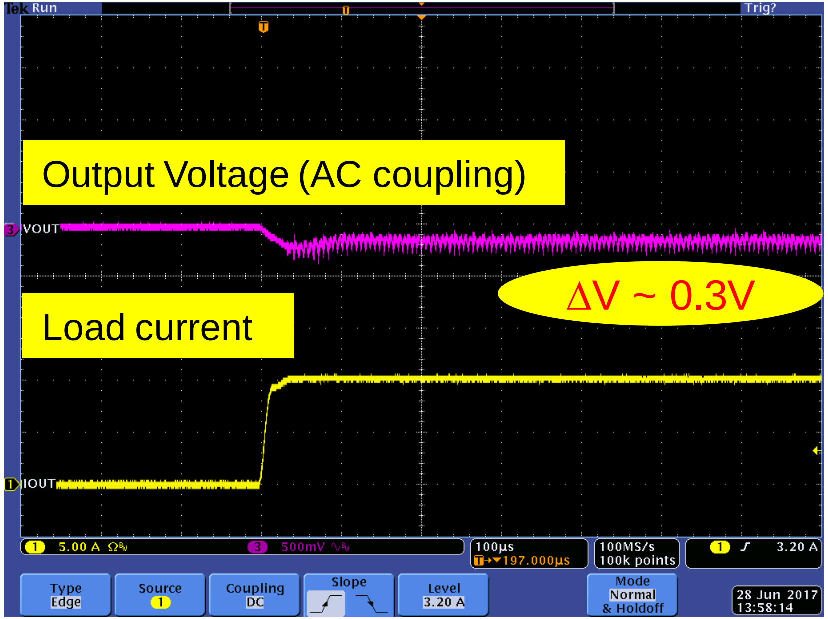


Output Voltage (AC coupling)

Low side gate pulses

Test Results: Transient Response

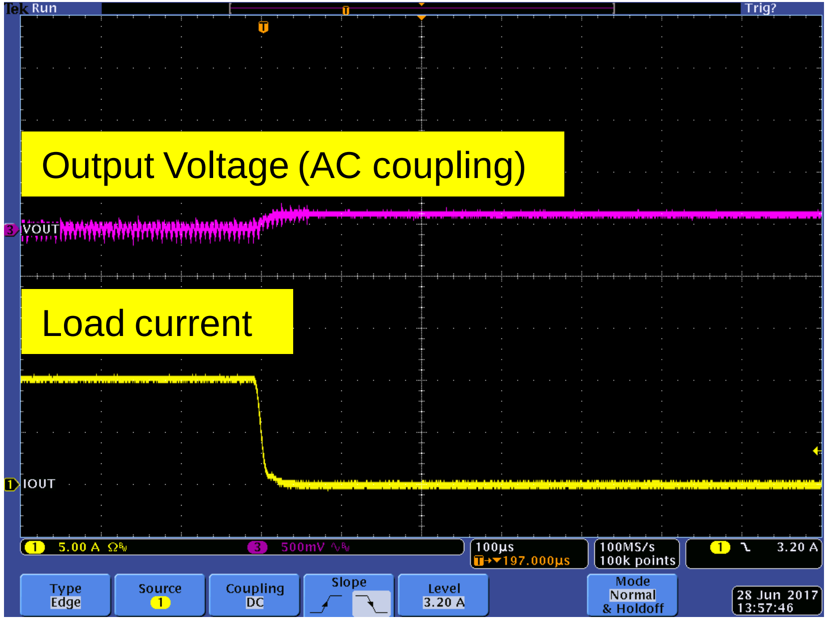
No Load to Full Load


Output Voltage (AC coupling)

Load current

ΔV ~ 0.3V

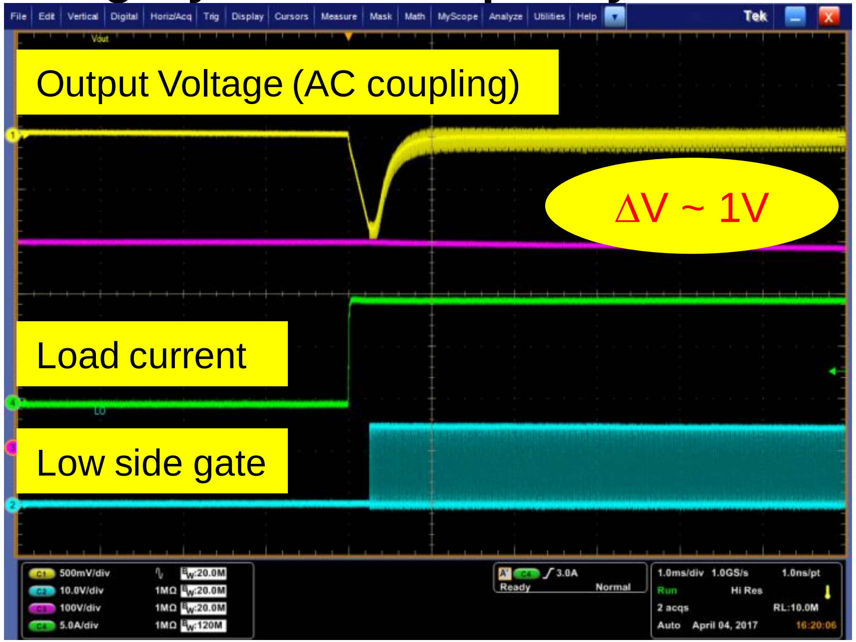
Full Load to No Load


Output Voltage (AC coupling)

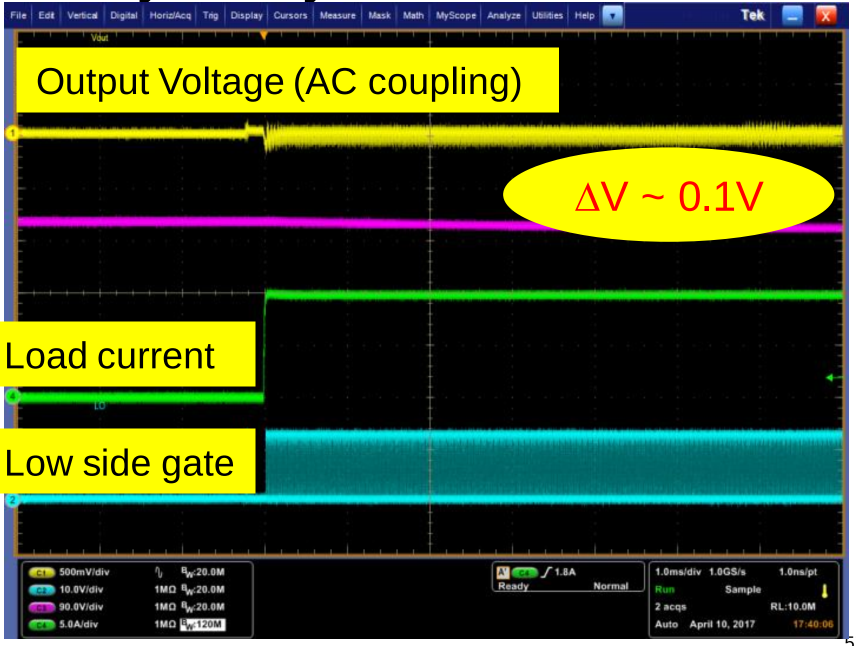
Load current

Transient Response DFC vs HHC: 12V Supply

Legacy: Direct Frequency Control

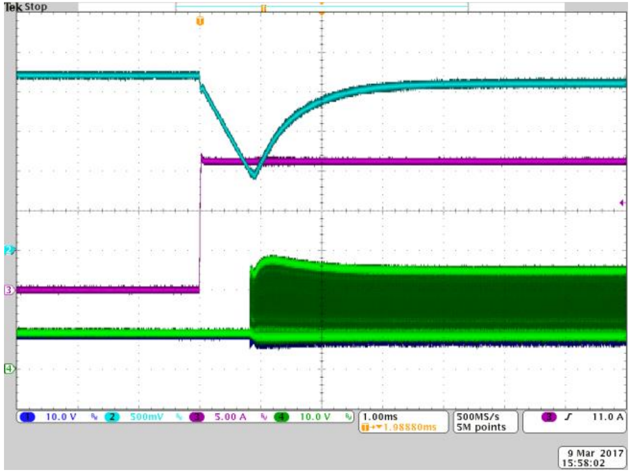


TI: Hybrid Hysteretic Control



Transient Response: Competitor #1 vs UCC25630x

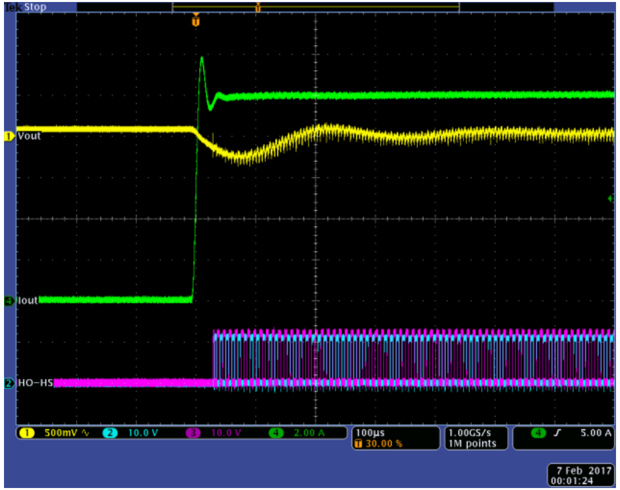
Competitor #1



CH1: LO
CH2: Vout
CH3: Iout
CH4: HO-HS

10.8% Vout dip from no load to full load

TI: UCC25630x

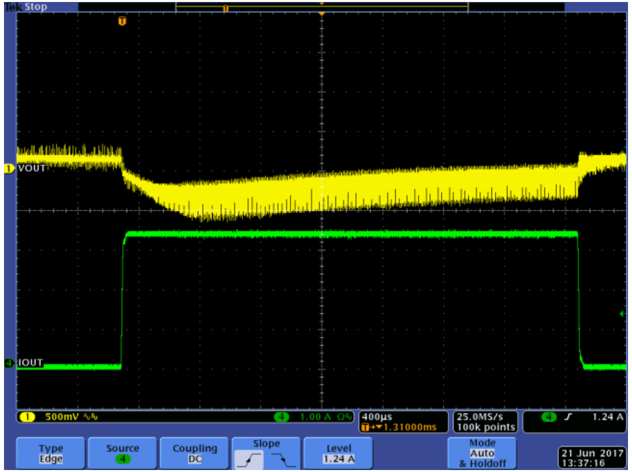


CH1: Vout
CH2: LO
CH3: HO-HS
CH4: Iout

1.25% Vout dip from no load to full load

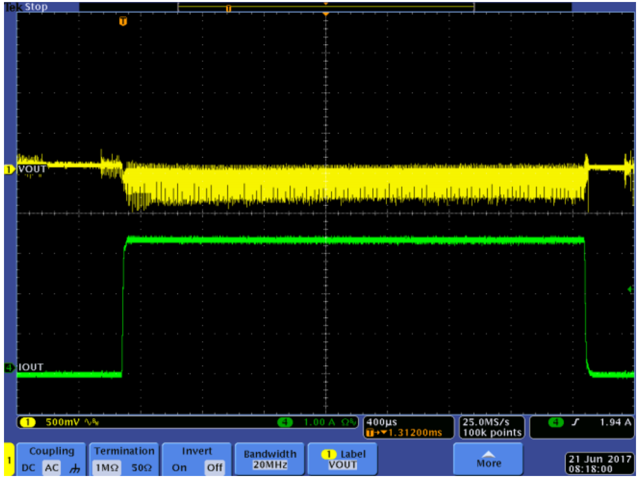
Transient Response: Competitor #2 vs UCC25630x

Competitor #2 using DFC Control



Vout dip: 600mV

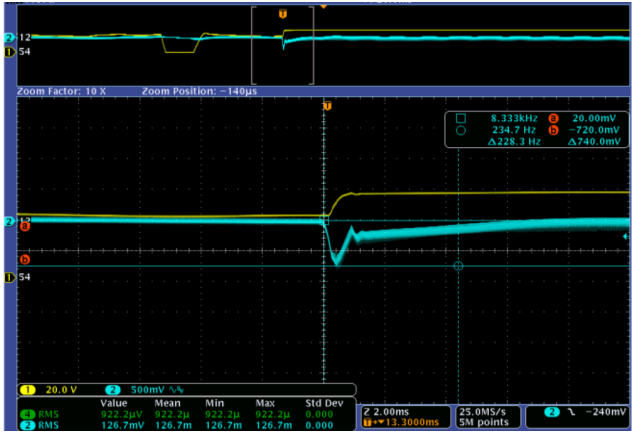
TI: UCC25630x



Vout dip:250mV

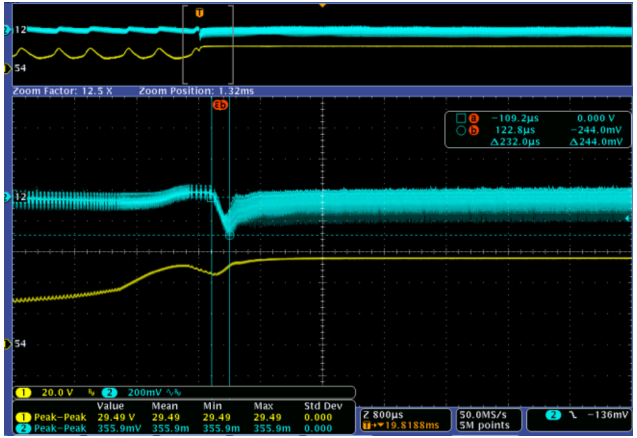
Transient Response: Competitor #3 vs UCC25630x

Competitor #3 using DFC Control



Vout dip:740mV

TI: UCC25630x



Vout dip: 244mV

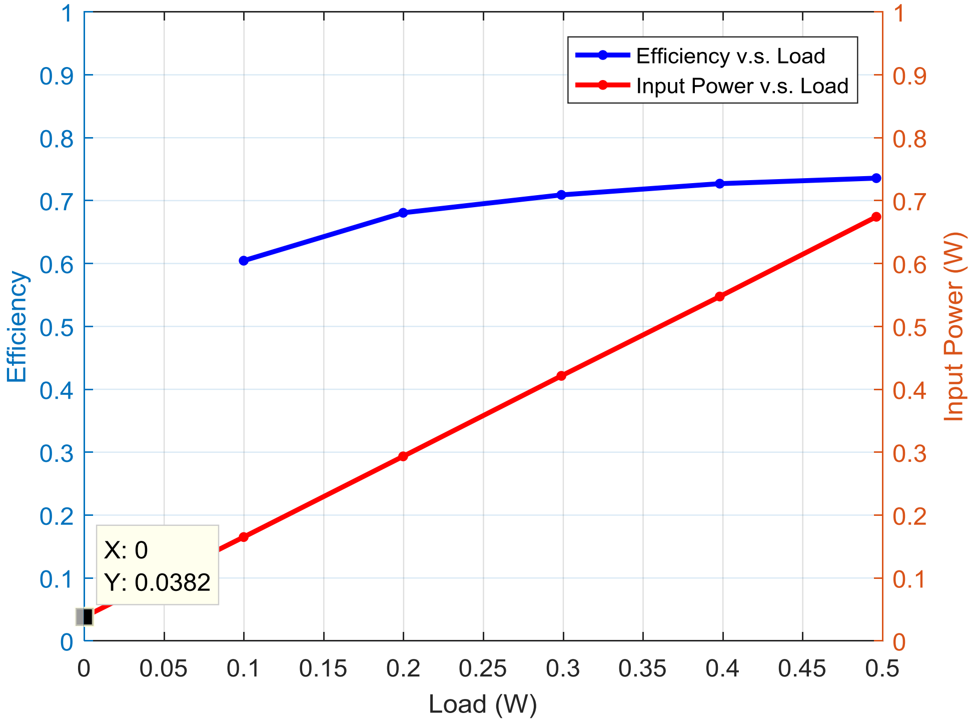
System Level Benefits to Improved Transient Response

- Tighter regulation of output voltage is realizable without needing additional output capacitance

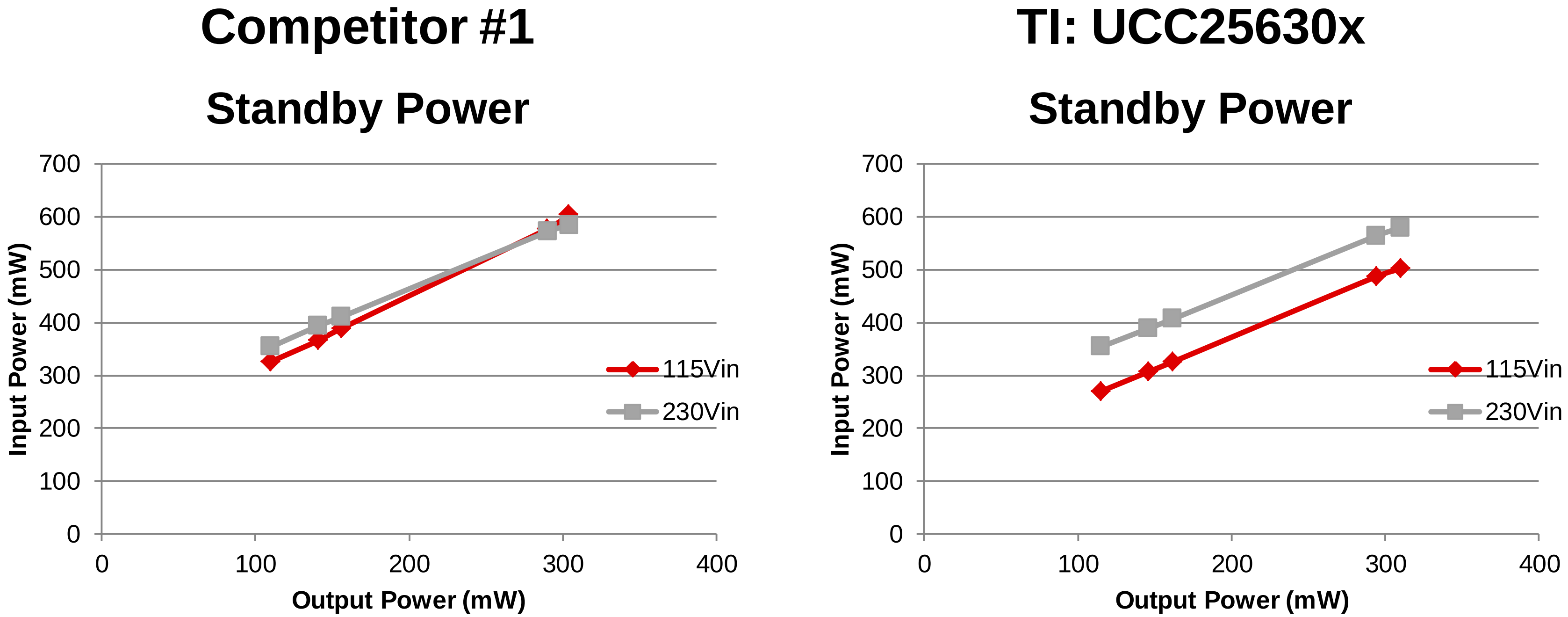
- Output capacitance can be significantly reduced and meet the same transient response performance as direct frequency control

Light Load Power Consumption (UCC25630-1EVM)

38.2 mW no load power consumption



Standby Power: Competitor #2 vs UCC25630x



UCC28056 + UCC25630x Standby Power

- PMP21251 170W transition mode PFC + LLC design
- 70mW no load standby power at 115Vac
- 89mW no load standby power at 230Vac

Standby Power System Level Benefits

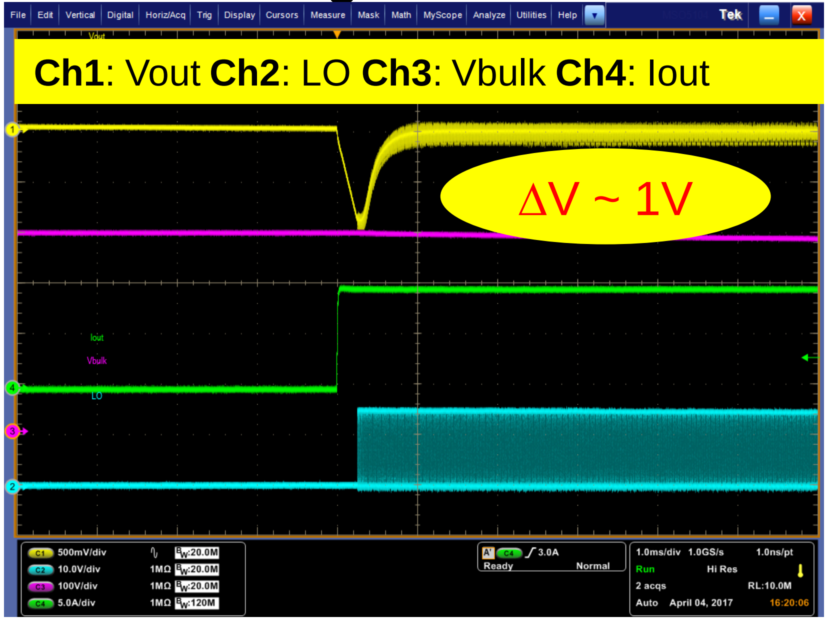
- Enables designs to meet modern energy standards such as DOE Level VI and CoC Tier II
- PFC does not need to be disabled at light load to meet efficiency goals
- Keeping PFC ‘always on’ simplifies power supply architecture and provides faster response from standby to full load

Retrofitting UCC25630x into Gaming Station

Gaming: Transient Response

- Test Condition: VinAC=115V, Vout=12V, Iout step from 0A to 10A
- Transient performance is 10x better with UCC25630x

Original Board

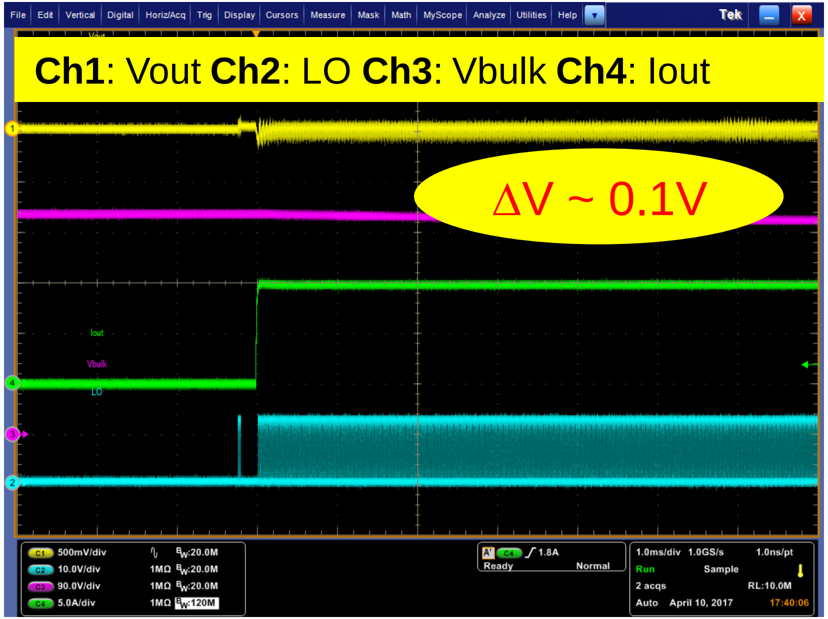


Ch1: Vout **Ch2**: LO **Ch3**: Vbulk **Ch4**: Iout

ΔV ~ 1V

C1 500mV/div BW:20.0M
C2 10.0V/div 1MΩ BW:20.0M
C3 100V/div 1MΩ BW:20.0M
C4 5.0A/div 1MΩ BW:120M
A' C4 3.0A Ready Normal
1.0ms/div 1.0GS/s 1.0ns/pt
Run Hi Res
2 acqs RL:10.0M
Auto April 04, 2017 16:20:06

TI: UCC25630x



Ch1: Vout **Ch2**: LO **Ch3**: Vbulk **Ch4**: Iout

ΔV ~ 0.1V

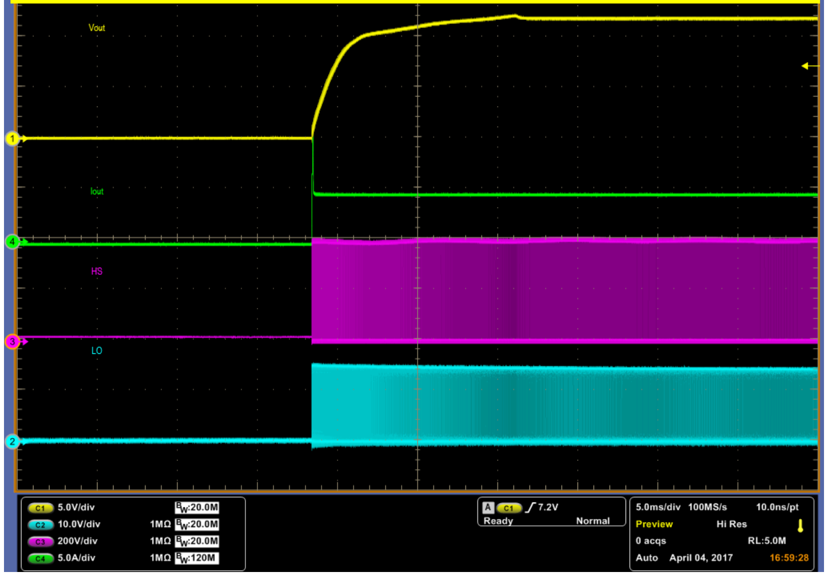
C1 500mV/div BW:20.0M
C2 10.0V/div 1MΩ BW:20.0M
C3 90.0V/div 1MΩ BW:20.0M
C4 5.0A/div 1MΩ BW:120M
A' C4 1.8A Ready Normal
1.0ms/div 1.0GS/s 1.0ns/pt
Run Sample
2 acqs RL:10.0M
Auto April 10, 2017 17:40:06

PS4: Startup

- Test Condition: VinAC=115V, Vout=12V, Iout=5A

Original Board

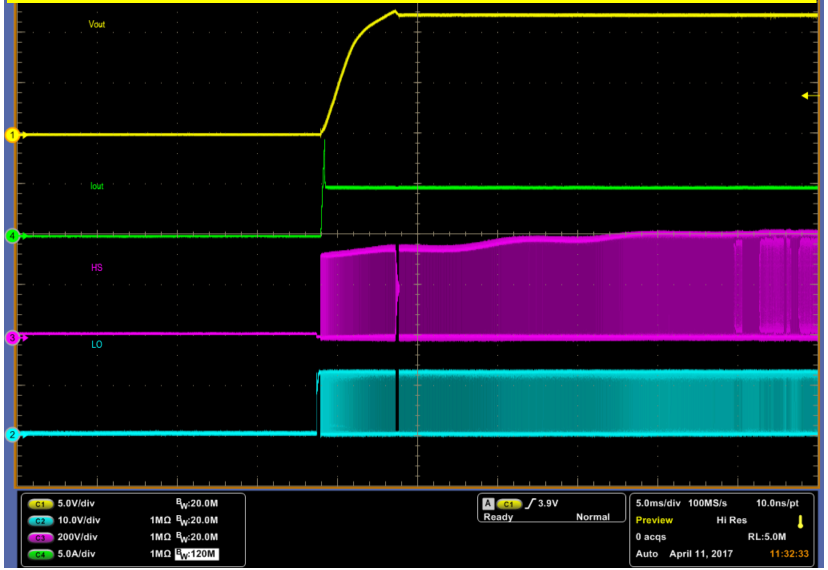
Ch1: Vout **Ch2**: LO **Ch3**: HS **Ch4**: Iout



C1 5.0V/div BW:20.0M
C2 10.0V/div 1MΩ BW:20.0M
C3 200V/div 1MΩ BW:20.0M
C4 5.0A/div 1MΩ BW:120M
A C1 7.2V Ready Normal
5.0ms/div 100MS/s 10.0ns/pt
Preview Hi Res
0 acqs RL:5.0M
Auto April 04, 2017 16:59:28

TI: UCC25630x

Ch1: Vout **Ch2**: LO **Ch3**: HS **Ch4**: Iout



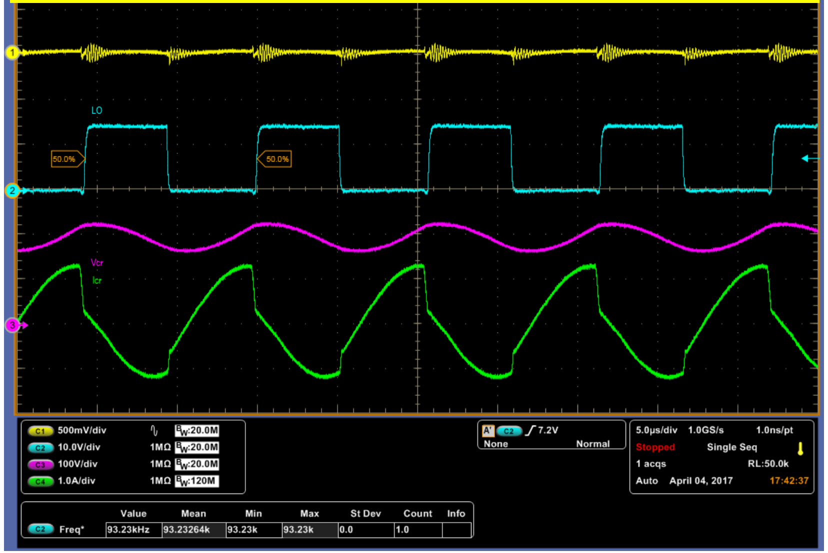
C1 5.0V/div BW:20.0M
C2 10.0V/div 1MΩ BW:20.0M
C3 200V/div 1MΩ BW:20.0M
C4 5.0A/div 1MΩ BW:120M
A C1 3.9V Ready Normal
5.0ms/div 100MS/s 10.0ns/pt
Preview Hi Res
0 acqs RL:5.0M
Auto April 11, 2017 11:32:33

PS4: Load Regulation

- Test Condition: VinAC=115V, Vout=12V, Iout=10A

Original Board

Ch1: Vout **Ch2**: LO **Ch3**: Vcr **Ch4**: Icr



C1 500mV/div BW:20.0M
C2 10.0V/div 1MΩ BW:20.0M
C3 100V/div 1MΩ BW:20.0M
C4 1.0A/div 1MΩ BW:120M

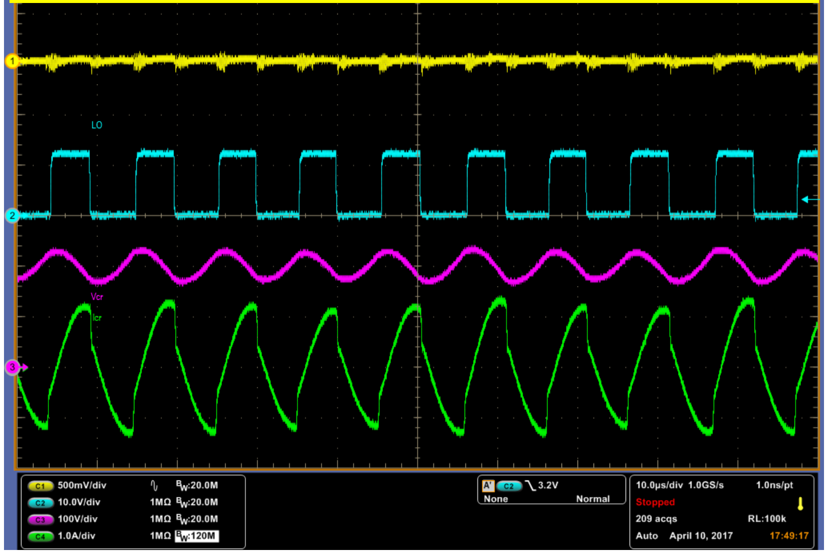
A' C2 ⎍ 7.2V
None Normal

5.0µs/div 1.0GS/s 1.0ns/pt
Stopped Single Seq
1 acqs RL:50.0k
Auto April 04, 2017 17:42:37

	Value	Mean	Min	Max	St Dev	Count	Info
C2 Freq*	93.23kHz	93.23264k	93.23k	93.23k	0.0	1.0	

TI: UCC25630x

Ch1: Vout **Ch2**: LO **Ch3**: Vcr **Ch4**: Icr



C1 500mV/div BW:20.0M
C2 10.0V/div 1MΩ BW:20.0M
C3 100V/div 1MΩ BW:20.0M
C4 1.0A/div 1MΩ BW:120M

A' C2 ⎍ 3.2V
None Normal

10.0µs/div 1.0GS/s 1.0ns/pt
Stopped
209 acqs RL:100k
Auto April 10, 2017 17:49:17

Summary

- LLC is an excellent topology choice for designs with narrow, high voltage input and requires high efficiency across entire load range.

- First harmonic approximation forms the foundation of the LLC design flow

- Hybrid hysteretic control offers improved transient performance, reducing the required output capacitance to meet a given output voltage regulation requirement