Designing with Isolated Gate Drivers for HEV/EV Applications

Xiong Li, Systems Engineer

Texas Instruments

Detailed agenda

- ***Brief introduction to isolated gate driver use case in automotive applications***

- ***Deep dive of functional blocks in an isolated gate driver***
  - **Power supply**: architecture, topologies, and protection functions
  - **PWM input**: *CMOS input, current input, and interlock and shoot-through protection*
  - **Output stage**: *integrated buffer or external buffer?*
  - **Short circuit and over current protection**: *DESAT, resistor voltage divider, or sense FET?*
  - **Overvoltage protection**: *Soft turn-off, two-level turn-off, or high voltage clamping?*
  - **Active Miller clamp**: internal vs external
  - **Over temperature protection***: NTC or diode?*
  - **HV isolation**: *capacitor, transformer, or opto-coupler?*
  - **Status feedback and diagnosis**

- ***TI Designs***

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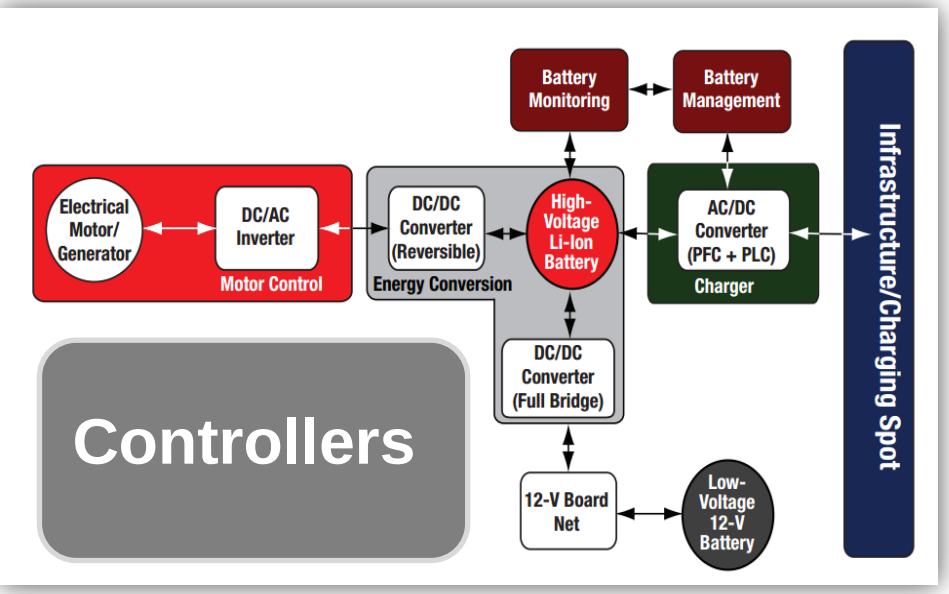
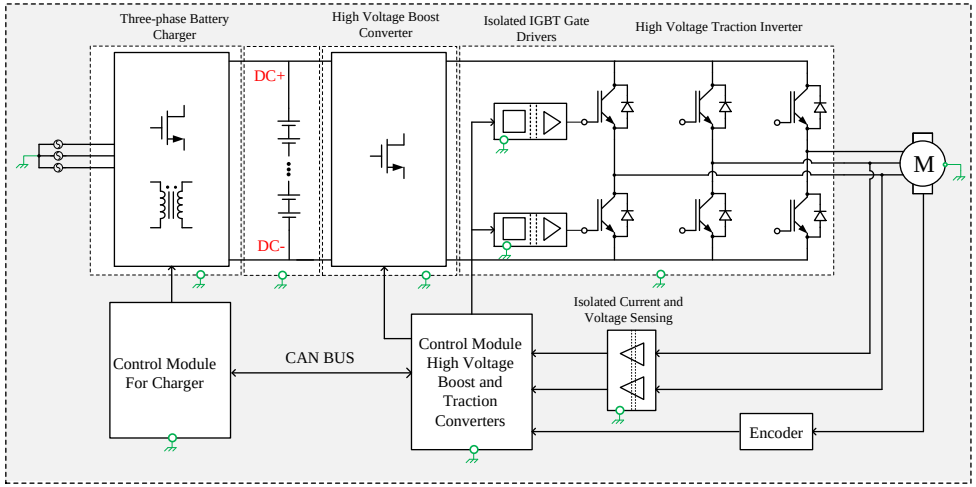
HEV/EV Traction Inverter System



- *High voltage and low voltage circuits co-exist in a HEV/EV system.*
  - ***High voltage*** li-ion battery
  - ***High voltage*** motor
  - ***High voltage*** drive inverter
  - ***High voltage*** on-board charger
  - ***High voltage*** dc/dc converter
  - ***Low voltage*** ECUs
- *Isolation is required between the high voltage and low voltage circuits for both safety and function purposes.*

HEV/EV Power Electronics System



Block diagram of high voltage power electronics system In a HEV/EV system

- **Isolated Gate Driver:**
  - *Isolation:*
    - Ground isolation for functional purpose.
    - Safety isolation to prevent human beings from electric shock.
  - *Signal buffer:*
    - A bridge between control module and power transistor.
    - Signal relay and amplification.
    - Gate driver is sitting in the critical path motor control. Failures in gate driver can lead to system single point failure.
  - Advanced gate drivers have access to all the three terminals of a power transistor (drain, source, and gate for MOSFET, and collector, emitter, and gate for IGBT).
  - Unique position to implement advanced protections and diagnosis.

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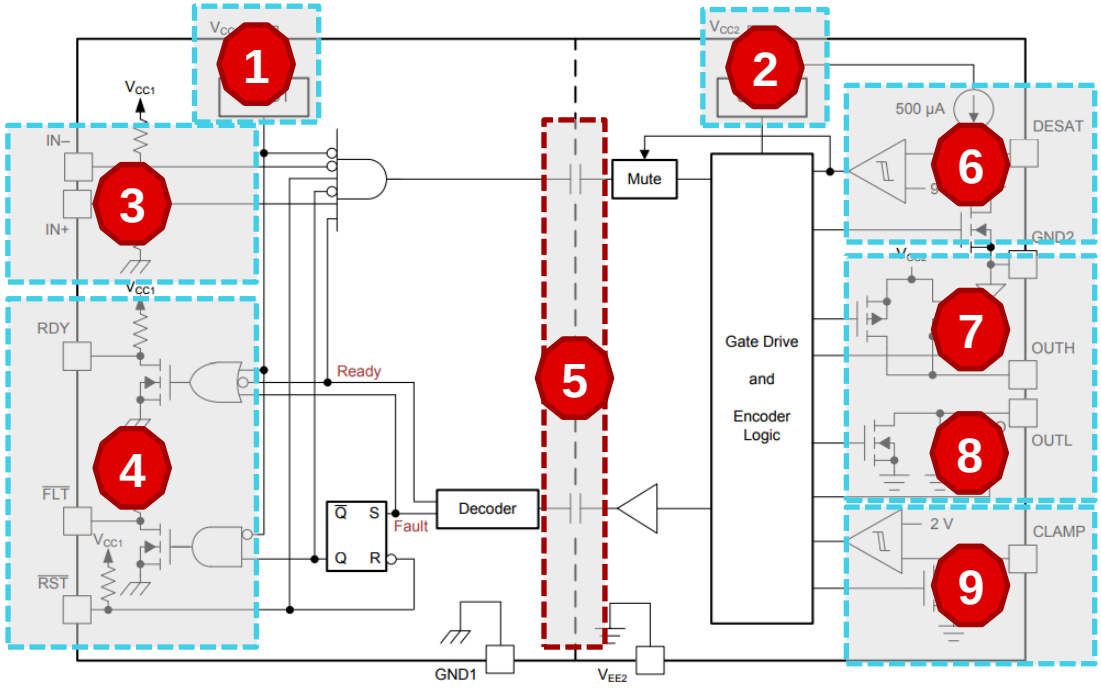
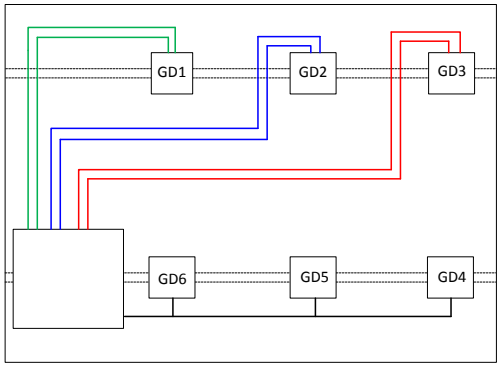
Example Isolated Gate Driver: ISO5452-Q1

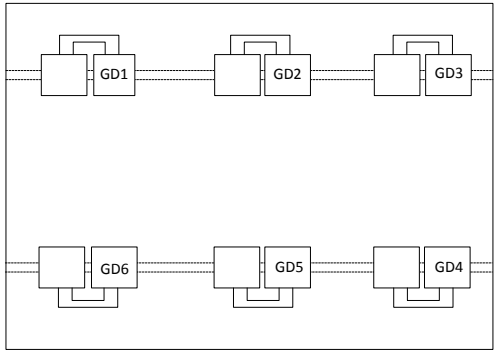


1. VCC1 monitor
2. VCC2 monitor
3. PWM input
4. Status feedback
5. HV isolation
6. DESAT protection
7. Output stage
8. Soft turn-off
9. Active Miller clamp

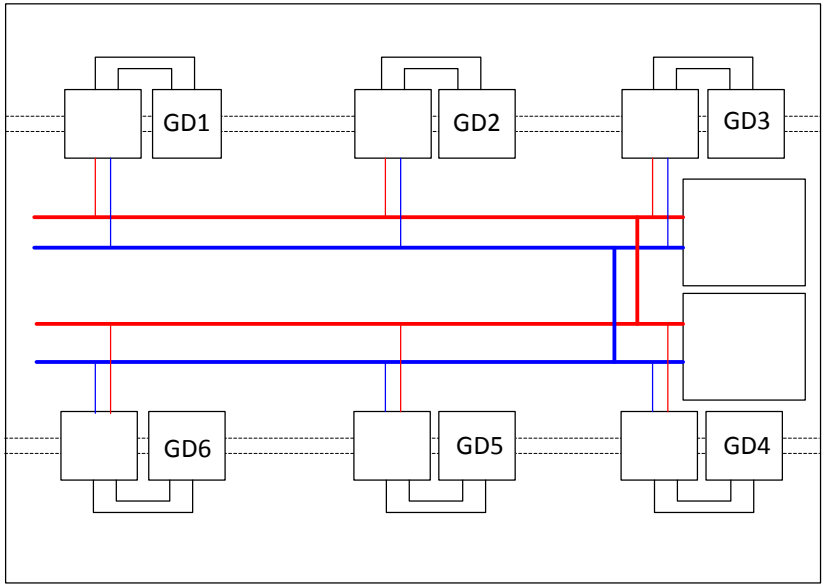
Power Supply: Architecture



Centralized Power



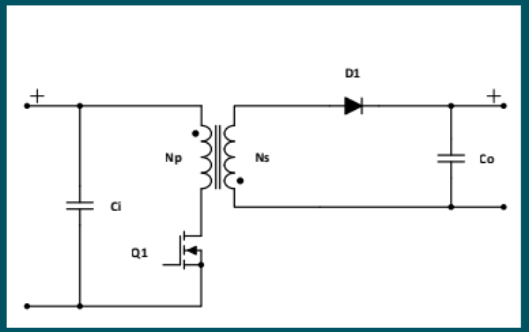
Distributed Power



Two-stage Power Architecture

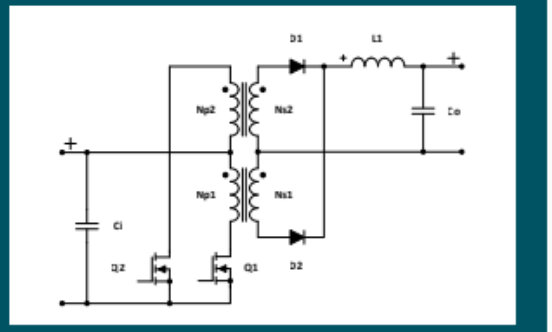
Power Supply: Topologies

Flyback



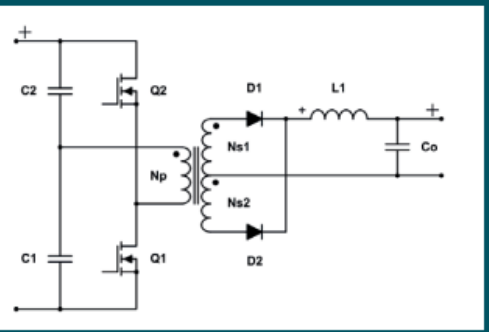
- Most commonly used top.
- Fewer component counts
- Easiness in control
- **Relatively large transformer size**

Push-Pull



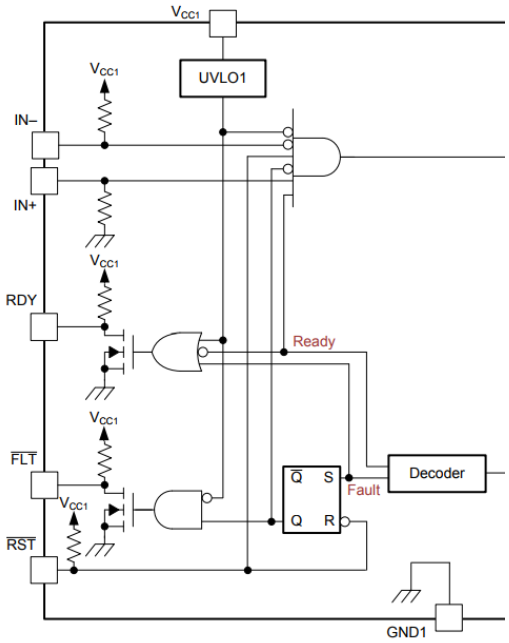
- Better utilization of transformer core that smaller transformer size
- **Potential flux walking issue.**
- **Two FETs need to be used.**
- **FETs need to withstand twice of the input voltage.**

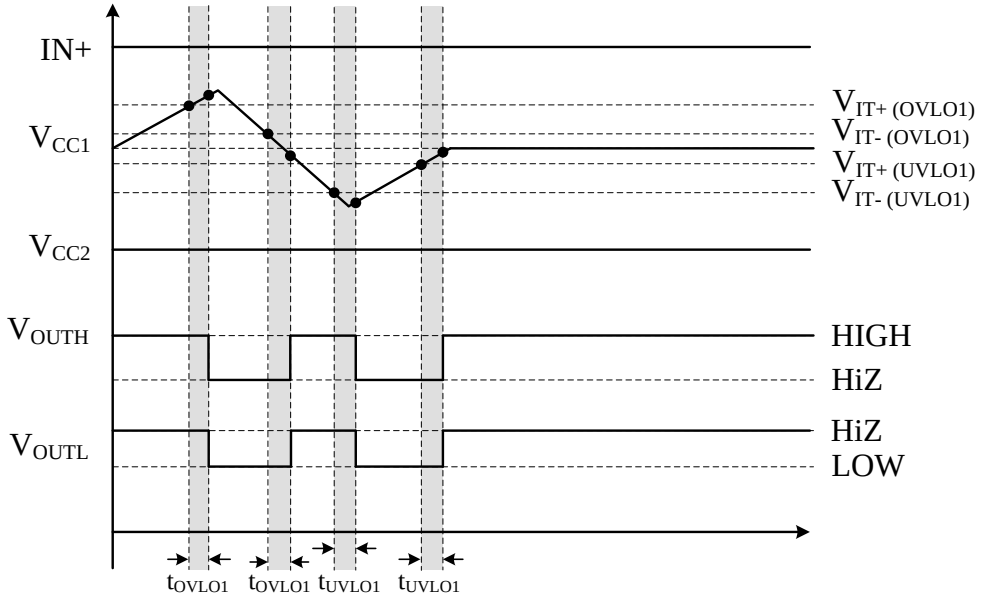
Half - Bridge



- Better utilization of transformer core that smaller transformer size
- **Potential flux walking issue**
- **Two FETs need to be used with high side driver.**
- **Current mode control not suitable.**

Power Supply: Protections





- VCC1 monitor is used to ensure the normal operations of circuits in VCC1 side.
- Driver output is disabled in case of VCC1 UVLO events.

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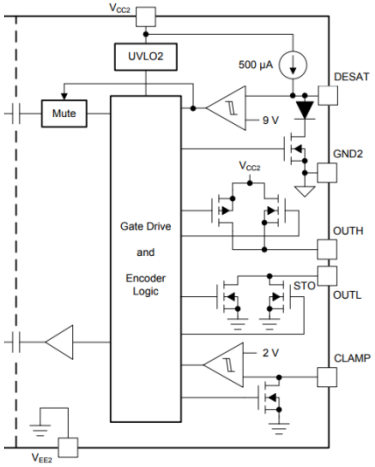
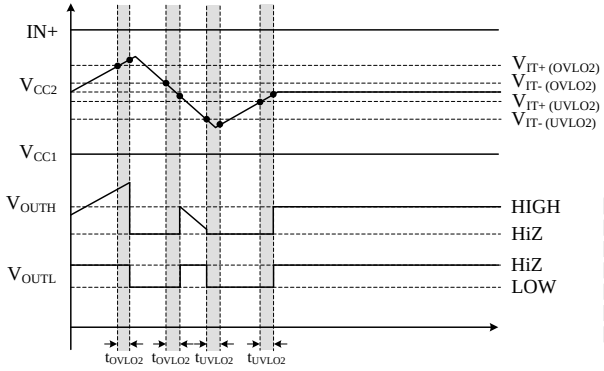
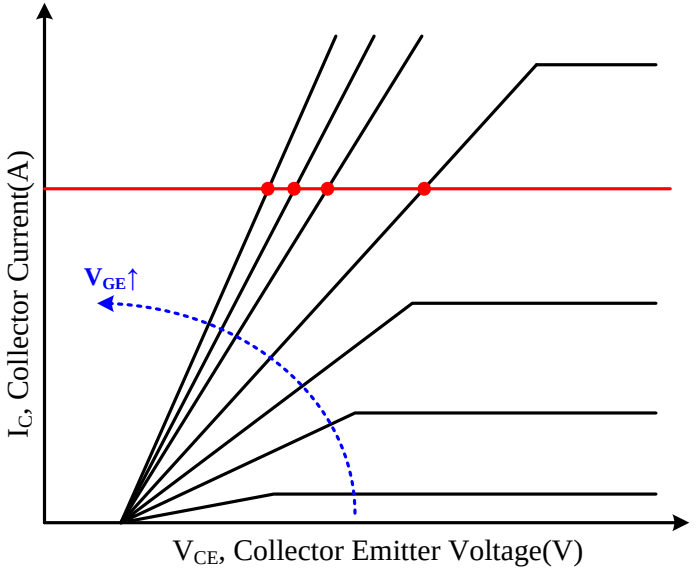
Power Supply: Protections

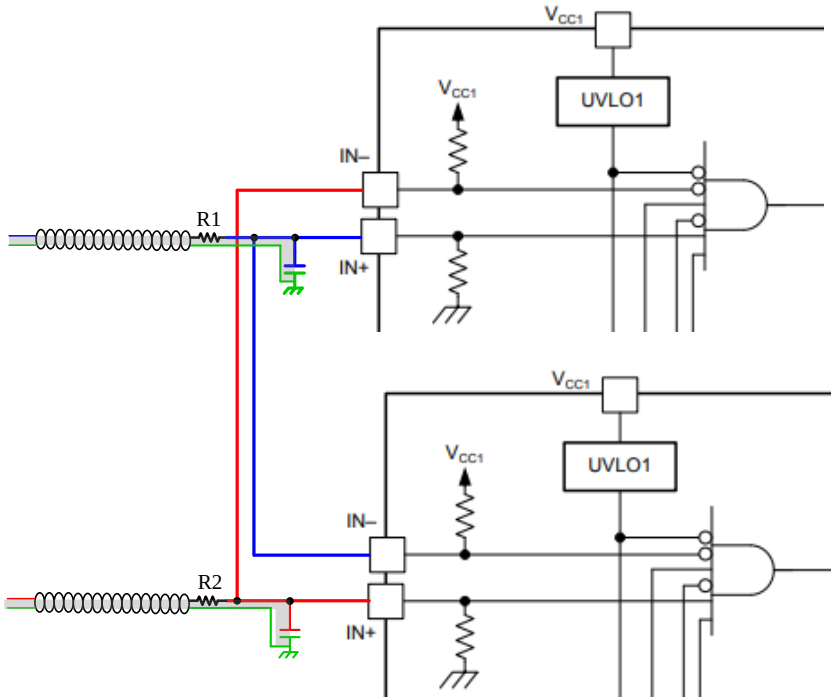






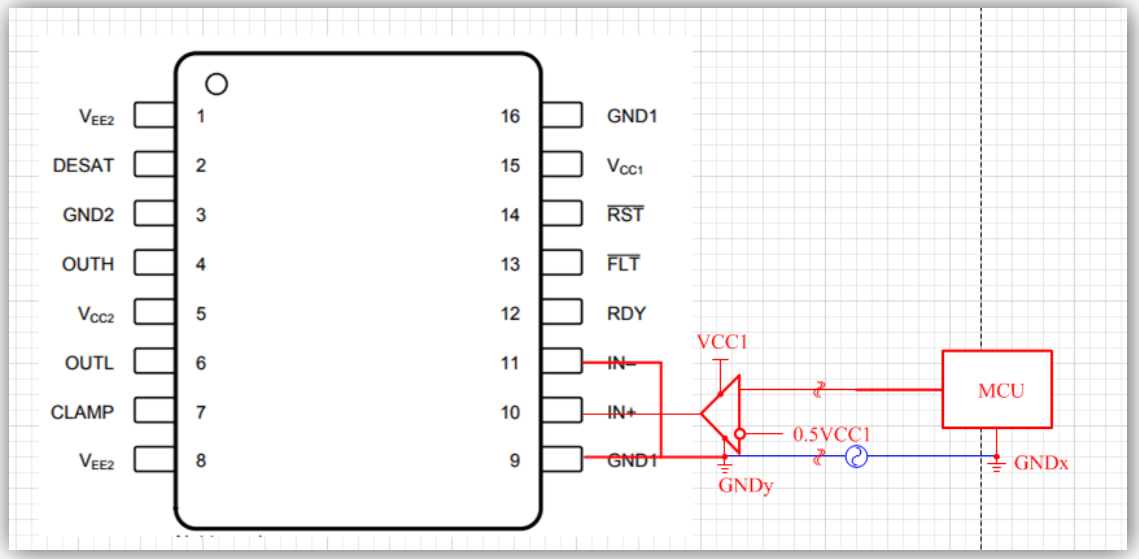
- The on state voltages of power transistors depend on the gate drive voltage. The VCC2 monitor function is used to ensure that power transistor to operate in low on state voltage region.

PWM Input: CMOS

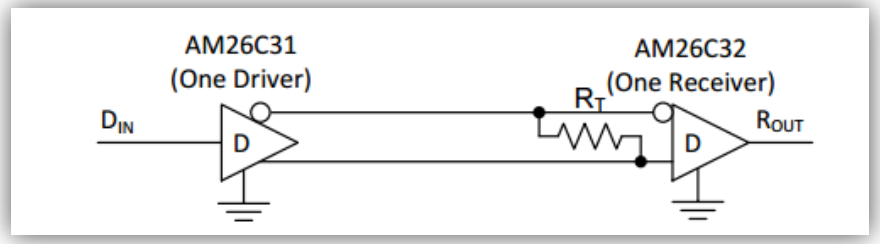


- CMOS voltage input is used. Signal is single-ended. By nature, it is more prone to common mode noise as compared with current inputs.
- In order to enhance the noise immunity to common mode noise, the PWM input signal is recommended to route in parallel with a ground line. The signal loop needs to be minimized.
- RC filters are recommended to use at the input to reject high frequency glitch noises.
- The R in the RC filter needs to be small enough to not affect the function of interlock circuits.
- Narrow PWM pulses are detrimental to the power transistors.
- Degltich filters are usually integrated into driver IC.

PWM Input: CMOS

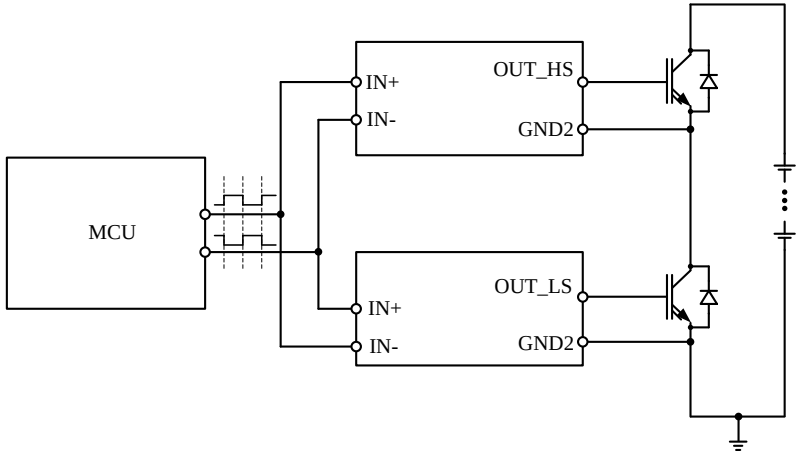


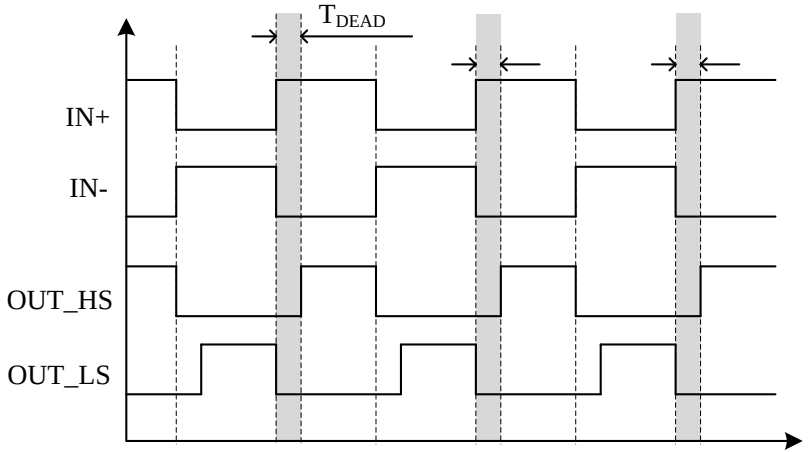
Mid-range MCU to driver IC input connection



Long-range MCU to driver IC input connection

PWM Input: Shoot-through Protection





- Shoot-through protection circuit is used to prevent the two drivers of a half bridge circuit to be turned on at the same time.
- A min dead time is forced between the falling edge of IN- signal and rising edge of IN+ signal.

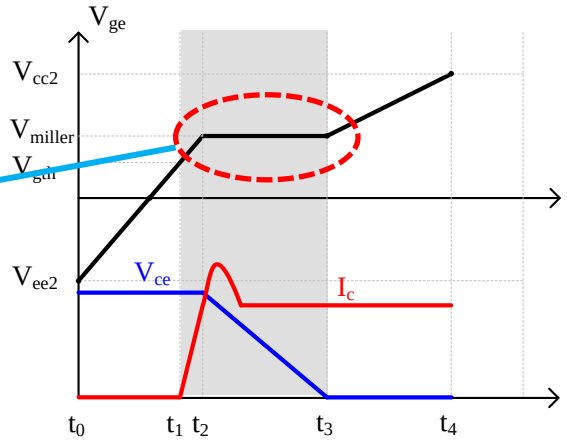
Output Stage: Sizing of External Gate Resistor

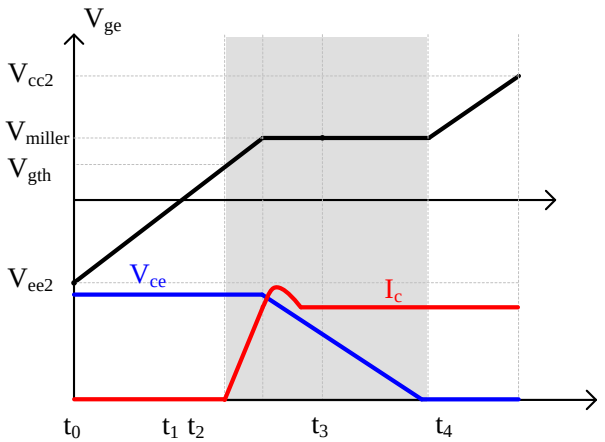
Fast switching
– High **di/dt** and **dv/dt** values
– Low **switching losses** $E_{on/off}$

Slow switching
– Low **di/dt** and **dv/dt** values
– High **switching losses** $E_{on/off}$

$$\frac{dV}{dt} = \frac{V_{CC2} - V_{PLAT}}{R_g \times C_{rss}}$$

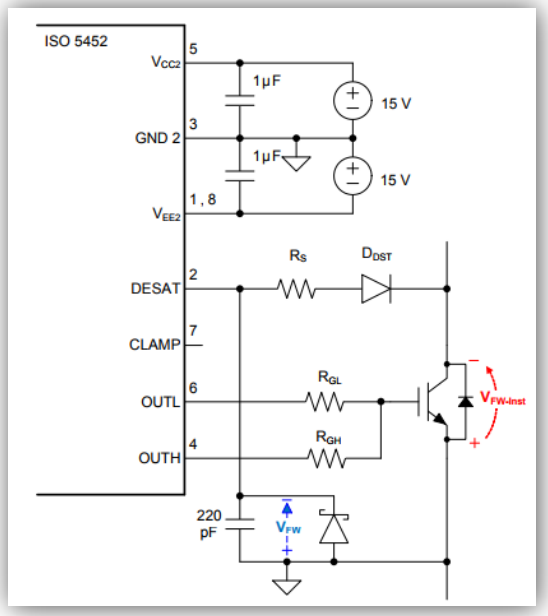
$$R_g > \sqrt{\frac{L_g}{C_{rss}}}$$



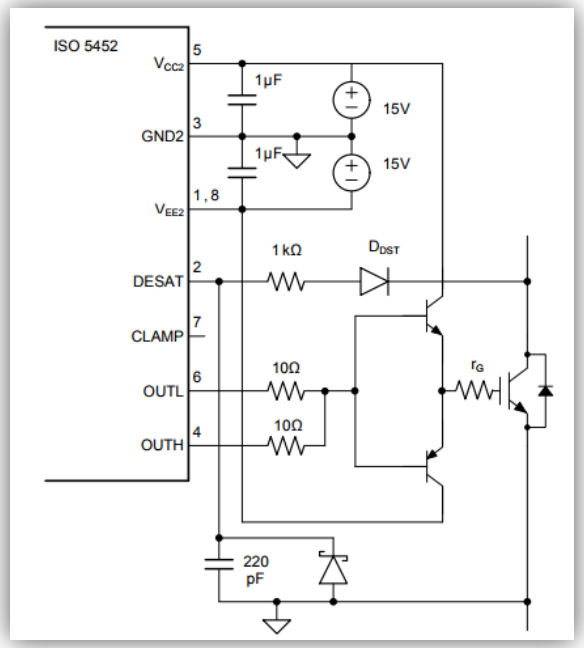


- Sizing of the driver output stage is a trade-off between power transistor switching loss and EM emissions.
- More drive current means less switching loss while more emissions, and vice versa.
- Rg needs to be large enough to damp the gate voltage ringing.
- Rg needs to be small enough to drive fast enough dv/dt to achieve reasonable switching loss.

Output Stage: External Buffer



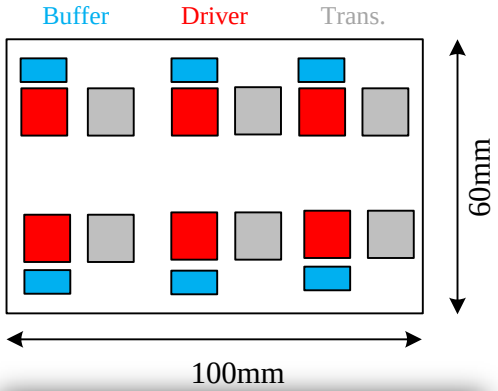
Direct Driving



Driving with current buffer

- Driver IC usually comes with limited drive current due to limitation of thermal dissipation.
- External BJT buffer can be used to boost the drive current if more drive current is needed.

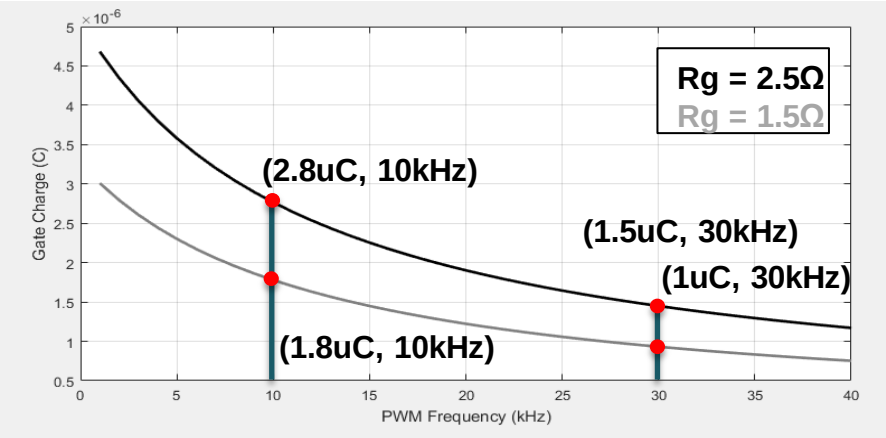
Output Stage: Integrated Buffer



Advantages of Integrated Buffer:

- **Cost and Board size Reduction**
  - Cost of a NPN+PNP buffer is 30cents at high volume.
  - 15A NPN+PNP accounts for 10mm x 5mm board space.
  - Board space can be a challenge for design with high power densities.
- **FIT rate reduction**
  - The FIT rate of a NPN+PNP buffer stage is 4-6FIT.
  - The total FIT budget for driver function is 10FIT in order to meet ASIL-D compliance.
- **Better match in timing:**
  - Integrated buffer is implemented with MOSFETs and would have better response time and matching.
- **Thermal management**
  - The R_{DSON} of driver internal FETs needs to be small enough to shift power dissipation outside of package to limit the max junction temperature to be less than 150C.

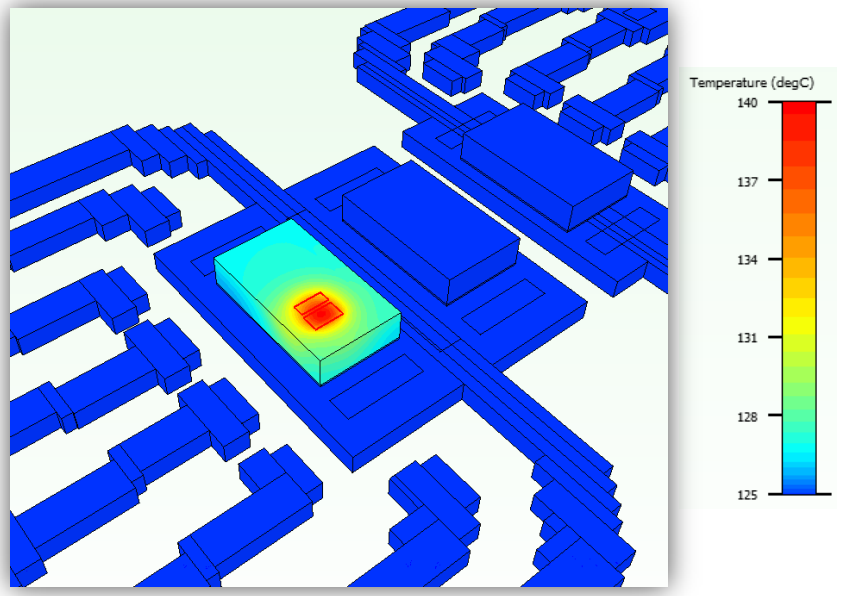
Output Stage: Integrated Buffer



V_{CC2} = 15V, V_{EE2} = -10V, I_{BIAS} = 12mA, ta = 125C

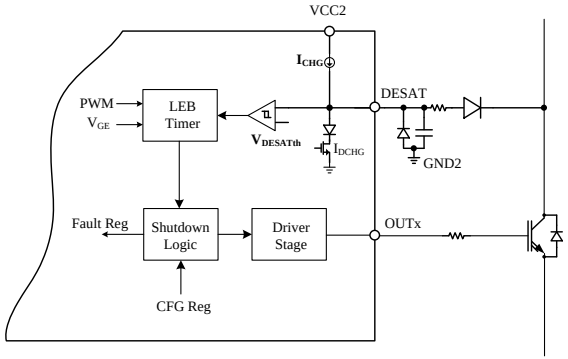
$$P_{loss} = \left[Q_g \times f_{PWM} \times (V_{CC2} - V_{EE2})\right] \times \frac{R_{int}}{R_{int} + R_g} + (V_{CC2} - V_{EE2}) \times I_{QVCC2}$$

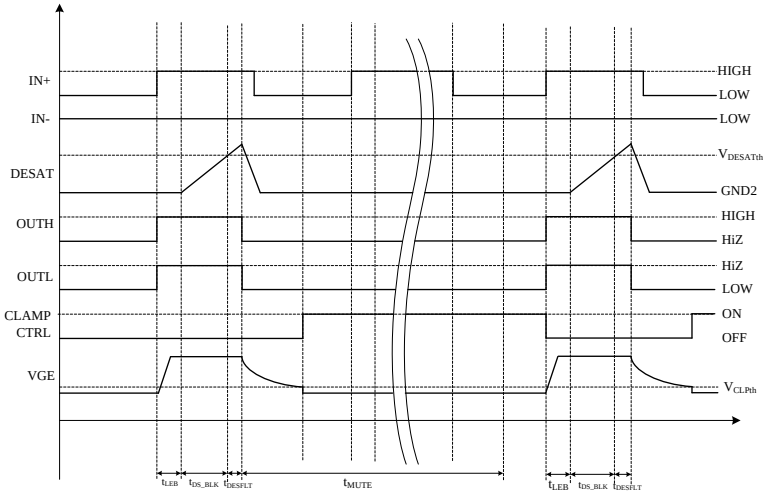
- ***Qg***: gate charge, V_{CC2}: positive supply voltage,
- V_{EE2}: negative supply voltage, I_{QVCC2}: quiescent bias current,
- f_{PWM}: PWM frequency, R_{int}: driver internal resistor,
- R_g: driver external gate resistor

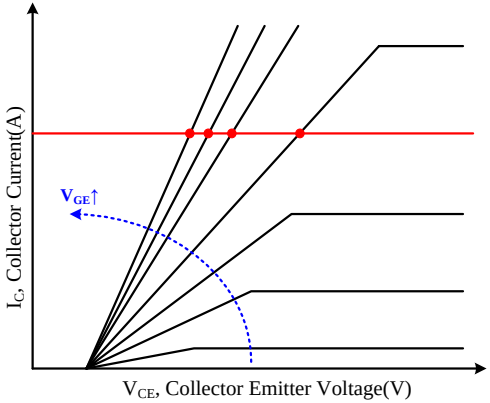


Comprehensive thermal run to extract the thermal impedance of different configurations.

Short Circuit Protection: DESAT







Blanking time: $t_{DS_BLK} = \dfrac{V_{DESAT} \times C_{BLK}}{I_{CHG}}$

- DESAT function is used to detect power transistor short circuit fault, and take protective measures to prevent power transistors from EOS damages.
- This approach is more common for applications with a system voltage less than 1200V as DESAT diodes with fast recovery are not easy to find at higher voltage levels.

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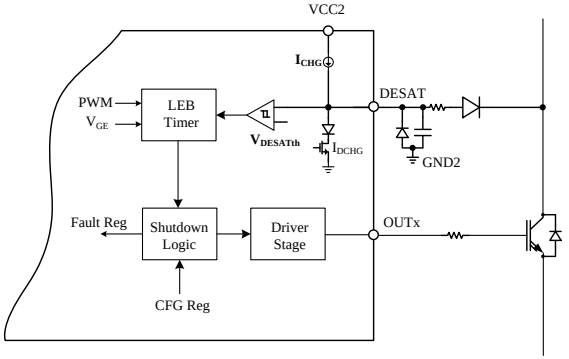
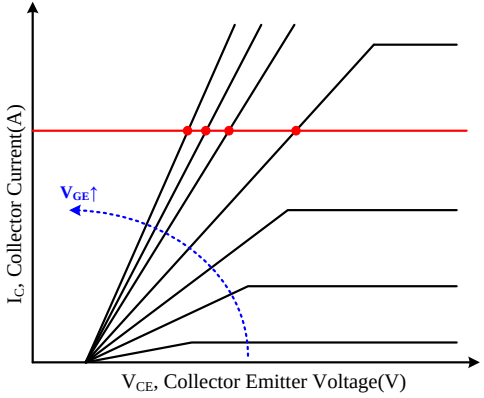
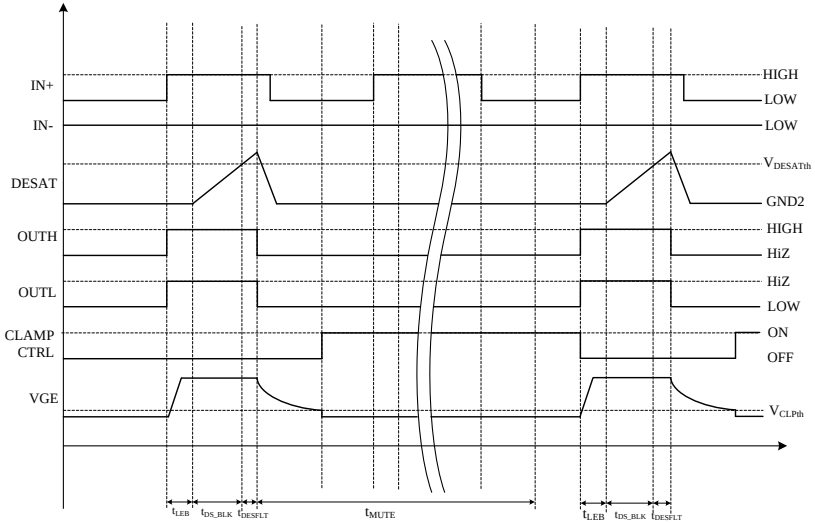
Short Circuit Protection: DESAT







Blanking time: $t_{DS_BLK} = \dfrac{V_{DESAT} \times C_{BLK}}{I_{CHG}}$

- The short circuit withstand time is around 10us for IGBTs.
- The short circuit withstand time for SiC depends on the system voltage, short circuit current, and critical energy of SiC FET.

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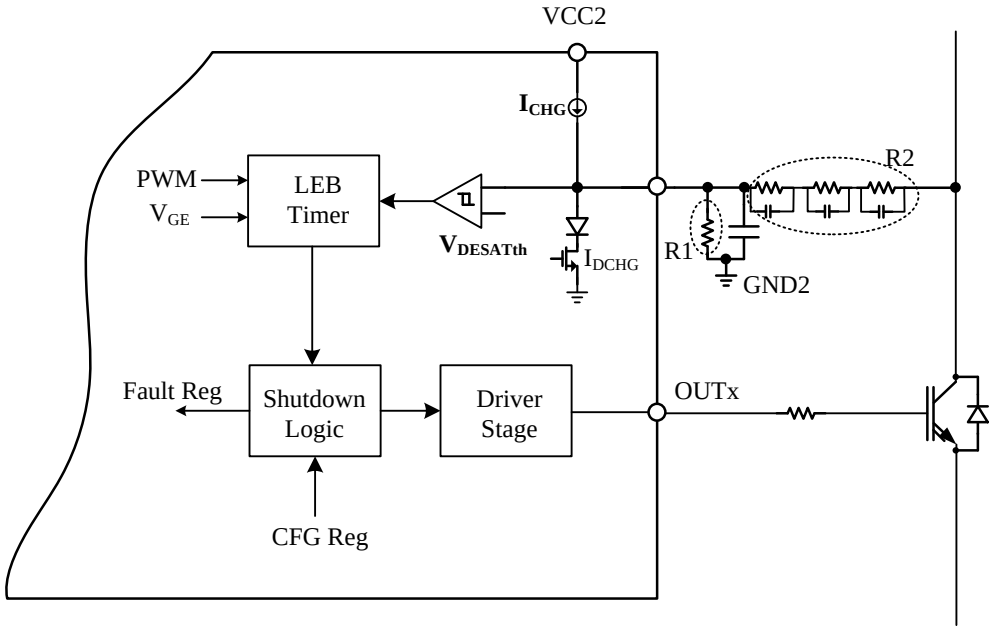
Short Circuit Protection: DESAT

- **The short circuit withstand time can be roughly calculated by the critical energy.**
- **The energy pulse generated during short circuit fault can be calculated as:**
  - $Ec = V_{DS} \times I_D \times t_{SC} \times 0.5$
  - V_{DS} is the dc link voltage
  - I_D is the peak current which is $I_D = V_{DS} \times \frac{t_{SC}}{L}$
  - The short circuit current is eventually limited by V_{DS}/R_{DSON}
  - The speed that the short circuit current rises depends on L/R_{DSON}
  - t_{SC} is the duration of the short circuit event
  - L is the loop inductance

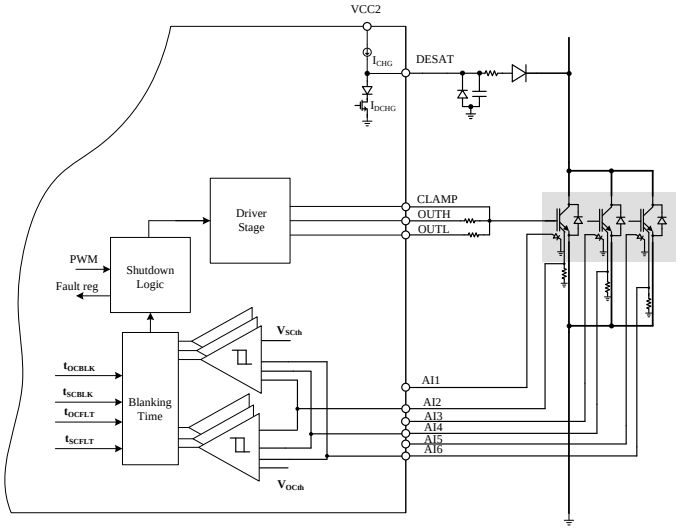
- ***The short circuit withstand time can be represented as***:
  - $t_{SC} = 0.5 \times \sqrt{E_C \times L}/V_{DS}$
  - Withstand time is also temperature dependent. Take the worst case for calculation.

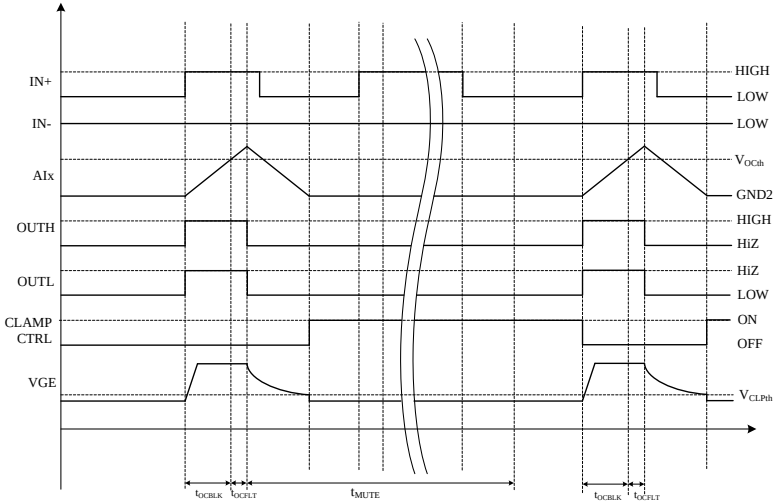
Short Circuit Protection: Voltage Divider



- Resistor divider R1 and R2 are used to scale the VCE/VDS down to a level within the ROA region of gate driver IC.
- High resistance values need to be used for R1 and R2 in order to limit the power loss.
- The high R2 value would limit the response speed because of RC delay.
- Capacitor can be added in parallel with resistor to boost-up the speed while can introduce additional power transistor switching loss.
- Usually, lots of discrete resistors are used to form R2 in order to find a sweet spot between power loss and response time.
- This approach is mostly used for applications where system voltage is higher than 1700V.

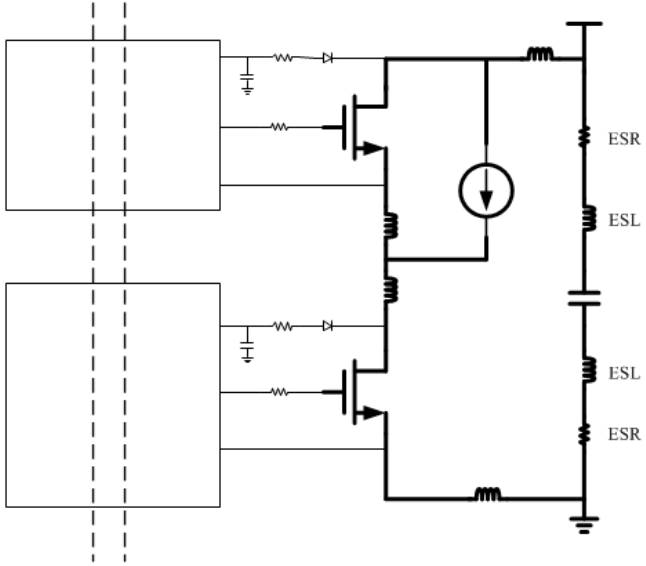
Short Circuit Protection: Current Mirror

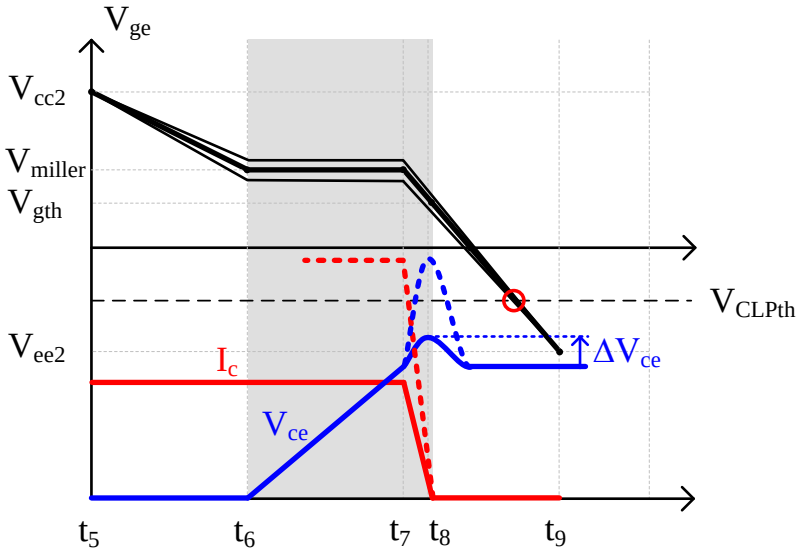




- Power transistor channel current is scaled down by a factor of 1,000 to 10,000 with integrated current mirror circuits.
- A shunt resistor is used to sense the scaled down current.
- **Faster and more accurate protection can be achieved**.
- Modules with current mirror are **more expensive due to more complex manufacturing process**.
- It is more commonly seen in automotive applications.

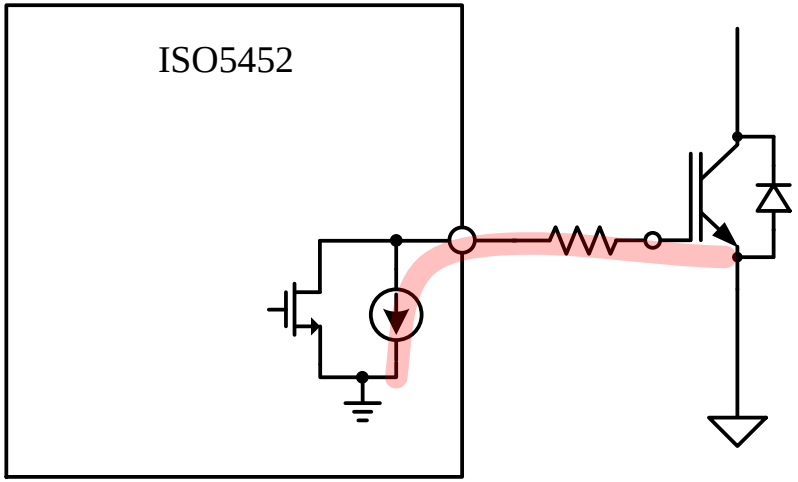
Over Voltage Protection





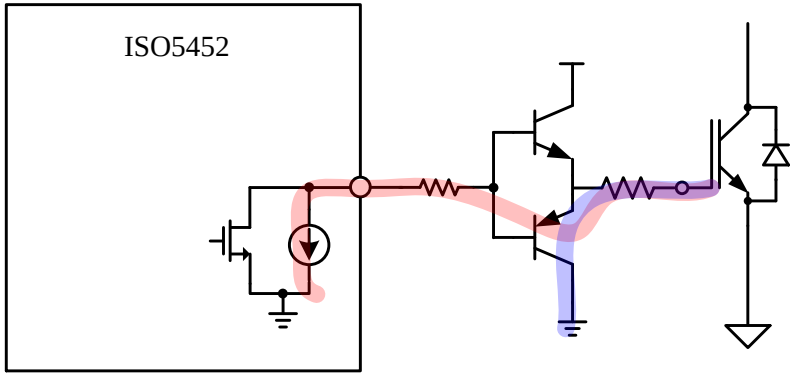
- There are parasitic inductances in the power loop.
- Parasitic inductances together with di/dt cause voltage spikes.
- **The di/dt rate is much higher under short circuit fault** that a preventive turn-off measure needs to be taken in order to limit the loop inductance induced voltage spike.
- Effectively, there are two ways to slow down the turn-off process: ***reduce di*** or ***extend dt***.

Over Voltage Protection: Soft Turn-Off (STO)



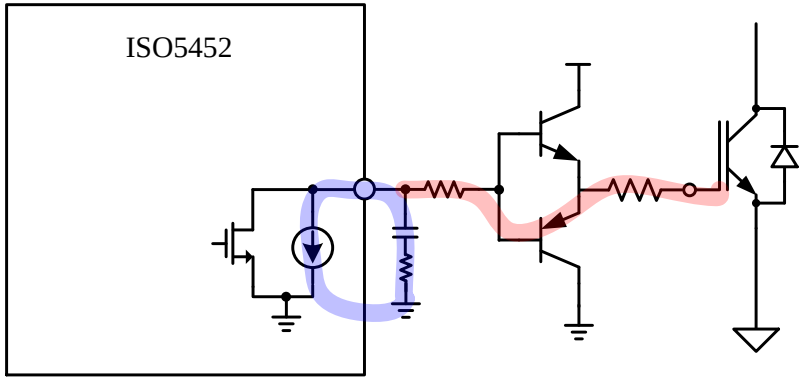
- A current source with an amplitude of 130mA is generated inside the gate driver to discharge IGBT gate capacitance under the condition of DESAT detection.
- IGBT is turned off in a soft manner and protected from OV breakdown.

Over Voltage Protection: Soft Turn-Off (STO)



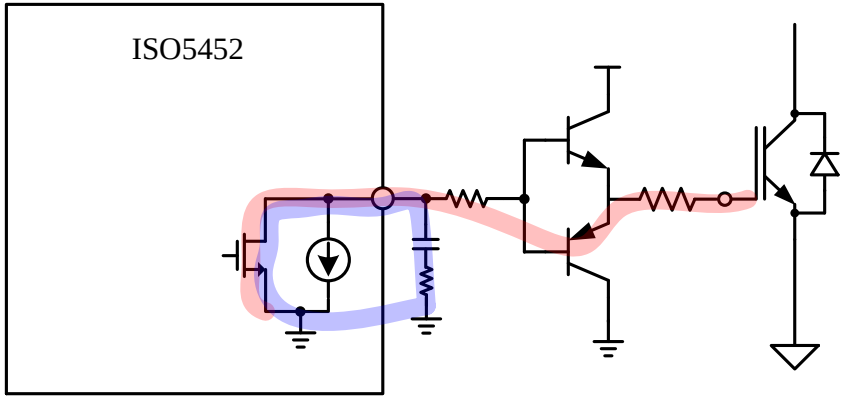
- A current source with an amplitude of 130mA is generated inside the gate driver to discharge IGBT gate capacitance under the condition of DESAT detection.
- The 130mA current is the base current of the external BJT. Such high base current would force the BJT to operate in saturation region.
- IGBT gate capacitance is discharged fast through the BJT CE channel, which is a hard turn-off mode for the IGBT.
- IGBT would face the potential of OV breakdown because of high di/dt.

Over Voltage Protection: Soft Turn-Off (STO)



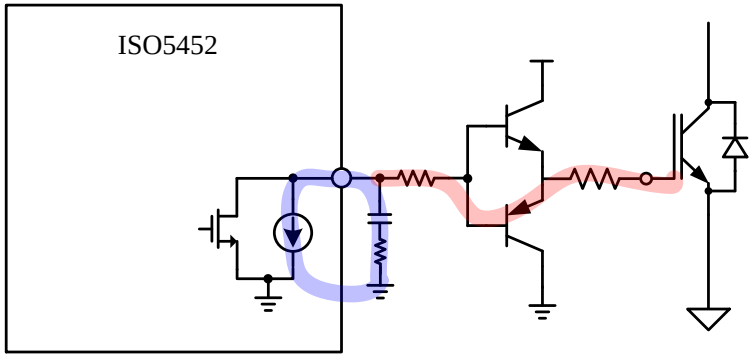
- A current source with an amplitude of 130mA is generated inside the gate driver to discharge IGBT gate capacitance under the condition of DESAT detection.
- The 130mA is used to discharge the STO cap in a slow manner, and the voltage across the ECB cap reduces slowly.
- BJT is functioning as a source follower, thus the emitter voltage also reduces slowly, which means the IGBT capacitance is discharged in a slow manner.
- IGBT is turned off in a soft manner.

Over Voltage Protection: Soft Turn-Off (STO)



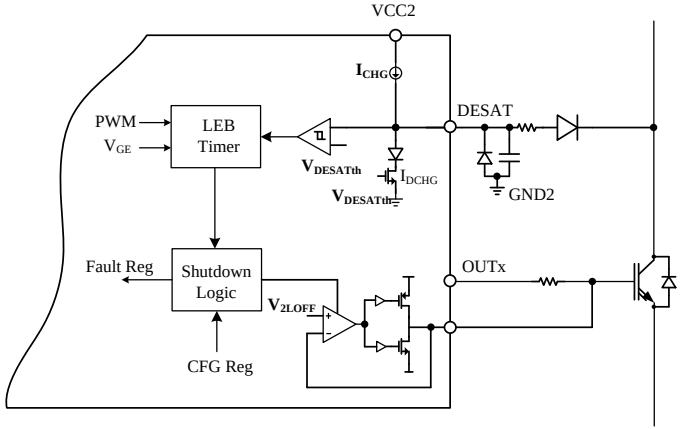
- In the regular turn-off session, the low side FET in the driver would short the STO cap, and an inrush current is generated. The inrush current may damage the gate driver.
- A resistor needs to be added in series with the STO cap to limit the inrush current.
- The low side FET can sink 5A current. A resistor of 5Ω is a good option to limit the inrush current.

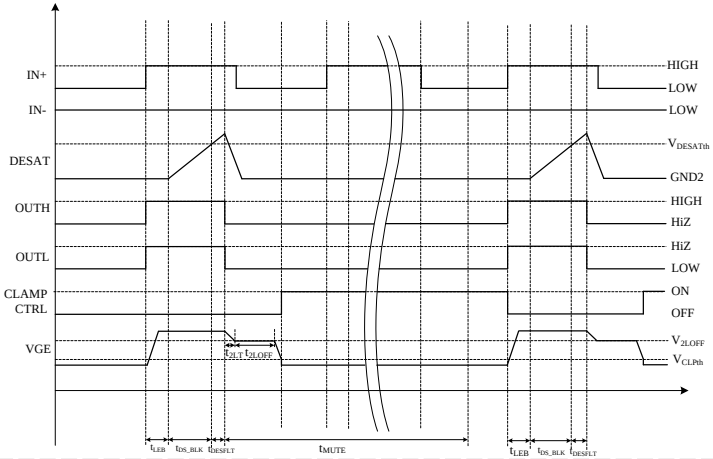
Over Voltage Protection: Soft Turn-Off (STO)



- In the case of short circuit fault, ISO5452 generates a current source of 130mA.
- This current source is used to discharge the STO cap, the value of the STO cap can be calculated as $C = (I \times T_{off})/(V_{CC2} - V_{EE2})$
  - Where I is the value of the current source which is 130mA
  - T_{off} is the desired soft turn-off time
  - V_{CC2} and V_{EE2} are the supply voltages
  - C is the STO cap.
- R can be calculated based on the inequality $R > (V_{CC2} - V_{EE2})/5$

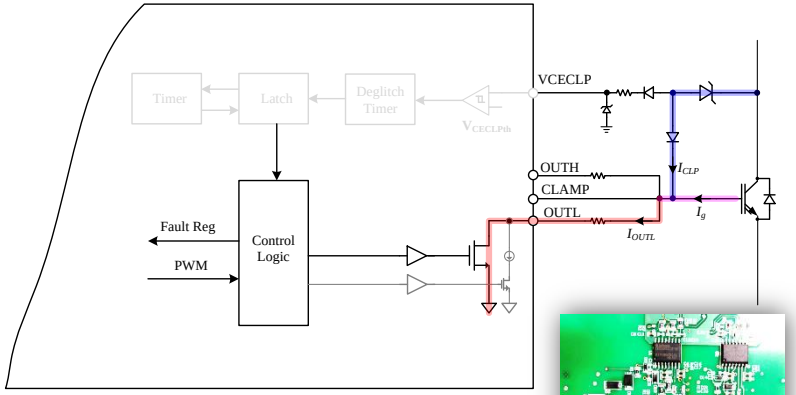
Over Voltage Protection: Two-Level Turn-Off (2LOFF)

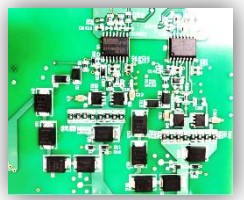




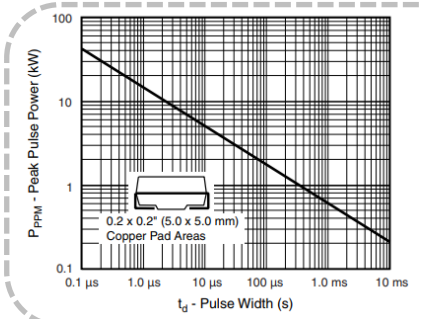
- In case of short circuit fault, the gate voltage is reduced to an intermediate level first before it is fully pulled down to ground.
- The intermediate voltage can be used to reduce the short circuit current.
- In the duration of a short circuit fault, an IGBT operating as voltage controlled current source while a SiC MOSFET is operating as a voltage controlled impedance.
- The di/dt rate is reduced through **reducing the di**.
- The two-level turn-off circuit can work with external buffer by nature.
- The driver output needs to have low impedance in the duration intermediate voltage level in order to have robust operation. ***Commercially available drivers have high Z.***

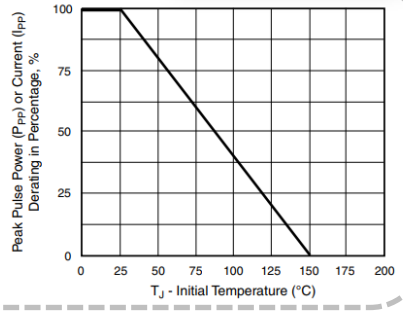
Over Voltage Protection: High Voltage Clamping





Source: Vishay



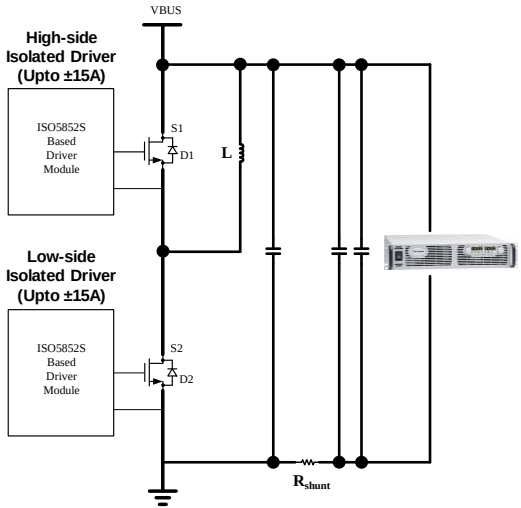


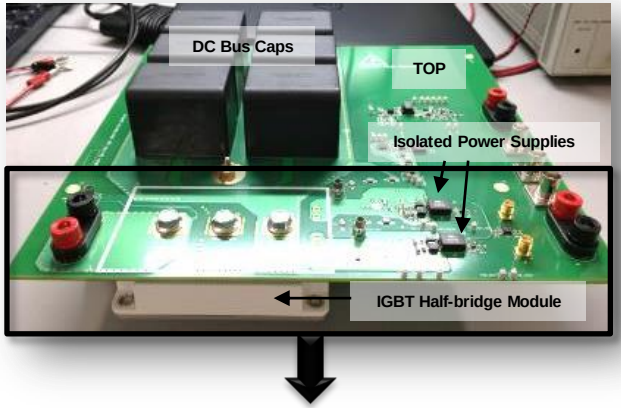
- TVS diode is used to clamp the voltage across the power transistor to be in SOA region.
- In case of OV condition, the TVS diode will be operating in reverse breakdown region, where a current I_{CLP} is injected to the gate terminal of the power transistor through the TVS diode.
- The I_{CLP} is used to diverge the driver pull down current I_{OUTL} from gate current I_g.
- Effectively, the turn-off time is extended that di/dt is reduced and voltage spike is suppressed.
- ***Challenges of high voltage clamping circuits***:
  - The clamp voltage changes with temperature and I_{CLP}, which can cause false triggering.
  - The TVS diode needs to handle high transient power V_{CLP} x I_{CLP}.
  - The TVS diode consumes lots of board space and comes with relatively high cost.

Short-Circuit Protection: Hardware Validation

Evaluation Hardware

Schematic for Double-Pulse Test Setup



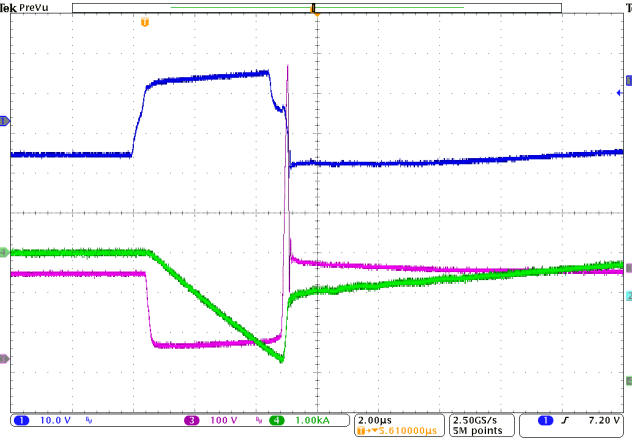


Isolated Half-bridge Drive Stage using ISO5852S-Q1 + 15A Buffer Driver

Texas Instruments

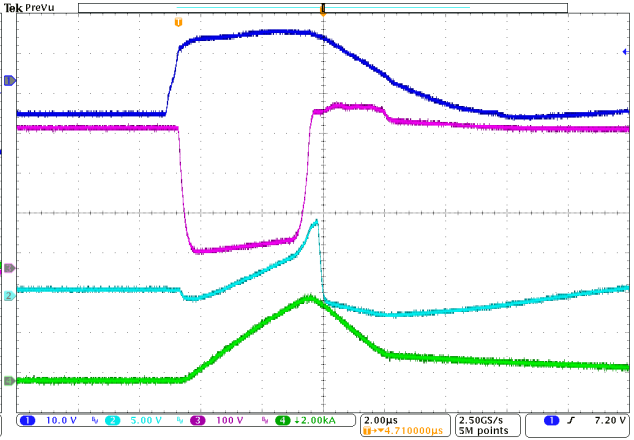
Short Circuit Protection for IGBT

VCE(100V/div), IC(1kA/div), VGE(10V/div)



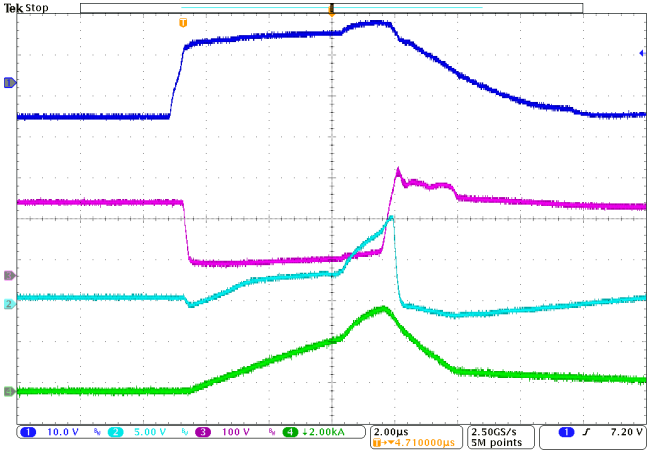
Hard Turn-off

VCE(100V/div), IC(2kA/div), VGE(10V/div), VDESAT(5V/div)



Soft Turn-off for Hard SC

VCE(100V/div), IC(2kA/div), VGE(10V/div), VDESAT(5V/div)

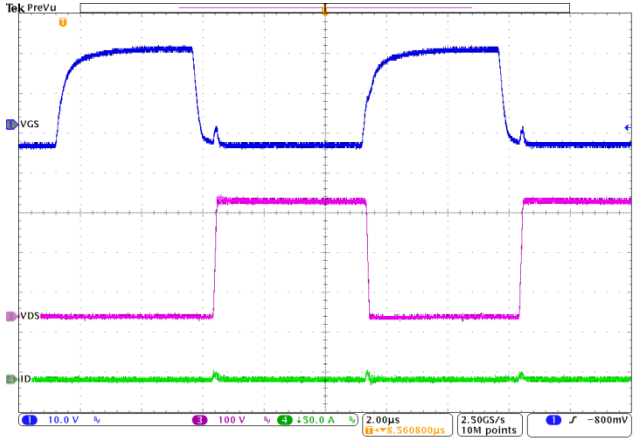


Soft Turn-off for SC under Load

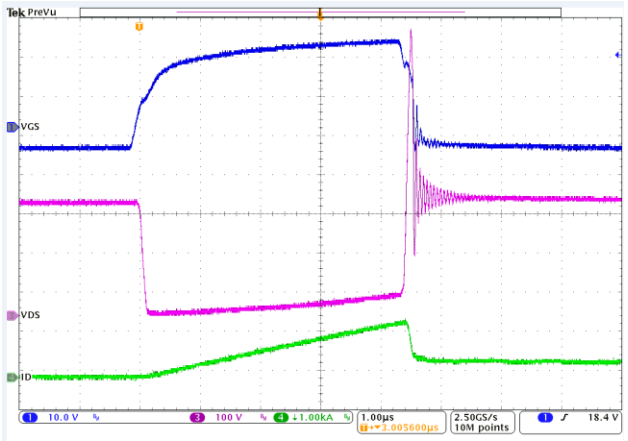
Texas Instruments

Double Pulse Test for SiC MOSFET

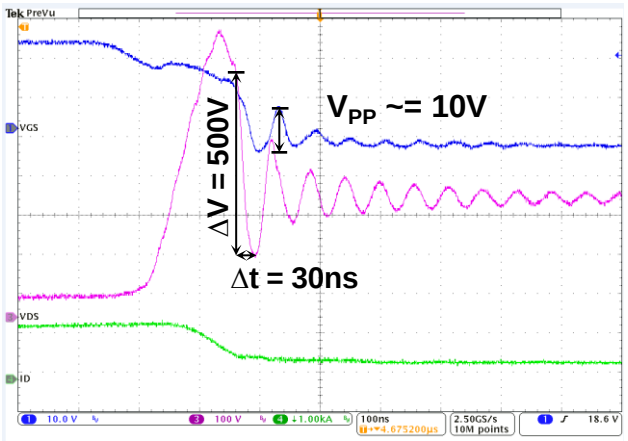
VDS(100V/div), IC(1kA/div), VGS(10V/div)



VDS(100V/div), IC(1kA/div), VGS(10V/div)

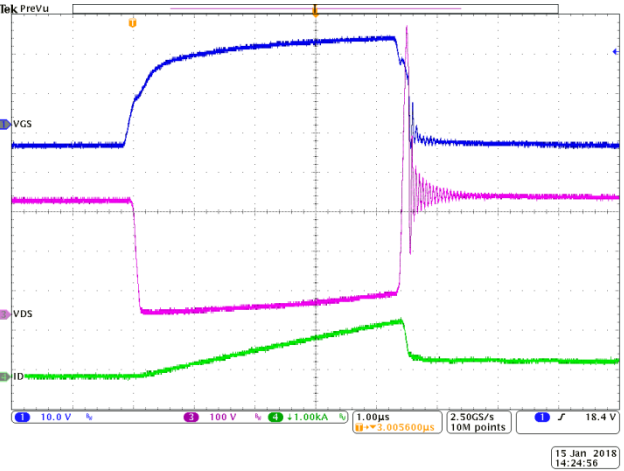


VDS(100V/div), IC(1kA/div), VGS(10V/div)



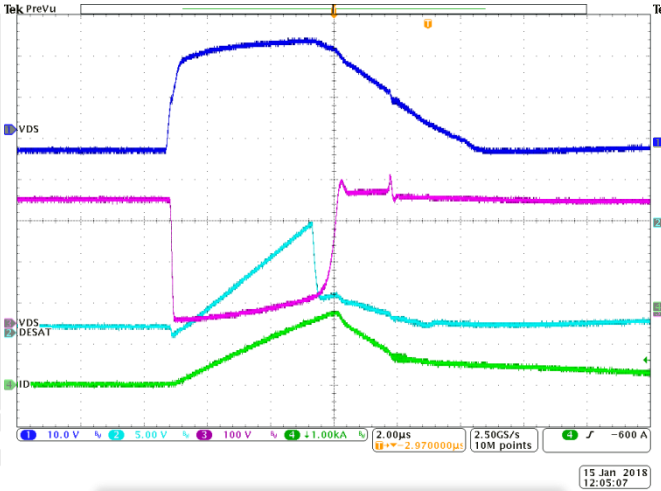
Short Circuit Protection for SiC

VDS(100V/div), IC(1kA/div), VGS(10V/div)



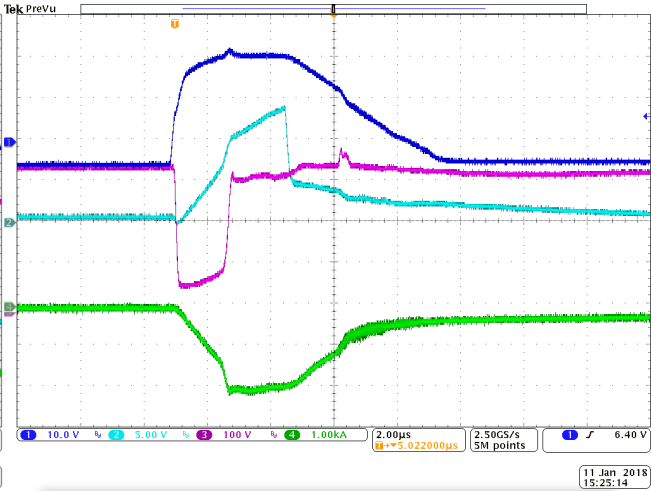
Hard Turn-off

VDS(100V/div), IC(1kA/div), VGS(10V/div), VDESAT(5V/div)



Soft Turn-off for Hard SC

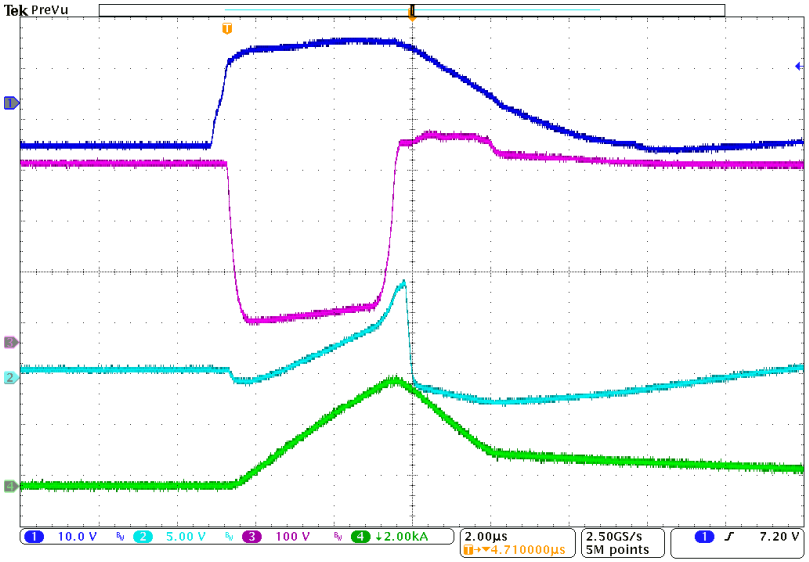
VDS(100V/div), IC(1kA/div), VGS(10V/div), VDESAT(5V/div)



Soft Turn-off for SC under Load

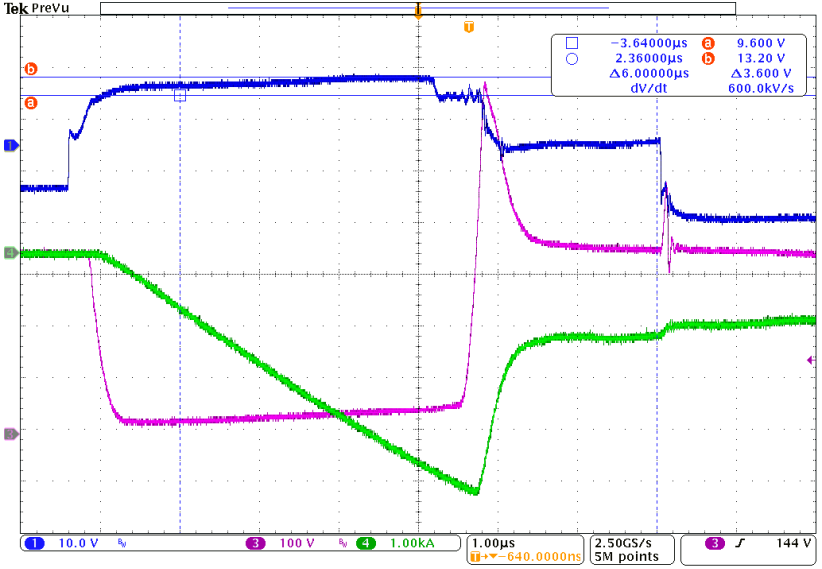
Short Circuit Protection: STO vs 2LTO

VCE(100V/div), IC(2kA/div),
VGE(10V/div), VDESAT(5V/div)



Soft Turn-off for Hard SC

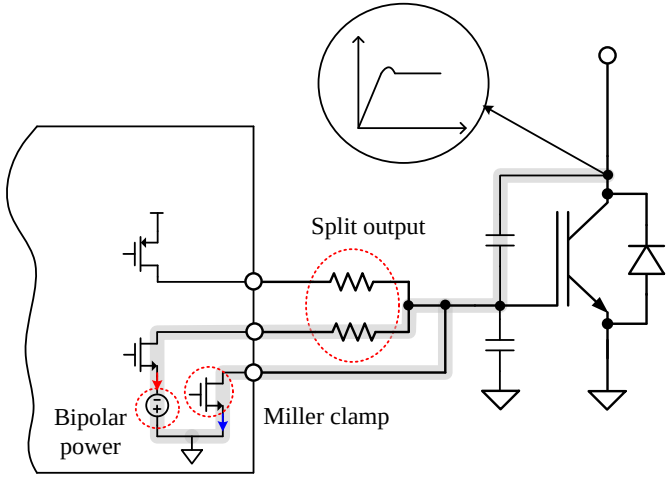
VCE(100V/div), IC(1kA/div),
VGE(10V/div)

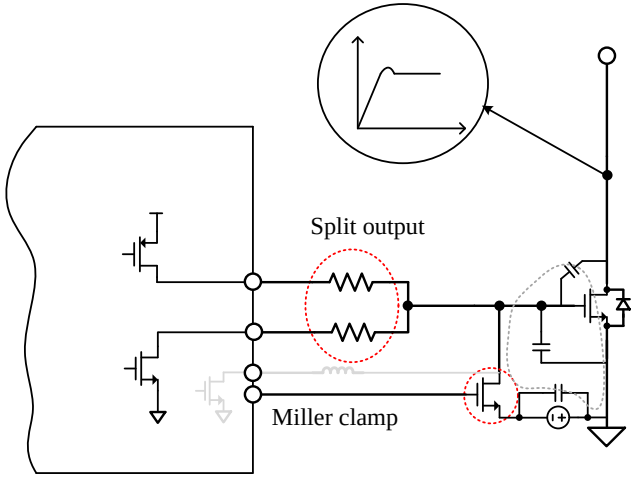


Two-level Turn-off for Hard SC

Texas Instruments

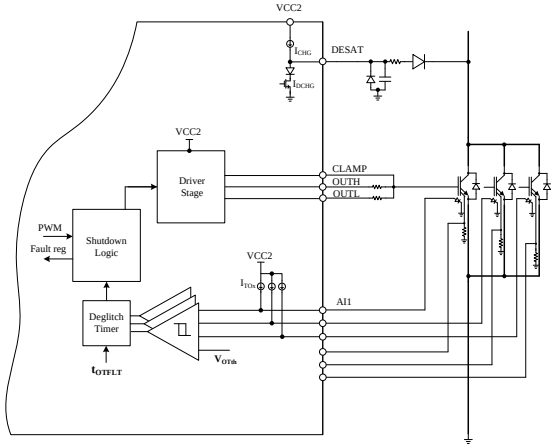
Active Miller Clamp



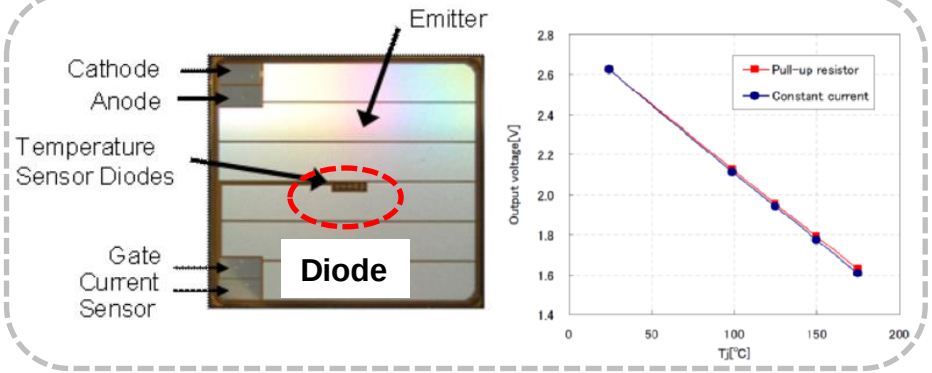


- Miller clamp is used to prevent power transistor from falsely turn-on due to the parasitic Miller capacitance.
- The Miller clamp function is implemented by adding a low impedance path between power transistor gate and power supply ground.
- Proper use of Miller clamp function can potentially help remove the needs of negative power supply.
- For SiC applications, both negative supply and Miller clamp functions are needed as the ***Crss/Ciss*** ratio is high. External Miller clamp can be more effective because of lower loop inductance.

Over Temperature Protection: Diode

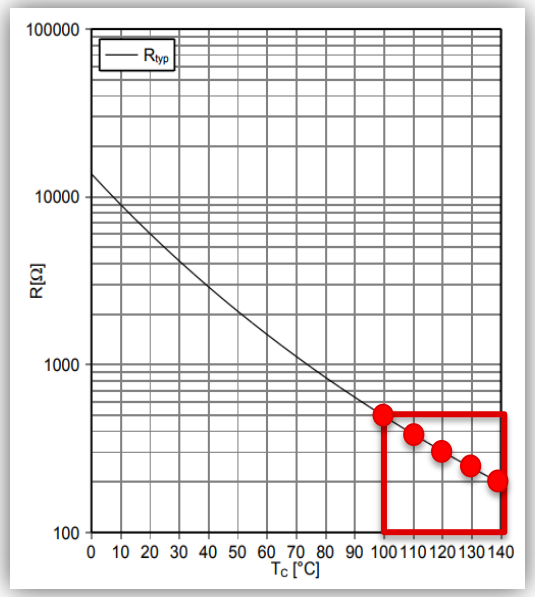


Photo/graph complements of Mitsubishi Electric US.

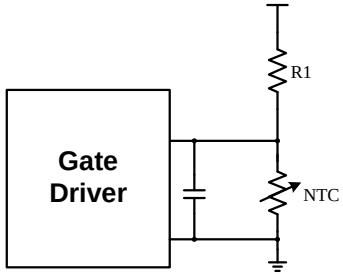


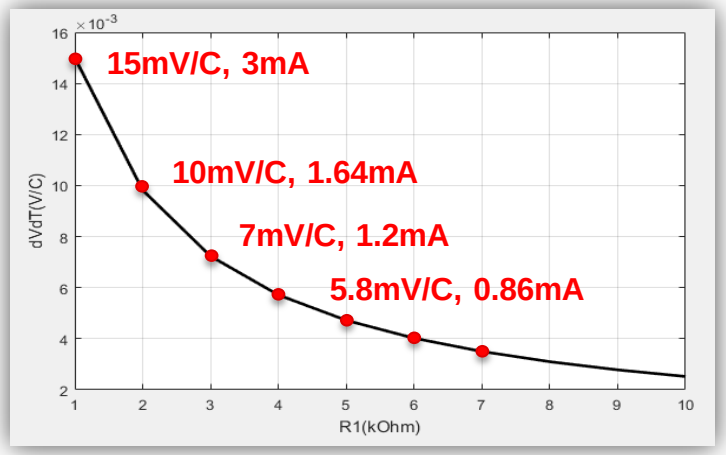
- The voltage across temp sense diode drops as temperature increases.
- The voltage across the temp sense diode can be sensed and interpreted as temp info. The voltage sensitivity to temperature is usually ***2mV/°C***.
- The ***V-T*** relationship is usually pretty linear while there are offset voltage due to process variations and needs to be calibrated in production.
- The diode is sitting together with the power transistor that ***junction temperature can be sensed directly*** that better accuracy can be achieved.
- An accurate bias current needs to be used to bias the diode to operate in the linear region.
- ***The temp sense accuracy and dynamic response are better than that with NTC based solution***.

Over Temperature Protection: NTC



Source: FP75R12KT4

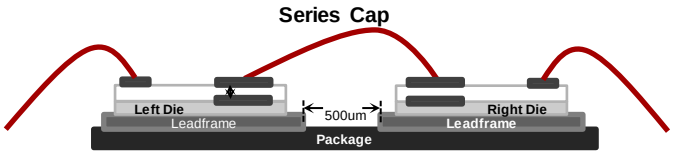




- The resistance of NTC changes with temperature.
- Temperature can be estimated with the NTC resistance based on predefined **R-T** curve.
- The NTC resistance can be measured through a voltage divider circuit. The temp sense resolution depends on the total impedance.
- The NTC is usually mounted on the base plate. The junction temperature of the power transistor is estimated per predefined $\boldsymbol{\theta_{JC}}$. Which limits temp sense accuracy.
- Response is slow with time constant of seconds.

HV Isolation

Technology Innovation

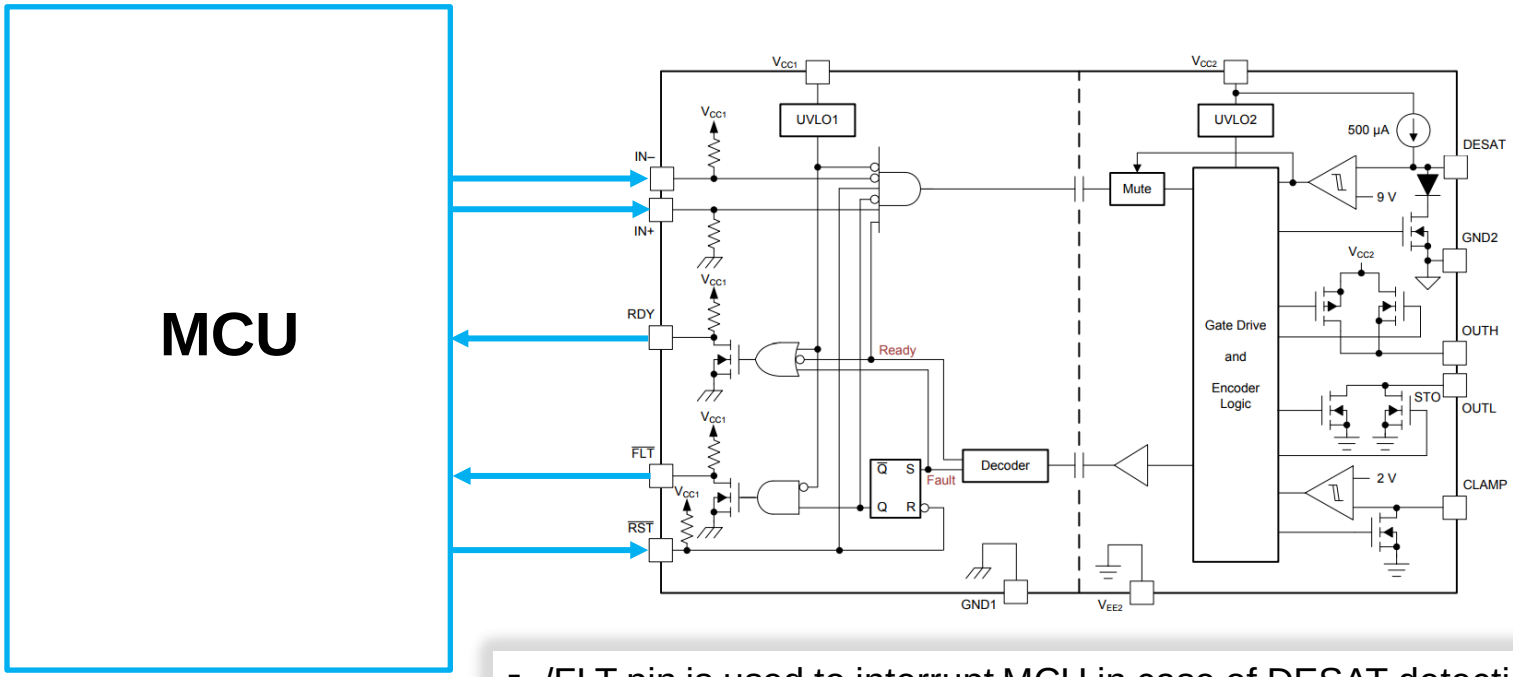


- Reinforced Isolation realized by Series Capacitor configuration
- Combined Isolation capacitor thickness is ~27um (SiO2)
- Galvanic barrier provides extraordinary EM immunity and excellent isolation barrier lifetime
- On-die HV SiO2 capacitors deliver extremely tight tolerances and high precision

Competitive Landscape

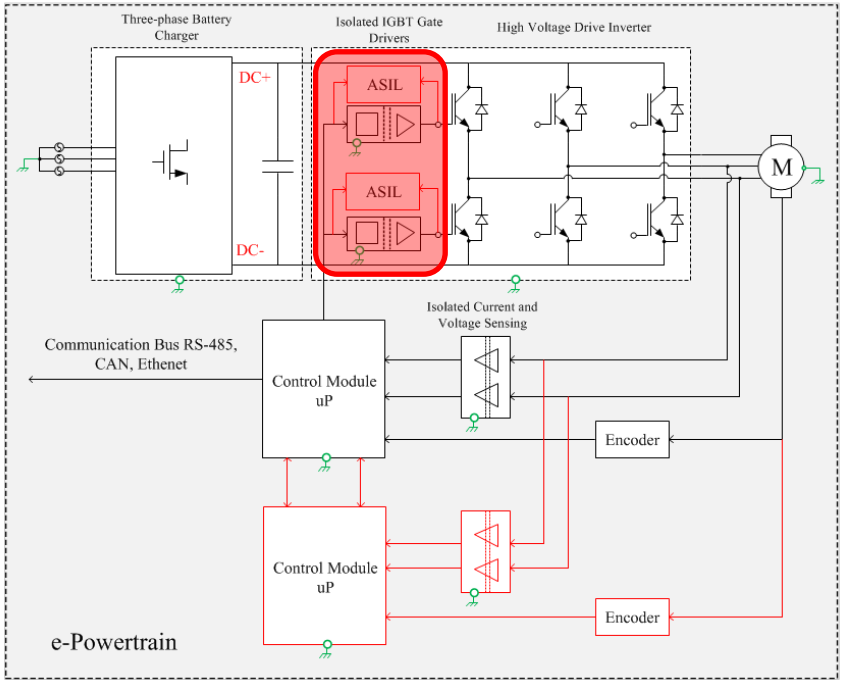
		TI Reinforced	Competitor A*	Competitor B*	Competitor C*
	Technology	Capacitor	Transformer	Opto	Capacitor
Strength	Reinforced	✔+	✔	✔	✔
	ISO Rating (1 minute withstand)	5.7 kVrms	5 kVrms	5.7 kVrms	5-5.7 kVrms
	ISO Surge (1us withstand)	12.8+ kVpk	16 kVpk	10+ kVpk	10 kVpk
	ISO Working Voltage (Lifetime Withstand)	1.5+ kVrms	600 Vrms	1 kVrms	1 kVrms
Robustness	EM Emission	Lowest	High		Lowest
	EM Immunity	Level 3	Level 3		Level 3
	CMTI (Minimum)	100KV/us	75KV/us		60KV/us
	Recovery from errors	1 * Prop. Delay	1*Prop Delay		1 * Prop. Delay
Performance	Power @1Mbps (/ch)	1.7mA	0.16mA		1.9mA
	Power @ 10Mbps (/ch)				
	Prop delay (Typical)	10 ns	7.5 ns		8ns
	Part-Part Variation	<4ns			
	Jitter (Typical)	1ns	<0.5ns		1ns

Status Feedbacks and Diagnosis



- /FLT pin is used to interrupt MCU in case of DESAT detection.
- RDY pin is used to indicate the condition of VCC2.
- /RST pin is used to reset driver once the fault condition is removed.

Functional Safety Support



- Integrated protection, monitor, and diagnosis functions can be integrated to support/simplify system design.
- Safe mechanisms are integrated to reduce system FIT.

Detailed agenda

- *Brief introduction to isolated gate driver use case in automotive applications*

- *Deep dive of functional blocks in an isolated gate driver*
  - **Power supply**: architecture, topologies, and protection functions
  - **PWM input**: *CMOS input, current input, and interlock and shoot-through protection*
  - **Output stage**: *integrated buffer or external buffer?*
  - **Short circuit and over current protection**: *DESAT, resistor voltage divider, or sense FET?*
  - **Overvoltage protection**: *Soft turn-off, two-level turn-off, or high voltage clamping?*
  - **Active Miller clamp**: internal vs external
  - **Over temperature protection**: *NTC or diode?*
  - **HV isolation**: *capacitor, transformer, or opto-coupler?*
  - **Status feedback and diagnosis**

- ***TI Designs***

ISO54XX/58XX: EVMs + TIDesigns

Type	Link	Description
EVM	ISO5851EVM	ISO5851 Evaluation Module Board
TIDesign	TIDA-01606	**10kW 3-Phase 3-Level Grid Tie Inverter** Reference Design using **SiC MOSFETs** for Solar String Inverter Board using
TIDesign	TIDA-00195	Isolated IGBT Gate Driver Evaluation Platform for **3-Phase Inverter** System Reference Design Board
TIDesign	TIDA-00446	Small Form-Factor Reinforced Isolated IGBT Gate Drive Reference Design for **3-Phase Inverter** Board
TIDesign	TIDA-00917	Gate Driver Reference Design for **Parallel IGBTs** With Short-Circuit Protection and Current Buffer Board
TIDesign	TIDA-00638	Reference Design for Isolated Gate Driver Power Stage with Active Miller Clamp for Solar Inverters Board

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