Understanding the SAR Reference Input Model

TIPL 4504
TI Precision Labs – ADCs

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Agenda

Reference Performance Specifications:

- Initial Accuracy, Drift, Long Term Drift, and Noise

Overview of SAR REF Drive Topologies:

- Reference standalone VS Buffered Reference
- SAR ADCs with Internal Reference Buffer

SAR REF Input Overview: The Capacitive DAC (CDAC)

Build TINA REF Input Model for a SAR:

- **Discrete Charge Model**
- TI Device Specific Model

SAR REF Drive Circuit Design:

- Reference Bypass Capacitor
- Reference Buffer Stability and Compensation

Important Datasheet Parameters

Example: ADS8881 18-B, 1-MSPS, Fully-Differential Input ADC

Sampling Rate = 1-MSPS
Throughput Period: t_{cycle}=1µs
Conversion Time: t_{conv}=710ns (max)

Input Equivalent Circuit: R_{SH} / C_{SH}

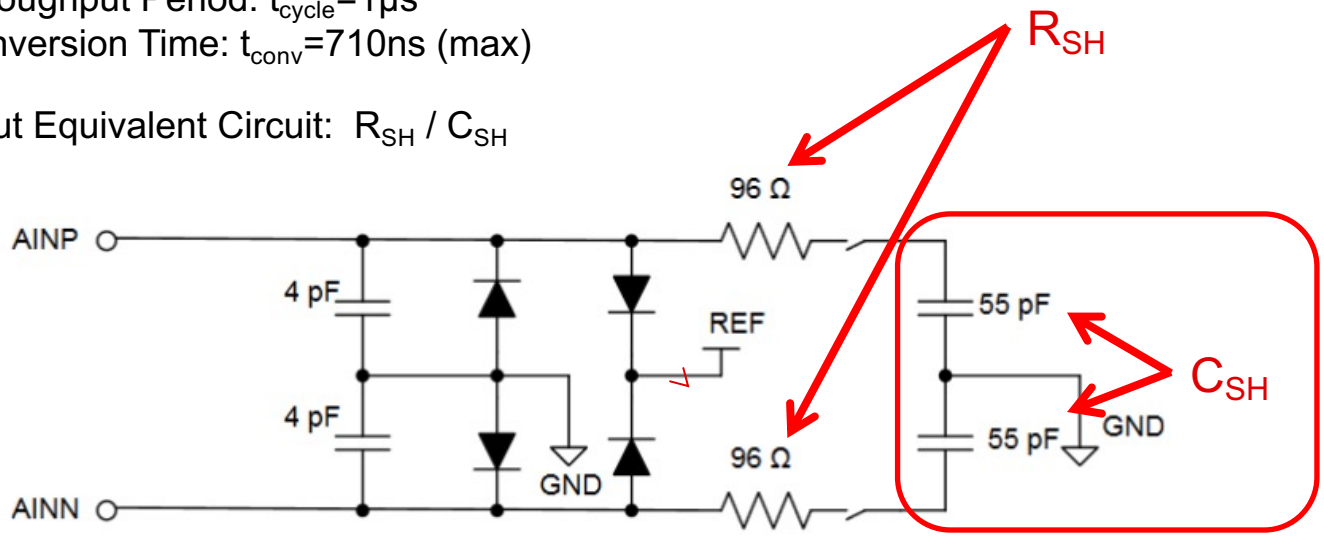


Figure 47. Input Sampling Stage Equivalent Circuit

Important Datasheet Parameters

Example: ADS8881 18-B, 1-MSPS, Fully-Differential Input ADC

VREF = 5V
Fully-Differential Input ADC

Full-scale Range: ±VREF = ±5V = 10V

ADC Resolution / Least Significant Bit (LSB):

$$LSB = \frac{\pm VREF}{2^N} = \frac{2 \cdot VREF}{2^{18}} = 38.14uV$$

$$\frac{1}{2} LSB = 19.07uV$$

Important Datasheet Parameters

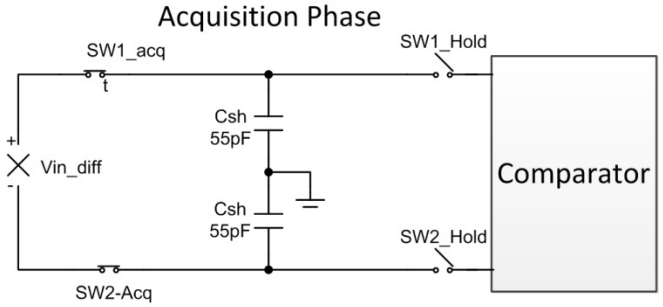
Example: ADS8881 18-B, 1-MSPS, Fully-Differential Input ADC

"Average" Reference Input Current:
Not a DC Current, combination of large fast current transients !!

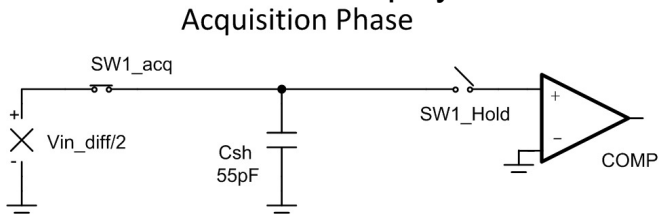
EXTERNAL REFERENCE INPUT					
V_{REF}	Input range	ADS8881C	3	5	V
		ADS8881I	2.5	5	
	Reference input current	During conversion, 1-MHz sample rate, mid-code		300	µA
	Reference leakage current			250	nA
C_{REF}	Decoupling capacitor at the REF input		10	22	µF

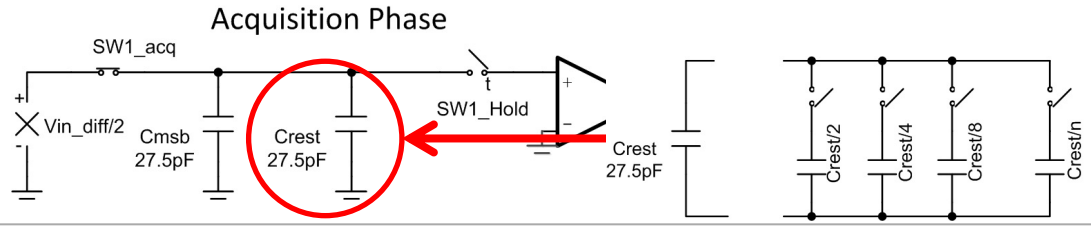
'Average' Reference Input Current at full throughput

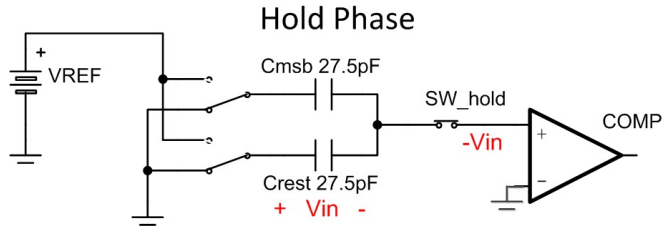
Estimate REFIN Capacitive Load:

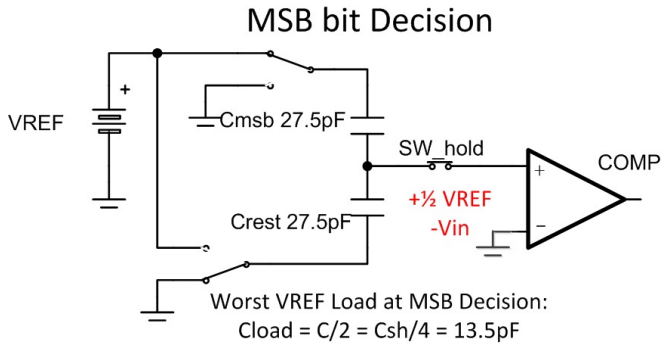


Simplify/Redraw as SE circuit









NOTE: REFIN Cmsb not always ¼ Csh; depends on device Architecture!!
This is a first order estimate.

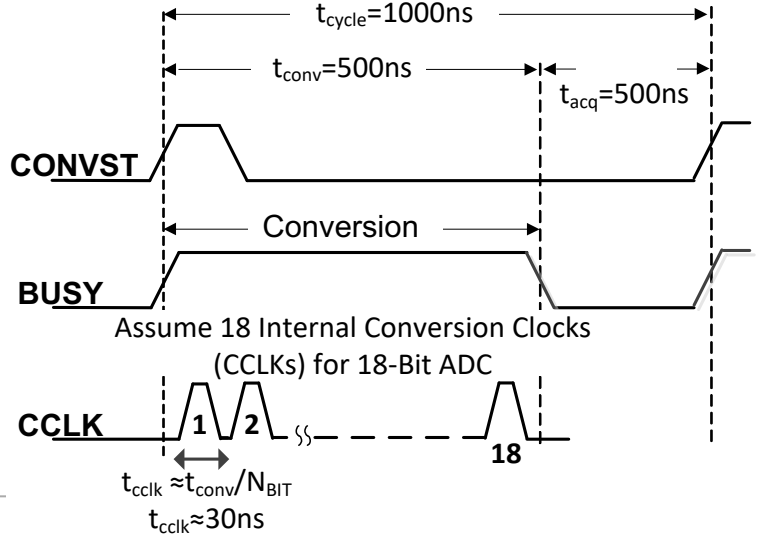
Conversion Period and Conversion Clock Timing

ADS8881 uses an internal conversion clock (CCLK)

Datasheet Specifies t_{conv} min

SAMPLING DYNAMICS					
t_{conv}	Conversion time		500	710	ns
t_{ACQ}	Acquisition time		290		ns
	Maximum throughput rate with or without latency			1000	kHz

Estimate internal Conversion Clock period



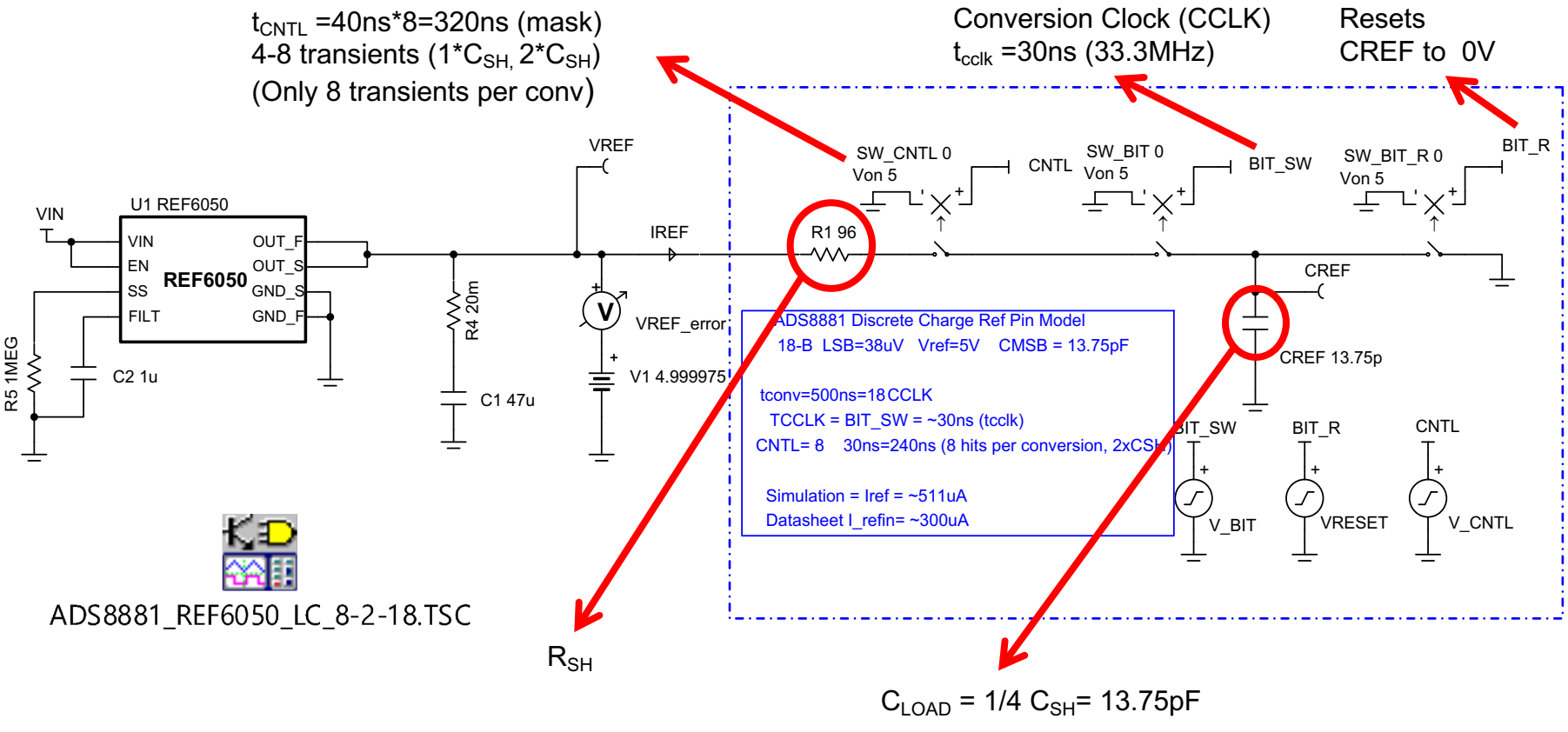
$$Fsample = 1000kHz$$

$$tcycle = \frac{1}{1000kHz} = 1us$$

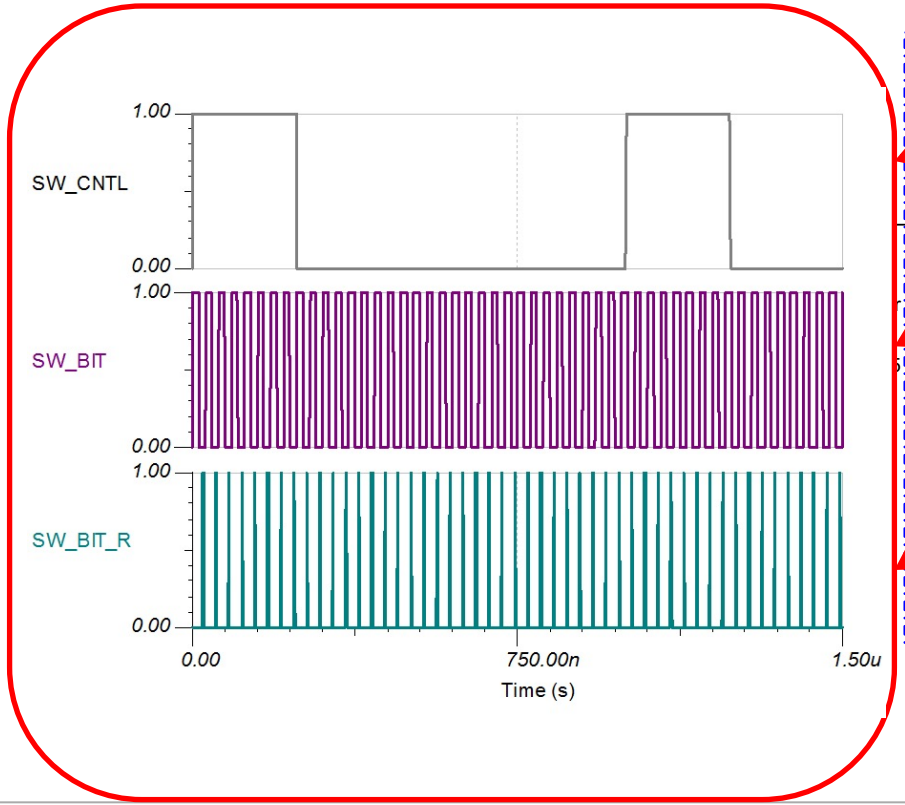
$$t_{conv} = 500ns$$

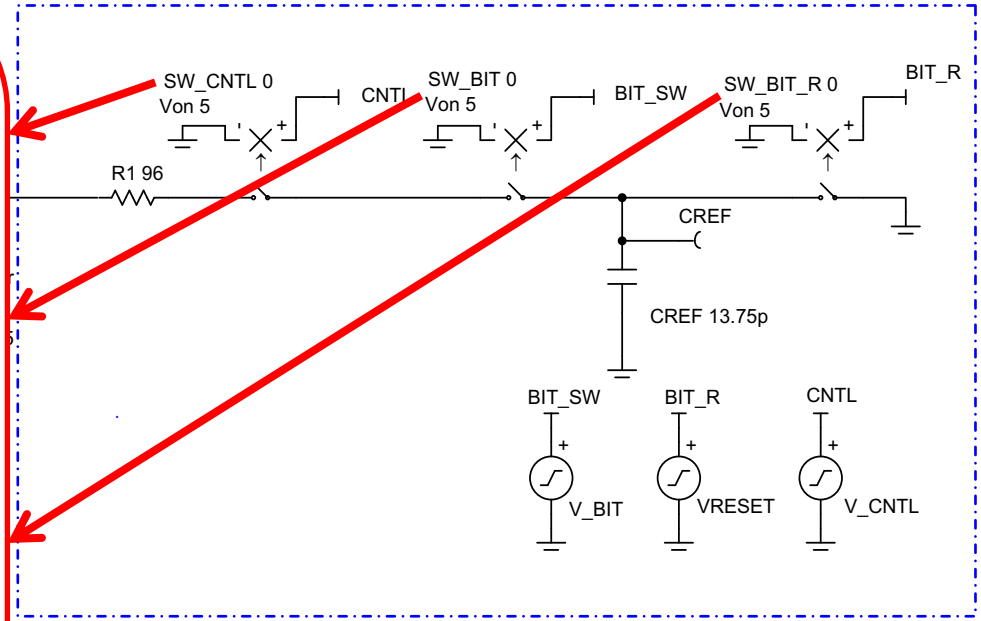
$$t_{cclk} \simeq \frac{t_{conv}}{N_{BIT}} = \frac{500ns}{18} \simeq 28ns$$

TINA SPICE Equivalent Model



TINA SPICE Equivalent Model





Thanks for your time!