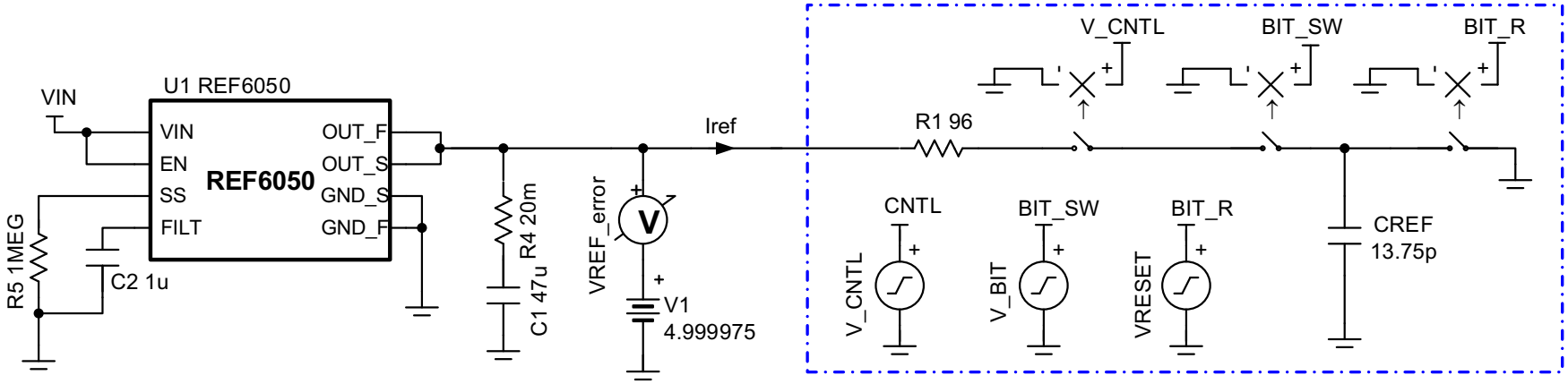
# Developing the SAR Reference Input Model

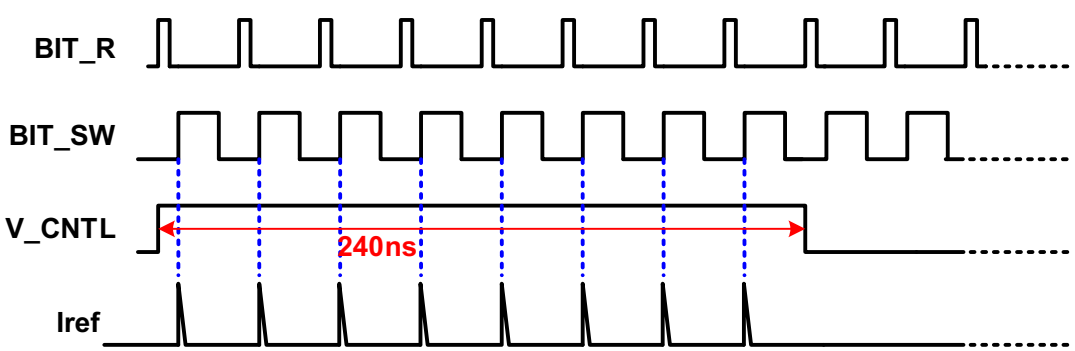
## TIPL 4505
## TI Precision Labs – ADCs

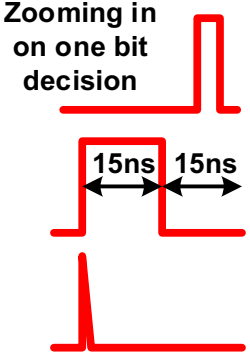
**Created by Luis Chioye**

**Presented by Cynthia Sosa**

# We need to configure the switch timing

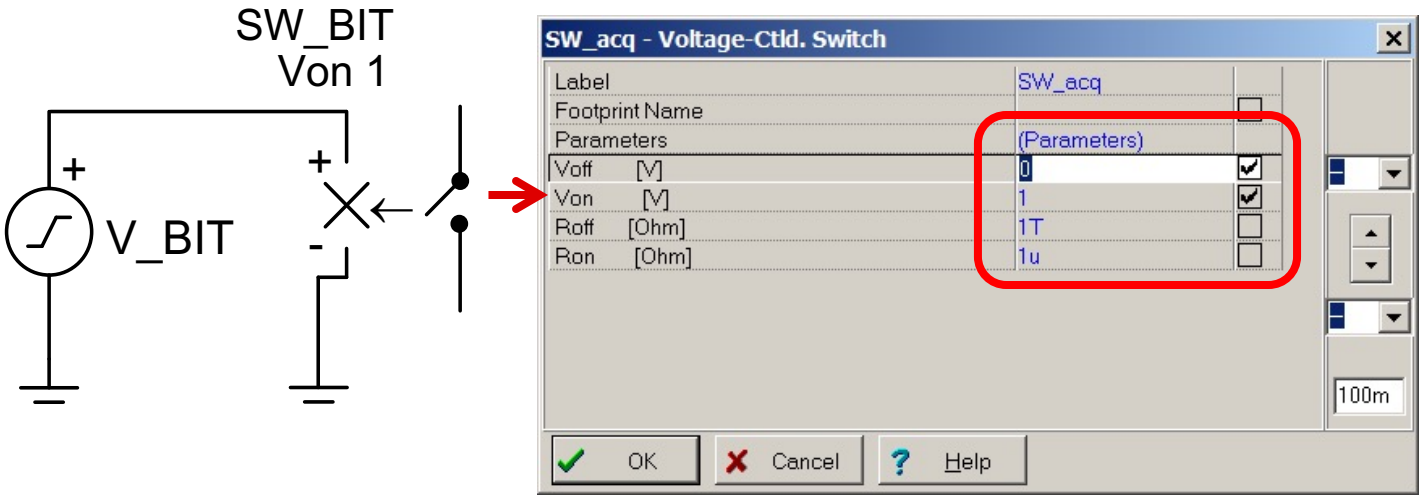



$$\frac{500ns}{18} \approx 30ns$$

# Configure the voltage controlled switch

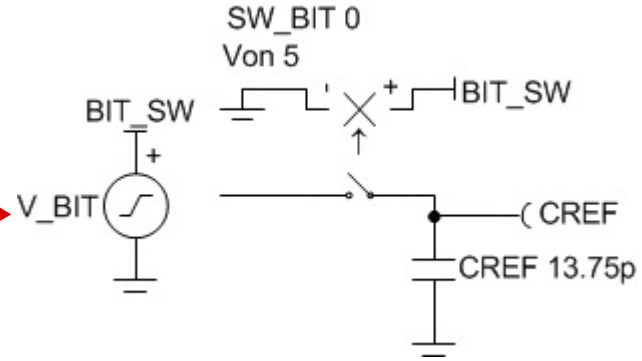



**Set all parameters as shown.**

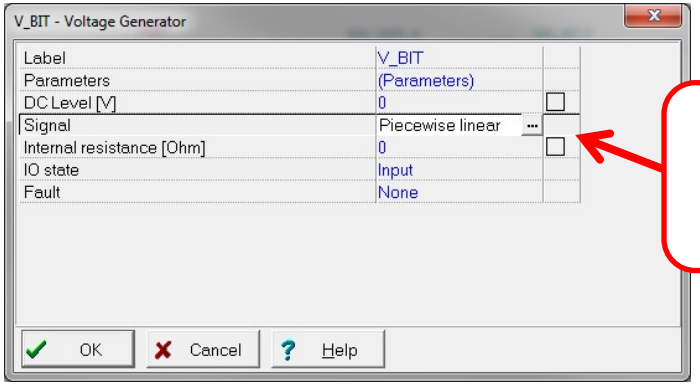
Default Roff=1GΩ and Ron=0Ω will impact accuracy.

# Configure the signal source to control the switch

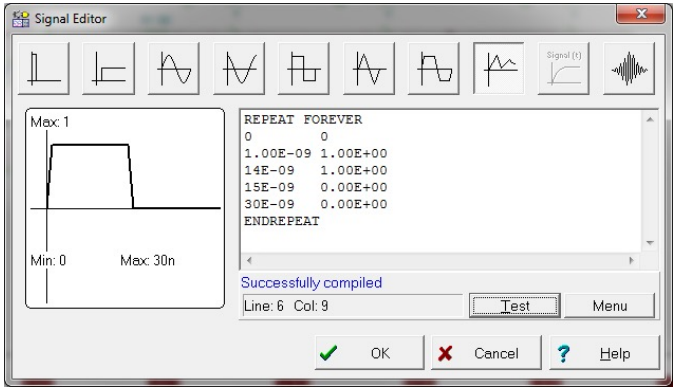
1. Click on source to select and edit switch control signal



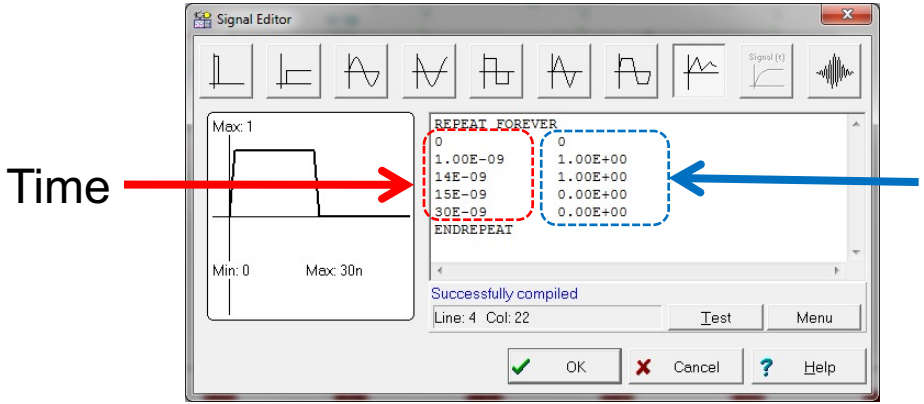

3. Select "Piecewise linear"




2. Under signal, click here to edit.

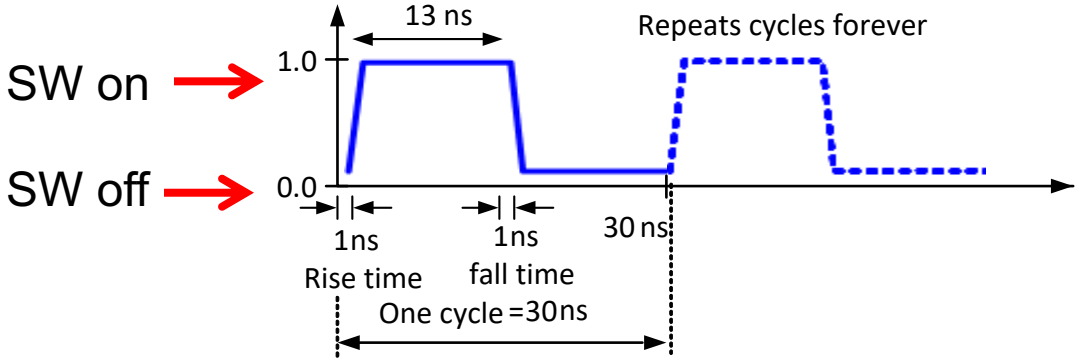


# Configure the signal source to control the switch



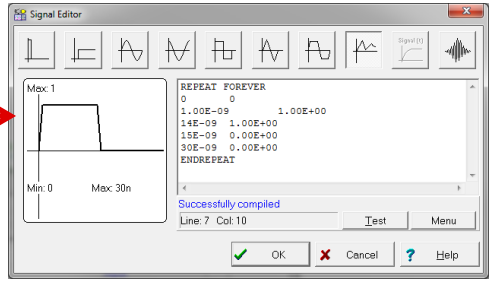

Time

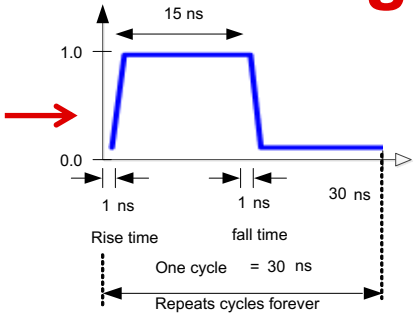
Voltage levels
On: V ≥ 1V
Off: V ≤ 0



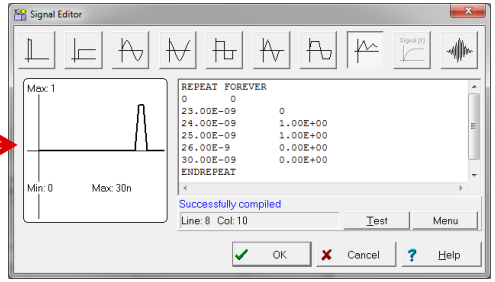
# Example simulation: simulator settings

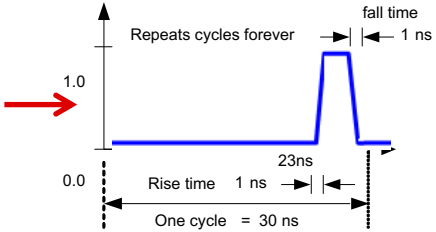
V_BIT



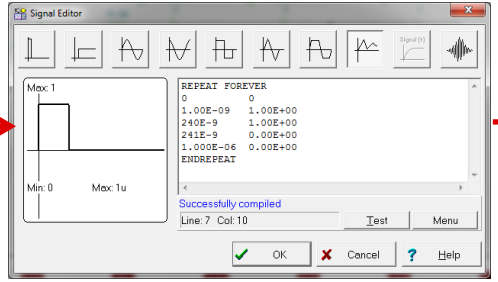



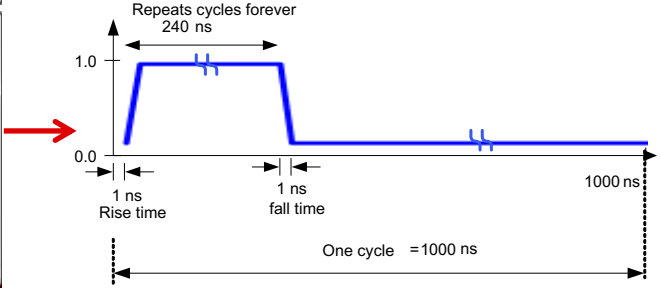

V_RESET



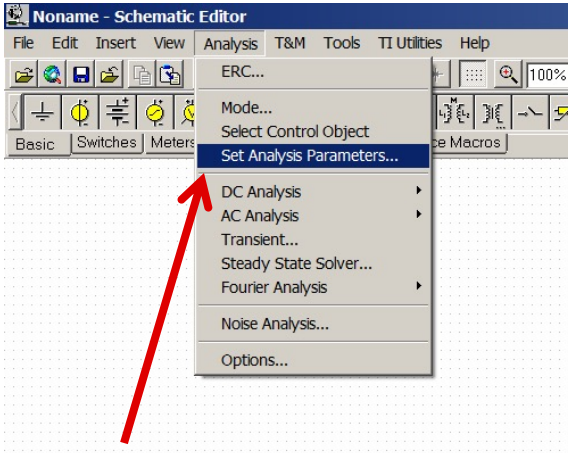




V_CNTL

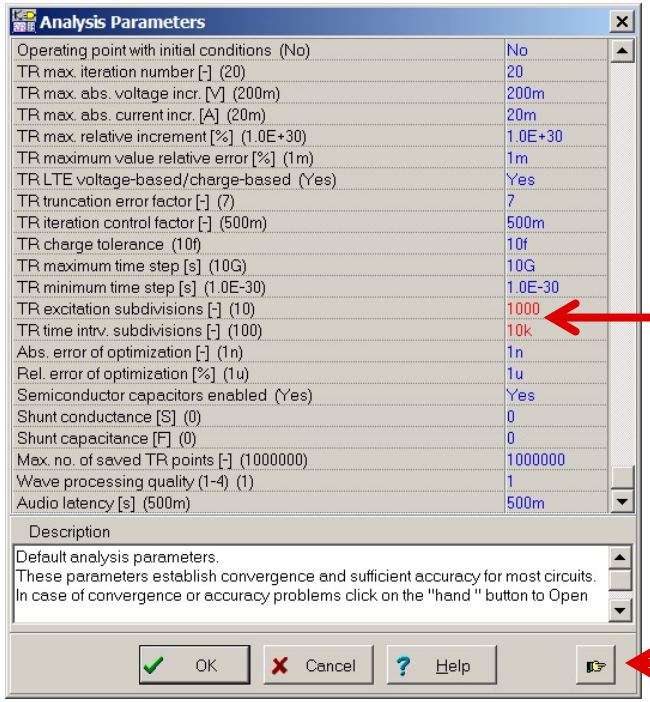


# Optimizing Simulation Results



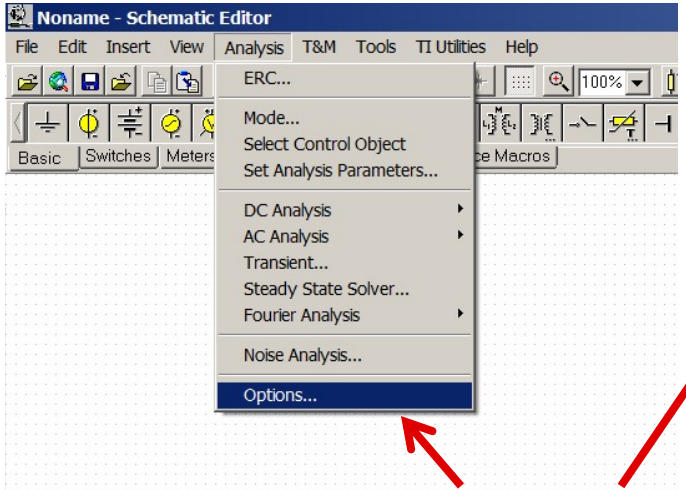

"Set Analysis Parameters" adjusts how the simulator math engine operates.

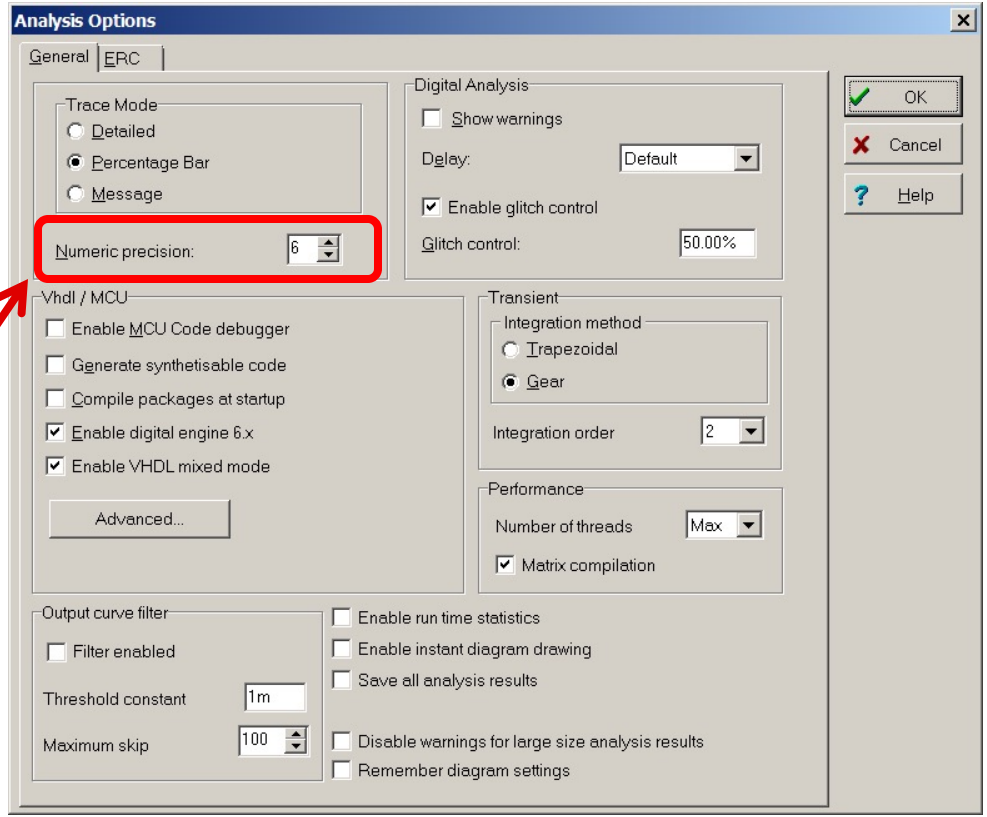



TR excitation subdivisions = 1000
TR time intrv. subdivisions = 10k
This increases the number of points vs time so that transient behaviors aren't obscured.

Press this button to expand the list.

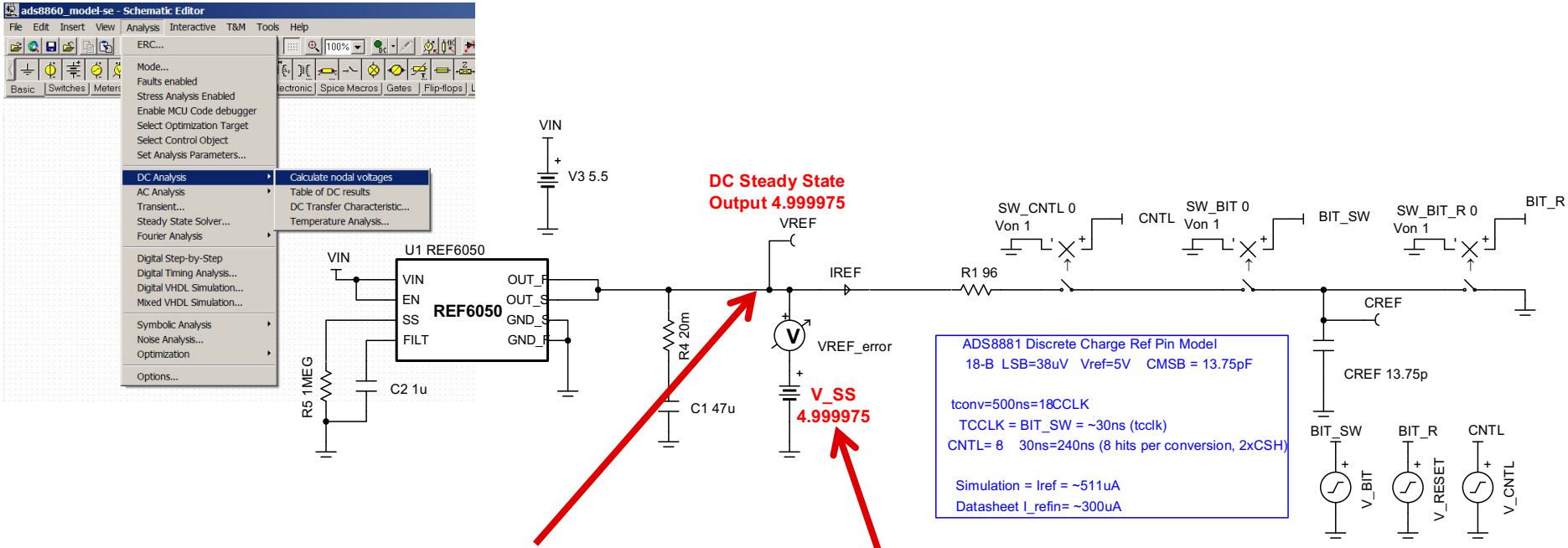
# Optimizing Simulation Results




Set the “numeric precision” to 6 digits. This will allow us to see dc operating points to six digits. The importance of this is highlighted on the next slide.

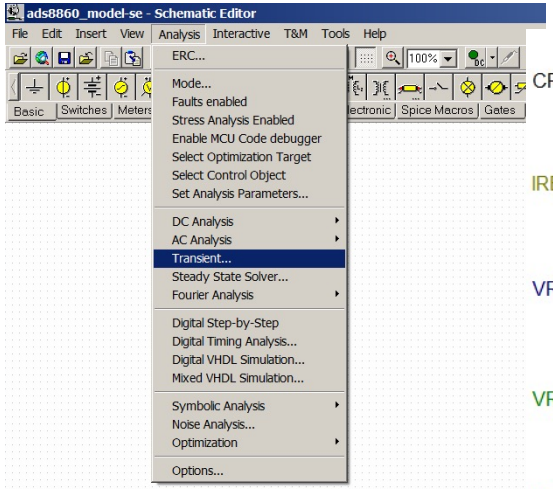
# Steady state Simulation Results

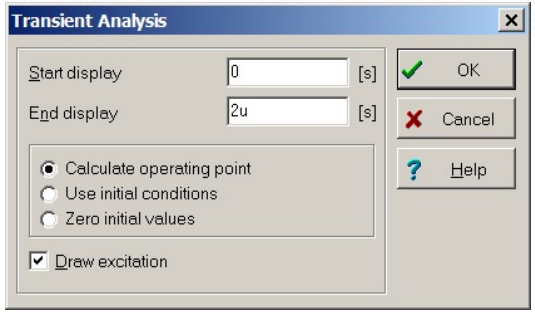


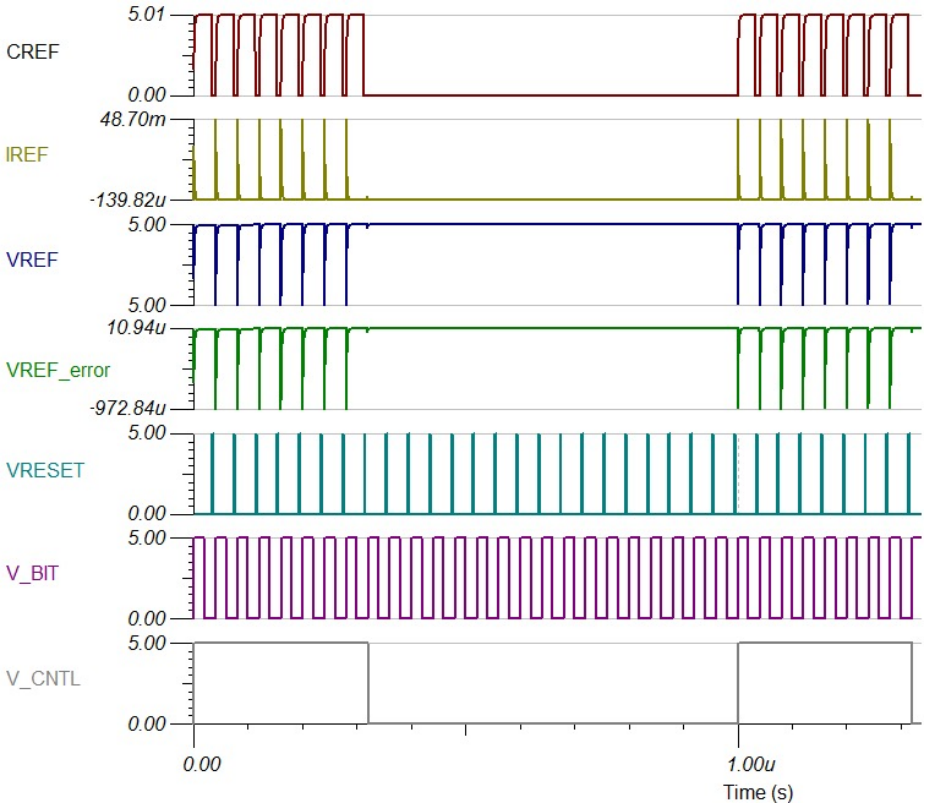

The steady state Reference input to the includes external reference initial accuracy error.

Set the V_SS source to match the steady state Reference input.

# Example simulation: transient results




Voltage across CREF Load Cap

Transient Current into REFIN Pin

REFIN Pin voltage

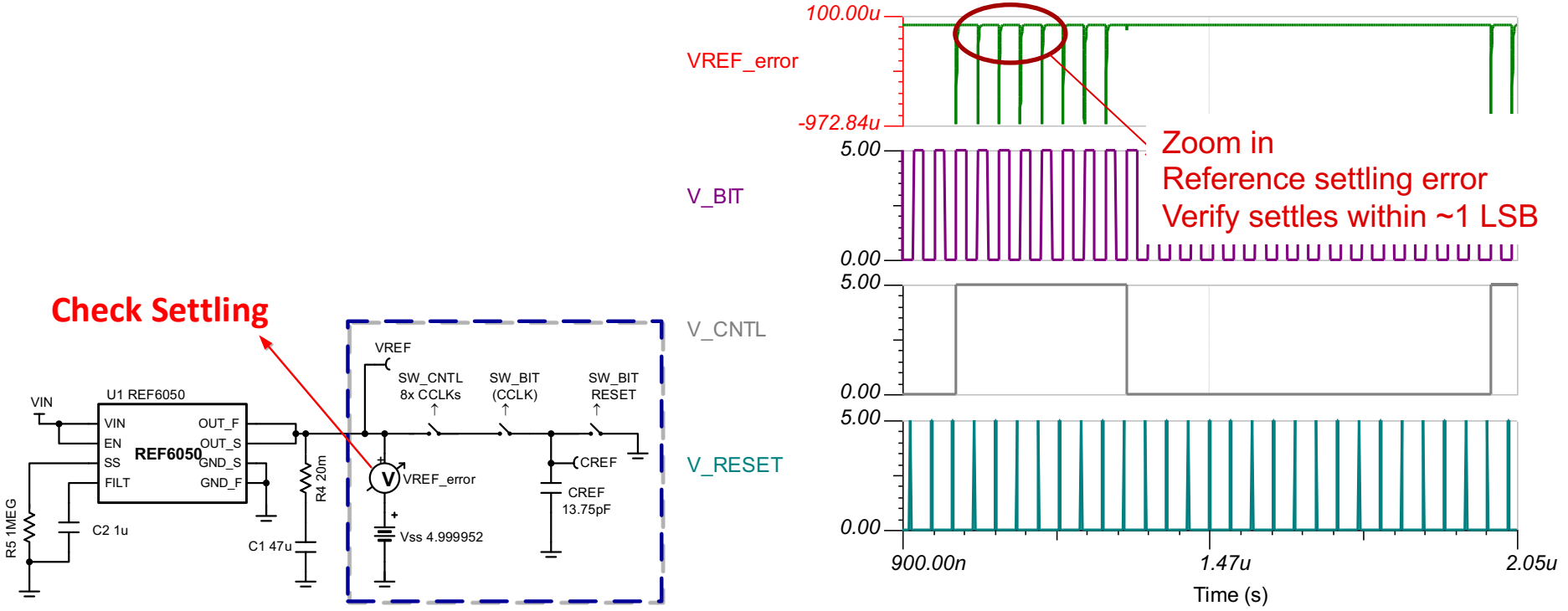
REFIN error Voltage

Switch control signal RESETs $C_{REF}$ voltage

Switch control signal Conv Clock (CCLK)

CNTL switch signal ($8xC_{REF}$ Loads per Conv)

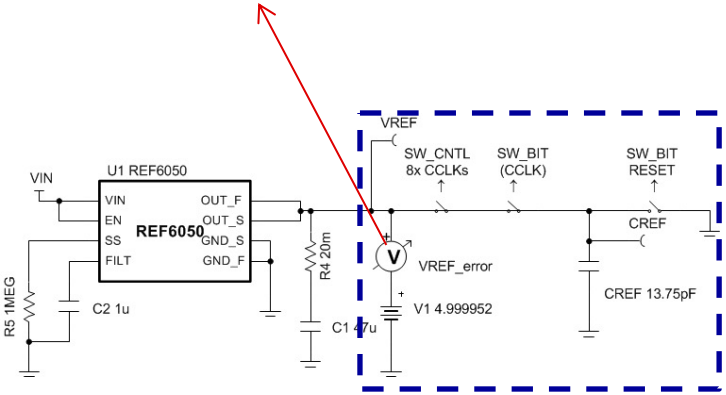
# Key Result: Error Signal

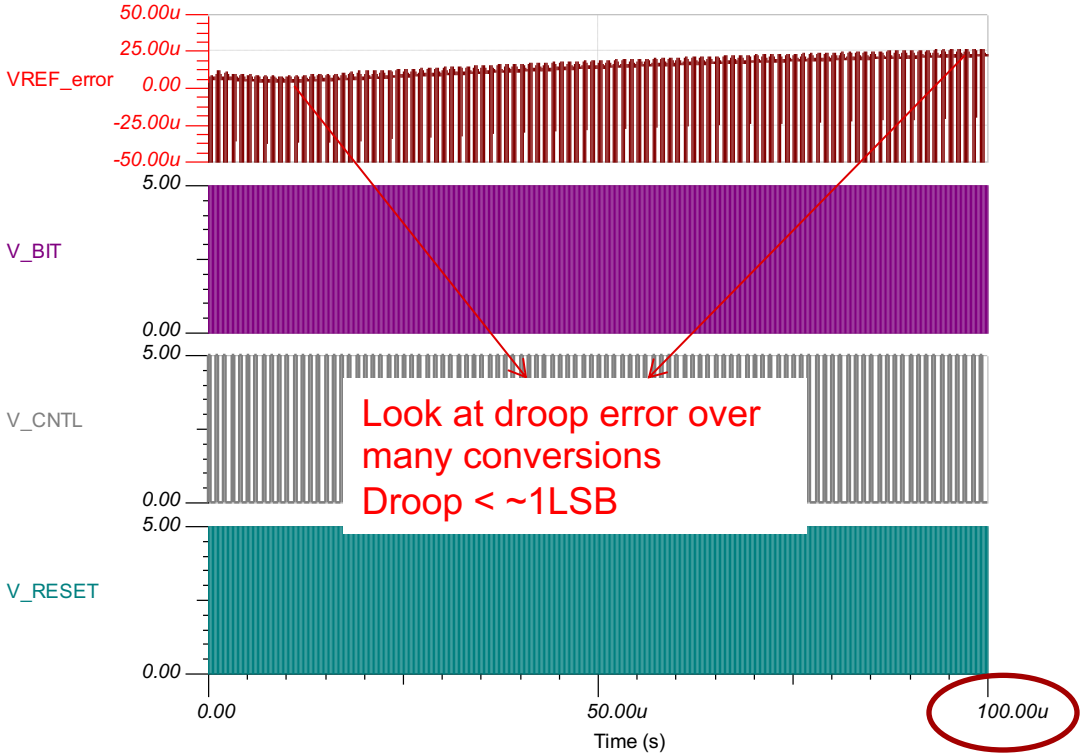


# Key Result: Error Signal

$$LSB = \frac{\pm VREF}{2^N} = \frac{2 \cdot VREF}{2^{18}} = 38.14uV$$

Check Settling



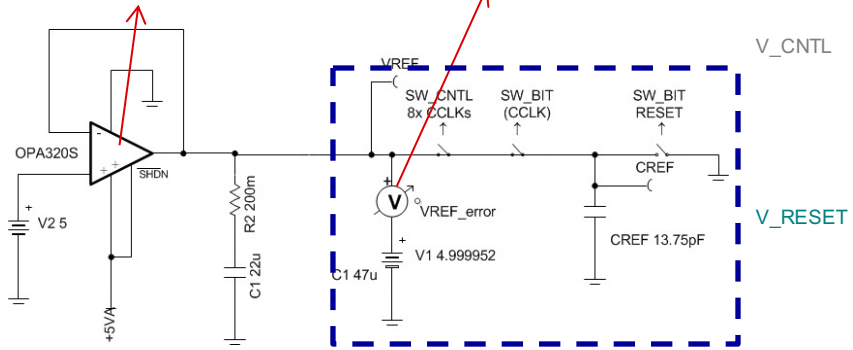



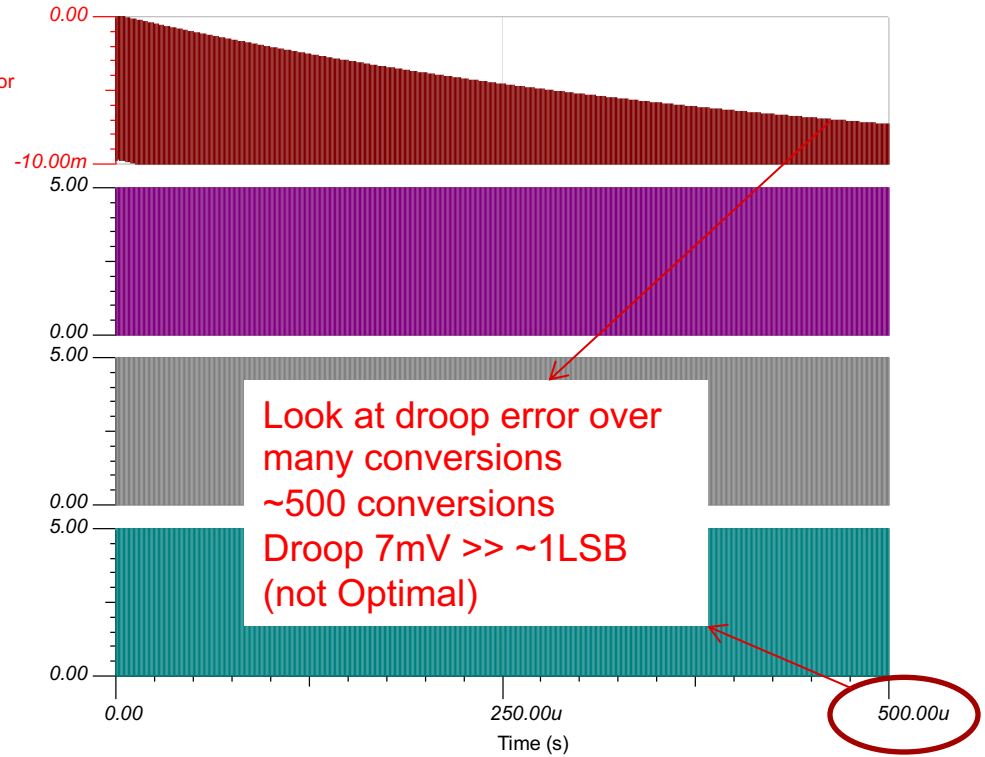
# Key Result: Error Signal

Example with excessive droop

OPA320 Stable
driving load,
but unable to recover
at 1-MSPS.

Check Settling



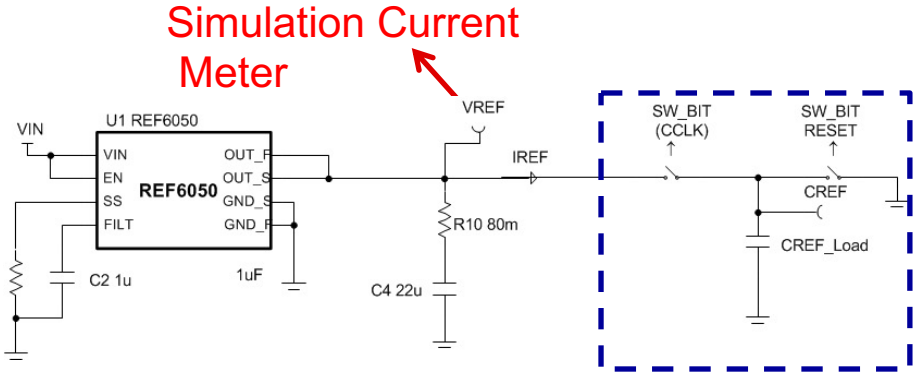



# Key Result: Average Current

Average Current per Datasheet spec is 300µA

Average Current per simulation spec is 530µA

Useful to compare sim vs datasheet



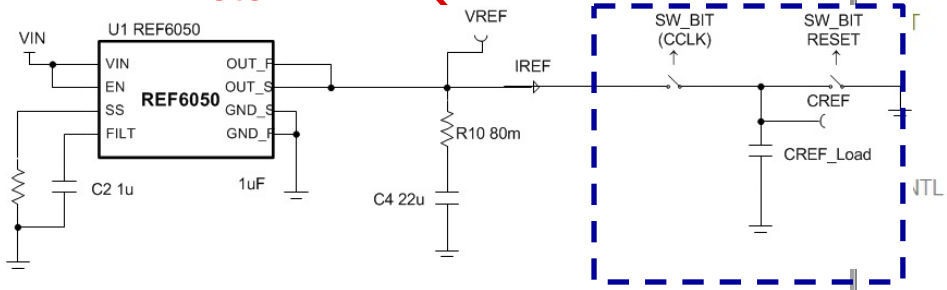
# Key Result: Average Current

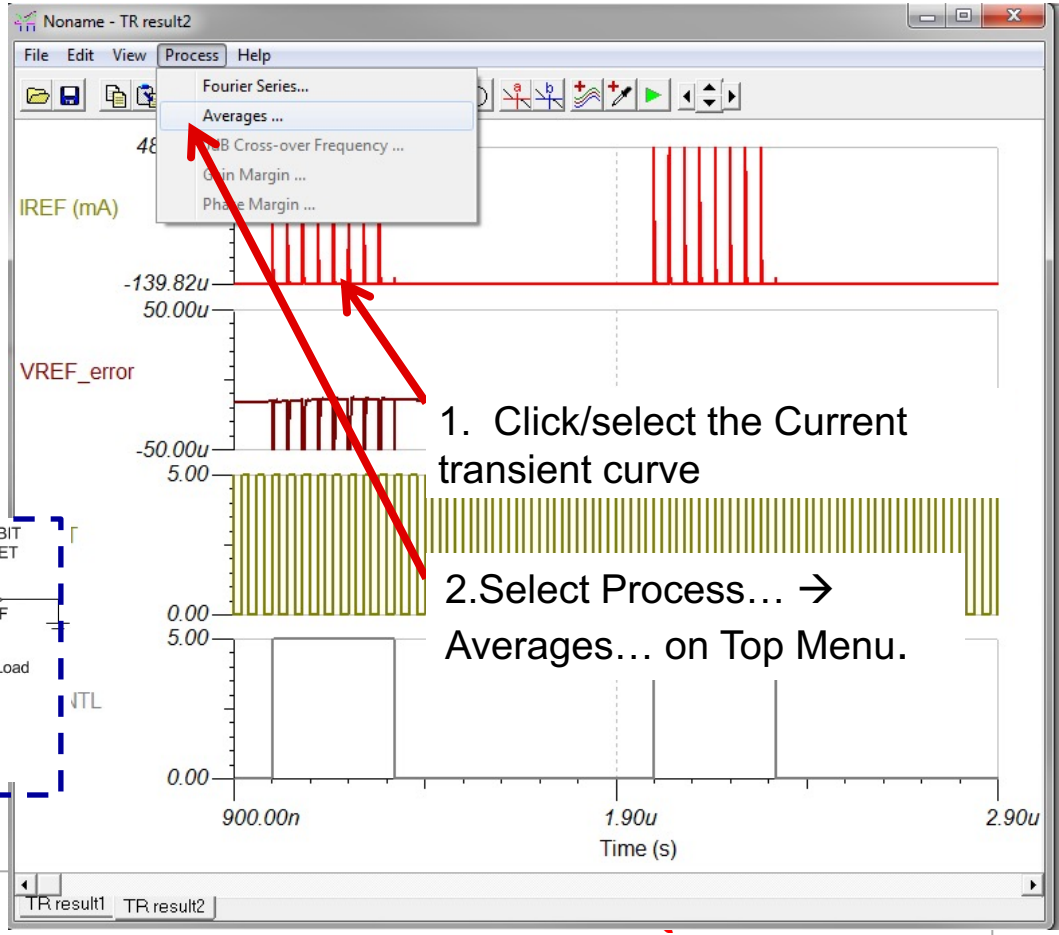
Average Current per Datasheet spec is 300µA

Average Current per simulation spec is 530µA

Useful to compare sim vs datasheet

Simulation Current Meter




1. Click/select the Current transient curve

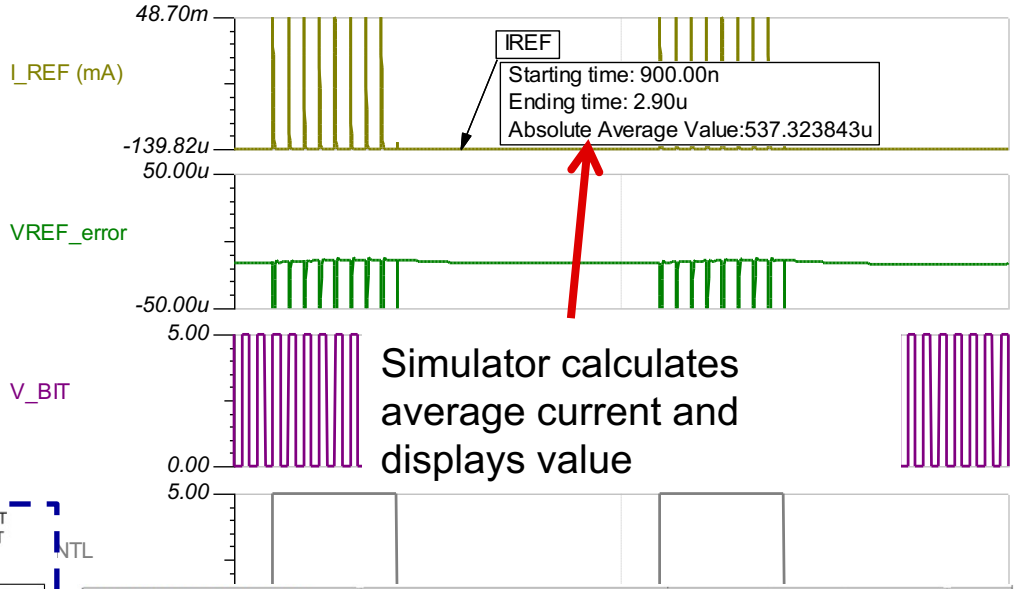
2.Select Process… → Averages… on Top Menu.

# Key Result: Average Current

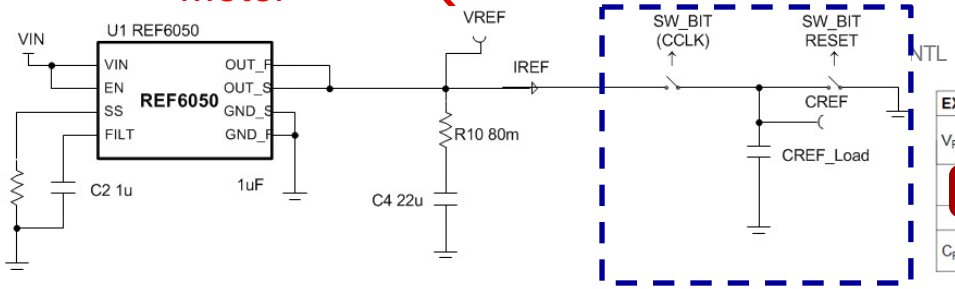
Average Current per Datasheet spec is 300µA

Average Current per simulation spec is 530µA

Useful to compare sim vs datasheet




Simulation Current Meter




| EXTERNAL REFERENCE INPUT | | | | | |
|---|---|---|---|---|---|
| $V_{REF}$ | Input range | ADS8881C | 3 | 5 | V |
| | | ADS8881I | 2.5 | 5 | |
| | Reference input current | During conversion, 1-MHz sample rate, mid-code | | 300 | µA |
| | Reference leakage current | | | 250 | nA |
| $C_{REF}$ | Decoupling capacitor at the REF input | | 10 | 22 | µF |

# Agenda

Reference Performance Specifications:

- Initial Accuracy, Drift, Long Term Drift, Noise and Output Drive

Overview of SAR REF Drive Topologies:

- Reference standalone VS Buffered Reference
- SAR ADCs with Internal Reference Buffer

SAR REF Input Overview: The Capacitive DAC (CDAC)

**Build TINA REF Input Model for a SAR:**

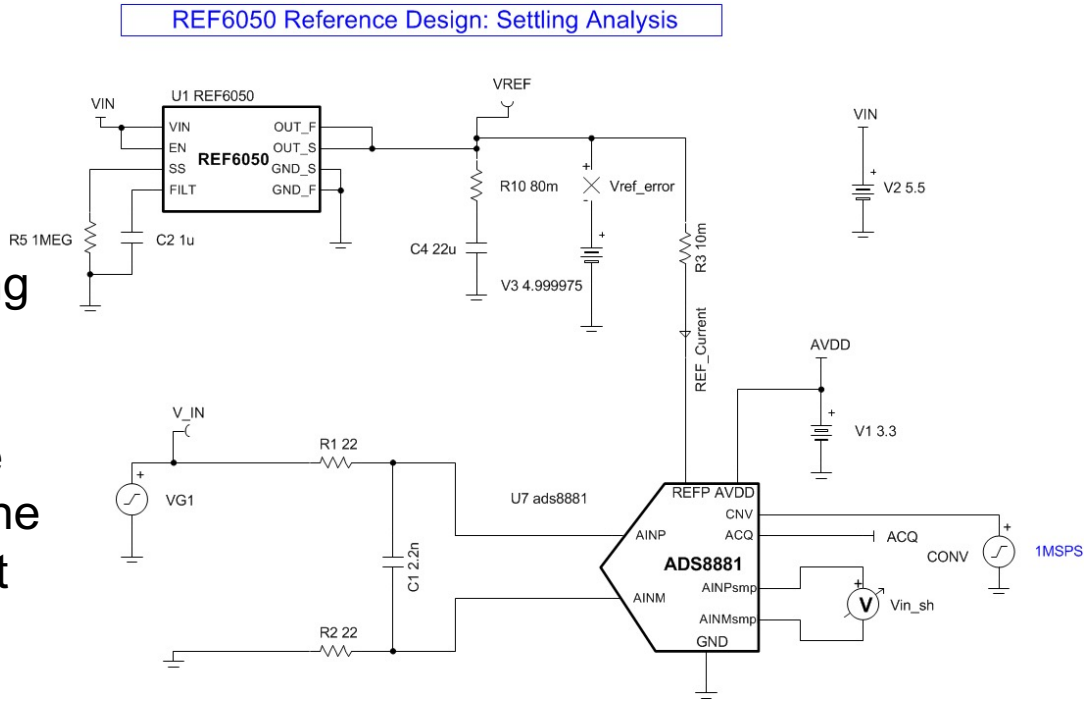
- Discrete Charge Model
- **TI Device Specific Model**

SAR REF Drive Circuit Design:

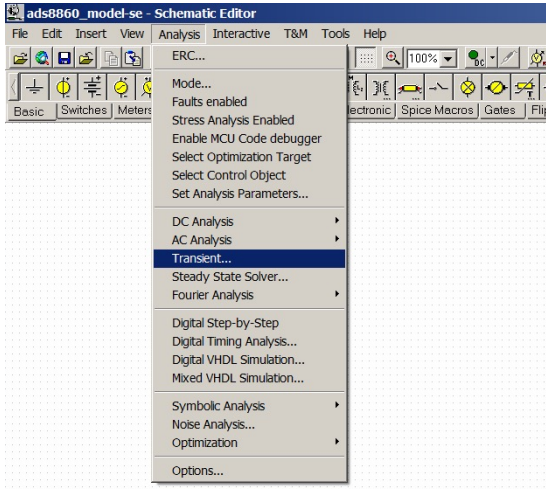
- Reference Bypass Capacitor
- Reference Buffer Stability and Compensation

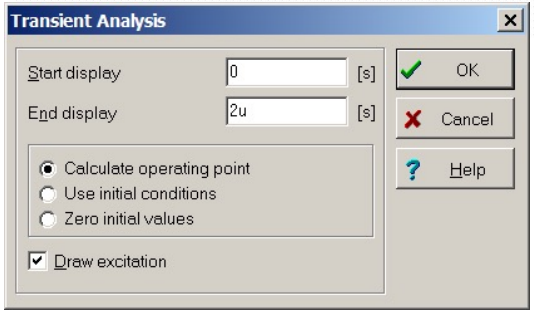
# REFIN TI Device Specific Model

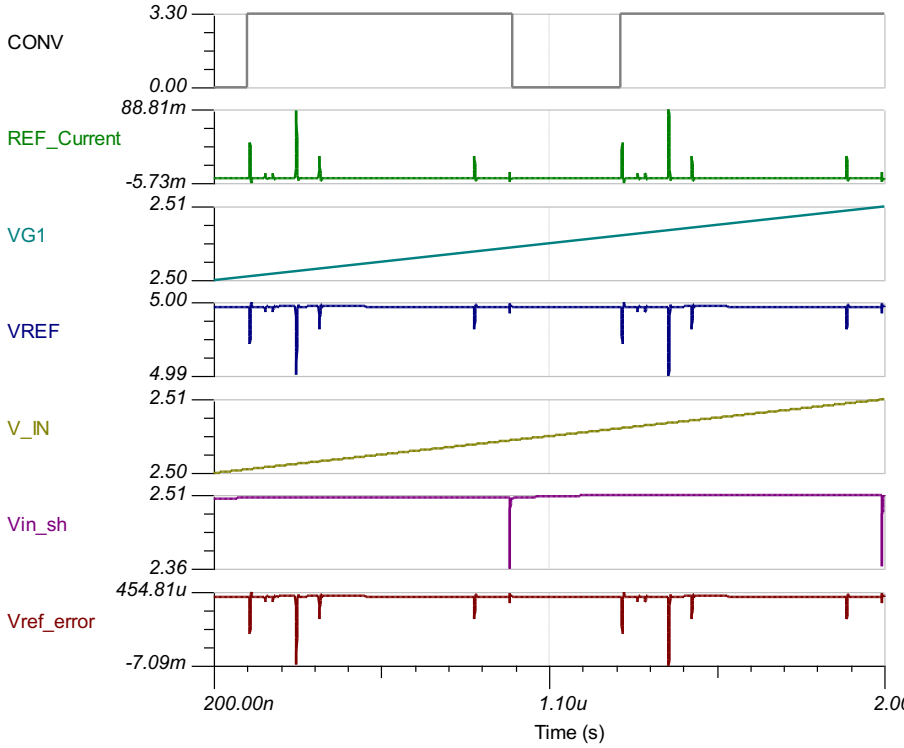
- Device specific: model closer to device topology
- Uses variable weighted switching capacitor load
- Behavior may be more accurate and/or closer to real silicon, at the cost of slower simulations/circuit complexity



# REFIN TI Device Specific Model: transient results




Convert Start signal

Transient Current into REFIN Pin

ADC Input Signal

REF voltage

Voltage across $C_{SH}$

REFIN error Voltage

# Device Specific VS Discrete Charge Model

| Discrete Charge REFIN model | Device Specific Model |
|---|---|
| Conservative approach to load: switching MSB load several times per conversion. | Binary Weighted or variable switching capacitive load, modeling specific device topology. |
| Offers faster simulation results, conservative approach | More accurate results, sometimes at the cost of circuit complexity and slower simulation. |
| Robust convergence/ fast simulations allows easy Reference drive circuit optimization | Tends to be more accurate, but slower. May have convergence issues on complex circuits. Can be used to verify final circuit. |
| Created from datasheet parameters | Provided by factory, not available on old devices |
| | |

# Thanks for your time!